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NORME INTERNATIONALE

Semiconductor devices – Metallization stress void test

Dispositifs à semiconducteurs – Essai sur les cavités dues aux contraintes de la métallisation

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SEMICONDUCTOR DEVICES – METALLIZATION STRESS VOID TEST

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The text of this standard is based on the following documents:

FDIS	Report on voting
47/2043/FDIS	47/2050/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

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SEMICONDUCTOR DEVICES – METALLIZATION STRESS VOID TEST

1 Scope

This International Standard describes a method of metallization stress void test and associated criteria. It is applicable to aluminium (Al) or copper (Cu) metallization.

This standard is applicable for reliability investigation and qualification of semiconductor process.

2 Test equipment

A calibrated hot chuck or thermal chamber is required to subject the wafers or packaged test structures to the specified temperature (±5 °C) for the specified time. For resistance measurements dedicated equipment is needed. For void inspection deprocessing equipment is required to remove the scratch protection layer. The inspections are performed with a scanning electron microscope (SEM).

3 Test structure

3.1 Test structure patterns

Test structures shall be used for all metal layers which have to be inspected and several different types of structure may be used. The following two types of test structures are applicable for this test standard.

NOTE For metallization without refractory shunt layers reflective notching at steps can occur in test structures with underlying topography, which will therefore tend to indicate a relatively worse stress-voiding behaviour.

3.2 Line pattern

Parallel lines which are patterned at the minimum linewidth allowed by design form an appropriate test structure. Unless otherwise specified a minimum length of 500 µm and a total length of 1 cm to 1 000 cm are recommended condition. Single long isolated lines are recommended because stress voiding is often sensitive to line-to-line separation.

NOTE 1 Narrow lines are susceptible for stress voiding because the stress in the metal is typically higher in narrower lines than in wider lines.

NOTE 2 The line length should be sufficient to insure that void nucleation sites will exist.

3.3 Via chain pattern

3.3.1 Pattern types

A via chain pattern is applicable as a test structure. For technology investigations a Kelvin-pattern for four-point measurements may also be used.

3.3.2 Pattern for aluminium (Al) process

Via chains need to consist of a pattern of vias connected by minimum linewidth. The recommended number of vias is between 1 000 and 100 000. It is recommended to use isolated and long minimum linewidths.

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3.3.3 Pattern for copper (Cu) process

For Cu metallization the following structures are applicable:

a) via chains with top and bottom metal segments with minimum allowed width;

b) via chains with either the top or the bottom metal segment at minimum allowed width, and the other segment at the maximum width allowed for a single via;

c) vias chains with both top and bottom metal segments at the maximum width allowed for a single via;

d) Kelvin via structures, with various widths for top and bottom metal.

Chains with 1 000 – 100 000 vias are recommended.

4 Stress temperature

To evaluate the impact of stress voiding on chip reliability under use conditions, accelerated testing is needed to generate voiding. The acceleration factor can be strongly affected by the factors listed in Annex B and Annex C. Therefore, it is recommended to determine empirically the temperature range for accelerated testing which will maximize voiding. Recommended temperature ranges are given in 5.2 and 5.3.

5 Procedure

5.1 Stress void evaluation methods

Two methods are specified for the metallization stress void test: a resistance measurement method and a visual inspection method.

– The resistance measure method is the default method.

– The inspection method is applicable for use as a verification when no stress voiding is expected. It cannot be used for lifetime extrapolations. This method is not applicable to Cu metallization. The inspection method shall not be used in case the visibility of voids is insufficient (see Note 2.)

NOTE 1 The test method most likely to detect sensitivity to stress voiding and the one most usually conducted is constant temperature (isothermal) aging, i.e., annealing or baking at temperatures between the passivation deposition temperature and the intended use temperature of the product.

NOTE 2 This is the case for e.g. metallization with multiple metal levels, where the lower levels are not clearly visible, masking of voids by other process features.

5.2 Resistance measurement method

This method assumes the void growth and therefore resistance changes can be modelled, to obtain an acceleration factor for void growth [1, 2] [1]. Unless otherwise specified, the temperature condition shall be determined within the range of 150 °C to 275 °C. Samples need to be separated into each temperature condition group and each group to be baked at the specified temperature. The procedure for resistance measurement is the following.

a) Measure the resistance of the metal line or via chain. Resistance measurements shall be made at currents that minimize joule heating.

b) Bake the samples. Unless otherwise specified three temperatures are recommended to determine the parameters for the extrapolation model. When these parameters are known it is sufficient to test at a single temperature. In some cases, three temperatures may not be enough if the temperature range is not chosen correctly - there could be an inflection point in the activation energy versus temperature curve. If zero or very few failures are

[1] Figures in square brackets refer to the Bibliography.

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observed it is not possible to determine an activation energy, and a value can be selected from the literature.

c) Measure the resistance. The samples may be cooled to room temperature for the resistance test. Cool in less than 2 h to room temperature. (Measurement of the resistance changes is, in principle, possible *in situ* at the aging temperature.) Recommended read points: 168 h, 500 h, 1 000 h.

NOTE Resistance measurements can extend beyond 2 000 h if saturation of void growth is desired.

d) Calculate the relative change in resistance, as a percentage of the line-resistance prior to the bake, ΔR (%).

e) Calculate the failure rate (number of failed samples/total sample size). For failure criterion see Clause 6.

f) Determine the total length of metal line inspected.

g) If necessary, inspect failed samples to confirm the failure mode (see 5.3 for Al and e.g. [3] for Cu).

5.3 Inspection method

The inspection method consists of the following steps.

a) Bake the samples at a specified temperature for a specified time. The recommended temperature is 200 °C for Al metallization. Recommended read points: 0 h, 168 h, 500 h, 1 000 h. Because the maximum void initiation and growth depends on the bake temperature, it is recommended to test at more than one temperature. The recommended temperature range is 150 °C to 275 °C for Al. Baking times can extend beyond 2 000 h if saturation of void growth is desired.

b) Remove the scratch protection layer with standard deprocessing techniques. If a lower level of metallization needs to be inspected, remove all other layers to expose the desired metallization level.

NOTE Deprocessing for Al technologies can be done with e.g. RIE (reactive-ion etching) etch for plasma nitride/oxynitride/TEOS (incl. TiN), H_2O_2 (50 °C) for Ti/TiN barrier layers, and PES (Phosphoric Acid, Acetic Acid, Nitric Acid) etch for Al.

c) The sample shall not be sputtered with a carbon or gold layer prior to mounting in the Scanning Electron Microscope (SEM).

d) Place the sample in the SEM, perpendicular to the incident electron beam.

e) Adjust the magnification of the SEM, such that voids down to class A (see Table 1) can be observed. Count the number of voids in the metal lines. Both wedge shaped voids and slit shaped voids shall be counted.

f) Perform detailed inspection at an appropriate magnification of the voids observed, to classify these in accordance with Table 1.

g) Determine the total length of metal line inspected.

h) Calculate the densities of Class A, Class B, and Class C voids N_A, N_B, N_C (in voids per cm) with 60 % confidence using Poisson statistics.

In order to classify the severity of the voids observed, the following classification scheme is used:

Table 1 – Void classification

Class	Void size/linewidth
Not counted	<10 %
A	≥10 %, …, <25 %
B	≥25 %, …, <50 %
C	≥50 %

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6 Failure criteria

6.1 Resistance method

The failure criterion for layered metallization with refractory shunt layers is a preselected percent resistance increase. The value shall be selected within the range from 5 % to 30 %.

NOTE If the metallization is a single-alloy component, such as AlSi or AlCu, the failure criterion of the method is an open-circuit of the test structure.

6.2 Inspection method

The failure criterion is predefined maximum number of voids in the classes A, B, C, e.g. $N_C < 1$/cm.

7 Data interpretation and lifetime extrapolation (resistance change method)

The most straightforward way to interpret the data employs the median time to failure, where failure is determined by either a specified resistance shift or an open circuit. Because extended duration can be required to produce sizeable resistance shifts, a lower relative resistance failure criterion may be desired.

A good way to avoid long test durations is to combine several test structures to effectively form one long line (or via chain) and plot the resistance change versus time. A well-behaved plot is usually obtained, which can be easily extrapolated to longer test times to determine the median time to failure.

The time-to-failure for the chosen fractional change in resistance is found either from plots of the fractional resistance change versus stress time or the square root of stress time. Void growth is generally agreed to be a diffusive process and the increase in line resistance (for layered metallizations) is proportional to the void length, which shall be proportional to a diffusion length (the average distance a species (i.e. a vacancy in stress voiding mechanism) travels due to diffusion within the lifetime of the species). Thus a plot of fractional resistance change versus the square root of the time has the advantage of being approximately linear until void growth approaches saturation. Failure time is recorded when the resistance exceeds the level defined for failure.

Plot cumulative failures vs. the log of readout time, assuming failure times are log-normally distributed, for determination of product lifetime.

A physical model [1, 2] can be used to relate the failure time to physical variables and is shown as below

$$t_f = A \times (T - T_{dep})^{-n} \times \exp(E_a/kT) \quad (1)$$

where

t_f is the median time to failure;

A is a constant;

T is the temperature during bake or in use;

E_a is the effective activation energy for the diffusion process;

k is Boltzmann's constant;

n is the creep exponent; and

T_{dep} is the effective deposition temperature of the isolation layer surrounding the metal.

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In first approximation this temperature is equal to the deposition temperature. For the exponent n a value of 2 is used, for Al and for Cu a value of 3 is more appropriate [4].

An effective acceleration factor for stress voiding can be obtained from the ratio of the failure time under use conditions to that under stress conditions, and is given by

$$A_F = t_{f,u}/t_{f,s} = (\Delta T_s/\Delta T_u)^n \times \exp\,[(E_a/k) \times (1/T_u - 1/T_s)], \quad (2)$$

where

A_F is the acceleration factor;

t_f is the median time to failure;

T is the temperature during bake or in use;

E_a is the effective activation energy for the diffusion process;

k is Boltzmann's constant;

n is the creep exponent; and

$\Delta T = (T - T_{dep})$.

The subscripts u and s denote use and stress conditions, respectively. The effective activation energy can be obtained from a plot of t_f versus $1/kT$ for several temperatures. The effective activation energy is influenced by the stress in the metal, by the microstructure of the line within several tens of microns on either side of the void, and by contributions to mass transport from interfacial diffusion. Care shall be taken when using Equation (2) that void growth has not saturated.

The effective activation energy can be determined from fit by the model (1) of the maximum or average resistance shifts for large numbers of structures of the same type baked at different temperatures. Alternatively, the median time to failure obtained for the same structure at several temperatures can be plotted against $1/kT$ and the resulting slope is interpreted as the effective activation energy. Data interpretation can be difficult in AlCu alloys because the Cu precipitation changes with temperature due to the change in solubility.

Arrhenius model (without stress term)

There is peak temperature in stress migration failure rate. By using Equation (1), the existence of peak failure rate temperature can be expressed. If the chosen temperature range is below the peak temperature, and if the Arrhenius-plot is a straight line, Equation (1) may be approximated by the Arrhenius model as shown in Equation (3):

$$t_f = A \times \exp(E_a/kT) \quad (3)$$

The activation energy can be obtained easily with only life test temperature and the lifetime.

An effective acceleration factor for stress voiding can be obtained in the same manner from the ratio of the failure time under use conditions to that under stress conditions, and is given by:

$$A_F = t_{f,u}/t_{f,s} = \exp\,[(E_a/k) \times (1/T_u - 1/T_s)] \quad (4)$$

8 Items to be specified and reported

8.1 Resistance change method

Items to be specified and reported in the resistance change method includes:

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a) bake temperatures;

b) failure criteria;

c) test structure (line configuration, straight, serpentine, etc.), linewidth and length, number of vias, via geometry and placement);

d) sample size;

e) wafer fabrication batch(s);

f) measurement intervals (test points);

g) plot(s) of the fractional resistance change versus stress time;

h) plot of the median time to failure t_f versus $1/KT$, including effective activation energy (if determined);

i) the extrapolated lifetime at use temperature (if determined).

NOTE In addition, any deviations from the standard stress void monitor procedure shall be noted.

8.2 Inspection method

Items to be specified and reported in the inspection method includes:

a) bake temperatures;

b) failure criteria;

c) test structure line configuration (straight, serpentine, etc), width or (line-width/grain size), ratio line length;

d) sample size;

e) wafer fabrication batch(s);

f) measurement Interval(s);

g) the total length of metal line inspected;

h) the number of voids detected per class (N_A, N_B, N_C);

i) inspection results (picture) of failure sample.

NOTE In addition, any deviations from the standard stress void monitor procedure shall be noted.

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