

INTERNATIONAL STANDARD

NORME INTERNATIONALE



Voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) power transmission – Electrical testing

Valves à convertisseur de source de tension (VSC) pour le transport d'énergie en courant continu à haute tension (CCHT) – Essais électriques



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Valves à convertisseur de source de tension (VSC) pour le transport d'énergie en courant continu à haute tension (CCHT) – Essais électriques

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**VOLTAGE SOURCED CONVERTER (VSC)
VALVES FOR HIGH-VOLTAGE DIRECT CURRENT (HVDC)
POWER TRANSMISSION – ELECTRICAL TESTING**

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IEC 62501 has been prepared by subcommittee 22F: Power electronics for electrical transmission and distribution systems, of IEC technical committee 22: Power electronic systems and equipment. It is an International Standard.

This second edition cancels and replaces the first edition published in 2009, Amendment 1:2014 and Amendment 2:2017. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) Conditions for use of evidence in lieu are inserted as a new Table 1;
- b) Test parameters for valve support DC voltage test, 7.3.2, and MVU DC voltage test, 8.4.1, updated;
- c) AC-DC voltage test between valve terminals, Clause 9, is restructured and alternative tests by individual AC and DC voltage tests, added in 9.4.2;

- d) Partial discharge test in routine test program is removed;
- e) More information on valve component fault tolerance, Annex B, is added;
- f) Valve losses determination is added as Annex C.

The text of this International Standard is based on the following documents:

Draft	Report on voting
22F/731/CDV	22F/748A/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

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VOLTAGE SOURCED CONVERTER (VSC) VALVES FOR HIGH-VOLTAGE DIRECT CURRENT (HVDC) POWER TRANSMISSION – ELECTRICAL TESTING

1 Scope

This International Standard applies to self-commutated converter valves, for use in a three-phase bridge voltage sourced converter (VSC) for high voltage DC power transmission or as part of a back-to-back link, and to dynamic braking valves. It is restricted to electrical type and production tests.

This document can be used as a guide for testing of high-voltage VSC valves used in energy storage systems (ESS).

The tests specified in this document are based on air insulated valves. The test requirements and acceptance criteria can be used for guidance to specify the electrical type and production tests of other types of valves.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60060 (all parts), *High-voltage test techniques*

IEC 60071 (all parts), *Insulation co-ordination*

IEC 60270, *High-voltage test techniques – Partial discharge measurements*

IEC 60700-1:2015, *Thyristor valves for high voltage direct current (HVDC) power transmission – Part 1: Electrical testing*
IEC 60700-1:2015/AMD1:2021

IEC 62747, *Terminology for voltage-sourced converters (VSC) for high-voltage direct current (HVDC) systems*

ISO/IEC 17025, *General requirements for the competence of testing and calibration laboratories*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 62747 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at <https://www.electropedia.org/>
- ISO Online browsing platform: available at <https://www.iso.org/obp>

3.1 Insulation coordination terms

3.1.1

test withstand voltage

value of a test voltage of standard waveshape at which a new valve, with unimpaired integrity, does not show any disruptive discharge and meets all other acceptance criteria specified for the particular test, when subjected to a specified number of applications or a specified duration of the test voltage, under specified conditions

3.1.2

internal insulation

air external to the components and insulating materials of the valve, but contained within the profile of the valve or multiple valve unit

3.1.3

external insulation

air between the external surface of the valve or multiple valve unit and its surroundings

3.2 Power semiconductor terms

3.2.1

turn-off semiconductor device

controllable semiconductor device which may be turned on and off by a control signal, for example an IGBT

Note 1 to entry: There are several types of turn-off semiconductor devices which can be used in VSC converters for HVDC. For convenience, the term IGBT is used throughout this standard to refer to the main turn-off semiconductor device. However, the standard is equally applicable to other types of turn-off semiconductor devices.

3.2.2

insulated gate bipolar transistor IGBT

turn-off semiconductor device with three terminals: a gate terminal (G) and two load terminals emitter (E) and collector (C)

Note 1 to entry: By applying appropriate gate to emitter voltages, the load current can be controlled, i.e. turned on and turned off.

3.2.3

free-wheeling diode

FWD

power semiconductor device with diode characteristic

Note 1 to entry: A FWD has two terminals: an anode (A) and a cathode (K). The current through FWDs is in the opposite direction to the IGBT current.

Note 2 to entry: FWDs are characterized by the capability to cope with high rates of decrease of current caused by the switching behaviour of the IGBT.

3.2.4

IGBT-diode pair

arrangement of IGBT and FWD connected in inverse parallel

3.3 Operating states of converter

3.3.1

blocking state

condition of the converter, in which a turn-off signal is applied continuously to all IGBTs of the converter

Note 1 to entry: Typically, the converter is in the blocking state condition after energization.

3.3.2**de-blocked state**

condition of the converter, in which turn-on and turn-off signals are applied repetitively to IGBTs of the converter

3.3.3**valve protective blocking**

means of protecting the valve or converter from excessive electrical stress by the emergency turn-off of all IGBTs in one or more valves

3.3.4**voltage step level**

voltage step caused by switching of a valve or part of a valve during the de-blocked state of the converter

Note 1 to entry: For valves of the controllable voltage source type, the voltage step level corresponds to the change of voltage caused by switching one submodule or cell. For valves of the switch type, the voltage step level corresponds to the change of voltage caused by switching the complete valve.

Note 2 to entry: Annex A gives an overview of VSC converters in HVDC power transmission.

3.4 VSC construction terms**3.4.1****VSC phase unit**

equipment used to connect the two DC busbars to one AC terminal

3.4.2**switch type VSC valve**

arrangement of IGBT-diode pairs connected in series and arranged to be switched simultaneously as a single function unit

3.4.3**controllable voltage source type VSC valve**

complete controllable voltage source assembly, which is generally connected between one AC terminal and one DC terminal

3.4.4**diode valve**

semiconductor valve containing only diodes as the main semiconductor devices, which might be used in some VSC topologies

3.4.5**dynamic braking valve**

complete controllable device assembly, which is used to control energy absorption in braking resistor or other components

3.4.6**valve**

VSC valve, dynamic braking valve or diode valve according to the context

3.4.7**submodule**

part of a VSC valve comprising controllable switches and diodes connected to a half bridge or full bridge arrangement, together with their immediate auxiliaries, storage capacitor, if any, where each controllable switch consists of only one switched valve device connected in series

3.4.8**cell**

MMC building block where each switch position consists of more than one IGBT-diode pair connected in series

Note 1 to entry: See Figure A.13.

3.4.9**VSC valve level**

smallest indivisible functional unit of VSC valve

Note 1 to entry: For any VSC valve in which IGBTs are connected in series and operated simultaneously, one VSC valve level is one IGBT-diode pair including its auxiliaries (see Figure A.13). For MMC type without IGBT-diode pairs connected in series one valve level is one submodule together with its auxiliaries (see Figure A.12).

3.4.10**diode valve level**

part of a diode valve composed of a diode and associated circuits and components, if any

3.4.11**redundant levels**

maximum number of series connected VSC valve levels or diode valve levels in a valve that may be short-circuited externally or internally without affecting the safe operation of the valve as demonstrated by type tests, and which if and when exceeded, would require shutdown of the valve to replace the failed levels or acceptance of increased risk of failures

Note 1 to entry: In valve designs such as the cascaded two level converter, which contain two or more conduction paths within each cell and have series-connected VSC valve levels in each path, redundant levels shall be counted only in one conduction path in each cell.

3.4.12**dynamic braking valve level**

part of a dynamic braking valve comprising a controllable switch and an associated diode, or controllable switches and diodes connected in parallel, or controllable switches and diodes connected to a bridge arrangement, together with their immediate auxiliaries, storage capacitor and energy dissipation resistors, if any

3.5 Valve structure terms**3.5.1****valve structure**

structural components of a valve, required in order to physically support the valve modules

3.5.2**valve support**

that part of the valve which mechanically supports and electrically insulates the active part of the valve from earth

3.5.3**multiple valve unit****MVU**

mechanical arrangement of 2 or more valves or 1 or more VSC phase units sharing a common valve support

Note 1 to entry: A MVU might not exist in all topologies and physical arrangement of converters.

3.5.4

valve section

electrical assembly defined for test purposes, comprising a number of valve levels and other components, which exhibits pro-rated electrical properties of a complete valve

Note 1 to entry: For valves of controllable voltage source type the valve section shall include cell or submodule DC capacitor in addition to VSC valve levels.

Note 2 to entry: The minimum number of VSC or diode valve levels allowed in a valve section is defined along with the requirements of each test.

4 General requirements

4.1 Guidelines for the performance of type tests

4.1.1 Evidence in lieu

Each design of valve shall be subjected to the type tests specified in this document. If the valve is demonstrably similar to one previously tested, the supplier may, in lieu of performing a type test or individual parts of it, submit a test report of a previous type test for consideration by the purchaser. This should be accompanied by a separate report detailing the differences in the design and demonstrating how the referenced type test satisfies the test objectives for the proposed design. Conditions for use of evidence in lieu are listed in Table 1.

Table 1 – Conditions for use of evidence in lieu from another HVDC project

Type test	Clause	Conditions
Operational tests	6	- Equal or smaller number of valve levels to be tested - Same valve level design - Same valve electronics design - Identical or lower voltage stress and thermal stress^a on each valve level
Dielectric tests on valve support structure	7	- Identical valve structure, including cooling pipes, cable paths, earthing system, if any - Same valve material and geometrical dimension - Equal or higher air clearance to valve hall and other related equipment inside the valve hall - Equal or lower voltage stress, including DC voltage stress, AC voltage stress and impulse voltage stresses
Dielectric tests on multiple valve unit	8	Same MVU geometry between valves
Dielectric tests between valve terminals	9	- Identical valve structure, including cooling pipes, cable paths and earthing system, if any - Same valve material and geometrical dimension - Equal or lower voltage stress
IGBT overcurrent turn-off test	10	- Same valve level design - Same valve electronics design - Identical or lower prospective current stress
Short-circuit current test	11	- Same valve level design - Same short-circuit bypass components, if any, and function - Same valve electronics design - Identical or lower short-circuit current stress
Tests for valve insensitivity to electromagnetic disturbance	12	Same as those indicated for Clauses 6 and 9
^a Semiconductor devices thermal stress is a combined effect of current and cooling. Device thermal stress is characterised by the device junction temperature.		

4.1.2 Selection of test object

This subclause does not apply to tests on the valve supporting structure and multiple valve unit. The test object for those tests is defined in 7.2 and 8.3.

- a) Type tests may be performed either on a complete valve or MVU, or parts thereof, as indicated in Table 4.
- b) The minimum number of valve levels to be operational type tested, depending on the valve levels in a single valve, is as shown in Table 2. This number applies to the type tests in Clauses 6, 10, 11 and 12. Those valve levels shall be tested in one test setup or multiple setups on several valve sections as defined in those clauses.

Table 2 – Minimum number of valve levels to be operational type tested as a function of the number of valve levels per valve

Number of valve levels, including redundant level per valve	Total number of valve levels to be tested
1 to 50	Number of valve levels in one valve
51 to 250	50
≥ 251	20 %

The minimum number of valve levels to be dielectric type tested can be equal to or lower than the number specified for the operational type test.

The minimum number of valve levels, however, shall be representative of the valve dielectric design.

- c) Generally, the same valve sections are recommended to be used for all type tests. However, different tests may be performed on different valve sections in parallel, in order to speed up the programme for executing the tests.
- d) Prior to commencement of type tests, the valve, valve sections and/or the components of them shall be demonstrated to have withstood the production tests to ensure proper manufacture.

4.1.3 Test procedure

The tests shall be performed in accordance with IEC 60060, where applicable with due account for IEC 60071 (all parts). Partial discharge measurements shall be performed in accordance with IEC 60270.

4.1.4 Ambient temperature for testing

The tests shall be performed at the prevailing ambient temperature of the test facility, unless otherwise specified.

4.1.5 Frequency for testing

AC dielectric tests can be performed at either 50 Hz or 60 Hz. Operational tests shall be performed at the service frequency.

4.1.6 Test reports

At the completion of the type tests, the supplier shall provide type test reports in accordance with Clause 15.

4.1.7 Conditions to be considered in determination of type test parameters

Type test parameters shall be determined based on the worst operating and fault conditions to which the valve can be subjected, according to system studies. Guidance on the conditions can be found in CIGRE Technical Brochure No. 447.

4.2 Atmospheric correction factor

When specified in the relevant clause, atmospheric correction shall be applied to the test voltages in accordance with IEC 60060-1. The reference conditions to which correction shall be made are the following:

- pressure:
 - If the insulation coordination of the tested part of the valve is based on standard rated withstand voltages according to IEC 60071-1, correction factors are only applied for altitudes exceeding 1 000 m. Hence if the altitude of the site a_s at which the equipment will be installed is $\leq 1\,000$ m, then the standard atmospheric air pressure ($b_0 = 101,3$ kPa) shall be used with no correction for altitude. If $a_s > 1\,000$ m, then the standard procedure according to IEC 60060-1 is used except that the reference atmospheric pressure b_0 is replaced by the atmospheric pressure corresponding to an altitude of 1 000 m ($b_{1\,000\text{ m}}$).
 - If the insulation coordination of the tested part of the valve is not based on standard rated withstand voltages according to IEC 60071-1, then the standard procedure according to IEC 60060-1 is used with the reference atmospheric pressure b_0 ($b_0 = 101,3$ kPa).
- temperature: design maximum valve hall air temperature ($^{\circ}\text{C}$);
- humidity: design minimum valve hall absolute humidity (g/m^3).

Realistic worst-case combinations of temperature and humidity which can occur in practice shall be used for atmospheric correction.

The values to be used shall be specified by the supplier.

4.3 Treatment of redundancy

4.3.1 Operational tests

For operational tests, redundant valve levels shall not be short-circuited. The test voltages used shall be adjusted by means of a scaling factor k_n :

$$k_n = \frac{N_{\text{tut}}}{N_t - N_r}$$

where

N_{tut} is the number of series valve levels in the test object;

N_t is the total number of series valve levels in the valve;

N_r is the total number of redundant series valve levels in the valve.

4.3.2 Dielectric tests

For all dielectric tests between valve terminals, the redundant valve levels shall be short-circuited. The location of valve levels to be short-circuited shall be agreed by the purchaser and supplier.

NOTE Depending on the design, limitations might be imposed upon the distribution of short-circuited valve levels. For example, there might be an upper limit to the number of short-circuited valve levels in one valve section.

For all dielectric tests on valve section, the test voltages used shall be adjusted by means of a scaling factor k_0 :

$$k_0 = \frac{N_{tu}}{N_t - N_r}$$

where

N_{tu} is the number of series valve levels not short circuit connected in the test object;

N_t is the total number of series valve levels in the valve;

N_r is the total number of redundant series valve levels in the valve.

4.4 Criteria for successful type testing

4.4.1 General

Experience in semiconductor application shows that, even with the most careful design of valves, it is not possible to avoid occasional random failures of valve level components during service operation. Even though these failures may be stress-related, they are considered random to the extent that the cause of failure or the relationship between failure rate and stress cannot be predicted or is not amenable to precise quantitative definition. Type tests subject valves or valve sections, within a short time, to multiple stresses that generally correspond to the worst stresses that can be experienced by the equipment not more than a few times during the life of the valve. Considering the above, the criteria for successful type testing set out below therefore permit a small number of valve levels to fail during type testing, providing that the failures are rare and do not show any pattern that is indicative of inadequate design and providing that the failed valve level permits the rest of the valve or valve section to continue operating without degraded performance.

4.4.2 Criteria applicable to valve levels

Criteria applicable to valve levels are as follows.

- a) If, following a type test as listed in Clause 5, more than one valve level (alternatively more than 1 % of the tested valve levels, if greater) has become short or open circuited, then the valve shall be deemed to have failed the type tests.
- b) If, following a type test, one valve level (or more if still within the 1 % limit) has become short or open circuited, then the failed level(s) shall be restored and this type test repeated.
- c) If the cumulative number of short or open circuited valve levels during all type tests is more than 3 % of the tested valve levels, then the valve shall be deemed to have failed the type test.
- d) The valve or valve sections shall be checked after each type test to determine whether or not any valve levels have become short or open circuited. Failed IGBT/diode or auxiliary components found during or at the end of a type test may be replaced before further testing.
- e) At the completion of the test programme, the valve or valve sections shall undergo a series of check tests, which shall include as a minimum:
 - check for voltage withstand of valve levels;
 - check of the gating circuits;
 - check of the monitoring circuits;
 - check of any protection circuits forming an integral part of the valve;
 - check of the voltage grading circuits.

- f) Valve levels short circuits occurring during the check tests shall be counted as part of the criteria for acceptance defined above. In addition to short or open circuited levels, the total number of valve levels exhibiting faults which do not result in valve level short circuit, which are discovered during the type test programme and the subsequent check test, shall not exceed 3 % of the number of tested valve levels in dielectric and operational type tests. If the number of such levels exceeds 3 %, then the nature of the faults and their cause shall be reviewed and additional action, if any, agreed between purchaser and supplier.
- g) When applying the percentage criteria to determine the permitted maximum number of short or open circuited valve levels and the permitted maximum number of levels with faults which have not resulted in a valve level becoming short or open circuited, it is usual practice to round off all fractions to the next highest integer, as illustrated in Table 3.

Table 3 – Valve level faults permitted during type tests

Number of valve levels tested	Number of valve levels permitted to become short or open circuited in any one type test	Total number of valve levels permitted to become short or open circuited in all type tests	Additional number of valve levels, in all type tests, which have experienced a fault but have not become short or open circuited
Up to 33	1	1	1
34 to 67	1	2	2
68 to 100	1	3	3
101 to 133	2	4	4

The distribution of short or open circuited levels and of other valve level faults at the end of all type tests shall be essentially random and not show any pattern that may be indicative of inadequate design.

4.4.3 Criteria applicable to the valve as a whole

Breakdown of or external flashover across common electrical equipment associated with more than one valve level of the valve, or disruptive discharge in dielectric material forming part of the valve structure, cooling ducts, light guides or other insulating parts of the pulse transmission and distribution system shall not be permitted.

Component and conductor surface temperatures, together with associated current-carrying joints and connections, and the temperature of adjacent mounting surfaces shall at all times remain within limits permitted by the design.

5 List of type tests

Table 4 lists the type tests given in Clauses 6, 7, 8, 9, 10, 11 and 12.

Table 4 – List of type tests

Type test	Clause or subclause	Test object
Maximum continuous operating duty test	6.4	Valve or valve section
Maximum temporary over-load operating duty test	6.5	Valve or valve section
Minimum DC voltage test	6.6	Valve or valve section
Valve support DC voltage test	7.3.2	Valve support
Valve support AC voltage test	7.3.3	Valve support
Valve support switching impulse test	7.3.4	Valve support
Valve support lightning impulse test	7.3.5	Valve support
MVU DC voltage test to earth	8.4.1	MVU
MVU AC voltage test	8.4.2	MVU
MVU switching impulse test	8.4.3	MVU
MVU lightning impulse test	8.4.4	MVU
Valve AC – DC voltage test	9.4.1 or 9.4.2	Valve or valve section
Valve switching impulse test	9.4.3.2	
Valve lightning impulse test	9.4.3.3	
IGBT overcurrent turn-off test	10	Valve or valve section
Short-circuit current test	11	Valve or valve section
Test for valve insensitivity to electromagnetic disturbance	12	Valve or valve section
NOTE Valve section used in the valve AC–DC voltage test (9.4.1 or 9.4.2), valve switching impulse voltage test (9.4.3.2) and valve lightning impulse voltage test (9.4.3.3) should be a single structure representative of valve dielectric design.		

6 Operational tests

6.1 Purpose of tests

The principal objectives of the operational tests are:

- to check the adequacy of the VSC/diode level and associated electrical circuits in a valve with regard to current, voltage and temperature stresses in the conducting state, at turn-on and turn-off under the worst repetitive stress conditions;
- to demonstrate correct interaction between valve electronics and power circuits of the VSC valves.

6.2 Test object

The tests may be performed on either the complete valve or on valve sections. The choice depends mainly upon the valve design and the test facilities available. The tests specified in this clause are valid for valve sections containing five or more series-connected valve levels. If tests with fewer than five levels are proposed, additional test safety factors shall be agreed. Under no circumstances shall the number of series-connected levels for tests be less than three.

The valve or valve sections under test shall be assembled with all auxiliary components. For the valves with valve surge arrester, a proportionally scaled valve arrester may be included.

The coolant shall be in a condition representative of service conditions. Flow and temperature, in particular, shall be set to the most unfavourable values appropriate to the test in question, such that the relevant component temperature(s) are equal to the values applicable in service.

6.3 Test circuit

For valve designs which act as a controllable voltage source and contain in-built DC capacitance, the DC capacitance and its connections to the semiconductor devices are an integral part of the test object.

However, for valve designs which function as switches, where the DC capacitor is separate from the valve, the DC capacitor needs to be correctly represented in the test circuit. In particular, the series stray inductance in the connections between the DC capacitor and the valve, and the stray capacitance across the valve section, shall be correctly reproduced and scaled to the size of valve section under test. Test circuit interconnections shall be of a type that is representative of the type used in the converter, in order not to introduce unrealistic levels of damping due to skin effects.

6.4 Maximum continuous operating duty test

The test needs to reproduce the following parameters based on the worst in service operating conditions of the converter. More than one test may be necessary to reproduce all parameters at their maximum values.

For VSC valves:

- maximum steady-state IGBT junction temperatures;
- maximum steady-state FWD junction temperatures;
- where snubbers are used, maximum steady-state snubber component temperatures;
- maximum steady-state turn-on and turn-off voltage and current.

For diode valves:

- maximum steady-state diode junction temperature;
- where snubbers are used, maximum steady-state snubber component temperatures;
- maximum steady-state diode turn-off voltage and current.

All of these parameters need to be reproduced during the maximum continuous operating duty test. They may be reproduced either in separate tests or as a combined test.

The test voltage shall be based on the maximum continuous direct voltage, the test switching frequency shall be based on the maximum continuous switching frequency and the modulation pattern shall be representative of that used in service.

The test current, in RMS, shall be determined taking harmonic currents into account and any other additional currents through the valve.

The test current value shall incorporate a test safety factor of 1,05.

For switch type valve, the test voltage U_{tpv1} corresponding to the maximum continuous operating DC voltage shall be determined as follows:

$$U_{tpv1} = U_{dmax} \times k_n \times k_1$$

where

U_{dmax} is the maximum continuous operating DC voltage of the valve, including ripple;

k_n is a test scaling factor according to 4.3.1;

k_1 is a test safety factor;

$k_1 = 1,05$.

For controllable voltage source type valve the test voltage, U_{tpv1} , per valve level shall be determined as follows:

$$U_{\text{tpv1}} = U_{\text{cmax}} \times k_1$$

where

U_{cmax} is the maximum continuous operating DC voltage of the valve level, including ripple;

k_1 is a test safety factor;

$k_1 = 1,05$.

The duration of the test shall be not less than 30 min after the exit coolant temperature has stabilized.

6.5 Maximum temporary over-load operating duty test

If the valve is specified for temporary over-load operation, a maximum temporary operating duty test shall be performed.

NOTE Capability of converter valves in a maximum temporary over-load operation is typically in a few seconds of time while valve cooling is unable to act.

The test conditions, where required, shall be determined using the same methodology as in 6.4 above. However, the test current shall be the specified over-load current without a test safety factor.

Prior to the test, the valve or valve section shall be brought to thermal equilibrium under the conditions of 6.4. The temporary operating duty test is then started from this initial condition and continued for a duration equal to the duration of the temporary overload multiplied by 1,2.

After the temporary over-load operation, return to the conditions of maximum continuous operation as in 6.4 and maintain constant for 10 min.

6.6 Minimum DC voltage test

This test is to verify the correct performance of those valve designs in which energy for the valve electronic circuits is extracted from the voltage appearing between the valve terminals.

The test consists of applying a DC voltage between the terminals of the valve or valve section. For this test, only the voltage, not the current, is important.

The correct operation of the valve electronic circuits may be demonstrated either by deblocking the valve or valve section, or by remaining in the blocked state and monitoring the data back signals from the valve electronics.

The test voltage U_{min} is defined as:

$$U_{\text{min}} = \frac{N_{\text{tut}}}{N_{\text{t}}} \times U_{\text{W}} \times k_2$$

where

U_{W} is the lowest DC voltage across one valve in service operation where proper function of the valve electronics is required;

N_{tut} is the number of series-connected VSC levels under test;

N_{t} is the total number of series-connected VSC levels in a single valve, including redundancy;

k_2 is a test safety factor;

$k_2 = 0,95$.

The duration of test shall be not less than 10 min.

7 Dielectric tests on valve support structure

7.1 Purpose of tests

The principal objectives of these tests are:

- a) to verify the voltage withstand capability of the insulation of the valve support, cooling ducts, light guides and other insulating components associated with the valve support. If there is insulation to earth other than the valve support, then additional tests may be necessary;
- b) to verify that the partial discharge inception and extinction voltages are above the maximum operating voltage appearing on the valve support.

NOTE Depending upon the application, it might be possible to eliminate some of the tests on the valve support, subject to agreement between purchaser and supplier.

7.2 Test object

The valve support to be used for the tests may be a representative separate object including representation of the adjacent parts of the valve or may form part of the assembly used for single valve or multiple valve unit tests. It shall be assembled with all ancillary components in place and shall have the adjacent earth potential surfaces properly represented. The proximity of adjacent earth potential surfaces (equipment or building infrastructure) shall be assessed, and representation included where appropriate. For clearances that are significantly greater than those determined by insulation co-ordination requirements, e.g. clearances driven instead by access requirements, then consideration may be given to omit earth potential surfaces in these locations. If a single valve consists of a single structure, then its large size may sometimes make it impractical to test the complete valve in a laboratory. In such cases it is permitted to perform the valve support structure tests on a pro-rated section of the support structure, provided it can be demonstrated that the design of the test object is representative of the design of the full structure and the tests cover the worst stresses experienced by any part of the valve support structure.

The coolant shall be in a condition representative of the most onerous service condition for the purpose of the test.

If a single valve consists of more than one structure such that there is more than one valve support structure per valve, then it shall be demonstrated that the tests proposed cover the worst stresses experienced by any of the valve support structures.

7.3 Test requirements

7.3.1 General

All test levels below are subject to atmospheric correction as described in 4.2.

7.3.2 Valve support DC voltage test

The two main terminals of the valve shall be connected together, and the DC voltage then applied between the two main terminals thus connected and earth. Starting from a voltage not higher than 50 % of the 1 min test voltage, the voltage shall be raised to the specified 1 min test voltage as fast as possible, kept constant for 1 min, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero. During the last hour of the specified 3 h test, the number of partial discharges exceeding 300 pC shall be recorded as described in IEC 60700-1:2015 and IEC 60700-1:2015/AMD1:2021, Annex B.

The number of pulses exceeding 300 pC shall not exceed 15 pulses per minute, averaged over the recording period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC and no more than one pulse per minute shall exceed 2 000 pC.

If an increasing trend in the magnitude or rate of partial discharge is observed, the test duration may be extended by mutual agreement between the purchaser and supplier.

The test shall then be repeated with the voltage of opposite polarity.

Prior to the test and before repeating the test with voltage of opposite polarity, the valve support may be short-circuited and earthed for a duration of several hours. The same procedure may be followed at the end of DC voltage test.

The valve support DC test voltage U_{tds} shall be determined in accordance with the following:

1 min test

$$U_{tds} = \pm U_{dmS1} \times k_3 \times k_t$$

3 h test

$$U_{tds} = \pm U_{dmS2} \times k_3$$

where

U_{dmS1} is the maximum short-duration voltage appearing across the valve support, as determined by insulation coordination studies. U_{dmS1} shall be the higher of (a) the highest voltage averaged over a 1 s period and (b) the average voltage during the time from the peak voltage to the time when the voltage decreases rapidly through the action of fast discharge devices or re-configuration, if any;

U_{dmS2} is the maximum value of the DC component of the steady-state operating voltage appearing across the valve support;

k_3 is a test safety factor;

k_3 = 1,10 for 1 min test;

k_3 = 1,15 for 3 h test;

k_t is the atmospheric correction factor according to 4.2.

7.3.3 Valve support AC voltage test

To perform the test, the two main terminals of the valve shall be connected together, and the AC test voltage then applied between the two main terminals thus connected and earth.

Starting from a voltage not higher than 50 % of the 1 min test voltage, the voltage shall be raised to the specified 1 min test voltage, kept constant for 1 min, reduced to the specified 30 min test voltage, kept constant for 30 min and then reduced to zero.

Before the end of the 30 min test, the level of partial discharge shall be monitored and recorded over a 1 min period. If the value of partial discharge is below 200 pC, the design may be accepted unconditionally. If the value of partial discharge exceeds 200 pC, the test results shall be evaluated.

The valve support AC test voltage U_{tas} shall be determined in accordance with the following:

1 min test:

$$U_{\text{tas}} = \frac{U_{\text{mS1}}}{\sqrt{2}} \times k_4 \times k_t$$

30 min test

$$U_{\text{tas}} = \frac{U_{\text{mS2}}}{\sqrt{2}} \times k_4$$

where

- U_{mS1} is the peak value of maximum voltage appearing on the valve support in service, particularly in system fault condition and valve fault operation condition. The overvoltage limiting effect of phase arrester or other overvoltage protection means, if any, shall be taken into account to derive this overvoltage;
- U_{mS2} is the peak value of the maximum repetitive operating voltage across the valve support during steady-state operation, including switching overshoot;
- k_4 is a test safety factor;
- k_4 = 1,10 for 1 min test;
- k_4 = 1,15 for 30 min test;
- k_t is the atmospheric correction factor according to 4.2.

7.3.4 Valve support switching impulse test

The test shall comprise three applications of positive polarity and three applications of negative polarity switching impulse voltages between the main terminals of the valve (connected together) and earth.

A standard switching impulse voltage wave shape in accordance with IEC 60060 shall be used.

The test voltage shall be selected in accordance with the insulation coordination of the VSC substation.

7.3.5 Valve support lightning impulse test

The test shall comprise three applications of positive polarity and three applications of negative polarity lightning impulse voltages between the main terminals of the valve (connected together) and earth.

A standard lightning impulse voltage wave shape in accordance with IEC 60060 shall be used.

The test voltage shall be selected in accordance with the insulation coordination of the VSC substation.

8 Dielectric tests on multiple valve unit

8.1 General

This clause is only applicable if more than one valve is installed in a common valve structure (multiple valve unit). In the case where each individual valve is mounted in a dedicated valve structure, this clause is not applicable.

8.2 Purpose of tests

The principal objectives of these tests are:

- a) to verify the voltage withstand capability of the external insulation of the MVU, with respect to its surroundings, especially for the valve(s) connected at pole potential;
- b) to verify the voltage withstand capability between single valves in a MVU structure;
- c) to verify that the partial discharge levels are within specified limits.

8.3 Test object

There are many possible arrangements of valves and multiple valve units. The test object(s) shall be chosen to reflect, as accurately as possible, the service configuration of valves insofar as is necessary for the test in question. The test object shall be fully equipped unless it can be shown that some components can be simulated or omitted without reducing the significance of the results.

Individual valves may have to be short-circuited depending on the configuration of the MVU and the objectives of the test.

When the low-voltage terminal of the MVU is not connected to earth potential, care shall be taken to suitably terminate the low voltage terminal of the MVU during tests to correctly simulate the voltage appearing at this terminal. Earth planes shall be used, whose separation shall be determined by the proximity of other valves and earth potential surfaces.

8.4 Test requirements

8.4.1 MVU DC voltage test to earth

The DC test voltage shall be applied between the highest potential DC terminal of the MVU and earth.

Starting from a voltage not higher than 50 % of the 1 min test voltage, the voltage shall be raised to the specified 1 min test voltage as fast as possible, kept constant for 1 min, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero.

Where possible the test voltage shall be increased from 50 % to the 1 min test voltage level within approximately 10 s.

During the last hour of the specified 3 h test, the number of partial discharges exceeding 300 pC shall be recorded.

The number of pulses exceeding 300 pC shall not exceed 15 pulses per minute, averaged over the recording period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC, and no more than one pulse per minute shall exceed 2 000 pC.

If an increasing trend in the magnitude or rate of partial discharge is observed, the test duration may be extended by mutual agreement between the purchaser and supplier.

The test shall then be repeated with the voltage of opposite polarity.

Prior to the test and before repeating the test with voltage of opposite polarity, the MVU terminals may be short-circuited together and earthed for a duration of several hours. The same procedure may be followed at the end of DC voltage test.

The MVU DC test voltage U_{tdm} shall be determined in accordance with the following:

1 min test

$$U_{\text{tdm}} = \pm U_{\text{dmm1}} \times k_5 \times k_t$$

3 h test

$$U_{\text{tdm}} = \pm U_{\text{dmm2}} \times k_5$$

where

U_{dmm1} is the maximum short-duration voltage appearing between the high-voltage terminal of MVU and earth, as determined by insulation coordination studies. U_{dmm1} shall be the higher of (a) the highest voltage averaged over a 1 second period and (b) the average voltage during the time from the peak voltage to the time when the voltage decreases rapidly through the action of fast discharge devices or re-configuration, if any;

U_{dmm2} is the maximum value of the DC component of the steady-state operating voltage appearing between the high-voltage terminal of the MVU and earth;

k_5 is a test safety factor;

$k_5 = 1,10$ for 1 min test;

$k_5 = 1,15$ for 3 h test;

k_t is the atmospheric correction factor according to 4.2.

8.4.2 MVU AC voltage test

If a MVU experiences AC or composite AC plus DC voltage stresses between any two terminals, the withstand capability of which is not adequately demonstrated by other tests, then it will be necessary to perform an AC voltage test between these terminals of the MVU.

To perform the test, the test voltage source shall be connected to the pair of MVU terminals in question. The point of earth connection is dependent on the test circuit arrangement.

Starting from a voltage not higher than 50 % of the 1 min test voltage, the voltage shall be raised to the specified 1 min test voltage, kept constant for 1 min, then reduced to the 30 min value, kept constant for 30 min and then reduced to zero.

Before the end of the 30 min test, the level of partial discharge shall be monitored and recorded over a 1 min period. If the value of partial discharge is below 200 pC, the design may be accepted unconditionally. If the value of partial discharge exceeds 200 pC, the test results shall be evaluated.

The MVU AC test voltage U_{tam} shall be determined in accordance with the following:

1 min test

$$U_{\text{tam}} = \frac{U_{\text{mm1}}}{\sqrt{2}} \times k_6 \times k_t$$

30 min test

$$U_{\text{tam}} = \frac{U_{\text{mm2}}}{\sqrt{2}} \times k_6$$

where

U_{mm1} is the peak value of maximum voltage between the terminals of the MVU in service, particularly in system fault condition and valve fault operation condition. The overvoltage limiting effect of phase arrester or other overvoltage protection means, if any, shall be taken into account to derive this overvoltage;

U_{mm2} is the peak value of the maximum repetitive operating voltage between the terminals of the MVU during steady-state operation, including switching overshoot;

k_6 is a test safety factor;

$k_6 = 1,10$ for 1 min test;

$k_6 = 1,15$ for 30 min test;

k_t is the atmospheric correction factor according to 4.2.

8.4.3 MVU switching impulse test

A standard switching impulse voltage waveshape in accordance with IEC 60060 shall be used.

The MVU switching impulse test voltage shall be applied between the high voltage terminal of the MVU and earth.

The test shall comprise three applications of positive polarity and three applications of negative polarity switching impulse voltage of a specified amplitude.

The MVU switching impulse test voltage U_{tsm} shall be determined in accordance with the following:

$$U_{\text{tsm}} = \pm U_{\text{SIPL_m}} \times k_7 \times k_t$$

where

$U_{\text{SIPL_m}}$ is the switching impulse protective level determined by insulation coordination taking into account the arrester(s) connected between the MVU high voltage terminal and earth;

k_7 is a test safety factor;

$k_7 = 1,10$;

k_t is the atmospheric correction factor;

k_t is the value according to 4.2.

If the test prescribed above does not adequately test the switching impulse withstand between all terminals of the MVU, then consideration shall be given to performing extra tests to check the insulation.

NOTE Subject to agreement between the purchaser and supplier, the MVU switching impulse test need not be performed if it can be shown by other means that:

- a) the external air clearances to other valves and to earth are adequate for the switching impulse voltage withstand level required, and
- b) the switching impulse withstand between any two terminals of the MVU is adequately demonstrated by other tests.

8.4.4 MVU lightning impulse test

A standard lightning impulse voltage wave shape in accordance with IEC 60060 shall be used.

The MVU lightning impulse test voltage shall be applied between the high voltage terminal of the MVU and earth.

The test shall comprise three applications of positive polarity and three applications of negative polarity lightning impulse voltage of specified amplitude.

The MVU lightning impulse test voltage U_{tlm} shall be determined in accordance with the following:

$$U_{\text{tlm}} = \pm U_{\text{LIPL_m}} \times k_8 \times k_t$$

where

$U_{\text{LIPL_m}}$ is the lightning impulse protective level determined by insulation co-ordination, taking into account the arrester(s) connected between the MVU high voltage terminal and earth;

k_8 is a test safety factor;

$k_8 = 1,10$;

k_t is the atmospheric correction factor;

k_t is the value according to 4.2.

If the test prescribed above does not adequately test the lightning impulse withstand voltage between all terminals of the MVU, then consideration shall be given to performing extra tests to check this insulation.

NOTE Subject to agreement between the purchaser and supplier, the MVU lightning impulse test need not be performed if it can be shown by other means that:

- a) the external air clearances to other valves and to earth are adequate for the lightning impulse voltage withstand level required, and
- b) the lightning impulse withstand voltage between any two terminals of the MVU is adequately demonstrated by other tests.

9 Dielectric tests between valve terminals

9.1 Purpose of the test

These tests are intended to verify the design of the valve regarding its voltage-related characteristics for various types of overvoltages (DC, AC, switching impulse and lightning impulse overvoltages). The tests shall demonstrate that:

- a) the valve will withstand the specified overvoltages;

- b) partial discharges will be within specified limits under specified test conditions;
- c) the internal voltage grading circuits, if any, have sufficient power rating.

It should be noted that the tests described in this clause are based on standard wave shapes and standard test procedures as developed for the testing of high-voltage AC systems and components. This approach offers great advantages to the industry because it allows much of the existing technology of high-voltage testing to be carried over to the qualification of HVDC valves. On the other hand, it must be recognized that a particular HVDC application may result in wave shapes different from the standards and, in this case, the test may be modified so as to realistically reflect expected conditions.

It should be also noted that the atmospheric correction is not needed in dielectric tests between valve terminals if the site altitude is less than 1 000 m. However, for valves installed at an altitude exceeding 1 000 m the valve internal air clearance shall be verified by additional tests under the atmospheric corrected test voltages. IGBT-diode pairs can be replaced by insulating blocks in these tests.

9.2 Test object

For valves of the switch type, the test object should generally be a complete valve. For valves of the controllable voltage source type, testing a complete valve might not be practical because of its large physical size. In such cases the test object should generally be a single structure representative of valve dielectric design. Tests on individual valve sections are acceptable if the supplier can demonstrate that the voltage distribution between valve sections, under test conditions, is representative of the voltage distribution within a complete valve in service. The test valve or valve section shall be assembled with all auxiliary components except for the valve arrester if provided. The valve may form part of a multiple valve unit.

If a valve section is used as the test object, the minimum number of valve levels in the test section shall be agreed by the purchaser. In such cases, additional tests to verify the insulation between different parts of the complete valve may be needed and shall be agreed between purchaser and supplier.

The coolant shall be in a condition that represents service conditions except for flow rate which can be reduced. If any object external to the structure is necessary for proper representation of the stresses during tests, it shall be included or simulated in the test. The proximity of adjacent earth potential surfaces (equipment or building infrastructure) shall be assessed, and representation included where appropriate. For clearances that are significantly greater than those determined by insulation coordination requirements, e.g. clearances driven instead by access requirements, then consideration may be given to omit earth potential surfaces in these locations.

9.3 Test methods

9.3.1 General

VSC valves differ from line commutated converter (LCC) valves and other high-voltage equipment in several aspects. One of the most important differences is that the converter contains very large capacitive energy storage. For valves of the controllable voltage-source type, the storage is an integral part of the valve while for switch-type valves it is closely connected to the valve. The second major difference is the active voltage control at individual VSC valve levels. As a result of these characteristics, the test method used in LCC valve dielectric tests cannot be applied to such valves.

Performing the valve dielectric test presents considerable practical difficulties on controllable voltage source type VSC valves because of the high current drawn by those in-built capacitances. The very limited current ratings of available test supplies in practical high-voltage test laboratories mean that, without modifying the test object, an excessively long time is required to charge up the capacitance of the test object to the required voltage during the AC–DC voltage test, and this unreasonably over-stresses the test object. The very large capacitance

also makes measurement of partial discharges impossible, and impulse voltages between the valve terminals do not occur on a deblocked valve during operation. For this reason, two valve dielectric test methods, on the same principle, are defined for controllable voltage source type valve dielectric tests. Supplier can use either of them for the valve dielectric test.

Valve dielectric test on switch type VSC valves shall follow Method one.

9.3.2 Method one

Temporary substitution of a special test capacitor with reduced capacitance but the same housing as the original capacitor in each valve level is necessary if this method is used in test of controllable voltage source type valves. This test capacitor shall allow a test voltage build-up across the test object during test.

In addition, it may be necessary to disable gate electronics or other auxiliary circuits in this test or provide independent means for powering them, in order to prevent interference with partial discharge measurement, for example, from gate unit power supply circuits.

When gate electronics or other auxiliary circuits are disabled for the 10 s test, the active voltage control function, if any, provided by gate electronics or other auxiliary circuits on each IGBT level may be represented by other means, for example, high resistance shunt resistors across test IGBT levels for appropriate voltage sharing.

If it is not possible to disable gate electronics or other auxiliary circuits in this test and interference can be proven to be caused by electronics circuit, then this interference may be deducted from measurement.

9.3.3 Method two

Tests on individual valve sections are acceptable if the supplier can demonstrate that the voltage distribution between valve sections under test conditions, is representative of the voltage distribution within a complete valve in service.

In case of a controllable voltage source type VSC valve the active control of sub-module capacitor voltages equalises the voltage distribution across the complete valve. The in-built capacitances react as constant voltage sources with very low internal impedance. An impulse voltage will drive a high current, the resulting change of the sub-module voltage follows the tolerance of the in-built capacitor.

Valve dielectric test is done in single steps. Step one focuses on the component level and step two on the valve or valve section.

In step one, valve levels are tested independently. Insulation and partial discharge tests with AC, DC and/or combined AC–DC voltage shall be performed on sub-component level (e.g. without power module electronics activated and without capacitor) or on full submodule level. The aim is to demonstrate both the insulation withstand capability for every single sub-component and freedom from partial discharge for every sensitive point within the valve level.

As stated, the even distribution by actively controlled sub-module voltages allows to perform the dielectric test between valve terminals and also between tiers with adjusted test voltage levels.

Consequently, in step two, the test is done with submodule levels short-circuited, interconnections between adjacent submodules removed, and valve or valve section voltage distribution controlled by an external grading circuit, for example a resistor array, capacitor array or RC array.

The inter-tier structure represents a typical section of the tower structure. Essential components of the tower structure are exposed to the specified voltage values and shapes. Test of air clearance and creepage distances of tier insulators and capacitor's housing, fibre optics including their ducts, water cooling pipes and mechanical design. AC, DC (both including PD measurement) and impulse voltages will be tested. Additional safety margin to the specific test voltages is possible and used, e.g. atmospheric correction to the specific test voltages can be added.

NOTE The addition of external grading networks could modify the profile of the test object such that it is not fully representative of in-service equipment. Practically this could lead to difficulties in performing the test, especially in determining sources of partial discharge. Hence an alternative method can be used instead of fitting grading networks, where each insulation gap is tested independently at voltages relevant to each particular gap. This can be achieved by a combination of either removing interconnections and/or shorting out relevant parts of the test object, then applying the equivalent scaled voltage across the gap. The test is performed once for each design of insulation gap e.g. inter-tier, inter-stack, inter-sub-module. Where appropriate in the design, the test set-up also needs to consider diagonal gaps (gaps between sub-modules belonging to different stacks and different tiers, one above the other).

9.4 Test requirements

9.4.1 Composite AC-DC voltage test

This test reproduces the composite AC-DC voltage resulting from certain converter or system faults and in steady-state operation. The test consists of a short-duration test and a long-duration test.

In this test, a capacitor can be used in conjunction with an AC test voltage source to produce a composite AC-DC voltage waveform. Depending on the converter topology, the capacitor could be an integral part of the valve, or it could be a separate item (part of the test circuit, not part of the test object).

Alternatively, a separate DC voltage source could be used to substitute the capacitor.

Starting from a voltage not higher than 50 % of the 10 s test voltage, the voltage shall be raised to the specified 10 s test level as fast as possible, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero.

For AC PD (partial discharge) measurement, the level of partial discharge recorded during the last minute of the 3 h test shall be less than 200 pC, provided that the components which are sensitive to partial discharge in the valve have been separately tested. For DC PD measurement the recording time shall be the last hour of the 3 h test. The number of pulses exceeding 300 pC shall not exceed 15 per minute, averaged over the record period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC and no more than one pulse per minute shall exceed 2 000 pC.

NOTE 1 If an increasing trend in the rate or magnitude of partial discharge is observed, the test duration might be extended by mutual agreement between the purchaser and supplier.

NOTE 2 It may be necessary to disable gate electronics or other auxiliary circuits in this test, or provide independent means for powering them, in order to prevent interference with partial discharge measurement, for example, from gate unit power supply circuits.

The valve test voltages have a sinusoidal waveshape superimposed on a DC level.

The valve 10 s test voltage U_{tv1} shall be determined in accordance with the following:

$$U_{tv1} = (k_{c1} \times U_{tac1} \times \sin(2\pi ft) + U_{tdc1}) \times k_0 \times k_g$$

where

- U_{tac1} is the peak value of the AC component of maximum temporary overvoltage appearing between the terminals of the valve, calculated from the peak-to-peak valve voltage divided by two;
- U_{tdc1} is the maximum of 1 s average value of the DC component of voltage appearing between the terminals of the valve at faults, after taking into account of voltage limiting effect of DC pole surge arrester;
- k_{c1} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define U_{tac1} . For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;
- k_0 is a test scaling factor according to 4.3.2;
- k_g is a test safety factor;
- $k_g = 1,1$;
- f is the test frequency (50 Hz or 60 Hz depending on test facilities).

NOTE 3 The conditions leading to the highest values of U_{tac1} and U_{tdc1} might not occur simultaneously. When performing a combined AC–DC test it is important to use self-consistent conditions that lead to the worst combined valve stress, in order to avoid over-stressing, the test object. For the 10 s test, the most important parameter is generally the peak of the combined voltage.

The valve 3 h test voltage U_{tv2} shall be determined in accordance with the following:

$$U_{tv2} = U_{tac2} + U_{tdc2}$$

$$U_{tac2} = U_{max-cont} \times \sin(2\pi ft) \times k_{c2} \times k_0 \times k_g$$

$$U_{tdc2} = U_{dmax} \times k_0 \times k_g$$

where

- $U_{max-cont}$ is the peak value of the AC component of steady-state voltage appearing between the terminals of the valve, calculated from the peak-to-peak valve voltage divided by two;
- U_{dmax} is the maximum value of the DC component of the steady-state operating voltage between the terminals of the valve, calculated from the voltage between the DC terminals of the converter divided by two;
- k_{c2} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define U_{tac2} . For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;
- f is the test frequency (50 Hz or 60 Hz depending on test facilities).

9.4.2 Alternative tests (Method 2 only)

9.4.2.1 General

When method two is adopted, the composite AC-DC voltage test specified in the previous sub-clause may be replaced, during step two, by an AC voltage test and an DC voltage test performed separately.

NOTE It is generally only possible to apply the alternative test method when testing passive insulation gaps, since the freewheel diodes in the valve will normally prevent the application of a pure AC voltage.

9.4.2.2 Valve AC voltage test

The test consists of applying the specified test voltages U_{tac1} and U_{tac2} for the specified duration. U_{tac1} and U_{tac2} have sinusoidal waveshapes with a frequency of 50 Hz or 60 Hz, depending on the test facility.

The test will be done with a short duration of 10 s and a long duration of 30 min.

Starting from a voltage not higher than 50 % of the 10 s test voltage, the voltage shall be raised to the specified 10 s test level, kept constant for 10 s, reduced to the specified 30 min test voltage, kept constant for 30 min and then reduced to zero. Before the end of the 30 min test, the level of partial discharge shall be monitored and recorded over a 1 min period. If the value of partial discharge is below 200 pC, the design may be accepted unconditionally. If the value of partial discharge exceeds 200 pC, the test results shall be evaluated.

The RMS value of valve 10 s AC test voltage, U_{tac1} , and 30 min AC test voltage, U_{tac2} , shall be determined in accordance with the following:

$$U_{tac1} = \frac{U_{vp1}}{\sqrt{2}} \times k_{c1} \times k_0 \times k_{10}$$

$$U_{tac2} = \frac{U_{vp2}}{\sqrt{2}} \times k_{c1} \times k_0 \times k_{10}$$

where

- U_{vp1} is the peak value of the maximum temporary overvoltage across the valve;
- U_{vp2} is the peak value of the maximum steady-state voltage across the valve;
- k_{c1} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define U_{tac1} . For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;
- k_{c2} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define U_{tac2} ; For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;
- k_0 is the test scaling factor according to 4.3.2;
- k_{10} is a test safety factor;
- $k_{10} = 1, 10$.

9.4.2.3 Valve DC voltage test

The test consists of applying the specified test voltages U_{tdc1} and U_{tdc2} for the specified duration.

The test will be done with a short duration of 10 s and a long duration of 3 h.

Starting from a voltage not higher than 50 % of 10 s test voltage, the voltage shall be raised to the specified 10 s test level as fast as possible, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero.

For DC PD measurement the recording time shall be the last hour of the 3 h test. The number of pulses exceeding 300 pC shall not exceed 15 per minute, averaged over the record period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC and no more than one pulse per minute shall exceed 2 000 pC.

The valve 10 s DC test voltage, U_{tdc1} , and 3 h DC test voltage, U_{tdc2} , shall be determined in accordance with the following:

$$U_{tdc1} = U_{vp1} \times k_0 \times k_{10}$$

$$U_{tdc2} = U_{vp2} \times k_0 \times k_{10}$$

9.4.3 Valve impulse tests

9.4.3.1 General

The following shall be taken into account during valve impulse tests.

- a) For some applications, for instance no overhead line is present in DC side and the busbar between phase reactor and valves is completely protected against direct lightning strike in AC side or in topologies, where the valve acts as a controllable voltage source with its own inbuilt DC capacitance, the valve impulse tests are less important since the valves do not see impulses at an amplitude which could be decisive in the electric performance of valves. Impulse tests in such applications can be omitted.

NOTE 1 Unless all equipment between the transformer and DC reactors are completely enclosed, the possibility of lightning striking an exposed section of busbar adjacent to the valve (for example between the valve reactors and the valve) cannot be excluded. However, taking into account the small area affected and the low probability of having a lightning impulse of magnitude low enough to evade the shielding, this event is extremely unlikely to occur in practice and can therefore be ignored.

NOTE 2 The emergency turn-off of the IGBT valve while it is carrying current (IGBT overcurrent turn-off test: Clause 10) can also generate a transient overvoltage between the terminals of the valve. Part of this overvoltage appears directly across the valve levels and is covered by the IGBT overcurrent turn-off test but there might, in addition, be a transient voltage developed across the stray inductance of the busbars through the valve which might need to be considered in the assessment of impulse voltage stresses between terminals.

- b) The impulse test will be applied only in one polarity which corresponds to the polarity of valve withstand voltage.
- c) If the valve impulse withstand levels are equal to or less than the valve AC-DC test level, it is deemed that the valve AC-DC test can cover the impulse tests and consequently the impulse tests can be omitted.

9.4.3.2 Valve switching impulse test

A standard switching impulse voltage waveshape in accordance with IEC 60060 shall be used.

The test shall comprise three applications of switching impulse voltages of specified amplitude on the valve.

The valve switching impulse test withstand voltage U_{tsv} shall be determined in accordance with the following:

- Valve with valve arrester protection:

$$U_{tsv} = U_{SIPL_v} \times k_0 \times k_{11}$$

where

U_{SIPL_V} is the switching impulse protective level of valve arrester or protection level derived from AC and DC side arresters;

k_0 is a test scaling factor according to 4.3.2;

k_{11} is a test safety factor;

$k_{11} = 1,10$.

- Valve without valve arrester protection:

This test is intended to verify the valve insulation when the valve is not directly protected by surge arresters.

$$U_{\text{tsv}} = U_{\text{cms}} \times k_0 \times k_{12}$$

where

U_{cms} is the switching impulse prospective voltage across valve terminals according to system insulation coordination studies;

k_0 is a test scaling factor according to 4.3.2;

k_{12} is a test safety factor;

$k_{12} = 1,15$.

The valve shall withstand the test voltage without switching or insulation breakdown.

9.4.3.3 Valve lightning impulse test

A standard lightning impulse voltage waveshape in accordance with IEC 60060 shall be used.

The test shall comprise three applications of impulse voltages of specified amplitude on the valve.

The valve lightning impulse withstand voltage U_{tlv} shall be determined in accordance with the following.

- Valve with valve surge arrester protection:

$$U_{\text{tlv}} = U_{\text{LIPL}_V} \times k_0 \times k_{13}$$

where

U_{LIPL_V} is the lightning impulse protective level of the valve arrester or protection level derived from AC and DC side arresters;

k_0 is a test scaling factor according to 4.3.2;

k_{13} is a test safety factor;

$k_{13} = 1,10$.

- Valve without valve surge arrester protection:

This test is intended to verify the valve insulation when the valve is not directly protected by surge arresters.

$$U_{\text{tlv}} = U_{\text{cml}} \times k_0 \times k_{14}$$

where

U_{cml} is the lightning impulse prospective voltage across valve terminals according to system insulation coordination studies;

k_0 is a test scaling factor according to 4.3.2;

k_{14} is a test safety factor;

$k_{14} = 1,15$.

The valve shall withstand the test voltage without switching or insulation breakdown.

10 IGBT overcurrent turn-off test

10.1 Purpose of test

The principal objective is to check the adequacy of the VSC valve design, especially the IGBT, and the associated electrical circuits with regard to current and voltage stresses at turn-off in the event of certain short circuit faults or misfiring events.

The test shall replicate the worst combination of voltage stress and instantaneous junction temperature, based on conditions that represent the most unfavourable tolerance settings of the monitoring/protection circuits. Depending on the control and protection strategy more than one test may be required in order to reproduce all relevant stresses.

General requirements related to the test circuit and the representation of DC capacitor, loop stray inductance, etc. are as stated in 6.3.

10.2 Test object

The test object is as described in 6.2. However, it is also necessary to represent certain protection or monitoring circuits if these are essential for the detection of an overcurrent event. For controllable voltage source type VSC valves, this test may also be performed on valve level.

10.3 Test requirements

The test consists of operating the test object to thermal equilibrium under the conditions which lead to the highest steady-state junction temperature of the relevant IGBT (see 6.4) and then initiating an overcurrent event. The control and protection system then detects the overcurrent and suppresses the overcurrent by turning off the IGBTs at a current below the maximum safe turn-off limit.

For switch type valve, the test voltage U_{tpv2} shall be determined as follows:

$$U_{tpv2} = U_{dtemp} \times k_n \times k_{15}$$

where

U_{dtemp} is the maximum temporary DC overvoltage of the valve, including ripple;

k_n is a test scaling factor according to 4.3.1;

k_{15} is a test safety factor;

$k_{15} = 1,05$.

For controllable voltage source type valve, the test voltage U_{tpvl2} per valve level shall be determined as follows:

$$U_{tpvl2} = U_{ctemp} \times k_{15}$$

where

U_{ctemp} is the maximum temporary DC overvoltage per valve level, including ripple;

k_{15} is a test safety factor;

$k_{15} = 1,05$.

The rate-of-rise di/dt of the overcurrent shall be taken into consideration in the test to show that the control and protection system is able to turn-off the IGBTs fast enough before maximum safe turn-off limits are reached. This consideration can be shown either by increasing the rate-of-rise di/dt of the test current waveform if the test circuit allows for it or by increasing the protection level by taking into consideration of the total inherent delay in the control and protection system.

11 Short-circuit current test

11.1 Purpose of tests

The principal objective is to check the adequacy of the devices, especially the diodes, any additional components used to protect the diodes (such as bypass thyristors) and the associated electrical circuits with regard to current stresses under specified short circuit conditions, such as short-circuit fault at DC side, until the control and protection circuit breaks the fault current. The VSC valves shall be designed to withstand the short circuit overcurrent for the number of cycles needed to open the main AC circuit breaker, without any failure or damage in the equipment, considering also that a possible recovery voltage could appear. Valve electronics shall normally be energized for the part of the fault event where any actions are taken by it. For example, when blocking the IGBTs or turning on protective devices such as bypass thyristors. For other parts of the fault event, it is not necessary to energize the valve electronics.

11.2 Test object

The test object is as described in 6.2.

11.3 Test requirements

The test consists of operating the test object to thermal equilibrium under the conditions which lead to the highest steady-state junction temperature of the relevant semiconductor component (see 6.4) and then initiating a fault current event. In order to define the maximum junction