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**Power losses in voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) systems –
Part 2: Modular multilevel converters**

**Pertes de puissance dans les valves à convertisseur de source de tension (VSC) des systèmes en courant continu à haute tension (CCHT) –
Partie 2: Convertisseurs multiniveaux modulaires**



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Part 2: Modular multilevel converters**

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Partie 2: Convertisseurs multiniveaux modulaires**

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Part 2: Modular multilevel converters

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

POWER LOSSES IN VOLTAGE SOURCED CONVERTER (VSC) VALVES FOR HIGH-VOLTAGE DIRECT CURRENT (HVDC) SYSTEMS –

Part 2: Modular multilevel converters

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In this Redline version, a vertical line in the margin shows where the technical content is modified by amendments 1 and 2. Additions are in green text, deletions are in strikethrough red text. A separate Final version with all changes accepted is available in this publication.

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A list of all parts in the IEC 62751series, published under the general title *Power losses in voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) systems*, can be found on the IEC website.

The committee has decided that the contents of this document and its amendments will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

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POWER LOSSES IN VOLTAGE SOURCED CONVERTER (VSC) VALVES FOR HIGH-VOLTAGE DIRECT CURRENT (HVDC) SYSTEMS –

Part 2: Modular multilevel converters

1 Scope

This part of IEC 62751 gives the detailed method to be adopted for calculating the power losses in the valves for an HVDC system based on the “modular multi-level converter”, where each valve in the converter consists of a number of self-contained, two-terminal controllable voltage sources connected in series. It is applicable both for the cases where each modular cell uses only a single turn-off semiconductor device in each switch position, and the case where each switch position consists of a number of turn-off semiconductor devices in series (topology also referred to as “cascaded two-level converter”). The main formulae are given for the two-level “half-bridge” configuration but guidance is also given in Annex A as to how to extend the results to certain other types of MMC building block configuration.

The standard is written mainly for insulated gate bipolar transistors (IGBTs) but may also be used for guidance in the event that other types of turn-off semiconductor devices are used.

Power losses in other items of equipment in the HVDC station, apart from the converter valves, are excluded from the scope of this standard.

This standard does not apply to converter valves for line-commutated converter HVDC systems.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60633, *Terminology for high-voltage direct-current (HVDC) transmission*

IEC 61803, *Determination of power losses in high-voltage direct current (HVDC) converter stations*

IEC 62747, *Terminology for voltage-sourced converters (VSC) for high-voltage direct current (HVDC) systems*

IEC 62751-1:2014, *Power losses in voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) systems – Part 1: General requirements*

ISO/IEC Guide 98-3, *Uncertainty of measurement – Part 3: Guide to the expression of uncertainty in measurement (GUM:1995)*

3 Terms, definitions, symbols and abbreviated terms

For the purposes of this document, the terms and definitions given in IEC 60633, IEC 62747, IEC 62751-1, as well as the following apply.

3.1 Terms and definitions

3.1.1

modular multi-level converter

MMC

multi-level converter in which each VSC valve consists of a number of MMC building blocks connected in series

Note 1 to entry: This note applies to the French language only.

3.1.2

MMC building block

self-contained, two-terminal controllable voltage source together with d.c. capacitor(s) and immediate auxiliaries, forming part of a MMC

3.1.3

IGBT-diode pair

arrangement of IGBT and free-wheeling diode connected in inverse parallel

3.1.4

switch position

semiconductor function which behaves as a single, indivisible switch

Note 1 to entry: A switch position may consist of a single IGBT-diode pair or, in the case of the cascaded two level converter, a series connection of multiple IGBT-diode pairs.

3.1.5

cascaded two-level converter

CTL

modular multi-level converter in which each switch position consists of more than one IGBT-diode pair connected in series

Note 1 to entry: This note applies to the French language only.

3.1.6

submodule

MMC building block where each switch position consists of only one IGBT-diode pair

3.1.7

cell

MMC building block where each switch position consists of more than one IGBT-diode pair connected in series

3.1.8

turn-off semiconductor device

controllable semiconductor device which may be turned on and off by a control signal, for example an IGBT

3.1.9

insulated gate bipolar transistor

IGBT

turn-off semiconductor device with three terminals: a gate terminal (G) and two load terminals emitter (E) and collector (C)

Note 1 to entry: This note applies to the French language only.

3.1.10

operating state

condition in which the HVDC substation is energized and the converters are de-blocked

Note 1 to entry: Unlike line-commutated converter, VSC can operate with zero active/reactive power output.

3.1.11

no-load operating state

condition in which the HVDC substation is energized but the IGBTs are blocked and all necessary substation service loads and auxiliary equipment are connected

Note 1 to entry: In the no-load state, in principle no switching should occur as the valve is blocked. However, in some designs, it may be necessary to make occasional switching operations to balance voltages between different parts of the converter. Here, some losses may occur and need to be accounted for. The integration time over which such losses are averaged might need to be longer than during normal operation, so as to obtain the correct weighted average of the losses while blocked and the losses while switching.

3.1.12

idling operating state

condition in which the HVDC substation is energized and the IGBTs are de-blocked but with no active or reactive power output at the point of common connection to the a.c. network

Note 1 to entry: The “idling operating” and “no-load” conditions are similar but from the no-load state, several seconds may be needed before power can be transmitted, while from the idling operating state, power transmission may be commenced almost immediately (less than 3 power frequency cycles).

Note 2 to entry: In the idling operating state, the converter is capable of actively controlling the d.c. voltage, in contrast to the no-load state where the behavior of the converter is essentially “passive”.

Note 3 to entry: Losses will generally be slightly lower in the no-load state than in the idling operating state, therefore this operating mode is preferred where the arrangement of the VSC system permits it.

3.1.13

modulation index of PWM converters

M

ratio of the peak line to ground a.c. converter voltage, to half of the converter d.c. terminal to terminal voltage

$$M = \frac{\sqrt{2} \cdot U_{c1}}{\sqrt{3} \cdot \frac{U_{dc}}{2}}$$

where

U_{c1} is the r.m.s value of the fundamental frequency component of the line-to-line voltage U_c ;

U_c is the output voltage of one VSC phase unit at its a.c. terminal;

U_{dc} is the output voltage of one VSC phase unit at its d.c. terminals.

Note 1 to entry: Some sources define modulation index in a different way such that a modulation index of 1 refers to a square-wave output, which means that the modulation index can never exceed 1. The modulation index according to that definition is given simply by $M \cdot (\pi/4)$. However, that definition is relevant mainly to two-level converters using PWM.

3.2 Symbols and abbreviated terms

3.2.1 Valve and simulation data

N_{tc}	number of MMC building blocks per valve
N_c	number of series-connected semiconductor devices per switch position
N_{sr}	total number of series resistive elements contributing to conduction losses in the valve, other than in the IGBTs and diodes
N_{cv}	number of d.c. capacitors in the valve
N_s	number of switching cycles (on or off) experienced by each VSC valve level during the integration time t_i
N_{pr}	total number of parallel resistive elements contributing to d.c. voltage dependent losses in the valve

N_{sn} number of snubber circuits per valve
 t_i integration time used in the simulation

3.2.2 Semiconductor device characteristics

V_{0T} average IGBT threshold voltage for the relevant operating conditions
 R_{0T} average IGBT slope resistance for the relevant operating conditions, valid at the device terminals
 V_{0D} average diode threshold voltage for the relevant operating conditions
 R_{0D} average diode slope resistance for the relevant operating condition, valid at the device terminals
 E_{on} average turn-on energy dissipated in the IGBT for the relevant operating conditions
 E_{off} average turn-off energy dissipated in the IGBT(s) for the relevant operating conditions
 $E_{\text{on},T1_j,k}$ turn-on energy dissipated in IGBT T1 in the j^{th} MMC building block for the k^{th} turn-on event for the relevant operating conditions (voltage, current and junction temperature)
 $E_{\text{on},T2_j,k}$ turn-on energy dissipated in IGBT T2 in the j^{th} MMC building block for the k^{th} turn-on event for the relevant operating conditions (voltage, current and junction temperature)
 $E_{\text{off},T1_j,k}$ turn-off energy dissipated in IGBT T1 in the j^{th} MMC building block for the k^{th} turn-off event for the relevant operating conditions (voltage, current and junction temperature)
 $E_{\text{off},T2_j,k}$ turn-off energy dissipated in IGBT T2 in the j^{th} MMC building block for the k^{th} turn-off event for the relevant operating conditions (voltage, current and junction temperature)
 $E_{\text{rec},D1_j,k}$ diode recovery energy dissipated in diode D1 in the j^{th} MMC building block for the k^{th} diode turn-off event for the relevant operating conditions (voltage, current and junction temperature)
 $E_{\text{rec},D2_j,k}$ diode recovery energy dissipated in diode D2 in the j^{th} MMC building block for the k^{th} diode turn-off event for the relevant operating conditions (voltage, current and junction temperature)

3.2.3 Other component characteristics

R_{s_k} total resistance of the k^{th} series resistive elements in the valve contributing to other conduction losses
 R_{dc_k} resistance of the k^{th} parallel resistive component in the valve
 R_{ESR_j} average equivalent series resistance of the j^{th} d.c. capacitor
 $E_{\text{sn,on}_j,k}$ energy dissipated in the snubber resistor of the j^{th} snubber circuit for the k^{th} turn-on event for the relevant operating conditions (voltage, and current where relevant to the design of the snubber)
 $E_{\text{sn,off}_j,k}$ energy dissipated in the snubber resistor of the j^{th} snubber circuit for the k^{th} turn-off event for the relevant operating conditions (voltage, and current where relevant to the design of the snubber)

3.2.4 Operating parameters

$I_{T1\text{av}_j}$ mean current of IGBT T1 in the j^{th} MMC building block, averaged over an integration time t_i
 $I_{T2\text{av}_j}$ mean current of IGBT T2 in the j^{th} MMC building block, averaged over an integration time t_i
 $I_{T1\text{rms}_j}$ rms current of IGBT T1 in the j^{th} MMC building block, averaged over an integration time t_i

I_{T2rms_j}	rms current of IGBT T2 in the j^{th} MMC building block, averaged over an integration time t_i
I_{D1av_j}	mean current of diode D1 in the j^{th} MMC building block, averaged over an integration time t_i
I_{D2av_j}	mean current of diode D2 in the j^{th} MMC building block, averaged over an integration time t_i
I_{D1rms_j}	rms current of diode D1 in the j^{th} MMC building block, averaged over an integration time t_i
I_{D2rms_j}	rms current of diode D2 in the j^{th} MMC building block, averaged over an integration time t_i
I_{rms_k}	rms current flowing in the k^{th} series resistive element for the relevant operating conditions
U_{rms_k}	rms value (including d.c. component) of the voltage across the k^{th} parallel resistive component in the valve
I_{crms_j}	rms current flowing in the j^{th} d.c. capacitor of the valve
$P_{GU_j,k}$	average power input to the power supply of k^{th} IGBT in j^{th} MMC building block
$p_{GU_j,k}(t)$	instantaneous power input to the power supply of k^{th} IGBT in j^{th} MMC building block
$u_{GU_j,k}(t)$	instantaneous voltage input to the power supply of k^{th} IGBT in j^{th} MMC building block
$i_{GU_j,k}(t)$	instantaneous current input to the power supply of k^{th} IGBT in j^{th} MMC building block
P_{GU_j}	average power input to the power supply in j^{th} MMC building block
$p_{GU_j}(t)$	instantaneous power input to the power supply in j^{th} MMC building block
$u_{GU_j}(t)$	instantaneous voltage input to the power supply in j^{th} MMC building block
$i_{GU_j}(t)$	instantaneous current input to the power supply in j^{th} MMC building block

3.2.5 Loss parameters

P_{V1}	IGBT conduction losses
P_{V2}	diode conduction losses
P_{V3}	other valve conduction losses
P_{V4}	d.c. voltage-dependent losses
P_{V5}	d.c. capacitor losses
P_{V6}	IGBT switching losses
P_{V7}	diode turn-off losses
P_{V8}	snubber losses
P_{V9}	valve electronics power consumption
P_{Vt}	total valve losses

4 General conditions

4.1 General

Modular multi-level converters (MMC) are a family of converters in which each valve forms a controllable voltage source. The converter a.c. voltage is synthesized by switching large numbers of relatively small, self-contained, two-terminal controllable voltage sources at different times, thereby obtaining a high-quality converter waveform with low switching losses and therefore a high overall efficiency. The MMC building blocks from which the overall converter is built up may use multiple IGBT-diode pairs connected in series (in which case the converter is referred to as the “Cascaded two level converter”, CTL^C) or only a single IGBT

diode pair per switch position. A detailed description of these types of converter is beyond the scope of this standard; however, Annex A includes a general description of the operation of the MMC (see also IEC TR 62543).

4.2 Principles for loss determination

Theoretically, the losses of a converter station can be determined either by direct measurements of the input and output powers or by means of component characteristics, using suitable mathematical models of the individual components of a converter. The selection of the principle under which the losses are to be determined shall take into consideration the uncertainties. **The manufacturer shall explain, in the loss calculation report, how the uncertainties have been considered.**

The overall uncertainty of the value of losses is an important parameter for a converter and for a converter station since it is used to compare investment cost to capitalised cost over the life-time of the converter station. To ensure that estimates are undisputed, adherence to the provisions of this standard and the provisions of ISO/IEC Guide 98-3 is indispensable. All measurements shall furthermore be traceable to national and/or international standards of measurement.

As mentioned above, a determination of the losses of a converter station could in principle be performed by making a direct measurement a.c. and d.c. side power. The difference between these two power values is however small, and a good accuracy will be very difficult to reach. In practice, this measurement would require the use of state-of-the-art measurement equipment that rivals the best equipment available at national metrology institutes, ~~equipment that is not intended for on-site use. While not impossible, this method is unlikely to be used.~~ To date, although some industry/academic partnership projects have demonstrated prototypes of measurement equipment claiming sufficient accuracy, there is little industry experience with using such equipment on site. The feasibility of using laboratory measurements on VSC valves to support a more accurate determination of valve losses has been studied by CIGRE WG B4-75 and is summarised in Annex C.

In rare cases, where there are two converters in a substation, there may be an opportunity to connect the two converters in a temporary back-to-back configuration and circulate d.c. power between them, with their total loss being supplied by the a.c. grid. This loss can be measured, using standard energy meters and voltage transformers, but with special current transformers that have a rated current that is on the order of 5 % to 10 % of the normal operating current of the converters in order to reach sufficient accuracy at the power levels to be measured. In order to enable back-to-back measurements, additional equipment and/or control and protection enhancements could be needed, which will increase the investment cost of the converter station.

For most cases, however, the losses have to be estimated from component characteristics, using suitable mathematical models of the converters, as discussed in this standard. It is however important that all such estimates have a base in actual measurements having sufficiently low uncertainty. ~~Care should also be taken to show the propagation of uncertainties from measurements and how they interact with the model. Estimates of the uncertainty contributions from imperfections in the models themselves should also be considered.~~

4.3 Categories of valve losses

The various components of valve losses are subdivided into terms referred to as P_{V1} to P_{V9} :

- P_{V1} IGBT conduction losses
- P_{V2} diode conduction losses
- P_{V3} other valve conduction losses
- P_{V4} d.c. voltage-dependent losses

P_{V5}	d.c. capacitor losses
P_{V6}	IGBT switching losses
P_{V7}	diode turn-off losses
P_{V8}	snubber losses
P_{V9}	valve electronics power consumption

For the MMC topology, because the switching frequency is usually low (less than 200 Hz) the largest contributors to the valve losses are usually the IGBT and diode conduction losses P_{V1} and P_{V2} . With half-bridge converters, P_{V1} is dominant in inverter mode and P_{V2} is dominant in rectifier mode, while with full-bridge converters there is no major difference between rectifier and inverter modes. IGBT switching losses P_{V6} and diode turn-off losses P_{V7} are also a significant (although not dominant) contribution. The other components of valve losses are generally minor.

4.4 Loss calculation method

The proposed method for determining valve losses is based on analytical formulae for the operating conditions. However, some of the necessary input parameters are difficult to obtain by purely analytical means. Numerical solutions using real-time or non-real-time simulations shall be applied, to derive such input parameters, ~~for example valve currents and switching energies~~. For that, the input parameters described in 4.5 are required.

An important requirement for such simulations is an accurate modelling of the system under investigation. Multi-level converters offer a high degree of freedom in terms of control strategies. Therefore the resulting valve ~~currents~~ losses strongly depend on the realization and the algorithms of the control itself.

In alignment with the statement presented in 4.2, uncertainties of numerical simulations shall be clearly stated ~~and justified~~ by the manufacturer. The main benefit of the numerical offline simulation is the determination of the average distribution of the switching events across a cycle.

The remaining calculations can be performed analytically with a reasonable accuracy. If it can be shown by the manufacturer that the distribution of switching events is reasonably accurate, then the remaining calculations shall be allowed to be performed analytically.

4.5 Input parameters

4.5.1 General

This subclause describes the input parameters necessary for the calculation of power losses in the valves of an MMC to take place. These input parameters refer to the data needed for the performance of numerical simulations as well as the converter and component data needed for calculation of losses. At the same time, converter and component data is divided into two categories: converter station data such as the number of MMC building blocks per valve and the on-state characteristics of the IGBT and free-wheeling diode, and operating parameters such as the converter a.c. and d.c. currents, converter voltage (amplitude and waveshape, including 3rd harmonic injection where applicable), a.c. system frequency and mean MMC building block switching frequency.

4.5.2 Input data for numerical simulations

For numerical simulations, the following requirements shall be considered.

- The simulation model shall include a control block which ~~represents the real control behaviour and realistic behaviour regarding measurements, dead and transfer times, interlocking times, etc~~ reproduces the correct valve current and switching pattern used in the complete system.

- The calculations shall be performed for a period of time with stable conditions in terms of active and reactive power transfer on the a.c. side and active power on the d.c. side.
- After the simulation has settled to steady-state conditions, a minimum integration time t_i of 1 s shall be used for operating state losses, but a longer time may be required for standby and no-load operating states, depending on the switching strategies used.
- The simulation models shall represent real conditions of the converter station in terms of number of MMC building blocks, main components, ~~parasitic elements~~, original control algorithms, voltage and current sensors. For the calculation of valve losses, all redundant VSC levels shall be assumed to be in operation.
- A simplification of the simulation model ~~with a reduced number of~~ using a lumped representation of the MMC building blocks is possible if it can be demonstrated that the resulting valve currents are not influenced by the simplification.
- ~~The simulation shall also consider the junction temperature dependent semiconductor properties, such as on-state voltages, switching and recovery losses. These properties are based on the characterisation testing as described in IEC 62751-1:2014, 4.4.2. The steady-state junction temperatures of the semiconductors are calculated iteratively for the relevant operating point to derive the semiconductor losses. Further outputs of the simulation are converter valve currents and MMC building block capacitor currents, which are the basis for the calculation of corresponding losses.~~

There are two different approaches/methods which may be applied:

1) Two-stage simulation and calculation method on the basis of simulated input values

In this approach, the input parameters required for a calculation shall be simulated using a model which at least represents the on-state characteristics of the converter as well as the switching pattern or control pattern for the switching of the cells. The on-state representation may be chosen on the basis of worst-case characteristics (at high junction temperatures) or on-state characteristics for lower junction temperatures. The simulated values (voltages, currents and switching pattern) shall be used as input for the calculations. For the calculations with the simulated values, the following two approaches may be used.

- a) The semiconductor parameters are chosen for the rated or worst-case junction temperature condition and the losses shall be calculated on the basis of the rated junction temperature.

NOTE Due to the assumption of a worst-case temperature condition, this calculation will result in higher losses than what can actually be observed in the real application.

- b) Using a thermal model, the temperature-dependent semiconductor properties shall be considered to calculate the losses for all semiconductors in the converter. Since only steady-state scenarios are the basis for the loss calculation, the thermal heat capacitances may be considered as negligible for the thermal model. The temperature-dependent loss calculation may be executed in an iterative manner. For the iterative calculation approach with the simulation values input, a steady-state condition shall be reached to end the iteration process (as a suggestion ± 1 K iteration error border).

2) Loss calculation with an exclusive simulation approach

In this approach, the junction temperature dependent semiconductor properties, such as on-state voltages, and switching and recovery losses, shall be included in the simulation model (i.e. a thermal model shall be included in the simulations, as for the mixed calculation and simulation approach the thermal heat capacitances may be neglected for steady state conditions). The simulation model shall represent the switching pattern or control pattern for the switching of the cells. On the basis of the simulations, the losses shall be extracted directly from the simulation model for all semiconductors in the converter. Similarly to option 1), it is possible to simplify the model by using semiconductor parameters applicable only to the maximum rated junction temperature, but this will result in a more conservative calculation.

4.5.3 Input data coming from numerical simulations

From the numerical simulations the currents through the devices of the valve that are needed as input for calculation of losses are determined. The list of parameters to be derived includes:

- mean and rms current through diodes,
- mean and rms current through IGBTs,
- rms currents through series resistive elements,
- rms currents through parallel resistive elements,
- rms currents flowing in the d.c. capacitors of the valve,
- switching energies in IGBTs and diodes.

Additionally, from numerical simulations, a selection of a suitable integration time can be derived. The mean and rms currents in IGBTs and diodes are not required if conduction losses in IGBTs and diodes are calculated using polynomials as discussed in 5.1. The required parameters to be derived from the simulations may vary depending on the chosen calculation approach.

4.5.4 Converter station data

The following converter station data are necessary for calculation of losses:

- interface transformer turns ratio and leakage reactance;
- filter configuration, if any;
- phase reactor inductance, if any;
- valve reactor(s) inductance;
- number of MMC building blocks per converter arm;
- number of VSC levels per cell (for CTL designs);
- capacitance per MMC building block;
- coolant inlet temperature; where several heat sinks are connected in series, the effect of the bulk water temperature rise shall be taken into account;
- average IGBT threshold voltage V_{0T} for each type of IGBT used;
- average IGBT slope resistance R_{0T} for each type of IGBT used;
- average IGBT turn-on energy per turn-on process E_{on} for each type of IGBT used;
- average IGBT turn-off energy per turn-off process E_{off} for each type of IGBT used;
- average diode threshold voltage V_{0D} for each type of diode used;
- average diode slope resistance R_{0D} for each type of diode used;
- average-corrected diode recovery energy per turn-off process E_{rec} for each type of diode used;
- equivalent thermal model representing relevant thermal resistances from average junction temperature of IGBTs and diodes to local coolant inlet temperature;

NOTE The average junction temperature of the IGBT or diode represents both a spatial and a temporal average, to remove effects such as lateral temperature variations and cyclic temperature ripple.

- snubber circuit parameters, if any, such as snubber capacitor, snubber resistor and inductance; for the case that the energy dissipated in the snubber resistor is determined by measurements (characterisation testing), the values of the energies have also to be provided;
- resistance R_{s_k} of series resistive elements in the valve;
- resistance R_{dc_k} of parallel resistive elements in the valve;
- equivalent series resistance R_{ESR_j} of d.c. capacitors.

4.5.5 Operating conditions

The following data concerning operation conditions are needed for calculation:

- active power at a defined point,
- reactive power at a defined point,
- a.c. line voltage,
- tap changer position, if applicable,
- d.c. voltage.

In the report of determination of losses to be provided by the converter manufacturer, the input data above described shall be presented.

4.6 Contents and structure of valve loss determination report

The manufacturer or bidder shall prepare and submit to the purchaser a detailed report explaining how the losses in the VSC valves have been determined at the project execution stage, including a breakdown of the valve losses into the constituent parts P_{V1} to P_{V9} for each operating condition at which losses are required to be guaranteed.

At the bid stage, and (where requested in the contract) after contract award but before the manufacturing of valve components, the report shall document the assumptions used in arriving at the calculated value of losses. After manufacturing, the report shall document the actual values of test data derived from characterisation tests and routine tests on components.

Although a breakdown of the valve losses into the constituent parts P_{V1} to P_{V9} is requested, only the total valve losses P_{Vt} shall be subject to financial evaluation.

A recommended list of data to be included in the report is presented in Annex B.

5 Conduction losses

5.1 General

Each MMC building block of the MMC contains a half-bridge configuration and a d.c. capacitor. Basically the design of the MMC building block is of one of the two following versions shown in Figure 1:

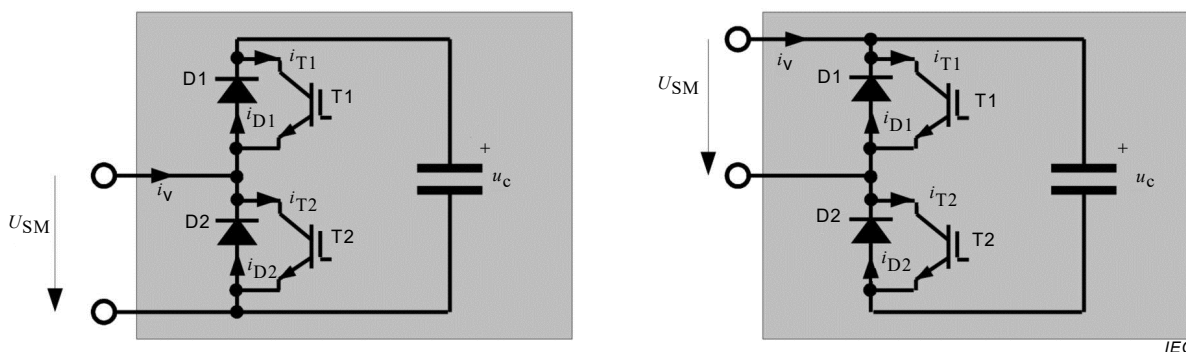
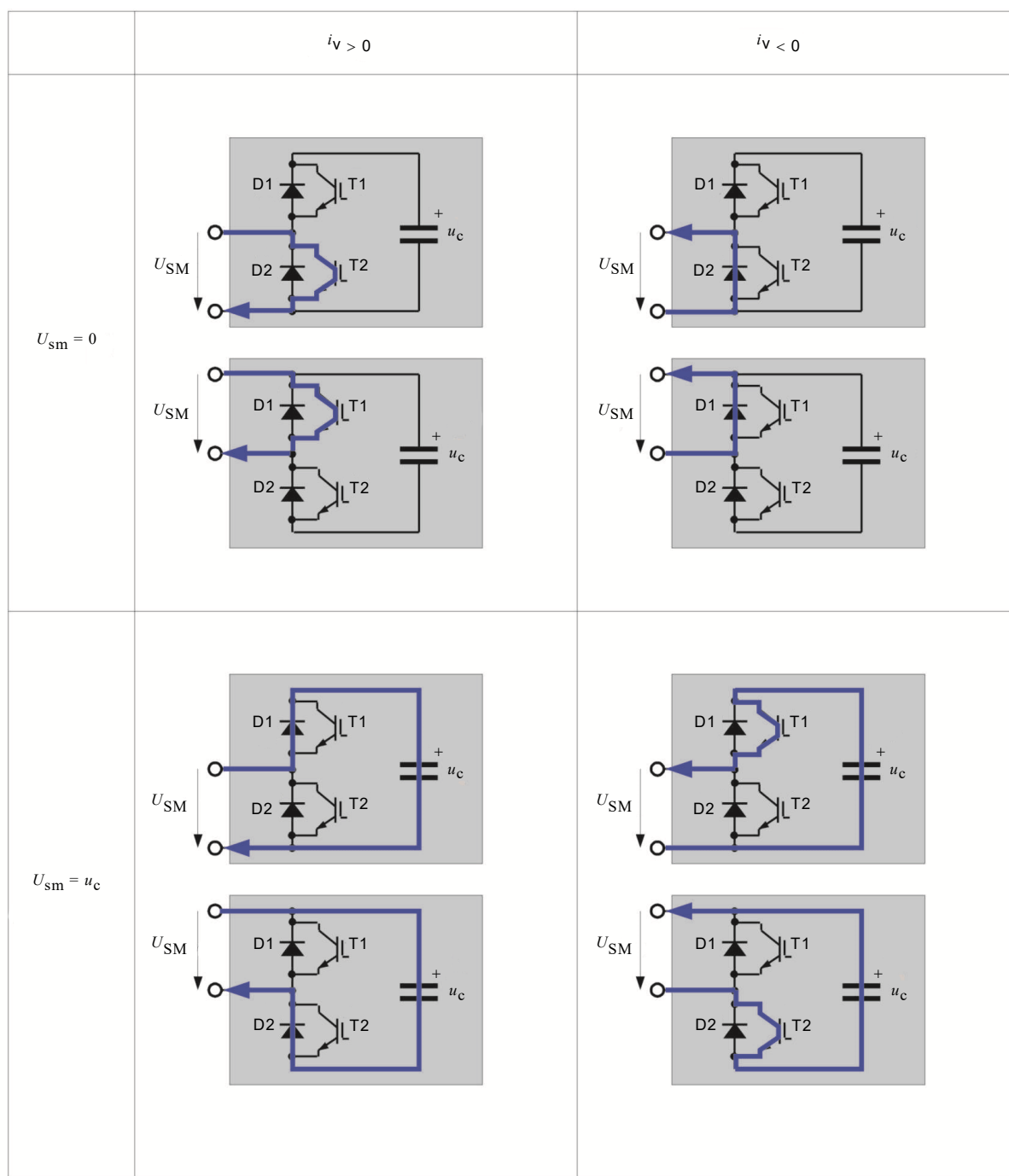


Figure 1 – Two basic versions of MMC building block designs

The designations D1, D2, T1 and T2 of the FWDs and IGBTs are defined so that the devices T1 and D1 are connected to the positive terminal of the capacitor, and T2, D2 are connected to the negative terminal.

In case of CTL converters, T1, T2, D1 and D2, respectively, represent a series connection of N_c IGBTs or diodes.

Dependent on the current direction and on the voltage at the terminals, the conducting paths shown in Figure 2, are possible during steady state operation.



IEC

Figure 2 – Conduction paths in MMC building blocks

To simplify the process of mathematically analysing conduction losses, the on-state voltage of IGBTs and diodes is usually represented as a piecewise-linear approximation with a threshold voltage V_0 and a slope resistance R_0 , as shown in Figure 2 of IEC 62751-1:2014.

It is possible to obtain greater accuracy by using a more exact model of the device on-state voltage (for example, using a polynomial function to represent the on-state voltage) rather than the piecewise-linear approximation, and then performing a direct numerical integration. However, the piecewise-linear approximation is preferred because it simplifies the calculation process, allows greater transparency and still permits good accuracy to be obtained, provided the measurements used to derive the piecewise-linear approximation are made at appropriate values of current. Therefore, it is recommended that V_0 and R_0 are determined by measuring on-state voltage at 100 % and 33 % of the device rated current and performing a linear extrapolation.

NOTE When the rated DC current of the HVDC scheme is significantly lower than the rated current of the IGBT, additional measurement points might be necessary in order to obtain acceptable accuracy.

In the event that the purchaser prefers to use the more accurate method using a polynomial function, then this shall be clearly stated in the purchasing specification, and all bidders are expected to calculate power losses in a comparable way.

5.2 IGBT conduction losses

Where the piecewise-linear approximation is used, the total IGBT conduction losses per valve may be calculated by summing the conduction losses of all IGBTs per valve:

$$P_{V1} = N_c \cdot \sum_{j=1}^{N_{tc}} (V_{0T} \cdot I_{T1av_j} + R_{0T} \cdot I_{T1rms_j}^2 + V_{0T} \cdot I_{T2av_j} + R_{0T} \cdot I_{T2rms_j}^2) \quad (1)$$

where

- N_{tc} is the number of MMC building blocks per valve;
- N_c is the number of series-connected semiconductor devices per switch position;
- V_{0T} is the average IGBT threshold voltage for the relevant operating conditions;
- R_{0T} is the average IGBT slope resistance for the relevant operating conditions, valid at the device terminals;
- I_{T1av_j} is the mean current of IGBT T1 in the j^{th} MMC building block, averaged over an integration time t_i ;
- I_{T2av_j} is the mean current of IGBT T2 in the j^{th} MMC building block, averaged over an integration time t_i ;
- I_{T1rms_j} is the rms current of IGBT T1 in the j^{th} MMC building block, averaged over an integration time t_i ;
- I_{T2rms_j} is the rms current of IGBT T2 in the j^{th} MMC building block, averaged over an integration time t_i .

By means of numerical simulation, the currents ~~have to~~ shall be calculated for the IGBTs T1 and T2 for each MMC building block, respectively:

$$I_{T1av} = \frac{1}{t_i} \cdot \int_0^{t_i} i_{T1}(t) \cdot dt \quad (2)$$

$$I_{T2av} = \frac{1}{t_i} \cdot \int_0^{t_i} i_{T2}(t) \cdot dt \quad (3)$$

$$I_{T1rms} = \sqrt{\frac{1}{t_i} \cdot \int_0^{t_i} i_{T1}(t)^2 \cdot dt} \quad (4)$$

$$I_{T2rms} = \sqrt{\frac{1}{t_i} \cdot \int_0^{t_i} i_{T2}(t)^2 \cdot dt} \quad (5)$$

where

t_i is the integration time used in the simulation;

t_i shall not be less than 1 s.

If different IGBT types are used for T1 and T2, ~~the~~ corresponding values for threshold voltages and slope resistances ~~have to~~ shall be used accordingly. An analytical approach to calculate the current distribution for the individual submodule elements may be acceptable (e.g. use of switching vector derived from simulation).

For parallel connected semiconductors, the current sharing may be calculated on the basis of the forward characteristics of the semiconductors (usually an equal current sharing).

5.3 Diode conduction losses

Where the piecewise-linear approximation is used, the total diode conduction losses per valve may be calculated by summing the conduction losses of all diodes per valve:

$$P_{V2} = N_c \cdot \sum_{j=1}^{N_{tc}} (V_{0D} \cdot I_{D1av_j} + R_{0D} \cdot I_{D1rms_j}^2 + V_{0D} \cdot I_{D2av_j} + R_{0D} \cdot I_{D2rms_j}^2) \quad (6)$$

where

N_{tc} is the number of MMC building blocks per valve;

N_c is the number of series-connected semiconductor devices per switch position;

V_{0D} is the average diode threshold voltage for the relevant operating conditions;

R_{0D} is the average diode slope resistance for the relevant operating condition, valid at the device terminals;

I_{D1av_j} is the mean current of diode D1 in the j^{th} MMC building block, averaged over an integration time t_i ;

I_{D2av_j} is the mean current of diode D2 in the j^{th} MMC building block, averaged over an integration time t_i ;

I_{D1rms_j} is the rms current of diode D1 in the j^{th} MMC building block, averaged over an integration time t_i ;

I_{D2rms_j} is the rms current of diode D2 in the j^{th} MMC building block, averaged over an integration time t_i .

By means of numerical simulation, the currents ~~have to~~ shall be calculated for the diodes D1 and D2 for each MMC building block, respectively:

$$I_{D1av} = \frac{1}{t_i} \cdot \int_0^{t_i} i_{D1}(t) \cdot dt \quad (7)$$

$$I_{D2av} = \frac{1}{t_i} \cdot \int_0^{t_i} i_{D2}(t) \cdot dt \quad (8)$$

$$I_{D1rms} = \sqrt{\frac{1}{t_i} \cdot \int_0^{t_i} i_{D1}(t)^2 \cdot dt} \quad (9)$$

$$I_{D2rms} = \sqrt{\frac{1}{t_i} \cdot \int_0^{t_i} i_{D2}(t)^2 \cdot dt} \quad (10)$$

where

t_i is the integration time used in the simulation;

t_i shall not be less than 1 s.

NOTE—If different diode types are used for D1 and D2, ~~the~~ corresponding values for threshold voltages and slope resistances ~~have to~~ shall be used accordingly. An analytical approach to calculate the current distribution for the individual submodule elements may be acceptable (e.g. use of switching vector derived from simulation).

For parallel connected semiconductors the current sharing may be calculated on the basis of the forward characteristics of the semiconductors (usually an equal current sharing).

5.4 Other conduction losses

This subclause covers the power losses due to conduction in components other than IGBTs and diodes. For modular multi-level converters, this mainly ~~includes the valve reactors and~~ consists of interconnecting busbars. The resistances of the busbars shall include not only the internal busbars within the MMC building blocks but also the busbars connecting between MMC building blocks and between the different stacks that make up the valve. Losses in valve reactors shall be considered separately from valve losses and calculated using the principles defined for AC filter reactors in IEC 61803.

Calculation of such losses is relatively straightforward and depends only on the resistance of each conducting element and the rms current that flows through it. The relevant rms currents within the MMC building blocks can be derived from the simulations of the current stresses according to 5.2 and 5.3. Also the rms currents through reactors and between the MMC building blocks respectively can be derived accordingly.

The value of these losses per valve is given by:

$$P_{V3} = \sum_{k=1}^{N_{sr}} I_{rms_k}^2 \cdot R_{s_k} \quad (11)$$

where

N_{sr} is the total number of series resistive elements contributing to conduction losses in the valve, other than in the IGBTs and diodes;

I_{rms_k} is the rms current flowing in the k^{th} series resistive element for the relevant operating conditions;

R_{s_k} is the total resistance of the k^{th} series resistive elements in the valve contributing to other conduction losses.

6 DC voltage-dependent losses

The d.c. voltage-dependent losses of the valve are simply the U^2/R losses in resistive components connected in parallel with the valve or with parts of the valve.

In principle, the total d.c. voltage-dependent losses in the valve can be found by calculating the power dissipation in each resistive component connected in parallel with part or all of the valve and summing them.

$$P_{V4} = \sum_{k=1}^{N_{pr}} \frac{U_{rms_k}^2}{R_{dc_k}} \quad (12)$$

where

N_{pr} is the total number of parallel resistive elements contributing to d.c. voltage dependent losses in the valve;

U_{rms_k} is the rms value (including d.c. component) of the voltage across the k^{th} parallel resistive component in the valve;

R_{dc_k} is the resistance of the k^{th} parallel resistive component in the valve.

In an MMC valve these resistive components fall into two main categories: those that are connected in parallel with the d.c. capacitor of each MMC building block (such as capacitor discharge resistors) and those that are connected in parallel with the complete valve or large parts of the valve (for example water cooling pipes).

NOTE The power supply circuit for the valve electronics is equivalent to a parallel resistive load across part of the valve, but these circuits are not included in the assessment of d.c. voltage-dependent losses because they are separately accounted for under "valve electronics power consumption", 9.2.

7 Losses in d.c. capacitors of the valve

Power losses in the MMC d.c. capacitors of the valve cannot be neglected. They represent $I^2 \cdot R$ losses in the metallic components within the capacitor, chiefly the film metallisation and internal leads, and dielectric losses within the dielectric material.

The total d.c. capacitor losses per valve are then calculated as follows:

$$P_{V5} = \sum_{j=1}^{N_{cv}} I_{crms_j}^2 \cdot R_{ESR_j} \quad (13)$$

where

N_{cv} is the number of d.c. capacitors in the valve;

I_{crms_j} is the rms current flowing in the j^{th} d.c. capacitor of the valve;

R_{ESR_j} is the average equivalent series resistance of the j^{th} d.c. capacitor.

The rms current in the d.c. capacitor can be derived by the calculations of 5.2 and 5.3.

NOTE 1 The MMC building block capacitor can be a series connection of individual capacitor units. The equivalent series resistance of that series connection has to be considered for the calculations.

~~NOTE 2—Dielectric losses are normally most significant in a.c. applications where the capacitor voltage polarity reverses twice per cycle. For d.c. capacitors the voltage is usually non-reversing and dielectric losses are therefore small, but depending on the capacitor technology used, they can be non-negligible.~~

NOTE 3 2 There can also be a third component of loss caused by the finite insulation resistance of the dielectric material, but this is normally very small. It is covered by d.c. voltage-dependent losses as described in the preceding subclause.

NOTE 4 3 Losses in balancing resistors in parallel with capacitor units connected in series are covered by d.c. voltage-dependent losses as described in the preceding subclause.

8 Switching losses

8.1 General

The devices in the MMC building block will be stressed with current and voltage during switching events. How the event will occur is dependent on the operational mode of the system. Because of the cyclic charging and discharging of the capacitor, each switching event occurs at a different voltage. The instances for switching can vary much dependent on ~~control~~ **principles switching regime** and a general formula to be applied at any type of converter valve is not feasible.

The integration time shall be at least one second in order to ensure reliable results also for control strategies where the switching pattern varies from one fundamental period to the next.

As input data from device characterisation, typical values representative for the whole population shall be used for E_{on} , E_{off} and E_{rec} .

8.2 IGBT switching losses

The total IGBT switching losses per valve are calculated by summing all the turn-on energies E_{on} and the turn-off energies E_{off} for all of the VSC valve levels in the valve, and for both T1 and T2 over an integration time t_i .

$$P_{V6} = \frac{1}{t_i} \cdot N_c \cdot \sum_{j=1}^{N_{tc}} \sum_{k=1}^{N_s} [E_{on,T1_j,k} + E_{on,T2_j,k} + E_{off,T1_j,k} + E_{off,T2_j,k}] \quad (14)$$

where

- N_{tc} is the number of MMC building blocks per valve;
- N_c is the number of series-connected semiconductor devices per switch position;
- N_s is the number of switching cycles (on or off) experienced by each VSC valve level during the integration time t_i ;
- $E_{on,T1_j,k}$ is the turn-on energy dissipated in IGBT T1 in the j^{th} MMC building block for the k^{th} turn-on event for the relevant operating conditions (voltage, current and junction temperature);
- $E_{on,T2_j,k}$ is the turn-on energy dissipated in IGBT T2 in the j^{th} MMC building block for the k^{th} turn-on event for the relevant operating conditions (voltage, current and junction temperature);
- $E_{off,T1_j,k}$ is the turn-off energy dissipated in IGBT T1 in the j^{th} MMC building block for the k^{th} turn-off event for the relevant operating conditions (voltage, current and junction temperature);
- $E_{off,T2_j,k}$ is the turn-off energy dissipated in IGBT T2 in the j^{th} MMC building block for the k^{th} turn-off event for the relevant operating conditions (voltage, current and junction temperature);
- t_i is the integration time used in the simulation;
- t_i shall not be less than 1 s.

For parallel connected semiconductors, the current sharing may be calculated on the basis of the forward characteristics of the semiconductors (usually an equal current sharing).

8.3 Diode switching losses

The total diode switching losses per valve are then calculated by summing all the recovery energies E_{rec} for all of the valve levels in the valve, and for both D1 and D2, over a defined integration time t_i .

$$P_{V7} = \frac{1}{t_i} \cdot N_c \cdot \sum_{j=1}^{N_{tc}} \sum_{k=1}^{N_s} (E_{\text{rec,D1}_j,k} + E_{\text{rec,D2}_j,k}) \quad (15)$$

where

- N_{tc} is the number of MMC building blocks per valve;
- N_c is the number of series-connected semiconductor devices per switch position;
- N_s is the number of switching cycles (on or off) experienced by each VSC valve level during the integration time t_i ;
- $E_{\text{rec,D1}_j,k}$ is the diode recovery energy dissipated in diode D1 in the j^{th} MMC building block for the k^{th} diode turn-off event for the relevant operating conditions (voltage, current and junction temperature);
- $E_{\text{rec,D2}_j,k}$ is the diode recovery energy dissipated in diode D2 in the j^{th} MMC building block for the k^{th} diode turn-off event for the relevant operating conditions (voltage, current and junction temperature);
- t_i is the integration time used in the simulation.

t_i shall not be less than 1 s.

For parallel connected semiconductors, the current sharing may be calculated on the basis of the forward characteristics of the semiconductors (usually an equal current sharing).

9 Other losses

9.1 Snubber circuit losses

Valves for modular multi-level converters are frequently not provided with snubber circuits; however this clause will provide general guidance to the method to be used to calculate the losses in snubber circuits where these are provided.

In case of using RC snubbers or other kind of snubbers (RCD and so on) in a design for Modular Multi-level Converters the losses in the resistor shall be included in the calculation.

The losses can be calculated as the energy in the snubber capacitor multiplied by the number of charge/discharging events that happen during the integration time. This is however very conservative for snubbers with very short time constant, since in this case part of the snubber capacitor energy will appear as additional switching energy in the IGBT.

NOTE Including a snubber parallel to a VSC valve level influences the turn-on/turn-off behaviour of the IGBT/diode which means that the snubber circuits ~~are~~ shall be correctly represented during the characterisation tests on the semiconductor devices.

To get a more realistic value, it is needed to do a simulation of the real snubber and evaluate it together with the switching times of the circuit and the switching energies.

$$P_{V8} = \frac{1}{t_i} \cdot \sum_{j=1}^{N_{sn}} \sum_{k=1}^{N_s} (E_{\text{sn_on}_j,k} + E_{\text{sn_off}_j,k}) \quad (16)$$

where

N_{sn}	is the number of snubber circuits per valve;
N_{s}	is the number of switching cycles (on or off) experienced by each VSC valve level during the integration time t_i ;
$E_{\text{sn,on}_j,k}$	is the energy dissipated in the snubber resistor of the j^{th} snubber circuit for the k^{th} turn-on event for the relevant operating conditions (voltage, and current where relevant to the design of the snubber);
$E_{\text{sn,off}_j,k}$	is the energy dissipated in the snubber resistor of the j^{th} snubber circuit for the k^{th} turn-off event for the relevant operating conditions (voltage, and current where relevant to the design of the snubber);
t_i	is the integration time used in the simulation.

t_i shall not be less than 1 s.

$E_{\text{sn,on}_j,k}$ and $E_{\text{sn,off}_j,k}$ may be derived either by calculation based on the design of the snubber circuit or by measurement as part of the IGBT and diode characterisation testing.

9.2 Valve electronics power consumption

9.2.1 General

The valve electronics consist of local IGBT gate drive units together with their associated auxiliary circuits for power supply, measurement, monitoring etc. In most cases, the power supply takes the power from the main circuit and feeds the valve electronics. Then, the power consumption of the valve electronics is given by measuring the power input to the power supply.

The gate circuit applies positive and negative voltages to the gate terminal of the IGBT for turn-on and turn-off respectively. At the instant of gate voltage application, some charge or discharge current flows in the gate capacitance and small amount of energy is consumed. The amount of the gate current is affected by the current flowing through the IGBT. Since the power is defined as energy per second, then, the gate power is also affected by the switching frequency of the IGBT.

NOTE Power consumption of valve electronics is generally small when IGBTs are used, but in the event that other types of semiconductor devices are used, such as gate turn-off thyristors (GTOs) or integrated gate-commutated thyristors (IGCTs), the power consumption can be significantly greater because of the much larger turn on and turn off energy required for the gate circuit.

Since the IGBTs in the modular multi-level converter are controlled individually, the instantaneous valve level power consumption varies from IGBT to IGBT, similar to the conduction loss or the switching loss already described in Clauses 5 and 8. Then, the averaging process is again required to evaluate the valve electronics power consumption.

The power consumption of each valve electronics unit should be determined by direct measurement on a **sample of real valve electronics unit** under representative switching conditions (voltage, current, switching frequency etc). **Tests shall be performed on a minimum quantity of valve electronics units equivalent to five submodules or 10 VSC valve levels (for the CTL design)**. As noted above, the measurement should be averaged over a period of at least one second, in order to smooth out the variations which take place from cycle to cycle. The measurement may be performed either with the valve electronics connected to a real IGBT or to a dummy capacitive load representing the gate capacitance of a worst-case IGBT.

The total valve electronics power consumption per valve is calculated by summing up the valve electronics power consumption per valve level.

Two basic methods exist for deriving the power supply for the valve electronics:

- type A: from the off-state voltage across each IGBT;
- type B: from the MMC building block d.c. capacitor.

9.2.2 Power supply from off-state voltage across each IGBT

In case that the power is derived from the off-state voltage across each IGBT, the total power consumption of the valve electronics is calculated by the following equation.

$$P_{V9} = \sum_{j=1}^{N_{tc}} \sum_{k=1}^{N_c} P_{GU_j,k} \quad (17)$$

where

N_{tc} number of MMC building blocks per valve;

N_c number of series-connected semiconductor devices per switch position;

$P_{GU_j,k}$ is the average power input to the power supply of k^{th} IGBT in j^{th} MMC building block.

The average power input to the power supply is calculated by the following equation.

$$P_{GU_j,k} = \frac{1}{t_i} \cdot \int_0^{t_i} p_{GU_j,k}(t) dt \quad (18)$$

where

$p_{GU_j,k}(t) = u_{GU_j,k}(t) \cdot i_{GU_j,k}(t)$, and

$p_{GU_j,k}(t)$ is the instantaneous power input to the power supply of k^{th} IGBT in j^{th} MMC building block;

$u_{GU_j,k}(t)$ is the instantaneous voltage input to the power supply of k^{th} IGBT in j^{th} MMC building block;

$i_{GU_j,k}(t)$ is the instantaneous current input to the power supply of k^{th} IGBT in j^{th} MMC building block;

t_i is the integration time used in the simulation.

t_i shall not be less than 1 s.

NOTE Where the valve electronics derives its power from a passive snubber circuit, the power consumption of the valve electronics can already be counted in the losses of the snubber circuit as described in the previous subclause.

9.2.3 Power supply from the d.c. capacitor

In case that the power is derived from d.c. capacitor terminals in the MMC building block, the total power consumption of the valve electronics is calculated by the following equation.

$$P_{V9} = \sum_{j=1}^{N_{tc}} P_{GU_j} \quad (19)$$

where

N_{tc} is the number of MMC building blocks per valve;

P_{GU_j} is the average power input to the power supply in j^{th} MMC building block.

The average power input to the power supply is calculated by the following equation.

$$P_{GU_j} = \frac{1}{t_i} \cdot \int_0^{t_i} p_{GU_j}(t) dt \quad (20)$$

where

$$p_{GU_j}(t) = u_{GU_j}(t) \cdot i_{GU_j}(t) \text{ and}$$

$p_{GU_j}(t)$ is the instantaneous power input to the power supply in j^{th} MMC building block;

$u_{GU_j}(t)$ is the instantaneous voltage input to the power supply in j^{th} MMC building block;

$i_{GU_j}(t)$ is the instantaneous current input to the power supply in j^{th} MMC building block;

t_i is the integration time used in the simulation.

t_i shall not be less than 1 s.

10 Total valve losses per HVDC substation

The total losses per valve are calculated by summing the contributions P_{V1} to P_{V9} :

$$P_{VT} = \sum_{i=1}^9 P_{Vi} \quad (21)$$

The total VSC valve losses per converter substation are equal to the losses per valve, P_{VT} multiplied by the number of valves in the converter substation.

Not all contributions to the valve losses are present in every operational mode. They may also need to be calculated with different input data dependent on operation mode. Table 1 below shows which loss contributions to apply in each state.

The total losses in the operating state include the losses appearing in no-load and/or standby states. It is not correct to add the no-load or standby losses to the operating state losses, since this would imply that the no-load or standby losses are counted twice.

Table 1 – Contributions to valve losses in different operating modes

	Operating state losses (deblocked valve with load)	Idling operating state losses (deblocked valve without load)	No-load operating state losses (blocked valve)
P_{V1} IGBT conduction losses	X	X ^a	^b
P_{V2} diode conduction losses P_{V2}	X	X ^a	^b
P_{V3} other valve conduction losses	X	X ^a	^b
P_{V4} d.c. voltage-dependent losses	X	X	X
P_{V5} d.c. capacitor losses	X	X	X
P_{V6} IGBT switching losses	X	X ^a	^b
P_{V7} diode turn-off losses	X	X ^a	^b
P_{V8} snubber losses	X	X ^a	X ^b
P_{V9} valve electronics power consumption	X	X	X
P_{Vt} total valve losses	Total losses in operating state	Total losses in idling operating state	Total losses in no-load operating state
^a Idling state is defined as deblocked valve. Here some current and switching can occur. The losses will depend very much on the control strategy, how the switching occur and at what current level. It may be at a different switching frequency and with a different harmonic content than at operating load. The fundamental current is only required to balance the reactive power generated by the filters, if any. ^b At no-load state in principle no switching shall occur as the valve is blocked. However in some designs it may be necessary to make occasional switching operations to balance voltages between different parts of the converter. Here some losses may occur and need to be accounted for.			

Annex A (informative)

Description of power loss mechanisms in MMC valves

A.1 Introduction to MMC Converter topology

Modular multi-level converters (MMC), including the cascaded two level converter (CTL) are a family of converters whereby each valve is a controllable voltage source. They use a large number of relatively small, two-terminal controllable voltage sources connected in series in each valve. Two series-connected valves form a “Phase Unit” and are used to connect each a.c. phase to the d.c. terminals of the converter. Each phase unit can synthesise a stepped voltage waveform that can be controlled in amplitude and phase independently of the other phase units in the converter.

The CTL converter is distinguished from other types of MMC by using two or more IGBTs connected in series in each switch position. Figure A.1 and Figure A.2 show the main differences between the MMC with submodules (without series-connection of IGBTs), and MMC with CTL, illustrated for the most common variant of each type, the “half-bridge” configuration.

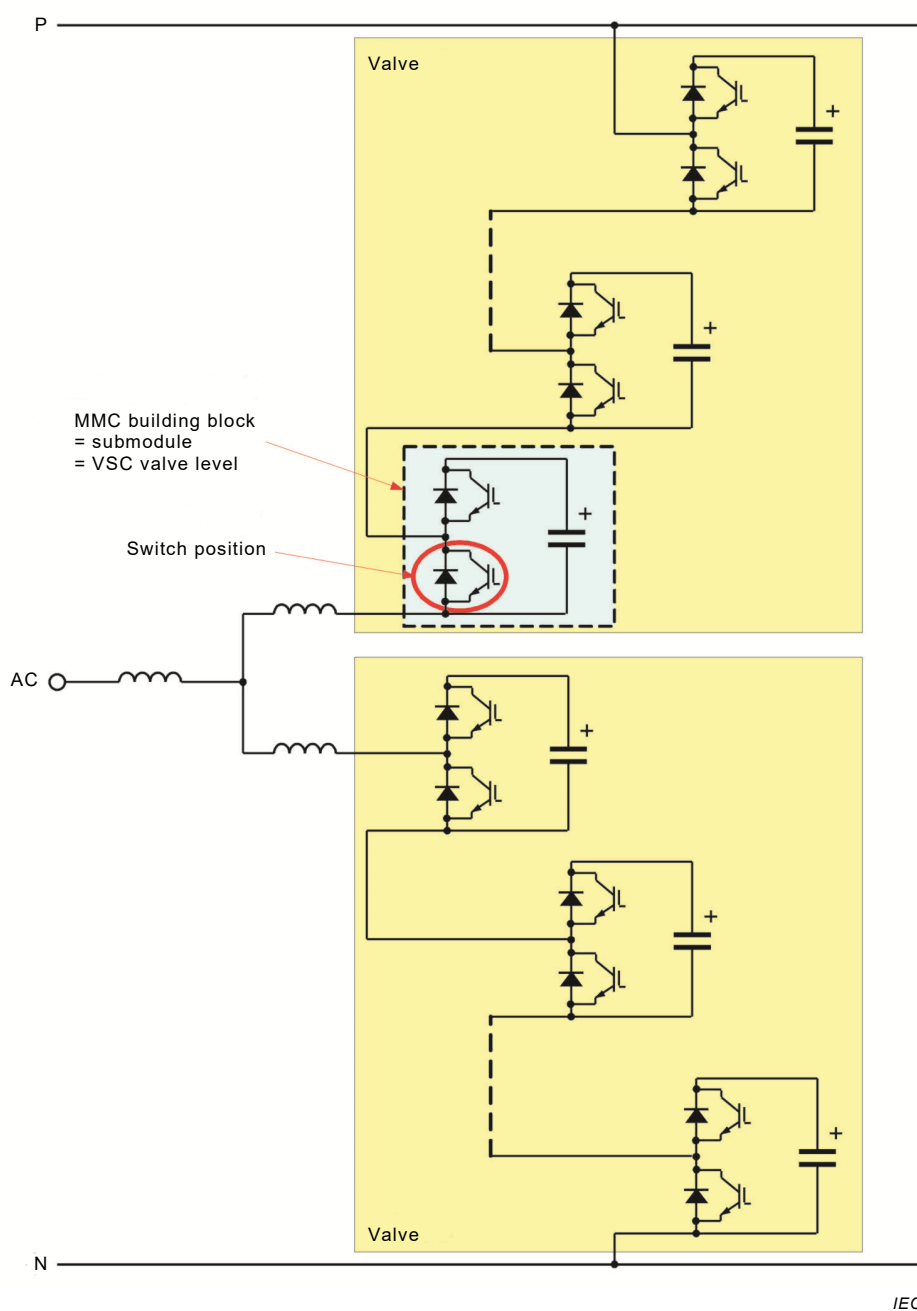


**Figure A.1 – Phase unit of the modular multi-level converter (MMC)
in basic half-bridge, two-level arrangement, with submodules**

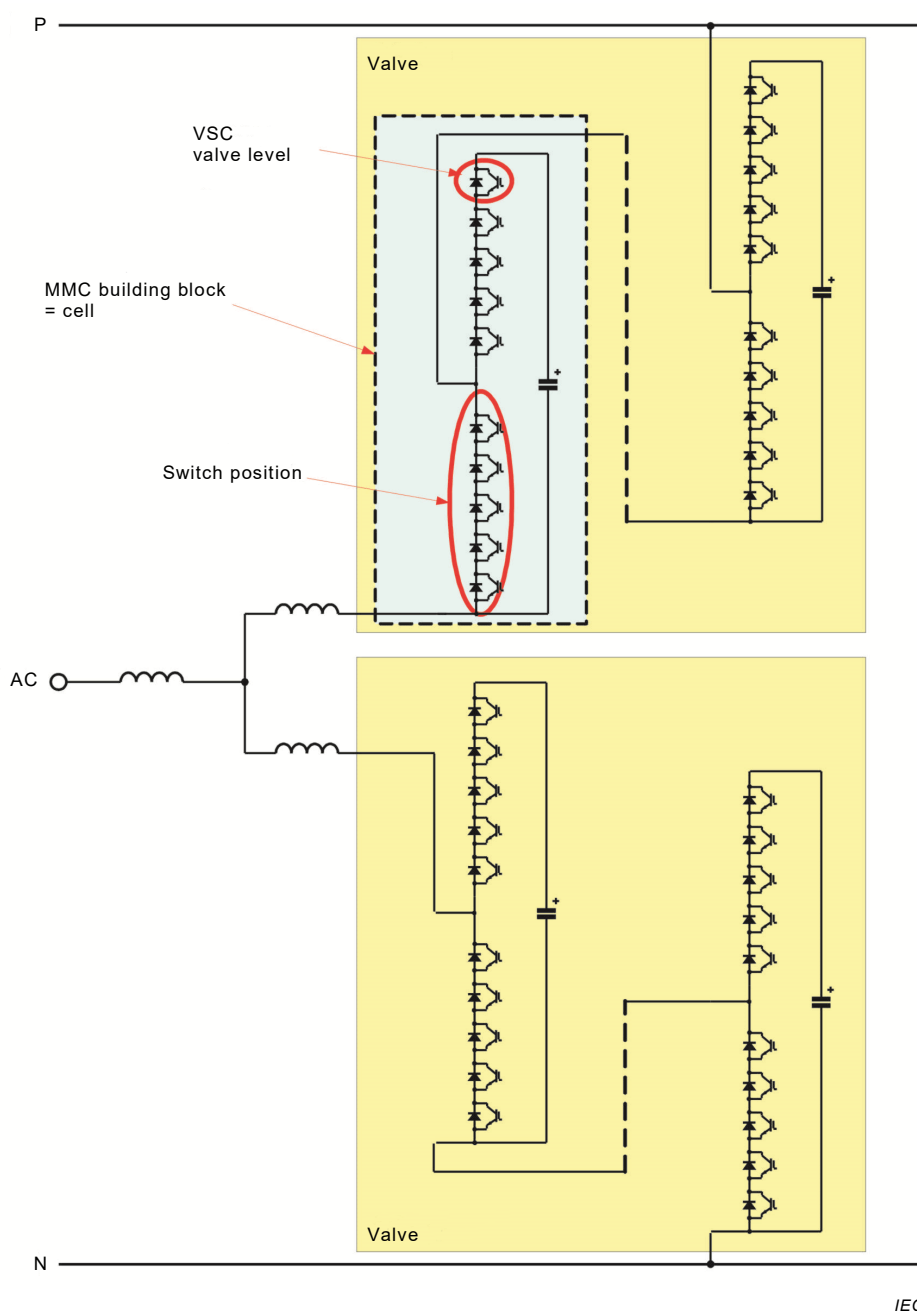


Figure A.2 – Phase unit of the cascaded two-level converter (CTL) in half-bridge form

The output voltage produced by each valve is an offset sinusoidal voltage with a mean value equal to half the d.c. line to line voltage, and the two valves in each phase unit are controlled such that the a.c. components of their output voltages are 180° out of phase (Figure A.3). In this way, the sum of the two valve voltages is almost a pure d.c. voltage (equal to the d.c. line to line voltage of the converter), and the difference between the two valve voltages is an almost pure a.c. voltage representing the a.c. output voltage of the converter.

The sum of the two valve voltages in each phase needs to be controlled accurately, in real time, to be equal to the converter d.c. voltage. However, since the complete converter consists of three phase units connected in parallel to a common d.c. bus, “valve reactors” need to be connected in series with each valve in order to prevent excessive circulating currents between phases caused by the inevitable slight errors in controlling the d.c. voltages of the three phase arms.

The operation of the converter, in so far as it affects the power losses in the valves, is described in the following Clauses A.2 to A.5 for the most commonly used variant of this family of converters, the MMC topology using “half-bridge”, two-level submodules, without series-connection of IGBTs. Other variants are possible, and their main differences are discussed, along with the CTL topology, in Clause A.6.

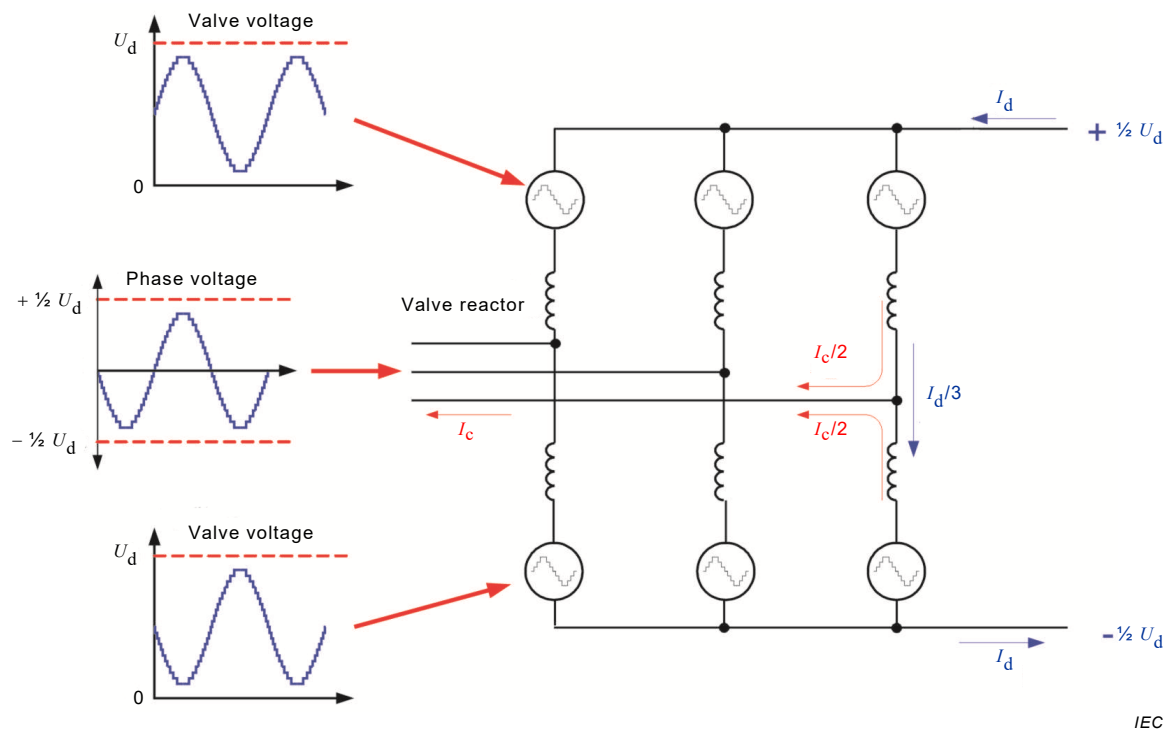


Figure A.3 – Basic operation of the MMC converters

A.2 Valve voltage and current stresses

A.2.1 Simplified analysis with voltage and current in phase

In contrast to converter topologies of the “controllable switch” type, such as the 2-level converter, or the classic “Grätz” bridge used in line-commutated converter HVDC systems, the MMC topology has the unusual feature that all six valves in the converter conduct current all the time.

Figure A.3 shows that the current flowing from each a.c. terminal of the converter splits into two equal parts – one flowing through the upper valve of that phase unit; the other flowing through the lower valve of the phase unit. Similarly the d.c. current splits into three equal branches flowing through each of the phase units. As a result, each valve carries a current equal to one third of the d.c. current plus half of the a.c. current of its associated phase, giving an offset sinusoidal current with a mean value of $I_d/3$.

Figure A.4 shows the typical waveforms of valve voltage and current. The condition shown on Figure A.4 applies when the converter a.c. output voltage and a.c. current are in phase, which means that the valve voltage and valve current are 180° out of phase. Hence, when the valve voltage is at its minimum, valve current is at its peak. This is approximately true when the converter is being used for transmitting active power only, without reactive power generation or absorption. However, even when the converter is not generating or absorbing reactive power, the valve voltage and current will generally not be exactly 180° out of phase, because of the phase shift across the interface transformer and valve reactors. Nevertheless the 180° phase shift shown on Figure A.4 is a useful simplifying assumption in order to aid the understanding of the circuit.

It will also be noted from Figure A.4 that the valve voltage varies cyclically from just above zero to just below the d.c. line to line voltage. When “half-bridge” MMC building blocks are used, the valve voltage can never exceed U_d , nor fall below zero, otherwise the free-wheeling diodes in parallel with each IGBT will conduct. This is an important limitation of the half-bridge design.

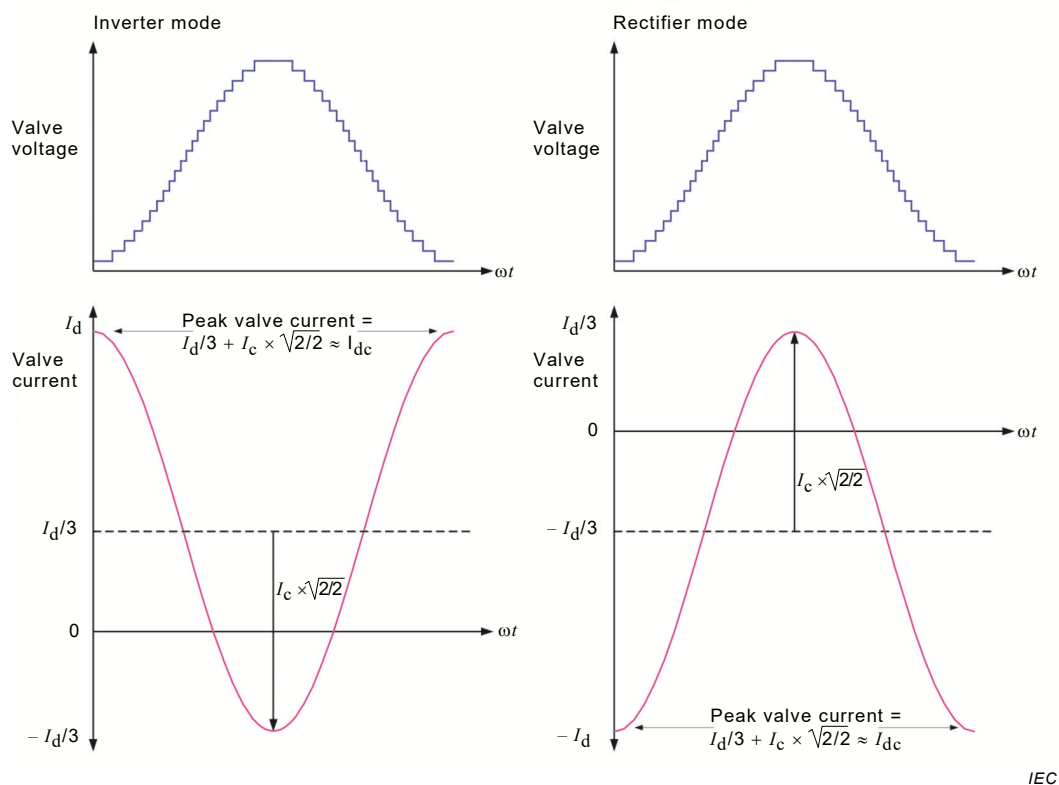


Figure A.4 – MMC converters showing composition of valve current

Optimum efficiency is obtained when the peak converter voltage is equal to $\frac{1}{2} U_d$. Operating with a peak converter voltage lower than $\frac{1}{2} U_d$ implies that the a.c. current has to be increased to reach the desired value of power; therefore, when “half-bridge” MMC building blocks are used, the controller usually attempts to keep the peak valve voltage just below U_d , so as to minimise the a.c. current (and hence the losses) required for a given amount of active power.

When the d.c. current is flowing into the positive d.c. terminal of the converter, as shown on Figure A.3, the converter is importing power to the a.c. network from the d.c. network and is therefore operating as an inverter. In rectifier operation, d.c. current flows out of the positive d.c. terminal and into the negative d.c. terminal.

In the remainder of this annex, the sign convention adopted is that the valve current is positive when it is flowing towards the negative d.c. terminal of the converter. This means that the valve current is mainly negative at a rectifier and mainly positive at an inverter.

A.2.2 Generalised analysis with voltage and current out of phase

In general, the converter a.c. voltage and a.c. current will not be exactly in phase, because of two effects:

- reactive power demand at the point of common connection with the a.c. system;
- the phase shift between the a.c. system voltage and the converter a.c. voltage.

A major advantage of VSC technology over LCC technology in HVDC is that the converter is inherently capable of generating or absorbing significant amounts of reactive power. Similarly to an electrical machine, the converter has various constraints which may limit the amount of reactive power available at a given operating point, such as an overall MVA limit, a (valve) current limit, a converter voltage limit (where “half-bridge” MMC building blocks are used), etc. Typically, purchasers of HVDC systems specify that the converter should be able to operate at full rated active power with a power factor ($\cos \varphi$) in the range 0,925 lagging to 0,925 leading, which equates to a phase shift of 22° and the generation or absorption of up to $\pm 0,4$ p.u. reactive power at rated active power. At lower values of active power, more reactive power is generally available and when the active power is zero, the converter can operate with a power factor of 0, becoming a STATCOM.

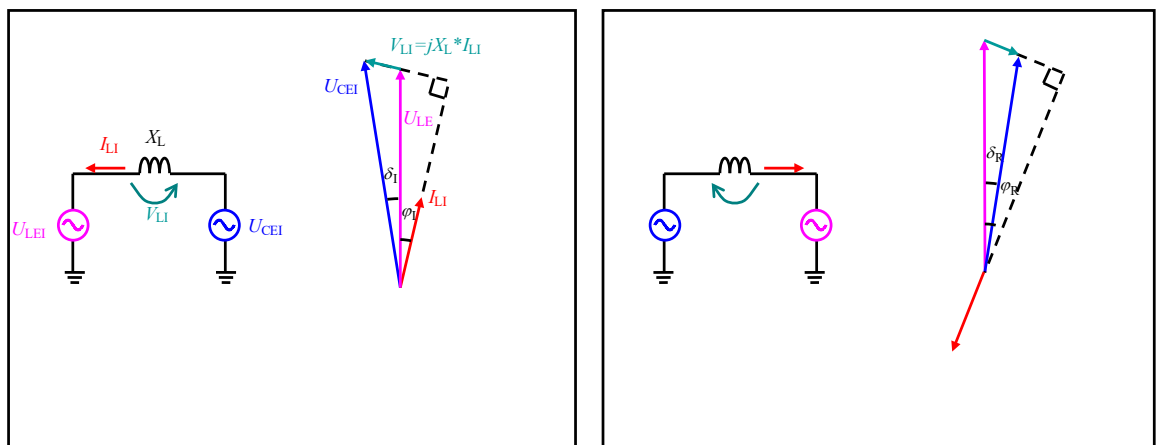
The phase shift between the a.c. system voltage and the converter a.c. voltage is equal to the phase shift across the interface transformer and valve reactors (the two valve reactors for a given phase are considered to be in parallel in this case). It is well known from a.c. power system theory that, under sinusoidal conditions, the active power flow through an inductance is related to the phase shift δ across the inductance, by the equation:

$$P = \frac{U_L \cdot U_C \cdot \sin \delta}{X_L} \quad (\text{A.1})$$

where U_L and U_C are the rms line to line voltages either side of the inductance and X_L is the inductive reactance.

At maximum rated power, $\sin \delta$ becomes approximately equal to the per-unit impedance of the interface transformer and valve reactors. Hence with a typical impedance of 0,15 p.u., the phase shift δ at rated power is typically in the range 8° to 9° .

The relationship between a.c. system voltage, converter a.c. voltage and converter current is best presented by a phasor diagram as in Figure A.5.



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Figure A.5 – Phasor diagram showing a.c. system voltage, converter a.c. voltage and converter a.c. current

A.2.3 Effects of third harmonic injection

The description above is based on the premise that the converter a.c. voltage is sinusoidal, or as close to sinusoidal as possible with the number of MMC building blocks available. However, a commonly used technique in many power electronic converters involves deliberately adding a proportion of third harmonic to the converter voltage. Actually, other odd multiples of 3rd harmonic can also be used, as for example 9th or 15th harmonics.

The advantage of this technique is that it can allow the peak of the fundamental component of the converter voltage to be higher than the peak of the actual converter voltage. This means that the peak of the fundamental component of the converter voltage can exceed the d.c. line to line voltage and allows a lower a.c. current to be used than would otherwise be possible, reducing the conduction losses of the converter. With 3rd harmonic, the maximum benefit is obtained when amplitude of the injected 3rd harmonic is 1/6 of the fundamental component. Because the injected harmonics are multiples of three, they cancel in the line-to-line voltage at the a.c. terminals of the converter; hence if the converter transformer has a delta secondary, the injected harmonics do not transfer to the connected power system.

Figure A.6 illustrates this technique, which is now becoming widespread in VSC HVDC converters because the significant reduction of a.c. current (of the order of 15 %) that it permits leads in turn to substantial reduction of conduction losses.

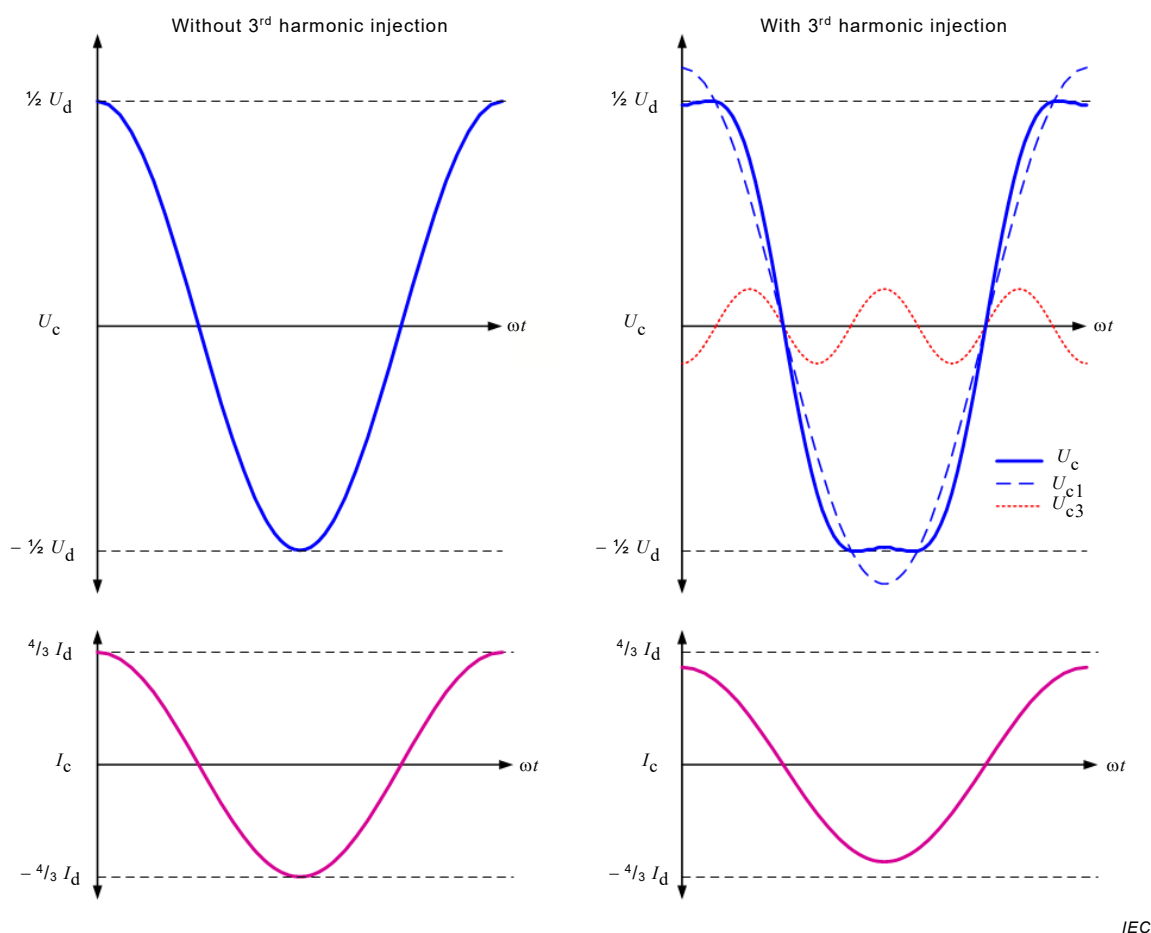


Figure A.6 – Effect of 3rd harmonic injection on converter voltage and current

A.3 Conduction losses in MMC building blocks

A.3.1 Description of conduction paths

Figure A.7 shows an MMC building block of a basic “half-bridge” MMC valve using a two-level converter arrangement. It will be seen that the MMC building block contains four main semiconductor devices: two IGBTs, T1 and T2, and two diodes D1 and D2.

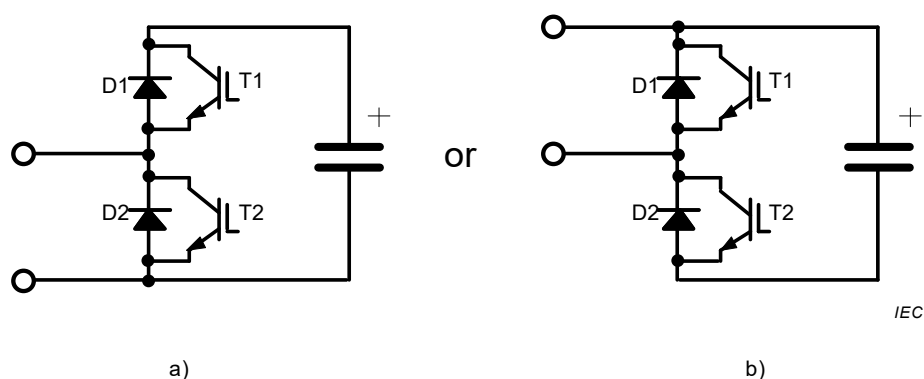


Figure A.7 – Two functionally equivalent variants of a “half-bridge”, two-level MMC building block

NOTE 1 Usually the IGBT and its anti-parallel diode are supplied as a single, integrated package.

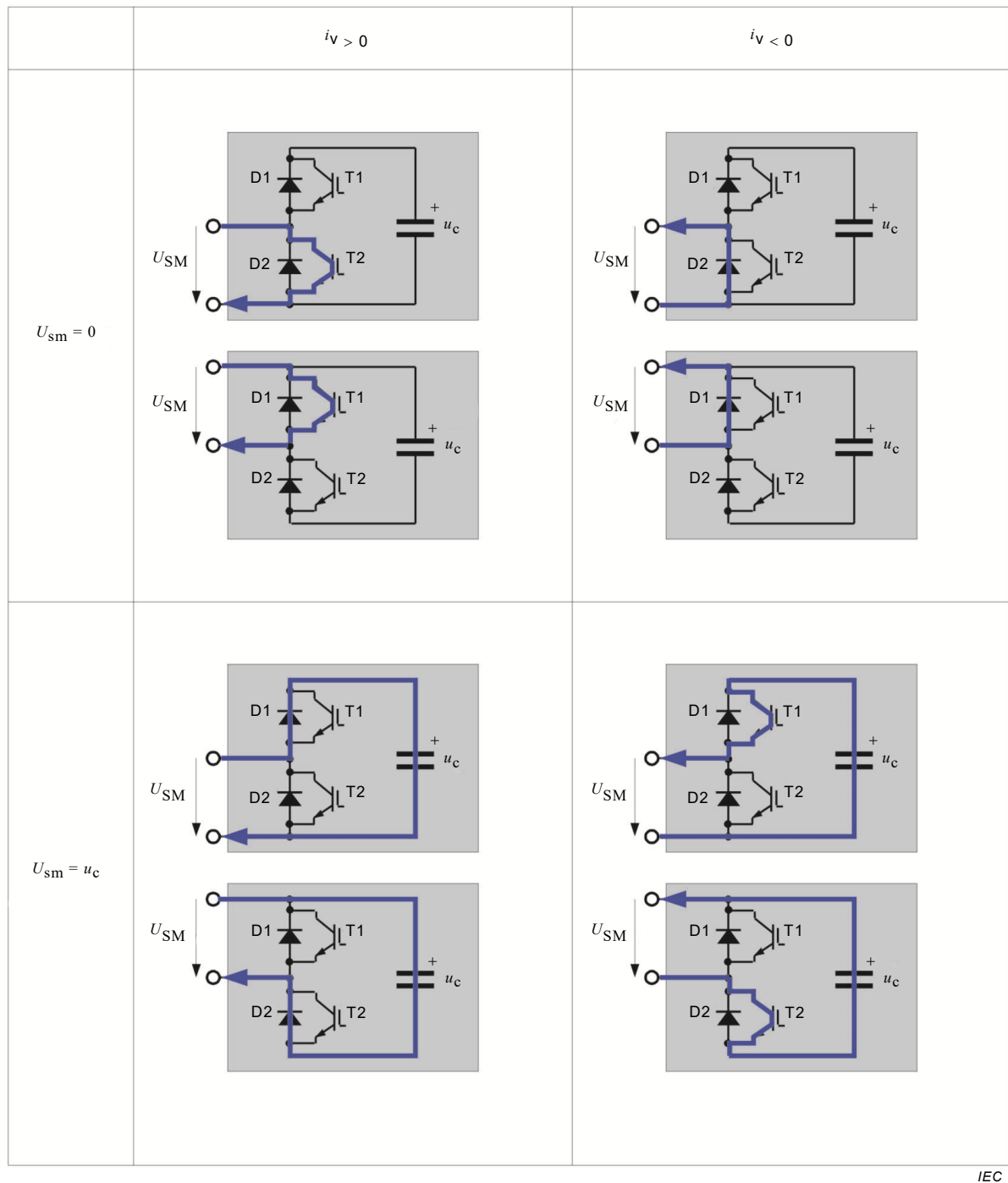
NOTE 2 An additional bypass thyristor can also be included for protection against fault currents, but this is usually arranged not to conduct current in steady-state operation and therefore contributes nothing to the losses of the converter.

Figure A.7 shows two variants of a half-bridge, two-level MMC building block which are functionally equivalent to each other. In both cases, the MMC building block has two possible operating states: bypassed and active. In Figure A.7 a), the bypassed mode is obtained by turning on IGBT T2 and active mode is obtained by turning on IGBT T1. In Figure A.7 b) the roles are reversed.

For the remainder of this annex, descriptions are based around the circuit shown in Figure A.7 a).

Since the valve carries current in both directions at different times, there are a total of four possible conducting states per MMC building block, listed below and shown on Figure A.8:

- negative current, bypassed: D2 conducting;
- negative current, active: T1 conducting;
- positive current, bypassed: T2 conducting;
- positive current, active: D1 conducting.



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Figure A.8 – Conducting states in “half-bridge”, two-level MMC building block

Figure A.9 illustrates how the patterns of conduction differ between rectifier and inverter operation.

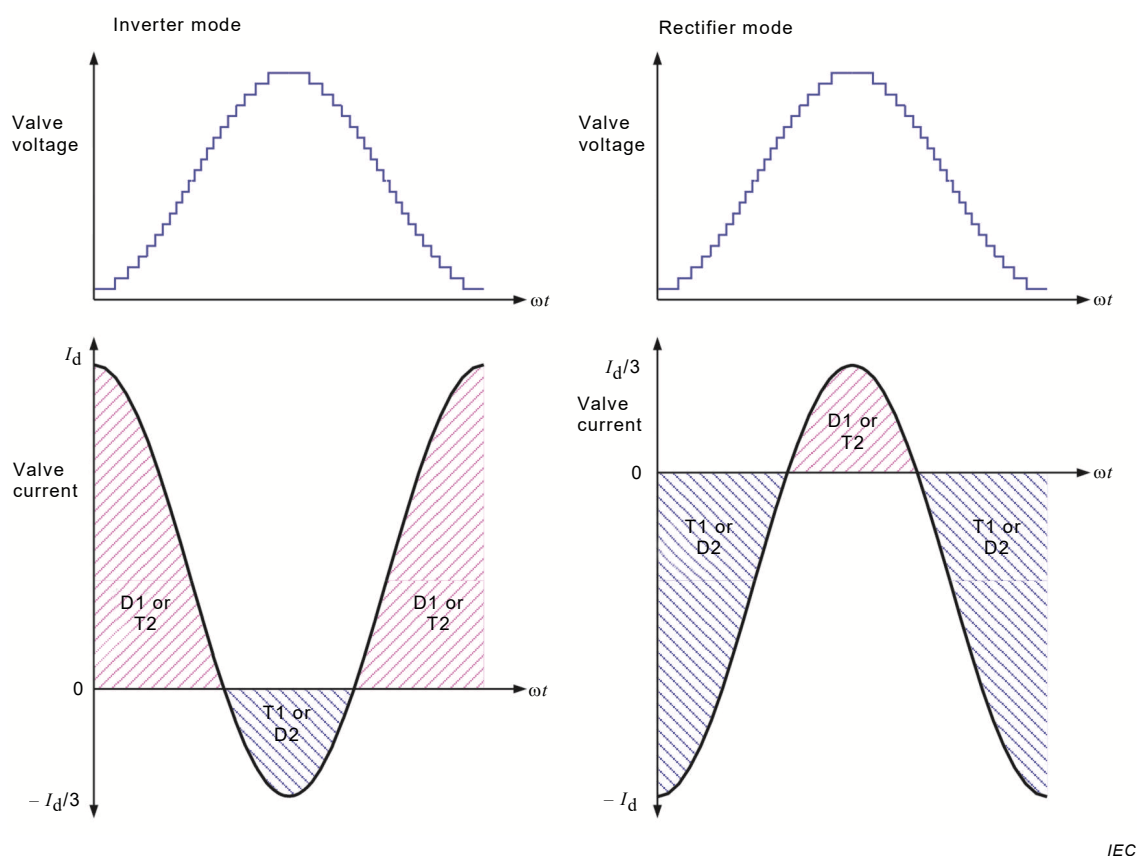


Figure A.9 – Typical patterns of conduction for inverter operation (left) and rectifier operation (right), based on the submodule configuration of Figure A.7 a)

An example of a converter with, for illustrative purposes, only one MMC building block per valve, is shown in Figure A.10 below.

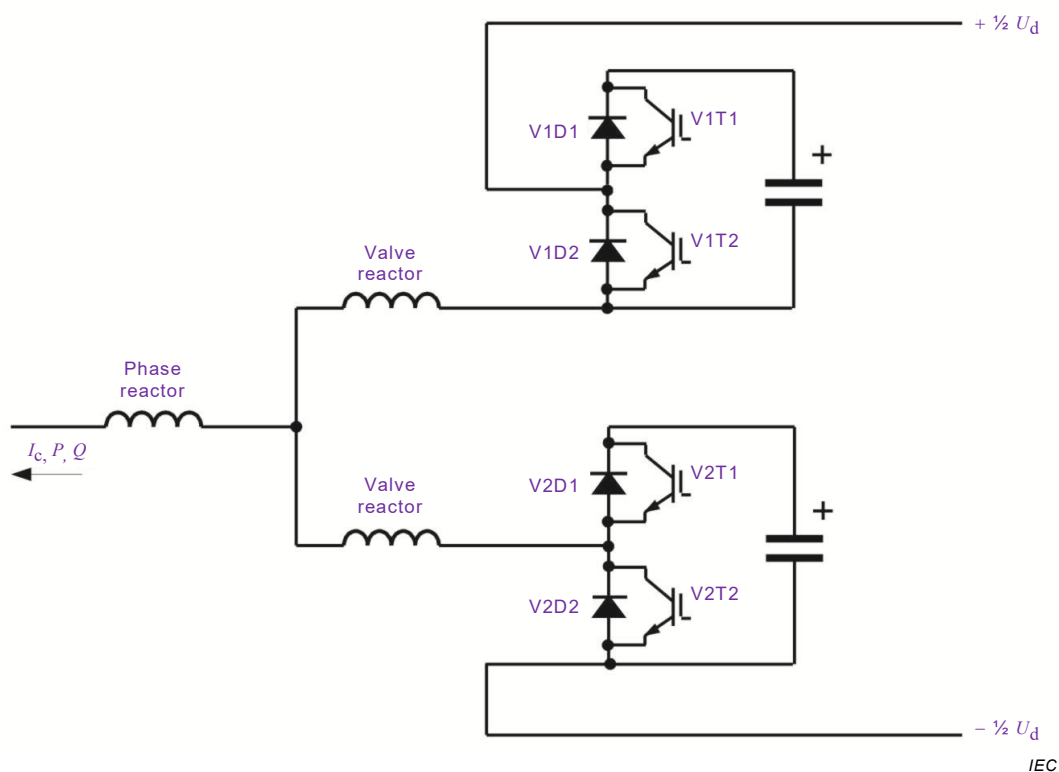


Figure A.10 – Example of converter with only one MMC building block per valve to illustrate switching behaviour

Inverter operation of this converter in a typical case is shown in an example in Figure A.11 and in rectifier operation in Figure A.12.

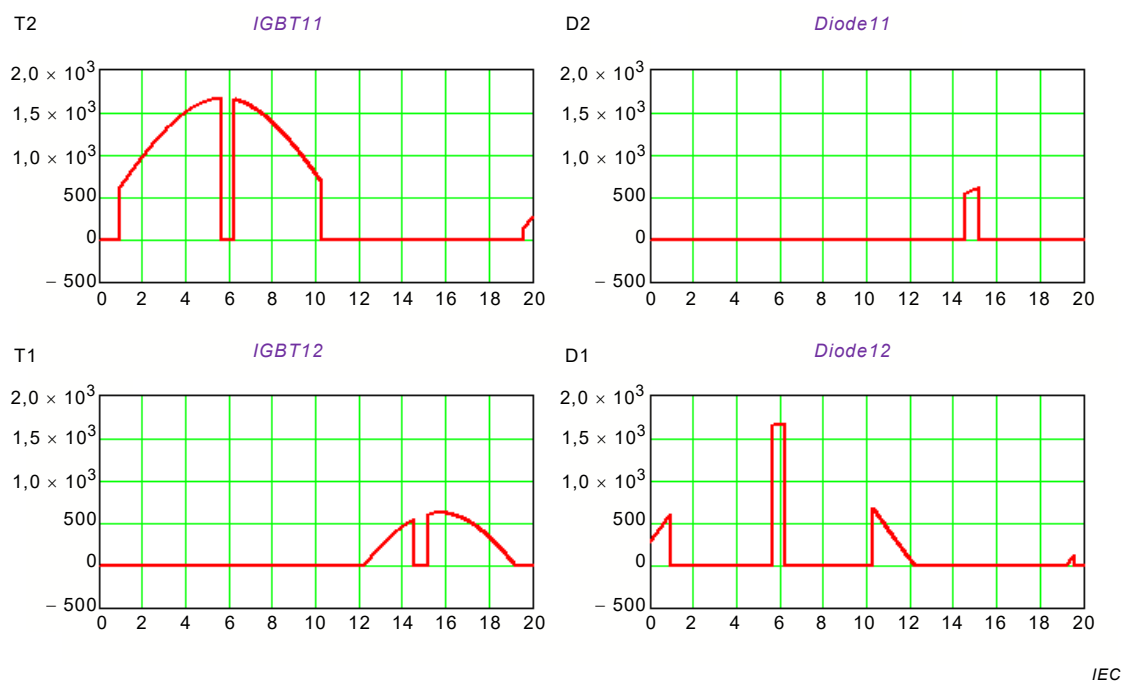


Figure A.11 – Inverter operation example of switching events

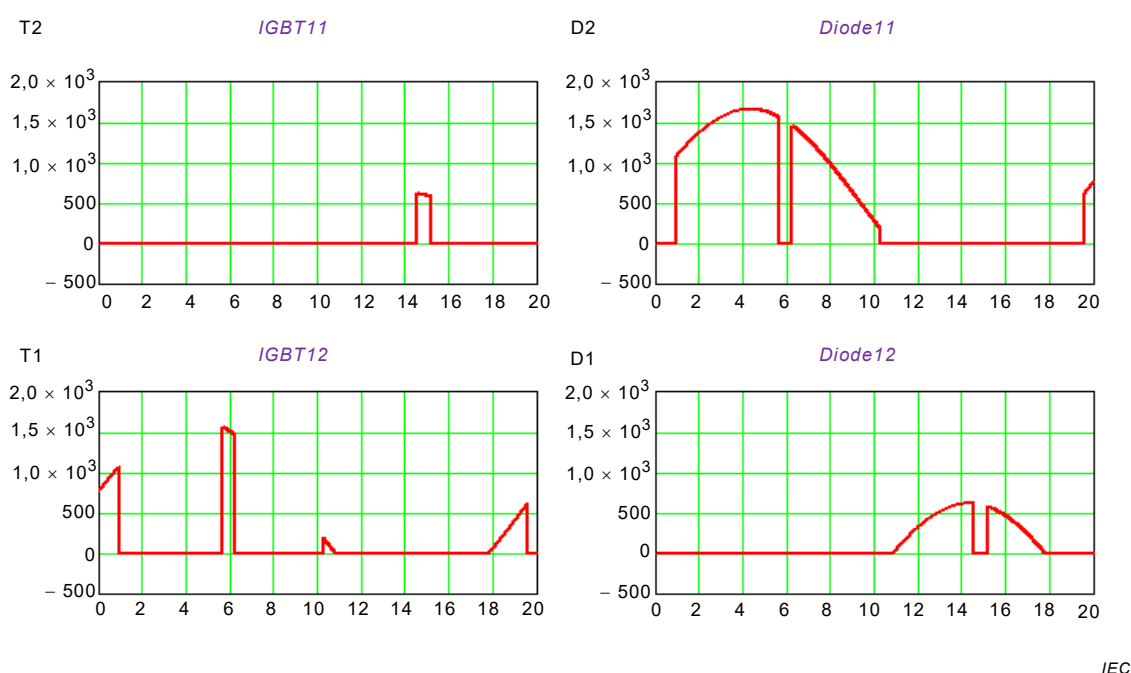


Figure A.12 – Rectifier operation example of switching events

As the two switches in each valve (S1 and S2 with its respective devices here denoted T1, D1 and T2, D2) are stressed with different current and switching events, they need to be calculated separately.

The time of the switching events and the amplitude of the current are dependent on the operational condition of the converter:

- a.c. voltage;
- d.c. voltage;
- active power;
- reactive power;
- modulation strategy.

All series connected MMC building blocks will be stressed with the same switching events, but at different occasions. Thus the same average and rms currents are valid for all MMC building blocks.

The upper valve arm and lower valve arms are also stressed in a similar way.

In rectifier mode, it can be seen that the highest currents flow in either T1 or D2. However, at the time when the current is highest, the valve voltage is near zero, so most MMC building blocks are bypassed and current flows predominantly in D2. D2 therefore has the highest conduction loss in rectifier mode, with only modest conduction losses in T1 and D1, and very low conduction losses in T2.

Conversely, in inverter mode, T2 experiences the highest conduction losses with only modest conduction losses in T1 and D1, and very low conduction losses in D2.

In Figure A.9 it can be seen that the peak valve current is approximately equal to the d.c. current; however this is in general not exactly the case, as the peak valve current may be higher or lower than the d.c. current, depending on the modulation strategy, amount of reactive power and transformer tapchanger position (if appropriate).

A.3.2 Conduction losses in semiconductors

A.3.2.1 Approximate analytical solution

It will be noted from Figure A.8 that at any time there is always one, and only one, current path conducting in each MMC building block.

If the on-state voltage characteristics of the four switch positions in the MMC building block were identical, calculation of the semiconductor device conduction losses would be straightforward, since there would be no need to know the operating state of the MMC building block at any time. The total semiconductor conduction loss per MMC building block would then simply be given by:

$$P_{\text{cond}} = N_c \left(V_0 \cdot I_{\text{vav}} + R_0 \cdot I_{\text{vrms}}^2 \right) \quad (\text{A.2})$$

where

N_c is the number of series-connected semiconductor devices per switch position;

V_0, R_0 are the threshold voltage and slope resistance of the device;

I_{vav} is the mean value of the rectified current in the valve, averaged over one power-frequency cycle (Figure A.13).

$$I_{\text{vav}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} |i_{\text{vtt}}(\omega t)| \cdot d(\omega t) \quad (\text{A.3})$$

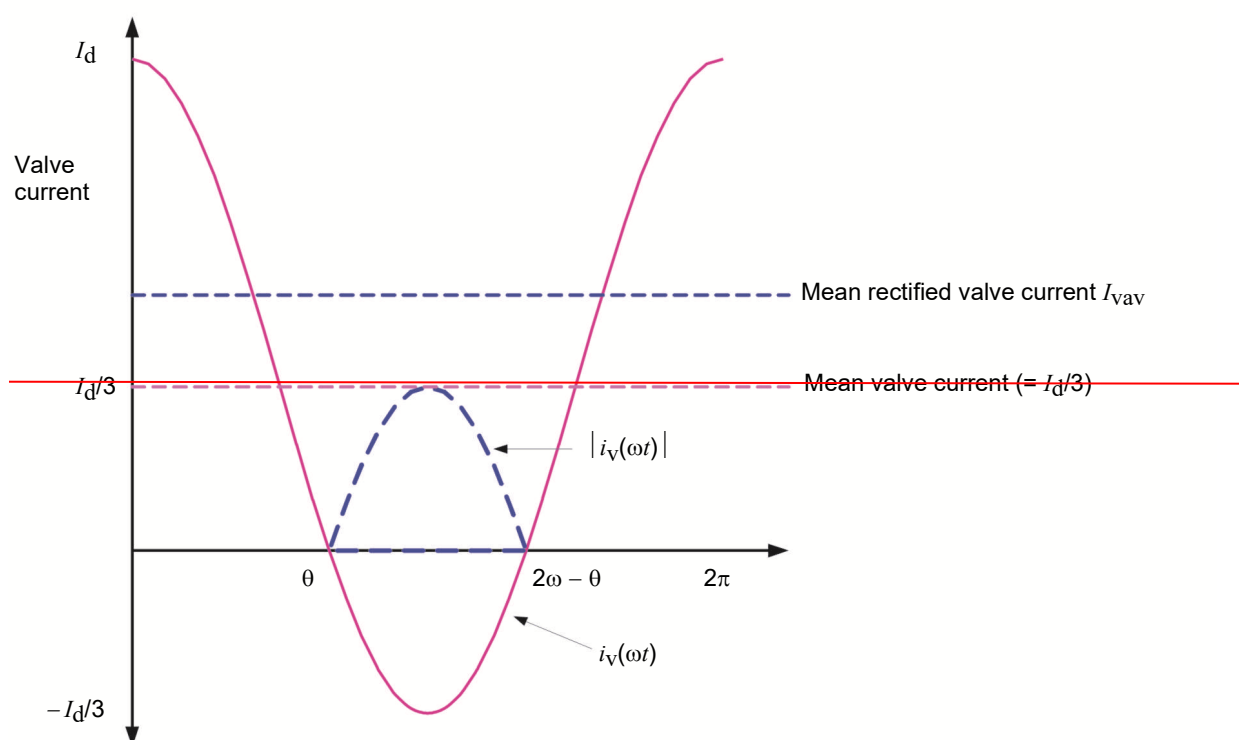
where

$i_{\text{vtt}}(\omega t)$ is the instantaneous current between the terminals of the valve.

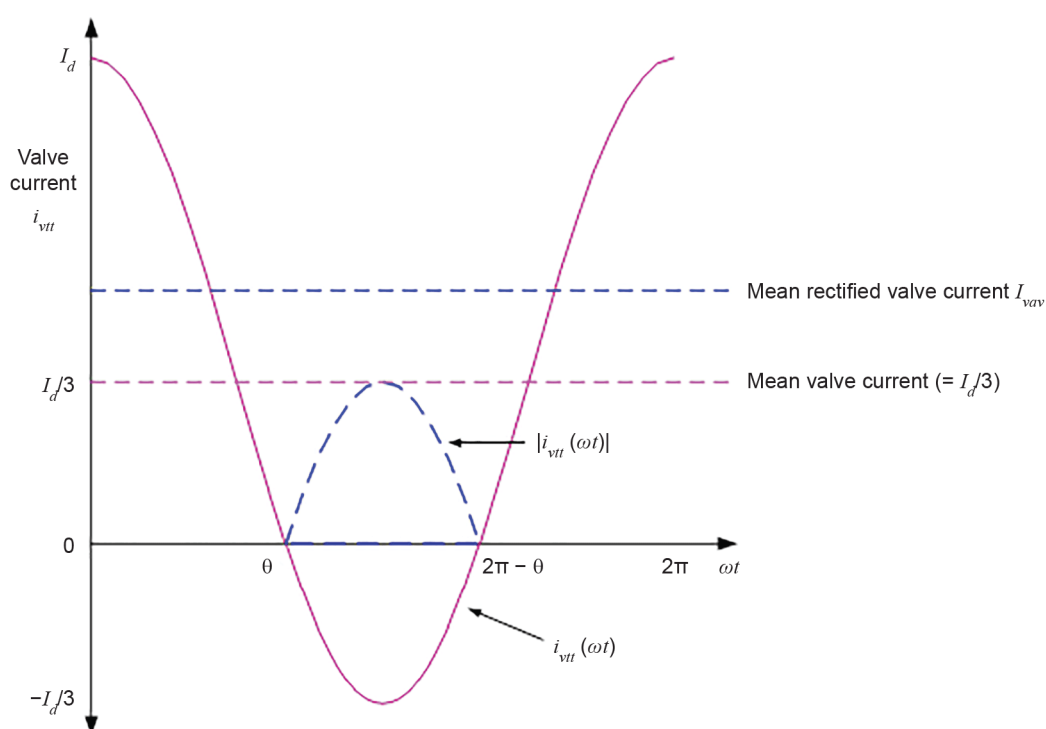
I_{vav} is not the same as the mean valve current, which is simply $I_d/3$. For these purposes, the rectified current is needed because current will only flow in those semiconductor device(s) which are forward biased.

I_{vrms} is the rms current in the valve, averaged over one power-frequency cycle.

$$I_{\text{vrms}} = \sqrt{\frac{1}{2\pi} \cdot \int_0^{2\pi} i_{\text{vtt}}(\omega t)^2 \cdot d(\omega t)} \quad (\text{A.4})$$



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Figure A.13 – Valve current and mean rectified valve current

Knowing that the valve current can be expressed as:

$$i_v(\omega t) = \frac{I_d}{3} + \frac{I_c \cdot \sqrt{2}}{2} \times \sin(\omega t) \quad (\text{A.5})$$

An analytical solution can easily be found:

$$I_{\text{vav}} = \frac{1}{\pi} \cdot \left[\frac{I_d}{3} \cdot (2\theta - \pi) + I_c \cdot \sqrt{2} \cdot \sin \theta \right] \quad (\text{A.6})$$

$$I_{\text{vrms}} = \sqrt{\frac{I_d^2}{9} + \frac{I_c^2}{4}} \quad (\text{A.7})$$

where

$$\theta = \cos^{-1} \left[\frac{-I_d \cdot \sqrt{2}}{3 \cdot I_c} \right] \quad (\text{A.8})$$

The angle θ corresponds to the point where valve current crosses zero.

Since the current flows mainly in diodes in rectifier mode, and mainly in IGBTs in inverter mode, a reasonable approximation to the conduction losses per MMC building block may be obtained from Equations (A.2), (A.6) and (A.7) as follows:

Rectifier mode:

$$P_{\text{cond_rec}} = V_{0_Diode} \cdot I_{\text{vav}} + R_{0_Diode} \cdot I_{\text{vrms}}^2 \quad (\text{A.9})$$

Inverter mode:

$$P_{\text{cond_inv}} = V_{0_IGBT} \cdot I_{\text{vav}} + R_{0_IGBT} \cdot I_{\text{vrms}}^2 \quad (\text{A.10})$$

A.3.2.2 **Exact Improved analytical solution**

The approximate analytical solution presented in the previous subclause assumes that V_0 and R_0 are the same for all the IGBTs and diodes in the MMC building block. Generally this is not true: the IGBTs normally have different values of V_0 and R_0 to the diodes (generally, V_0 and R_0 are higher for the IGBT than the diode) and it is possible for different types of IGBT and diode to be used in the upper and lower switch positions in the MMC building block. In addition, this approach neglects the circulating currents which may occur between phases, depending on the design of controller.

In many cases these assumptions could introduce an unacceptably large error into the calculation process.

A more exact process involves separately calculating the values of I_{av} and I_{rms} for each of the four switch positions in the MMC building block and thus calculating the conduction loss separately for each device.

As noted in the previous subclause, the location of the one switch position that is carrying current at a given time depends on the direction of the current and the switching state of the

MMC building block (bypassed or active state). Since the switching state may change several times per fundamental-frequency cycle, it is not practical to calculate the instantaneous conduction loss in each switch position, but neither is it necessary. What is needed is to calculate the conduction loss in each switch position averaged over a period of some few cycles or seconds. However, this is also not straightforward to calculate, since it depends in a complex way on the control strategy for the converter.

For some operating points, for example when the valve current and valve voltage are exactly 180° out of phase, an exact (though complex) analytical solution is possible. Such solutions rely on a statistical approach to the operating state (active or bypassed) of the MMC building block. Although it is not possible to know the exact operating state of an MMC building block at any given time, it is possible to calculate the probability that the MMC building block will be in a given state at that time, since the probability that the MMC building block is in the active state is directly proportional to the valve voltage. It is therefore possible to construct a mathematical equation linking the valve current to the valve voltage, both of which can be described mathematically.

The statistical probability that a given MMC building block will be in the active state can be expressed by the term $p_c(\omega t)$:

$$p_c(\omega t) = \frac{u_{vtt}(\omega t)}{N_{tc} \cdot u_{c_av}(\omega t)} \quad (\text{A.11})$$

where

N_{tc} is the number of MMC building blocks per valve;

~~$u_v(\omega t)$ is the valve voltage as a function of time;~~

$u_{vtt}(\omega t)$ is the valve terminal-to-terminal voltage as a function of time;

$u_{c_av}(\omega t)$ is the mean MMC building block d.c. capacitor voltage as a function of time.

The probability that a given MMC building block is in the bypassed state is then simply $(1 - p_c(\omega t))$.

T1 and D1 only conduct when the link is in the active state. So the average and rms currents are found by integrating the product of valve current and $p_c(\omega t)$ over the conduction period appropriate to each semiconductor.

$$I_{av} = \frac{1}{2\pi} \cdot \int_{\omega t_1}^{\omega t_2} i_{vtt}(\omega t) \cdot p_c(\omega t) \cdot d(\omega t) \quad (\text{A.12})$$

$$I_{rms} = \sqrt{\frac{1}{2\pi} \cdot \int_{\omega t_1}^{\omega t_2} i_{vtt}^2(\omega t) \cdot p_c(\omega t) \cdot d(\omega t)} \quad (\text{A.13})$$

where

ωt_1 and ωt_2 are the points at which the valve current changes sign.

T1 only conducts when current is negative. Hence for evaluation of the current in T1, ωt_1 is taken to be where current changes from positive to negative and ωt_2 is taken to be where current changes from negative to positive.

D1 only conducts when current is positive. Hence for evaluation of the current in D1, ωt_1 is taken to be where current changes from negative to positive and ωt_2 is taken to be where current changes from positive to negative.

T2 and D2 only conduct when the link is in the bypassed state. So the average and rms currents are found by integrating the product of valve current and $(1 - p_c(\omega t))$ over the conduction period appropriate to each semiconductor:

$$I_{av} = \frac{1}{2\pi} \cdot \int_{\omega t_1}^{\omega t_2} i_{vt}(\omega t) \cdot (1 - p_c(\omega t)) \cdot d(\omega t) \quad (A.14)$$

$$I_{rms} = \sqrt{\frac{1}{2\pi} \cdot \int_{\omega t_1}^{\omega t_2} i_{vt}^2(\omega t) \cdot (1 - p_c(\omega t)) \cdot d(\omega t)} \quad (A.15)$$

T2 only conducts when current is positive. Hence for evaluation of the current in T2, ωt_1 is taken to be where current changes from negative to positive and ωt_2 is taken to be where current changes from positive to negative.

D2 only conducts when current is negative. Hence for evaluation of the current in D2, ωt_1 is taken to be where current changes from positive to negative and ωt_2 is taken to be where current changes from negative to positive.

Even when it is possible to represent i_v and p_c mathematically, and even for the simplified case where the valve current and valve voltage are exactly 180° out of phase, the analytical solution to these equations is complex. At the time of publication, no exact analytical solution has been found for the general case where valve current and valve voltage are not exactly 180° out of phase.

A further improvement to the analytical calculation of semiconductor conduction losses can be made by using a more sophisticated approximation for the device on-state voltage instead of the piecewise-linear model using V_0 and R_0 . For example:

$$V_{ce(sat)}, V_f = A + B \cdot I + C \cdot \ln(I + 1) + D \cdot \sqrt{I} \quad (A.16)$$

However, this improved model comes at the price of increased simulation complexity and reduced transparency and should only be used when specifically agreed by the purchaser.

A.3.3 MMC building block d.c. capacitor losses

To calculate the MMC building block d.c. capacitor losses, it is necessary only to know the rms current in the capacitor, I_{crms} . The mean current in the capacitor is zero in steady-state:

$$I_{D1_av} + I_{T1_av} = 0 \quad (A.17)$$

Once the rms current has been determined for each of the four semiconductor devices, according to the preceding subclause, the rms capacitor current can be found easily from the vectorial sum of the rms currents in T1 and D1:

$$I_{crms} = \sqrt{I_{D1_rms}^2 + I_{T1_rms}^2} \quad (A.18)$$

A.3.4 Other conduction losses

Other conduction losses in the valve are dominated by the resistive (I^2R) losses in busbars from each MMC building block to its neighbours. Here, only the rms valve current I_{vrms} , as given in Equation (A.7), is required.

A.4 Switching losses

A.4.1 Description of state changes

A.4.1.1 General

Every time an MMC building block changes state from bypassed to active state or vice versa, or the direction of current reverses, one switch position in the MMC building block turns off and another turns on. The turn-on of an IGBT is always accompanied by the turn-off of a diode, and vice-versa.

Switching events may be categorised as “soft” or “hard”. Transitions which occur as a result of the reversal of valve current that occurs twice per cycle are referred to as “soft”, while those that occur as a result of state changes from bypassed to active state or vice versa, are referred to as “hard”. Only the hard switching events are of significance in the calculation of losses, because the rate of change of current (di/dt) is several orders of magnitude higher than for soft-switching events.

A.4.1.2 Hard switching events

Table A.1 summarises the effects of the four possible hard switching events in the MMC building block.

Table A.1 – Hard switching events

Current direction	MMC building block state change	Effects	Total switching energy
Negative	Bypassed to active	T1 turns on; D2 turns off	$E_{\text{on T1}} + E_{\text{rec D2}}$
Negative	Active to bypassed	T1 turns off; D2 turns on	$E_{\text{off T1}}$
Positive	Bypassed to active	T2 turns off; D1 turns on	$E_{\text{off T2}}$
Positive	Active to bypassed	T2 turns on; D1 turns off	$E_{\text{on T2}} + E_{\text{rec D1}}$

Since diodes are not controllable, hard switching events are always initiated by the switching of an IGBT. The transition from IGBT to diode is initiated by turning off the IGBT while current is flowing in it. The current, which is flowing through a substantial external inductance, then has nowhere else to flow except into the diode in the other switch position of the MMC building block. Current then commutates from the IGBT to the diode at a rate determined by the inductance of the loop formed by the IGBT, diode and capacitor. The IGBT experiences a voltage overshoot as a result of this event.

The transition from diode to IGBT is initiated by turning on the IGBT while the diode in the other switch position of the MMC building block is conducting. This temporarily creates a short circuit with the d.c. capacitor connected in series with the diode and the IGBT that has just turned on. The current in the diode falls very rapidly at a rate given by the capacitor voltage divided by the inductance of the loop formed by the IGBT, diode and capacitor. After the current in the diode passes through zero, the diode experiences a short period of reverse current and then finally turns off, incurring a “recovery energy”.

Each hard switching event results in a switching energy dissipation in the IGBT (E_{on} or E_{off}) and those events that involve the turn-off of a diode also result in a recovery energy E_{rec} (diodes have negligible turn-on loss). E_{on} , E_{off} and E_{rec} depend on the instantaneous device

current at the time of switching, the d.c. capacitor voltage and the junction temperature. The dependence on current is illustrated on Figure A.14. Switching and recovery energies also increase with voltage (almost linearly) and with temperature.

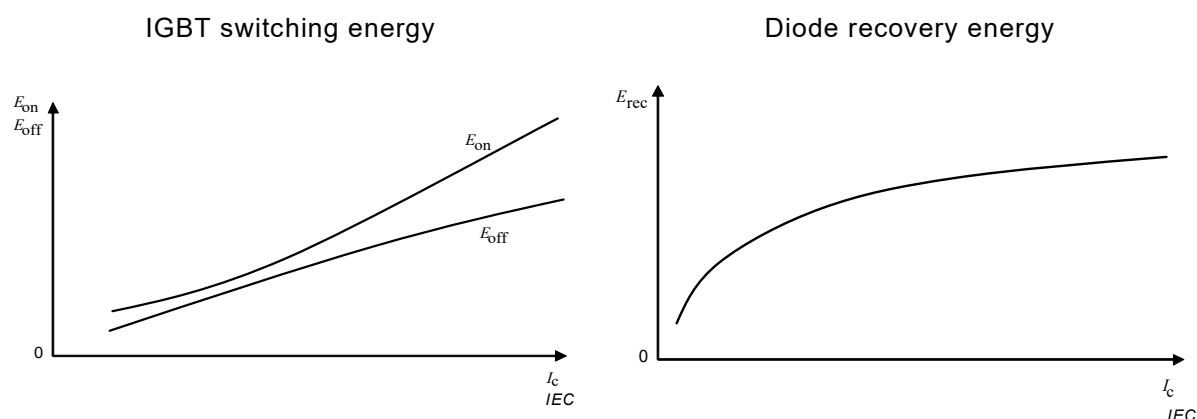


Figure A.14 – IGBT and diode switching energy as a function of collector current

In order to be able to calculate the switching losses for any operating condition, the IGBT and diode used should be characterised thoroughly to define E_{on} , E_{off} and E_{rec} as functions of voltage, current and temperature. The characterisation results may be presented graphically or in a look-up table but a mathematical model is preferred, since it permits the subsequent calculation process to be more easily automated.

A.4.1.3 Soft switching events

Table A.2 summarises the effects of the four possible soft switching events in the MMC building block.

The soft switching events are mentioned only for the sake of completeness, since they do not directly result in switching energy dissipation in the semiconductors. However, the changes of current direction may indirectly provoke some hard switching events, as the capacitor voltage balancing algorithm may cause some MMC building blocks to change from active to bypassed and some others to change from bypassed to active.

Table A.2 – Soft switching events

Change of current direction	MMC building block state	Effects
Negative to positive	Bypassed	D2 turns off; T2 turns on
Negative to positive	Active	T1 turns off; D1 turns on
Positive to negative	Bypassed	T2 turns off; D2 turns on
Positive to negative	Active	D1 turns off; T1 turns on

A.4.2 Analysis of state changes during cycle

In principle, calculation of the total switching losses in the MMC building block requires only that the instantaneous voltage and current is known for each of the various switching events during a cycle. The switching energy per event can then be calculated from knowledge of how E_{on} , E_{off} and E_{rec} vary with voltage and current for the applicable junction temperature, and the switching losses in the complete cycle are obtained by summing each individual event.

However, unlike a 2-level converter, where the d.c. capacitor voltage is fixed and the switching pattern is deterministic and easily analysed, calculating the switching conditions for every switching event in a modular multi-level converter ~~is very~~ can, depending on the