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INTERNATIONAL STANDARD

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Semiconductor devices – Stress migration test standard – Part 1: Copper stress migration test standard

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SEMICONDUCTOR DEVICES – STRESS MIGRATION TEST STANDARD –

Part 1: Copper stress migration test standard

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The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/2407/FDIS	47/2416/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

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SEMICONDUCTOR DEVICES – STRESS MIGRATION TEST STANDARD –

Part 1: Copper stress migration test standard

1 Scope

This part of IEC 62880 describes a constant temperature (isothermal) aging method for testing copper (Cu) metallization test structures on microelectronics wafers for susceptibility to stress-induced voiding (SIV). This method is to be conducted primarily at the wafer level of production during technology development, and the results are to be used for lifetime prediction and failure analysis. Under some conditions, the method can be applied to package-level testing. This method is not intended to check production lots for shipment, because of the long test time.

Dual damascene Cu metallization systems usually have liners, such as tantalum (Ta) or tantalum nitride (TaN) on the bottom and sides of trenches etched into dielectric layers. Hence, for structures in which a single via contacts a wide line below it, a void under the via can cause an open circuit at almost the same time as any percentage resistance shift that would satisfy a failure criterion.

2 Normative references

There are no normative references in this document.

NOTE Related documents are listed in the Bibliography.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
stress migration
SM
crucial failure phenomenon of the semiconductor device interconnects

3.2
stress induced voiding
SIV
voiding generated in the semiconductor device interconnects which is caused by thermal stress

Note 1 to entry: In copper interconnect, voiding occurs under VIA or inside VIA, and causes resistance increase or open failure.

Note 2 to entry: See Annex B for mechanism.

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3.3
wide pattern
chain pattern, which VIA connects wide pattern

Note 1 to entry: There are some combinations of connection.

SEE: Figure 1

3.4
nose pattern
chain pattern, narrow pattern connected to a VIA and attached to a wider pattern

Note 1 to entry: THe SIV risk of this VIA is determined by the width of the plate and the distance of the VIA away from the plate (described in 4.1).

SEE: Figure 1

3.5
nose length
length of a narrow pattern portion of the nose pattern

SEE: Figure 1

3.6
nose width
width of a narrow pattern portion of the nose pattern

SEE: Figure 1

3.7
DRC
Design Rule Compliant
pattern rule that the designer shall follow, e.g. permitted pattern width, VIA location ,etc.

3.8
VIM
VIA-in-the-middle
wide pattern type of VIA chain

Note 1 to entry: See Figure 1 and Annex A.

3.9
co-axial stacked VIA
SM test structure where VIA is stacked in the vertical direction and coaxially

Note 1 to entry: See Figure 2 and 4.1.

3.10
off-center stacked VIA
SM test structure where VIA is aligned in the vertical direction and the center of VIA is shifted

Note 1 to entry: See Figure 2 and 4.1; a zig-zag type and a spiral type are proposed.

3.11
mesh type VIA
SM test structure chain pattern, VIA is connected to narrow pattern and narrow pattern is connected to the mesh type wide pattern

Note 1 to entry: See Figure 2 and 4.1.

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4 Test method

4.1 Test structures

To test the susceptibility to stress voiding of the technology under evaluation, structures that emphasize each extreme risk of the technology shall be designed, evaluated, and used in the test procedure.

Typical SM test structures are in the formats of VIA chains and single VIAs. Special considerations shall be carried out to assure that the appropriate test structures are used. The following are the structures that shall be used in the evaluation of stress migration reliability:

– Design rule compliant (DRC) linewidth test structures:
  - Around 100-VIA chains, both conventional (VIA-at-end) and the VIA-in-the-middle (VIM) VIA chains. Bi-polar or plate-above VIA and plate-below VIA types. Modest VIA numbers of around 100 to a few hundred are recommended to ensure resistance sensitivity for SIV risk detections.
  - VIA chains with larger VIA numbers such as around 1 000 to around 1E5, are used at the individual company's discretion in case of needs for VIA scaling.
  - Single Kelvin VIA structures, VIM type.
– For test structures, specific dimensions (nose length/width) shall correspond to each user's processes and designs. Potential options may range from 10x min to 100x min width or its equivalence (e.g., slotted plates) VIM VIA chains, for measuring SM margin and estimated SM lifetime within limited testing time.

Figure 1 shows the sketches of test structure formats of:

a) conventional VIA chains (around 10 µm interconnect length);

b) VIA-in-the-middle (VIM) VIA chains (around 10 µm interconnect length);

c) single Kelvin VIA (L-shaped);

d) SM nose VIA chain structure of plate-below and plate-above VIA chains.

The plate widths of VIA chains, single Kelvin VIA and SM nose VIA chains can be DRC and wide plate widths.

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