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INTERNATIONAL STANDARD

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Integrated circuits – Three dimensional integrated circuits – Part 3: Model and measurement conditions of through-silicon via

Circuits intégrés – Circuits intégrés tridimensionnels – Partie 3: Modèle et conditions de mesure des trous de liaison à travers le silicium

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INTEGRATED CIRCUITS – THREE DIMENSIONAL INTEGRATED CIRCUITS –

Part 3: Model and measurement conditions of through-silicon via

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The text of this International Standard is based on the following documents:

FDIS	Report on voting
47A/1057/FDIS	47A/1063/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

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INTRODUCTION

The embedded system implementation such as digital consumer and mobile devices is a history of functional integration and power reduction for faster and smaller. At the beginning, the embedded system was developed by various digital ASIC chips to implement required functions. They were then integrated on one chip as a system on chip (SoC), which includes application processor and peripheral I/F logic, such as PCIe, SATA, USB, and DDRx memory controller. Because required performance and image resolution is growing, SoC has embedded many functions through adopting advanced semiconductor technology.

Since advanced semiconductor technology is complicated and its development cost is higher, the application is limited to use only for a few products. Those SoC's cost is not appropriate for all embedded systems. Multi-chip implementation is a way to solve this issue. It implements very large logic gate on the separated SoC and ASIC logic chips, connecting each other. This multi-chip interconnection technique provides also implementation of heterogeneous technology VLSI chips.

This document is focused to interconnect methodology to implement multi-chip VLSI for three-dimensional integrated circuit. Thanks to through-silicon via (TSV) and micro bump interconnect technology; the wire number between VLSI can be tremendously wider. It also allows to connect chips with on-chip bus interconnection, which has several thousand signal connections.

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INTEGRATED CIRCUITS – THREE DIMENSIONAL INTEGRATED CIRCUITS –

Part 3: Model and measurement conditions of through-silicon via

1 Scope

This part of IEC 63011 specifies a reference model of through-silicon via (TSV) electrical characteristics required for an interface design in three dimensional integrated circuit (3-D IC) to transmit and receive digital data and measurement conditions for resistance and capacitance to specify TSV characteristics in 3-D IC.

3-D IC specifications covered by this document are the following:

- application: digital consumer and mobile;
- operating voltage: 0,1 V to 5,0 V,
- operating frequency: less than 2,0 GHz.

This document does not describe the equipment for the measurement. Figure 1 describes a typical case of multi-chip interconnect system discussed in this document.

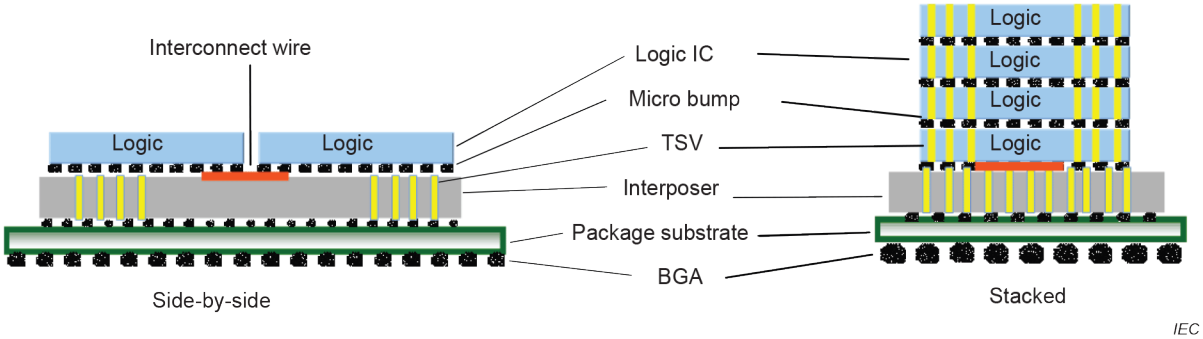

Figure 1 – Reference of a multi-chip interconnect system

Power devices, RF devices and micro-electromechanical systems (MEMS) are not in the scope of this document.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 63011-1, *Integrated circuits – Three dimensional integrated circuits – Part 1: Terminology*

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3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 63011-1 apply.

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- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.2 Abbreviated terms

3-D IC	three-dimensional integrated circuit
ASIC	application specific integrated circuit
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
SoC	system on chip
TSV	through-silicon via
VLSI	very large scale integration

4 Measurement conditions to specify TSV characteristics

4.1 Supply chain and TSV circuit model

3-D IC supply chain employing the TSV circuit model is shown in Figure 2. Foundry manufacturers of logic chip and 3-D stacking provide the TSV model. The circuit model is determined based on an actual experimental result.

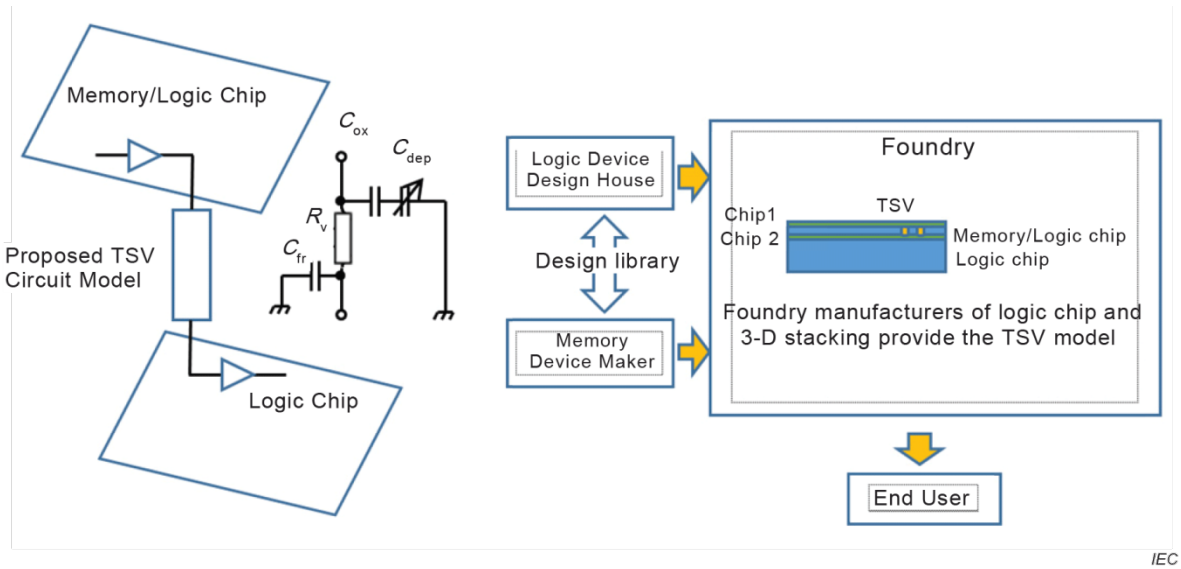

Figure 2 – 3-D IC Supply chain model

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4.2 Reference model of TSV electrical characteristics

Reference model of TSV electrical characteristics shown in Figure 3 is composed of a capacitance (C_v) and a resistance (R_v). C_v is the total capacitance and consists of capacitance of oxide layer (C_{ox}), capacitance by depletion layer (C_{dep}) and fringe capacitance (C_{fr}). C_{ox} and C_{dep} are capacitances between the TSV and the semiconductor substrate and dependent on the voltage applied to the TSV since depletion layer exists. C_{fr} is a fringe capacitance between a bump and the semiconductor substrate. The node of C_{dep} is connected to the ground through the substrate. When the interval of TSV is very short, coupling model is recommended. Table 1 shows a policy for model standardization. Circuit definition explains the view of proposed model. The device structure is the structure which will be the requisite in the case of using the proposed model. Measurement condition explains device structure and operating conditions for measurement. The parameters of the TSV model are derived from TSV and its surrounding structure. An example of a typical concept is shown in Annex A.

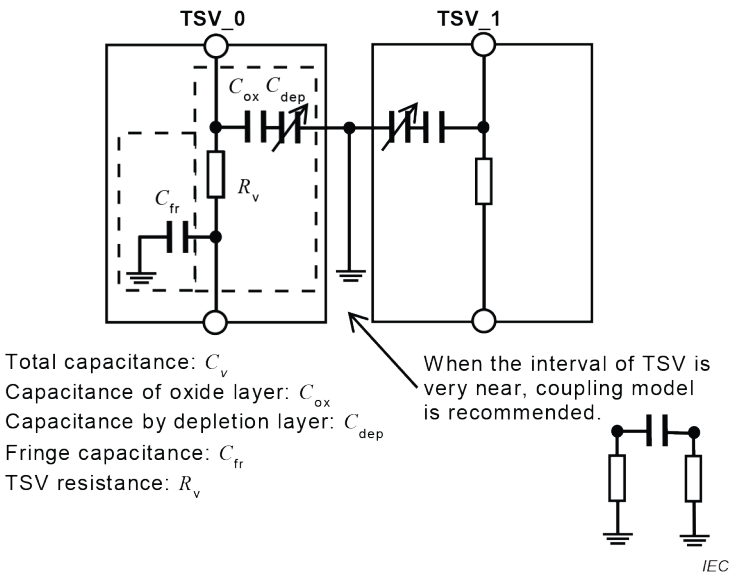

Figure 3 – TSV electrical characteristic model

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