IEC 61691-6

Edition 1.0 2009-12

INTERNATIONAL STANDARD

IEEE Std 1076.1™

Behavioural languages –
Part 6: VHDL Analog and Mixed-Signal Extensions

IEC 61691-6:2009(E) IEEE Std 1076.1-2007(E)

Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

THIS PUBLICATION IS COPYRIGHT PROTECTED

Copyright © 2009 IEEE

All rights reserved. IEEE is a registered trademark in the U.S. Patent & Trademark Office, owned by the Institute of Electrical and Electronics Engineers, Inc.

Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from the IEC Central Office.

Any questions about IEEE copyright should be addressed to the IEEE. Enquiries about obtaining additional rights to this publication and other information requests should be addressed to the IEC or your local IEC member National Committee.

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland
Email: inmail@iec.ch
Web: www.iec.ch

Institute of Electrical and Electronics Engineers, Inc
3 Park Avenue
New York, NY10016-5997
USA
Email: stds.ipr@ieee.org
Web: www.ieee.org

About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigenda or an amendment might have been published.

- Catalogue of IEC publications: www.iec.ch/searchpub
The IEC on-line Catalogue enables you to search by a variety of criteria (reference number, text, technical committee,…). It also gives information on projects, withdrawn and replaced publications.

- IEC Just Published: www.iec.ch/online_news/justpub
Stay up to date on all new IEC publications. Just Published details twice a month all new publications released. Available on-line and also by email.

- Electropedia: www.electropedia.org
The world's leading online dictionary of electronic and electrical terms containing more than 20 000 terms and definitions in English and French, with equivalent terms in additional languages. Also known as the International Electrotechnical Vocabulary online.

- Customer Service Centre: www.iec.ch/webstore/custserv
If you wish to give us your feedback on this publication or need further assistance, please visit the Customer Service Centre FAQ or contact us:

Email: csc@iec.ch
Tel.: +41 22 919 02 11

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEC/IEEE 61691-6-2009

IEC 61691-6

Edition 1.0 2009-12

INTERNATIONAL STANDARD

IEEE Std 1076.1™

Behavioural languages –
Part 6: VHDL Analog and Mixed-Signal Extensions

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

PRICE CODE XM

ICS 25.040, 35.060

ISBN 2-8318-1069-0

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEC/IEEE 61691-6-2009

CONTENTS

Foreword v
IEEE introduction viii

0. Overview 1

0.1 Purpose and scope 1
0.2 Normative references 1
0.3 Structure and terminology of this standard 2

1. Design entities and configurations 5

1.1 Entity declarations 5
1.2 Architecture bodies 10
1.3 Configuration declarations 12

2. Subprograms and packages 19

2.1 Subprogram declarations 19
2.2 Subprogram bodies 22
2.3 Subprogram overloading 24
2.4 Resolution functions 27
2.5 Package declarations 27
2.6 Package bodies 29
2.7 Conformance rules 30

3. Types and natures 31

3.1 Scalar types 32
3.2 Composite types 38
3.3 Access types 43
3.4 File types 46
3.5 Protected types 48
3.6 Natures 51

4. Declarations 55

4.1 Type declarations 55
4.2 Subtype declarations 56
4.3 Objects 57
4.4 Attribute declarations 75
4.5 Component declarations 76
4.6 Group template declarations 77
4.7 Group declarations 77
4.8 Nature declaration 78

5. Specifications 81

5.1 Attribute specification 81
5.2 Configuration specification 83
5.3 Disconnection specification 91
5.4 Step limit specification 93

Documents
Document Sharing Hub
Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

6. Names ... 97

6.1 Names ... 97
6.2 Simple names ... 98
6.3 Selected names ... 99
6.4 Indexed names ... 101
6.5 Slice names ... 102
6.6 Attribute names ... 102

7. Expressions ... 105

7.1 Expressions ... 105
7.2 Operators ... 106
7.3 Operands ... 115
7.4 Static expressions ... 121
7.5 Universal expressions ... 123
7.6 Linear forms ... 124

8. Sequential statements ... 127

8.1 Wait statement ... 127
8.2 Assertion statement ... 129
8.3 Report statement ... 130
8.4 Signal assignment statement ... 130
8.5 Variable assignment statement ... 135
8.6 Procedure call statement ... 137
8.7 If statement ... 137
8.8 Case statement ... 138
8.9 Loop statement ... 139
8.10 Next statement ... 140
8.11 Exit statement ... 140
8.12 Return statement ... 140
8.13 Null statement ... 141
8.14 Break statement ... 141

9. Concurrent statements ... 143

9.1 Block statement ... 143
9.2 Process statement ... 144
9.3 Concurrent procedure call statements ... 145
9.4 Concurrent assertion statements ... 146
9.5 Concurrent signal assignment statements ... 147
9.6 Component instantiation statements ... 151
9.7 Generate statements ... 157
9.8 Concurrent break statement ... 158

10. Scope and visibility ... 159

10.1 Declarative region ... 159
10.2 Scope of declarations ... 160
10.3 Visibility ... 161
10.4 Use clauses ... 164
10.5 The context of overload resolution ... 165

Documents
Document Sharing Hub
Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

11. Design units and their analysis 167

11.1 Design units 167
11.2 Design libraries 167
11.3 Context clauses 168
11.4 Order of analysis 169

12. Elaboration and execution 171

12.1 Elaboration of a design hierarchy 171
12.2 Elaboration of a block header 173
12.3 Elaboration of a declarative part 175
12.4 Elaboration of a statement part 179
12.5 Dynamic elaboration 182
12.6 Execution of a model 183
12.7 Time and the analog solver 194
12.8 Frequency and noise calculation 195

13. Lexical elements 197

13.1 Character set 197
13.2 Lexical elements, separators, and delimiters 199
13.3 Identifiers 200
13.4 Abstract literals 201
13.5 Character literals 202
13.6 String literals 202
13.7 Bit string literals 203
13.8 Comments 204
13.9 Reserved words 205
13.10 Allowable replacements of characters 207

14. Predefined language environment 209

14.1 Predefined attributes 209
14.2 Package STANDARD 231
14.3 Package TEXTIO 240

15. Simultaneous statements 245

15.1 Simple simultaneous statement 245
15.2 Simultaneous if statement 246
15.3 Simultaneous case statement 246
15.4 Simultaneous procedural statement 247
15.5 Simultaneous null statement 250

Annex A (informative) Syntax summary 251

Annex B (informative) Glossary 275

Annex C (informative) Potentially nonportable constructs 297

Annex D (informative) Changes from IEEE Std 1076.1-1999 299

Annex E (informative) Features under consideration for removal 301

.

Documents
Document Sharing Hub
Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

Annex F (informative) Bibliography 303

Annex G (informative) List of Participants.....305

Index 307

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

INTERNATIONAL ELECTROTECHNICAL COMMISSION

BEHAVIOURAL LANGUAGES –

Part 6: VHDL Analog and Mixed-Signal Extensions

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.

2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.

3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.

4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.

5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.

6) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 61691-6/IEEE Std 1076.1 has been processed through IEC technical committee 93: *Design automation*.

The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1076.1 (2007)	93/280/FDIS	93/286/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

A list of parts of the IEC 61691 series can be found on the IEC web site.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

Documents
Document Sharing Hub
Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

IEC/IEEE Dual Logo International Standards

This Dual Logo International Standard is the result of an agreement between the IEC and the Institute of Electrical and Electronics Engineers, Inc. (IEEE). The original IEEE Standard was submitted to the IEC for consideration under the agreement, and the resulting IEC/IEEE Dual Logo International Standard has been published in accordance with the ISO/IEC Directives.

IEEE Standards documents are developed within the IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association (IEEE-SA) Standards Board. The IEEE develops its standards through a consensus development process, approved by the American National Standards Institute, which brings together volunteers representing varied viewpoints and interests to achieve the final product. Volunteers are not necessarily members of the Institute and serve without compensation. While the IEEE administers the process and establishes rules to promote fairness in the consensus development process, the IEEE does not independently evaluate, test, or verify the accuracy of any of the information contained in its standards.

Use of an IEC/IEEE Dual Logo International Standard is wholly voluntary. The IEC and IEEE disclaim liability for any personal injury, property or other damage, of any nature whatsoever, whether special, indirect, consequential, or compensatory, directly or indirectly resulting from the publication, use of, or reliance upon this, or any other IEC or IEEE Standard document.

The IEC and IEEE do not warrant or represent the accuracy or content of the material contained herein, and expressly disclaim any express or implied warranty, including any implied warranty of merchantability or fitness for a specific purpose, or that the use of the material contained herein is free from patent infringement. IEC/IEEE Dual Logo International Standards documents are supplied “AS IS”.

The existence of an IEC/IEEE Dual Logo International Standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEC/IEEE Dual Logo International Standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard.

Every IEEE Standard is subjected to review at least every five years for revision or reaffirmation. When a document is more than five years old and has not been reaffirmed, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE Standard.

In publishing and making this document available, the IEC and IEEE are not suggesting or rendering professional or other services for, or on behalf of, any person or entity. Neither the IEC nor IEEE is undertaking to perform any duty owed by any other person or entity to another. Any person utilizing this, and any other IEC/IEEE Dual Logo International Standards or IEEE Standards document, should rely upon the advice of a competent professional in determining the exercise of reasonable care in any given circumstances.

Interpretations – Occasionally questions may arise regarding the meaning of portions of standards as they relate to specific applications. When the need for interpretations is brought to the attention of IEEE, the Institute will initiate action to prepare appropriate responses. Since IEEE Standards represent a consensus of concerned interests, it is important to ensure that any interpretation has also received the concurrence of a balance of interests. For this reason, IEEE and the members of its societies and Standards Coordinating Committees are not able to provide an instant response to interpretation requests except in those cases where the matter has previously received formal consideration.

Comments for revision of IEC/IEEE Dual Logo International Standards are welcome from any interested party, regardless of membership affiliation with the IEC or IEEE. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments. Comments on standards and requests for interpretations should be addressed to:

Secretary, IEEE-SA Standards Board, 445 Hoes Lane, Piscataway, NJ 08854, USA and/or General Secretary, IEC, 3, rue de Varembé, PO Box 131, 1211 Geneva 20, Switzerland.

Authorization to photocopy portions of any individual standard for internal or personal use is granted by the Institute of Electrical and Electronics Engineers, Inc., provided that the appropriate fee is paid to Copyright Clearance Center. To arrange for payment of licensing fee, please contact Copyright Clearance Center, Customer Service, 222 Rosewood Drive, Danvers, MA 01923 USA; +1 978 750 8400. Permission to photocopy portions of any individual standard for educational classroom use can also be obtained through the Copyright Clearance Center.

NOTE – Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken with respect to the existence or validity of any patent rights in connection therewith. The IEEE shall not be responsible for identifying patents for which a license may be required by an IEEE standard or for conducting inquiries into the legal validity or scope of those patents that are brought to its attention.

Documents
Document Sharing Hub
Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

IEEE Standard VHDL Analog and Mixed-Signal Extensions

Sponsor

Design Automation Standards Committee
of the
IEEE Computer Society

Approved 17 May 2007

IEEE SA-Standards Board

Abstract: This standard defines the IEEE 1076.1 language, a hardware description language for the description and the simulation of analog, digital, and mixed-signal systems. The language, also informally known as VHDL-AMS, is built on IEEE Std 1076™-2002 (VHDL) and extends it with additions and changes to provide capabilities of writing and simulating analog and mixed-signal models.
Keywords: analog design, computer, computer languages, hardware design, mixed-signal design, VHDL

Documents
Document Sharing Hub
Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

IEEE introduction

The IEEE 1076.1 language, informally known as VHDL-AMS, is a superset of IEEE Std 1076-2002 (VHDL) that provides capabilities for describing and simulating analog and mixed-signal systems with conservative and nonconservative semantics for the analog portion of the system. The language supports many abstraction levels in electrical and non electrical energy domains. The modeled analog systems arelumped systems that can be described by ordinary differential equations and algebraic equations. The language does not specify any particular technique to solve the equations, but it rather defines the results that must be achieved. The solution of the equations may include discontinuities. Interaction between the digital part of a model and its analog part is supported in a flexible and efficient manner. Finally, support for frequency domain small-signal and noise simulation is provided.

The extension of VHDL to support analog and mixed-signal systems began in 1989, as part of the second revision of IEEE Std 1076 targeted for a 1993 release. A large number of requirements to support analog and mixed-signal systems were submitted, and it soon became apparent that the complexity of the topic required the formation of a separate working group. The design of the IEEE 1076.1 language formally began in 1993, when the IEEE 1076.1 Working Group was formed under the auspices of the Design Automation Standards Committee of the IEEE Computer Society, under Project Authorization Request (PAR) 1076.1. Its charter was to extend the IEEE 1076 (VHDL) language to support the requirements for the description and simulation of analog and mixed-signal systems. The IEEE 1076.1 Working Group approved the draft standard in June 1997. The first release of the draft of IEEE Std 1076.1-1999 was approved by the IEEE Standards Board on 18 March 1999.

The 2007 revision includes changes made to IEEE Std 1076-2002 since the first release of the IEEE 1076.1 standard. It also includes clarification of IEEE 1076.1 language definitions and corrections of typographical errors that were introduced in the 1999 version of the IEEE 1076.1 language reference manual. See the Annex D for a list of changes from the 1999 release.

Notice to users

Errata

Errata, if any, for this and all other standards can be accessed at the following URL: http://standards.ieee.org/reading/ieee/updates/errata/index.html. Users are encouraged to check this URL for errata periodically.

Interpretations

Current interpretations can be accessed at the following URL: http://standards.ieee.org/reading/ieee/interp/index.html.

Patents

Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken with respect to the existence or validity of any patent rights in connection therewith. The IEEE is not responsible for identifying Essential Patent Claims for which a license may be required, for conducting inquiries into the legal validity or scope of Patents Claims or determining whether any licensing terms or conditions provided in connection with submission of a Letter of Assurance, if any, or in any licensing agreements are reasonable or non-discriminatory. Users of this standard are expressly advised that determination of the validity of any patent rights, and the risk of infringement of such rights, is entirely their own responsibility. Further information may be obtained from the IEEE Standards Association.

IMPORTANT NOTICE: This standard is not intended to ensure safety, security, health, or environmental protection in all circumstances. Implementers of the standard are responsible for determining appropriate safety, security, environmental, and health practices or regulatory requirements.

This IEEE document is made available for use subject to important notices and legal disclaimers. These notices and disclaimers appear in all publications containing this document and may be found under the heading "Important Notice" or "Important Notices and Disclaimers Concerning IEEE Documents." They can also be obtained on request from IEEE or viewed at http://standards.ieee.org/IPR/disclaimers.html.

Documents
Document Sharing Hub
Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

Documents
Document Sharing Hub

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEC/IEEE 61691-6-2009

BEHAVIOURAL LANGUAGES –

Part 6: VHDL Analog and Mixed-Signal Extensions

0. Overview

This clause describes the purpose, scope, and organization of this standard.

0.1 Purpose and scope

This standard defines IEC 61691-6/IEEE 1076.1™ language, a hardware description language for the description and the simulation of analog, digital, and mixed-signal systems. The language, also informally known as VHDLAMS, is built on the IEC 61691-1-1/IEEE 1076™ (VHDL) language and extends it to provide capabilities of writing and simulating analog and mixed-signal models.

This document contains the complete reference of the IEC 61691-6/IEEE 1076.1 VHDL language, including the unchanged portions of the base language and the extensions. Formally, IEC 61691-6:2009/IEEE Std 1076.1-2007 defines the extensions only, and portions of text marked with change bars are either exclusively part of IEC 61691-6:2009/IEEE Std 1076.1-2007 or define changes compared to IEC 61691-1-1:2004/IEEE Std 1076-2002.[1] Portions of text not marked with change bars are identical in this document and in IEC 61691-1-1:2004/IEEE Std 1076-2002.

The primary audience of this document are implementers of tools supporting the language and advanced users of the language. The document is not intended to provide any introductory or tutorial information. It rather provides formal definitions of language elements and language constructs.

The IEC 61691-6/IEEE 1076.1 language is a superset of the IEC 61691-1-1/IEEE 1076 language (VHDL). As such, any legal IEC 61691-1-1/IEEE 1076 model is a IEC 61691-6/IEEE 1076.1 model, and any IEC 61691-6/IEEE 1076.1 tool shall provide the same simulation results as obtained with an IEC 61691-1-1/IEEE 1076 tool. IEC 61691-1-1:2004/IEEE Std 1076-2002 and IEC 61691-6:2009/IEEE Std 1076.1-2007 will remain separate standards. This means that when IEC 61691-1-1:2004/IEEE Std 1076-2002 is revised, IEC 61691-6:2009/IEEE Std 1076.1-2007 will not be automatically revised accordingly. A separate effort will be required to keep both standards synchronized and to avoid inconsistencies.

0.2 Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in the text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

This standard is dependent upon IEC 61691-1-1:2004/IEEE Std 1076-2002. In addition, certain definitions in this document depend on IEEE Std 1076.2-1996, which describes via standard packages and definitions mathematical functions that can be used within VHDL design units.

IEC 61691-1-1:2004 *Behavioural languages - Part 1-1: VHDL language reference manual*

IEEE Std 1076-2002, *IEEE Standard VHDL Language Reference Manual*.[2, 3, 4]

---

[1] Information on references can be found in 0.2.

[2] IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854, USA (http://standards.ieee.org/). IEC publications are available from the Sales Department of the International Electrotechnical Commission, Case Postale 131, 3, rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse (http://www.iec.ch/).'

[3] The IEEE standards or products referred to in this clause are trademarks of the Institute of Electrical and Electronics Engineers, Inc.

[4] IEEE Std 1076-2002 was adopted as IEC 61691-1-1:2004.

Documents
Document Sharing Hub
Published by IEC under license from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

IEEE Std 1076.2-1996 (Reaff 2002), IEEE Standard VHDL Mathematical Packages.

0.3 Structure and terminology of this standard

This standard is organized into clauses, each of which focuses on some particular area of the language. Within each clause, individual constructs or concepts are discussed in each subclause.

Each subclause describing a specific construct begins with an introductory paragraph. Next, the syntax of the construct is described using one or more grammatical *productions*.

A set of paragraphs describing the meaning and restrictions of the construct in narrative form then follow.

In this document, the word *shall* is used to indicate a mandatory requirement. The word *should* is used to indicate a recommendation. The word *may* is used to indicate a permissible action. The word *can* is used for statements of possibility and capability.

Finally, each clause may end with examples, notes, and references to other pertinent clauses.

0.3.1 Syntactic description

The form of a VHDL description is described by means of context-free syntax using a simple variant of the Backus-Naur Form; in particular:

a) Lowercase words in roman font, some containing embedded underlines, are used to denote syntactic categories, for example:

   formal_port_list

   Whenever the name of a syntactic category is used, apart from the syntax rules themselves, spaces take the place of underlines [thus, “formal port list” would appear in the narrative description when referring to the syntactic category in item a)].

b) Boldface words are used to denote reserved words, for example:

   array

   Reserved words shall be used only in those places indicated by the syntax.

c) A *production* consists of a *left-hand side*, the symbol “::=” (which is read as “can be replaced by”), and a *right-hand side*. The left-hand side of a production is always a syntactic category; the right-hand side is a replacement rule. The meaning of a production is a textual-replacement rule: any occurrence of the left-hand side may be replaced by an instance of the right-hand side.

d) A vertical bar (|) separates alternative items on the right-hand side of a production unless it occurs immediately after an opening brace, in which case it stands for itself, as follows:

   letter_or_digit ::= letter | digit
   choices ::= choice { | choice }

   In the first instance, an occurrence of “letter_or_digit” can be replaced by either “letter” or “digit.” In the second case, “choices” can be replaced by a list of “choice,” separated by vertical bars [see item f) for the meaning of braces].

e) Square brackets [ ] enclose optional items on the right-hand side of a production; thus, the following two productions are equivalent:

   return_statement ::= **return** [expression] ;
   return_statement ::= **return** ; | **return** expression ;

   Note, however, that the initial and terminal square brackets in the right-hand side of the production for signatures (see 2.3.2) are part of the syntax of signatures and do not indicate that the entire right-hand side is optional.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Documents
Document Sharing Hub
Full document details: IEC/IEEE 61691-6-2009

f) Braces { } enclose a repeated item or items on the right-hand side of a production. The items may appear zero or more times; the repetitions occur from left to right as with an equivalent left-recursive rule. Thus, the following two productions are equivalent:

term ::= factor { multiplying_operator factor }
term ::= factor | term multiplying_operator factor

g) If the name of any syntactic category starts with an italicized part, it is equivalent to the category name without the italicized part. The italicized part is intended to convey some semantic information. For example, *type*_name and *subtype*_name are both syntactically equivalent to name alone.

h) The term simple_name is used for any occurrence of an identifier that already denotes some declared entity.

0.3.2 Semantic description

The meaning and restrictions of a particular construct are described with a set of narrative rules immediately following the syntactic productions. In these rules, an italicized term indicates the definition of that term and identifiers appearing entirely in uppercase letters refer to definitions in package STANDARD (see 14.2).

The following terms are used in these semantic descriptions with the following meanings:

erroneous: The condition described represents an ill-formed description; however, implementations are not required to detect and report this condition. Conditions are deemed erroneous only when it is impossible in general to detect the condition during the processing of the language.

error: The condition described represents an ill-formed description; implementations are required to detect the condition and report an error to the user of the tool.

illegal: A synonym for “error.”

legal: The condition described represents a well-formed description.

0.3.3 Front matter, examples, notes, references, and annexes

Prior to this subclause are several pieces of introductory material; following Clause 15 are some annexes and an index. The front matter, annexes, and index serve to orient and otherwise aid the user of this standard, but are not part of the definition of VHDL.

Some clauses of this standard contain examples, notes, and cross-references to other clauses of the standard; these parts always appear at the end of a clause. Examples are meant to illustrate the possible forms of the construct described. Illegal examples are italicized. Notes are meant to emphasize consequences of the rules described in the clause or elsewhere. In order to distinguish notes from the other narrative portions of this standard, notes are set as enumerated paragraphs in a font smaller than the rest of the text. Cross-references are meant to guide the user to other relevant clauses of the standard. Examples, notes, and cross-references are not part of the definition of the language.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Documents
Document Sharing Hub
Full document details: IEC/IEEE 61691-6-2009

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Documents
Document Sharing Hub
Full document details: IEC/IEEE 61691-6-2009

1. Design entities and configurations

The *design entity* is the primary hardware abstraction in VHDL. It represents a portion of a hardware design that has well-defined inputs and outputs and performs a well-defined function. A design entity may represent an entire system, a subsystem, a board, a chip, a macro-cell, a logic gate, or any level of abstraction in-between. A *configuration* can be used to describe how design entities are put together to form a complete design.

A design entity may be described in terms of a hierarchy of *blocks*, each of which represents a portion of the whole design. The top-level block in such a hierarchy is the design entity itself; such a block is an *external* block that resides in a library and may be used as a component of other designs. Nested blocks in the hierarchy are *internal* blocks, defined by block statements (see 9.1).

A design entity may also be described in terms of interconnected components. Each component of a design entity may be bound to a lower-level design entity in order to define the structure or behavior of that component. Successive decomposition of a design entity into components, and binding those components to other design entities that may be decomposed in like manner, results in a hierarchy of design entities representing a complete design. Such a collection of design entities is called a *design hierarchy*. The bindings necessary to identify a design hierarchy can be specified in a configuration of the top-level entity in the hierarchy.

This clause describes the way in which design entities and configurations are defined. A design entity is defined by an *entity declaration* together with a corresponding *architecture body*. A configuration is defined by a *configuration declaration*.

1.1 Entity declarations

An entity declaration defines the interface between a given design entity and the environment in which it is used. It may also specify declarations and statements that are part of the design entity. A given entity declaration may be shared by many design entities, each of which has a different architecture. Thus, an entity declaration can potentially represent a class of design entities, each with the same interface.

```
entity_declaration ::=
    entity identifier is
        entity_header
        entity_declarative_part
    [ begin
        entity_statement_part ]
    end [ entity ] [ entity_simple_name ];
```

The entity header and entity declarative part consist of declarative items that pertain to each design entity whose interface is defined by the entity declaration. The entity statement part, if present, consists of concurrent statements that are present in each such design entity.

If a simple name appears at the end of an entity declaration, it shall repeat the identifier of the entity declaration.

1.1.1 Entity header

The entity header declares objects used for communication between a design entity and its environment.

```
entity_header ::=
    [formal_generic_clause ]
```

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

[*formal*_port_clause]

generic_clause ::=
generic (generic_list) ;

port_clause ::=
port (port_list) ;

The generic list in the formal generic clause defines generic constants whose values may be determined by the environment. The port list in the formal port clause defines the ports of the design entity, and their direction, if any.

In certain circumstances, the names of generic constants and ports declared in the entity header become visible outside of the design entity (see 10.2 and 10.3).

Examples:

— An entity declaration with port declarations only:

```
entity Full_Adder is
   port (X, Y, Cin: in Bit; Cout, Sum: out Bit);
end Full_Adder;
```

— An entity declaration with generic declarations also:

```
entity AndGate is
   generic (N: Natural := 2);
   port (Inputs: in Bit_Vector (1 to N);
         Result: out Bit);
end entity AndGate;
```

— An entity declaration with neither:

```
entity TestBench is
end TestBench;
```

— An entity with both signal and quantity declarations:

```
entity Multiplier is
   generic (Bound: REAL);
   port (quantity Input1, Input2: in  REAL;
         quantity Output:         out REAL;
         signal   OutOfBound:     out BOOLEAN);
end entity multiplier;
```

1.1.1.1 Generics

Generics provide a channel for static information to be communicated to a block from its environment. The following applies to both external blocks defined by design entities and to internal blocks defined by block statements.

generic_list ::= *generic*_interface_list

The generics of a block are defined by a generic interface list; interface lists are described in 4.3.2.1. Each interface element in such a generic interface list declares a formal generic.

The value of a generic constant may be specified by the corresponding actual in a generic association list. If no such actual is specified for a given formal generic (either because the formal generic is unassociated or because the actual is **open**), and if a default expression is specified for that generic, the value of this expression is the value of the generic. It is an error if no actual is specified for a given formal generic and no

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

default expression is present in the corresponding interface element. It is an error if some of the subelements of a composite formal generic are connected and others are either unconnected or unassociated.

NOTE—Generics may be used to control structural, data flow, or behavioral characteristics of a block, or may simply be used as documentation. In particular, generics may be used to specify the size of ports; the number of subcomponents within a block; the timing characteristics of a block; or even the physical characteristics of a design such as temperature, capacitance, or location.[4]

1.1.1.2 Ports

Ports provide channels for dynamic communication between a block and its environment. The following applies to both external blocks defined by design entities and to internal blocks defined by block statements, including those equivalent to component instantiation statements and generate statements (see 9.7).

port_list ::= *port*_interface_list

The ports of a block are defined by a port interface list; interface lists are described in 4.3.2.1. Each interface element in the port interface list declares a formal port. A formal port is a signal port, a quantity port, or a terminal port.

To communicate with other blocks, the signal ports, terminal ports, or quantity ports of a block can be associated with signals, terminals, or quantities, respectively, in the environment in which the block is used. Moreover, the signal ports and quantity ports of a block may be associated with an expression in order to provide these ports with constant driving values; such ports shall be of mode **in**. A signal port is itself a signal (see 4.3.1.2); a terminal port is itself a terminal (see 4.3.1.5); and a quantity port is itself a quantity (see 4.3.1.6); thus, a formal port of a block may be associated as an actual with a formal port of an inner block. The port, signal, quantity, terminal, or expression associated with a given formal port is called the *actual* corresponding to the formal port (see 4.3.2.2). The actual, if not an expression, shall be denoted by a static name (see 6.1). The actual, if an expression, shall be a globally static expression (see 7.4). A terminal port shall not be associated with an expression.

After a given description is completely elaborated (see Clause 12), if a formal port is associated with an actual that is itself a port, then the following restrictions apply depending upon the mode (see 4.3.2), if any, of the formal port:

a) For a formal port of mode **in**,
   — If the formal port is a signal port, the associated actual shall be a signal port of mode **in**, **inout**, or **buffer**.
   — If the formal port is a quantity port, the associated actual shall be a quantity port of mode **in** or **out**.
b) For a formal port of mode **out**,
   — If the formal port is a signal port, the associated actual shall be a signal port of mode **out**, **inout**, or **buffer**.
   — If the formal port is a quantity port, the associated actual shall be a quantity port of mode **out**.
c) For a formal port of mode **inout**, the associated actual shall be a port of mode **inout**, or **buffer**.
d) For a formal port of mode **buffer**, the associated actual shall be a port of mode **out**, **inout**, or **buffer**.
e) For a formal port of mode **linkage**, the associated actual may be a port of any mode.

If a formal port is associated with an actual port, signal, terminal, quantity, or expression, then the formal port is said to be *connected*. If a formal port is instead associated with the reserved word **open**, then the formal is said to be *unconnected*. It is an error if a signal or quantity port of mode **in** is unconnected or

[4]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Documents
Document Sharing Hub
Full document details: IEC/IEEE 61691-6-2009

unassociated (see 4.3.2.2) unless its declaration includes a default expression (see 4.3.2). It is an error if a signal port or quantity port of any mode other than **in** is unconnected or unassociated and its type is an unconstrained array type. It is an error if a terminal port is unconnected or unassociated and its nature is an unconstrained array nature. It is an error if some of the subelements of a composite formal port are connected and others are either unconnected or unassociated. It is an error if any quantity is associated as an actual with more than one formal of mode **out**.

NOTE—Ports of mode linkage may be removed from a future version of the language (see Annex E).

1.1.2 Entity declarative part

The entity declarative part of a given entity declaration declares items that are common to all design entities whose interfaces are defined by the given entity declaration.

entity_declarative_part ::=
  { entity_declarative_item }

entity_declarative_item ::=
  subprogram_declaration
| subprogram_body
| type_declaration
| subtype_declaration
| constant_declaration
| signal_declaration
| *shared*_variable_declaration
| file_declaration
| alias_declaration
| attribute_declaration
| attribute_specification
| disconnection_specification
| step_limit_specification
| use_clause
| group_template_declaration
| group_declaration
| nature_declaration
| subnature_declaration
| quantity_declaration
| terminal_declaration

Names declared by declarative items in the entity declarative part of a given entity declaration are visible within the bodies of corresponding design entities, as well as within certain portions of a corresponding configuration declaration.

The various kinds of declaration are described in Clause 4, and the various kinds of specification are described in Clause 5. The use clause, which makes externally defined names visible within the block, is described in Clause 10.

Example:

— An entity declaration with entity declarative items:

```
entity ROM is
   port (Addr: in  Word;
         Data: out Word;
         Sel:  in  Bit);
   type Instruction is array (1 to 5) of Natural;
```

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Documents
Document Sharing Hub
Full document details: IEC/IEEE 61691-6-2009

```
        type Program is array (Natural range <>) of Instruction;
        use Work.OpCodes.all, Work.RegisterNames.all;
        constant ROM_Code: Program :=
           (
              (STM, R14, R12, 12, R13),
              (LD,  R7,  32,  0,  R1 ),
              (BAL, R14, 0,   0,  R7 ),
                    .
                    .    --  etc.
                    .
           ) ;
     end ROM;
```

NOTE—The entity declarative part of a design entity whose corresponding architecture is decorated with the 'FOREIGN attribute is subject to special elaboration rules. See 12.3.

1.1.3 Entity statement part

The entity statement part contains concurrent statements that are common to each design entity with this interface.

entity_statement_part ::=
  { entity_statement }

entity_statement ::=
  concurrent_assertion_statement
 | *passive*_concurrent_procedure_call
 | *passive*_process_statement

It is an error if any statements other than concurrent assertion statements, concurrent procedure call statements, or process statements appear in the entity statement part. All entity statements shall be passive (see 9.2). Such statements may be used to monitor the operating conditions or characteristics of a design entity.

Example:

— An entity declaration with statements:

```
     entity Latch is
        port (Din:  in  Word;
              Dout: out Word;
              Load: in  Bit;
              Clk:  in  Bit );
        constant Setup: Time := 12 ns;
        constant PulseWidth: Time := 50 ns;
        use Work.TimingMonitors.all;
     begin
        assert Clk='1' or Clk'Delayed'Stable (PulseWidth);
        CheckTiming (Setup, Din, Load, Clk);
     end;
```

NOTE—The entity statement part of a design entity whose corresponding architecture is decorated with the 'FOREIGN attribute is subject to special elaboration rules. See 12.4.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

1.2 Architecture bodies

An architecture body defines the body of a design entity. It specifies the relationships between the inputs, outputs, quantities, and terminals of a design entity and may be expressed in terms of structure, data flow, equations, or behavior. Such specifications may be partial or complete.

architecture_body ::=
  architecture identifier **of** *entity*_name **is**
    architecture_declarative_part
  begin
    architecture_statement_part
  end [**architecture**] [*architecture*_simple_name] ;

The identifier defines the simple name of the architecture body; this simple name distinguishes architecture bodies associated with the same entity declaration.

The entity name identifies the name of the entity declaration that defines the interface of this design entity. For a given design entity, both the entity declaration and the associated architecture body shall reside in the same library.

If a simple name appears at the end of an architecture body, it shall repeat the identifier of the architecture body.

More than one architecture body may exist corresponding to a given entity declaration. Each declares a different body with the same interface; thus, each together with the entity declaration represents a different design entity with the same interface.

NOTE—Two architecture bodies that are associated with different entity declarations may have the same simple name, even if both architecture bodies (and the corresponding entity declarations) reside in the same library.

1.2.1 Architecture declarative part

The architecture declarative part contains declarations of items that are available for use within the block defined by the design entity.

architecture_declarative_part ::=
  { block_declarative_item }

block_declarative_item ::=
    subprogram_declaration
  | subprogram_body
  | type_declaration
  | subtype_declaration
  | constant_declaration
  | signal_declaration
  | *shared*_variable_declaration
  | file_declaration
  | alias_declaration
  | component_declaration
  | attribute_declaration
  | attribute_specification
  | configuration_specification
  | disconnection_specification
  | step_limit_specification

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

| use_clause
| group_template_declaration
| group_declaration
| nature_declaration
| subnature_declaration
| quantity_declaration
| terminal_declaration

The various kinds of declaration are described in Clause 4, and the various kinds of specification are described in Clause 5. The use clause, which makes externally defined names visible within the block, is described in Clause 10.

NOTE—The declarative part of an architecture decorated with the 'FOREIGN attribute is subject to special elaboration rules. See 12.3.

1.2.2 Architecture statement part

The architecture statement part contains statements that describe the internal organization and/or operation of the block defined by the design entity.

architecture_statement_part ::=
{ architecture_statement }

architecture_statement ::= simultaneous_statement | concurrent_statement

All of the statements in the architecture statement part are either concurrent or simultaneous statements, which execute asynchronously with respect to one another. The various kinds of concurrent statements are described in Clause 9; the various kinds of simultaneous statements are described in Clause 15.

Examples:

— A body of entity Full_Adder:

```
architecture DataFlow of Full_Adder is
   signal A,B: Bit;
begin
   A <= X xor Y;
   B <= A and Cin;
   Sum <= A xor Cin;
   Cout <= B or (X and Y);
end architecture DataFlow;
```

— A body of entity TestBench:

```
library Test;
use Test.Components.all;
architecture Structure of TestBench is
   component Full_Adder
      port (X, Y, Cin: Bit; Cout, Sum: out Bit);
   end component;
signal A,B,C,D,E,F,G: Bit;
   signal OK: Boolean;
begin
   UUT:        Full_Adder port map (A,B,C,D,E);
   Generator:  AdderTest  port map (A,B,C,F,G);
   Comparator: AdderCheck port map (D,E,F,G,OK);
end Structure;
```

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

— A body of entity AndGate:

```
architecture Behavior of AndGate is
begin
   process (Inputs)
      variable Temp: Bit;
   begin
      Temp := '1';
      for i in Inputs'Range loop
         if Inputs(i) = '0' then
            Temp := '0';
            exit;
         end if;
      end loop;
      Result <= Temp after 10 ns;
   end process;
end Behavior;
```

— A body of entity Multiplier:

```
architecture Sample of Multiplier
begin
   Output == Input1 * Input2;
   OutOfBound <= Output'Above(Bound) or not Output'Above(-Bound);
end architecture Sample;
```

NOTE—The statement part of an architecture decorated with the 'FOREIGN attribute is subject to special elaboration rules. See 12.4.

1.3 Configuration declarations

The binding of component instances to design entities is performed by configuration specifications (see 5.2); such specifications appear in the declarative part of the block in which the corresponding component instances are created. In certain cases, however, it may be appropriate to leave unspecified the binding of component instances in a given block and to defer such specification until later. A configuration declaration provides the mechanism for specifying such deferred bindings.

configuration_declaration ::=
  configuration identifier **of** *entity*_name **is**
    configuration_declarative_part
    block_configuration
  end [**configuration**] [*configuration*_simple_name] ;

configuration_declarative_part ::=
  { configuration_declarative_item }

configuration_declarative_item ::=
   use_clause
  | attribute_specification
  | group_declaration

The entity name identifies the name of the entity declaration that defines the design entity at the apex of the design hierarchy. For a configuration of a given design entity, both the configuration declaration and the corresponding entity declaration shall reside in the same library.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

If a simple name appears at the end of a configuration declaration, it shall repeat the identifier of the configuration declaration.

NOTE 1—A configuration declaration achieves its effect entirely through elaboration (see Clause 12). There are no behavioral semantics associated with a configuration declaration.

NOTE 2—A given configuration may be used in the definition of another, more complex configuration.

Examples:

— An architecture of a microprocessor:

```
architecture Structure_View of Processor is
   component ALU port ( ··· ); end component;
   component MUX port ( ··· ); end component;
   component Latch port ( ··· ); end component;
begin
   A1: ALU port map ( ··· );
   M1: MUX port map ( ··· );
   M2: MUX port map ( ··· );
   M3: MUX port map ( ··· );
   L1: Latch port map ( ··· );
   L2: Latch port map ( ··· );
end Structure_View;
```

— A configuration of the microprocessor:

```
library TTL, Work;
configuration V4_27_87 of Processor is
   use Work.all;
   for Structure_View
      for A1: ALU
         use configuration TTL.SN74LS181;
      end for;
      for M1,M2,M3: MUX
         use entity Multiplex4 (Behavior);
      end for;
      for all: Latch
         -- use defaults
      end for;
   end for;
end configuration V4_27_87;
```

1.3.1 Block configuration

A block configuration defines the configuration of a block. Such a block is either an internal block defined by a block statement or an external block defined by a design entity. If the block is an internal block, the defining block statement is either an explicit block statement or an implicit block statement that is itself defined by a generate statement.

block_configuration ::=
  for block_specification
    { use_clause }
    { configuration_item }
  end for ;

block_specification ::=
  *architecture*_name

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

| *block_statement*_label
| *generate_statement*_label [(index_specification)]

index_specification ::=
discrete_range
| *static*_expression

configuration_item ::=
block_configuration
| component_configuration

The block specification identifies the internal or external block to which this block configuration applies.

If a block configuration appears immediately within a configuration declaration, then the block specification of that block configuration shall be an architecture name, and that architecture name shall denote a design entity body whose interface is defined by the entity declaration denoted by the entity name of the enclosing configuration declaration.

If a block configuration appears immediately within a component configuration, then the corresponding components shall be fully bound (see 5.2.1.1), the block specification of that block configuration shall be an architecture name, and that architecture name shall denote the same architecture body as that to which the corresponding components are bound.

If a block configuration appears immediately within another block configuration, then the block specification of the contained block configuration shall be a block statement or generate statement label, and the label shall denote a block statement or generate statement that is contained immediately within the block denoted by the block specification of the containing block configuration.

If the scope of a declaration (see 10.2) includes the end of the declarative part of a block corresponding to a given block configuration, then the scope of that declaration extends to each configuration item contained in that block configuration, with the exception of block configurations that configure external blocks. Similarly, if a declaration is visible (either directly or by selection) at the end of the declarative part of a block corresponding to a given block configuration, then the declaration is visible in each configuration item contained in that block configuration, with the exception of block configurations that configure external blocks. Additionally, if a given declaration is a homograph of a declaration that a use clause in the block configuration makes potentially directly visible, then the given declaration is not directly visible in the block configuration or any of its configuration items. See 10.3.

For any name that is the label of a block statement appearing immediately within a given block, a corresponding block configuration may appear as a configuration item immediately within a block configuration corresponding to the given block. For any collection of names that are labels of instances of the same component appearing immediately within a given block, a corresponding component configuration may appear as a configuration item immediately within a block configuration corresponding to the given block.

For any name that is the label of a generate statement immediately within a given block, one or more corresponding block configurations may appear as configuration items immediately within a block configuration corresponding to the given block. Such block configurations apply to implicit blocks generated by that generate statement. If such a block configuration contains an index specification that is a discrete range, then the block configuration applies to those implicit block statements that are generated for the specified range of values of the corresponding generate parameter; the discrete range has no significance other than to define the set of generate statement parameter values implied by the discrete range. If such a block configuration contains an index specification that is a static expression, then the block configuration applies only to the implicit block statement generated for the specified value of the corresponding generate

Documents
Document Sharing Hub
Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

parameter. If no index specification appears in such a block configuration, then it applies to exactly one of the following sets of blocks:

— All implicit blocks (if any) generated by the corresponding generate statement, if and only if the corresponding generate statement has a generation scheme including the reserved word **for.**

— The implicit block generated by the corresponding generate statement, if and only if the corresponding generate statement has a generation scheme including the reserved word **if** and if the condition in the generate scheme evaluates to TRUE.

— No implicit or explicit blocks, if and only if the corresponding generate statement has a generation scheme including the reserved word **if** and the condition in the generate scheme evaluates to FALSE.

If the block specification of a block configuration contains a generate statement label, and if this label contains an index specification, then it is an error if the generate statement denoted by the label does not have a generation scheme including the reserved word.

Within a given block configuration, whether implicit or explicit, an implicit block configuration is assumed to appear for any block statement that appears within the block corresponding to the given block configuration, if no explicit block configuration appears for that block statement. Similarly, an implicit component configuration is assumed to appear for each component instance that appears within the block corresponding to the given block configuration, if no explicit component configuration appears for that instance. Such implicit configuration items are assumed to appear following all explicit configuration items in the block configuration.

It is an error if, in a given block configuration, more than one configuration item is defined for the same block or component instance.

NOTE 1—As a result of the rules described in the preceding paragraphs and in Clause 10, a simple name that is visible by selection at the end of the declarative part of a given block is also visible by selection within any configuration item contained in a corresponding block configuration. If such a name is directly visible at the end of the given block declarative part, it will likewise be directly visible in the corresponding configuration items, unless a use clause for a different declaration with the same simple name appears in the corresponding configuration declaration, and the scope of that use clause encompasses all or part of those configuration items. If such a use clause appears, then the name will be directly visible within the corresponding configuration items except at those places that fall within the scope of the additional use clause (at which places neither name will be directly visible).

NOTE 2—If an implicit configuration item is assumed to appear within a block configuration, that implicit configuration item will never contain explicit configuration items.

NOTE 3—If the block specification in a block configuration specifies a generate statement label, and if this label contains an index specification that is a discrete range, then the direction specified or implied by the discrete range has no significance other than to define, together with the bounds of the range, the set of generate statement parameter values denoted by the range. Thus, the following two block configurations are equivalent:

```
for Adders(31 downto 0) ··· end for;
for Adders(0 to 31) ··· end for;
```

NOTE 4—A block configuration is allowed to appear immediately within a configuration declaration only if the entity declaration denoted by the entity name of the enclosing configuration declaration has associated architectures. Furthermore, the block specification of the block configuration shall denote one of these architectures.

Examples:

— A block configuration for a design entity:

```
for ShiftRegStruct                    --  An architecture name.
   --  Configuration items
   --  for blocks and components
   --  within ShiftRegStruct.
end for;
```

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Documents
Document Sharing Hub
Full document details: IEC/IEEE 61691-6-2009

— A block configuration for a block statement:

```
for B1                                  --  A block label.
   --  Configuration items
   --  for blocks and components
   --  within block B1.
end for;
```

1.3.2 Component configuration

A component configuration defines the configuration of one or more component instances in a corresponding block.

component_configuration ::=
  for component_specification
    [binding_indication ;]
    [block_configuration]
  end for ;

The component specification (see 5.2) identifies the component instances to which this component configuration applies. A component configuration that appears immediately within a given block configuration applies to component instances that appear immediately within the corresponding block.

It is an error if two component configurations apply to the same component instance.

If the component configuration contains a binding indication (see 5.2.1), then the component configuration implies a configuration specification for the component instances to which it applies. This implicit configuration specification has the same component specification and binding indication as that of the component configuration.

If a given component instance is unbound in the corresponding block, then any explicit component configuration for that instance that does not contain an explicit binding indication will contain an implicit, default binding indication (see 5.2.2). Similarly, if a given component instance is unbound in the corresponding block, then any implicit component configuration for that instance will contain an implicit, default binding indication.

It is an error if a component configuration contains an explicit block configuration and the component configuration does not bind all identified component instances to the same design entity.

Within a given component configuration, whether implicit or explicit, an implicit block configuration is assumed for the design entity to which the corresponding component instance is bound, if no explicit block configuration appears and if the corresponding component instance is fully bound.

Examples:

— A component configuration with binding indication:

```
for all: IOPort
   use entity StdCells.PadTriState4 (DataFlow)
      port map (Pout=>A, Pin=>B, IO=>Dir, Vdd=>Pwr, Gnd=>Gnd);
end for;
```

— A component configuration containing block configurations:

```
for D1: DSP
   for DSP_STRUCTURE
      --  Binding specified in design entity or else defaults.
```

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Documents
Document Sharing Hub
Full document details: IEC/IEEE 61691-6-2009

```
            for Filterer
               --  Configuration items for filtering components.
            end for;
            for Processor
               --  Configuration items for processing components.
            end for;
         end for;
      end for;
```

NOTE—The requirement that all component instances corresponding to a block configuration be bound to the same design entity makes the following configuration illegal:

```
architecture A of E is
   component C is end component C;
   for L1: C use entity E1(X);
   for L2: C use entity E2(X);
begin
   L1: C;
   L2: C;
end architecture A;

configuration Illegal of Work.E is
   for A
      for all: C
         for X        --  Does not apply to the same design entity in all instances of C.
            ...
         end for;     -- X
      end for; -- C
   end for; -- A
end configuration Illegal;
```

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Documents
Document Sharing Hub
Full document details: IEC/IEEE 61691-6-2009

2. Subprograms and packages

Subprograms define algorithms for computing values or exhibiting behavior. They may be used as computational resources to convert between values of different types, to define the resolution of output values driving a common signal, or to define portions of a process. Packages provide a means of defining these and other resources in a way that allows different design units to share the same declarations.

There are two forms of subprograms: procedures and functions. A procedure call is a statement; a function call is an expression and returns a value. Certain functions, designated *pure* functions, return the same value each time they are called with the same values as actual parameters; the remainder, impure functions, may return a different value each time they are called, even when multiple calls have the same actual parameter values. In addition, *impure* functions can update objects outside of their scope and can access a broader class of values than can pure functions. The definition of a subprogram can be given in two parts: a subprogram declaration defining its calling conventions, and a subprogram body defining its execution.

Packages may also be defined in two parts. A package declaration defines the visible contents of a package; a package body provides hidden details. In particular, a package body contains the bodies of any subprograms declared in the package declaration.

2.1 Subprogram declarations

A subprogram declaration declares a procedure or a function, as indicated by the appropriate reserved word.

subprogram_declaration ::=
    subprogram_specification ;

subprogram_specification ::=
    procedure designator [(formal_parameter_list)]
  | [**pure** | **impure**] **function** designator [(formal_parameter_list)]
        return type_mark

designator ::= identifier | operator_symbol

operator_symbol ::= string_literal

The specification of a procedure specifies its designator and its formal parameters (if any). The specification of a function specifies its designator, its formal parameters (if any), the subtype of the returned value (the *result subtype*), and whether or not the function is pure. A function is *impure* if its specification contains the reserved word **impure**; otherwise, it is said to be *pure*. A procedure designator is always an identifier. A function designator is either an identifier or an operator symbol. A designator that is an operator symbol is used for the overloading of an operator (see 2.3.1). The sequence of characters represented by an operator symbol shall be an operator belonging to one of the classes of operators defined in 7.2. Extra spaces are not allowed in an operator symbol, and the case of letters is not significant.

NOTE 1—All subprograms can be called recursively.

NOTE 2—The restrictions on pure functions are enforced even when the function appears within a protected type. That is, pure functions whose body appears in the protected type body shall not directly reference variables declared immediately within the declarative region associated with the protected type. However, impure functions and procedures whose bodies appear in the protected type body may make such references. Such references are made only when the referencing subprogram has exclusive access to the declarative region associated with the protected type.

2.1.1 Formal parameters

The formal parameter list in a subprogram specification defines the formal parameters of the subprogram.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

formal_parameter_list ::= *parameter*_interface_list

Formal parameters of subprograms may be constants, variables, signals, or files. In the first three cases, the mode of a parameter determines how a given formal parameter is accessed within the subprogram. The mode of a formal parameter, together with its class, also determines how such access is implemented. In the fourth case, that of files, the parameters have no mode.

For those parameters with modes, the only modes that are allowed for formal parameters of a procedure are **in**, **inout**, and **out**. If the mode is **in** and no object class is explicitly specified, **constant** is assumed. If the mode is **inout** or **out**, and no object class is explicitly specified, **variable** is assumed.

For those parameters with modes, the only mode that is allowed for formal parameters of a function is the mode **in** (whether this mode is specified explicitly or implicitly). The object class shall be **constant**, **signal**, or **file**. If no object class is explicitly given, **constant** is assumed.

In a subprogram call, the actual designator (see 4.3.2.2) associated with a formal parameter of class **signal** shall be a name denoting a signal. The actual designator associated with a formal of class **variable** shall be a name denoting a variable. The actual designator associated with a formal of class **constant** shall be an expression. The actual designator associated with a formal of class **file** shall be a name denoting a file.

NOTE—Attributes of an actual are never passed into a subprogram. References to an attribute of a formal parameter are legal only if that formal has such an attribute. Such references retrieve the value of the attribute associated with the formal.

2.1.1.1 Constant and variable parameters

For parameters of class **constant** or **variable**, only the values of the actual or formal are transferred into or out of the subprogram call. The manner of such transfers, and the accompanying access privileges that are granted for constant and variable parameters, are described in this subclause.

For a nonforeign subprogram having a parameter of a scalar type or an access type, the parameter is passed by copy. At the start of each call, if the mode is **in** or **inout**, the value of the actual parameter is copied into the associated formal parameter; it is an error if, after applying any conversion function or type conversion present in the actual part of the applicable association element (see 4.3.2.2), the value of the actual parameter does not belong to the subtype denoted by the subtype indication of the formal. After completion of the subprogram body, if the mode is **inout** or **out**, the value of the formal parameter is copied back into the associated actual parameter; it is similarly an error if, after applying any conversion function or type conversion present in the formal part of the applicable association element, the value of the formal parameter does not belong to the subtype denoted by the subtype indication of the actual.

For a nonforeign subprogram having a parameter whose type is an array or record, an implementation may pass parameter values by copy, as for scalar types. If a parameter of mode **out** is passed by copy, then the range of each index position of the actual parameter is copied in, and likewise for its subelements or slices. Alternatively, an implementation may achieve these effects by reference; that is, by arranging that every use of the formal parameter (to read or update its value) be treated as a use of the associated actual parameter throughout the execution of the subprogram call. The language does not define which of these two mechanisms is to be adopted for parameter passing, nor whether different calls to the same subprogram are to use the same mechanism. The execution of a subprogram is erroneous if its effect depends on which mechanism is selected by the implementation.

For a subprogram having a parameter whose type is a protected type, the parameter is passed by reference. It is an error if the mode of the parameter is other than **inout**.

For a formal parameter of a constrained array subtype of mode **in** or **inout**, it is an error if the value of the associated actual parameter (after application of any conversion function or type conversion present in the

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Documents
Document Sharing Hub
Full document details: IEC/IEEE 61691-6-2009

actual part) does not contain a matching element for each element of the formal. For a formal parameter whose declaration contains a subtype indication denoting an unconstrained array type, the subtype of the formal in any call to the subprogram is taken from the actual associated with that formal in the call to the subprogram. It is also an error if, in either case, the value of each element of the actual array (after applying any conversion function or type conversion present in the actual part) does not belong to the element subtype of the formal. If the formal parameter is of mode **out** or **inout**, it is also an error if, at the end of the subprogram call, the value of each element of the formal (after applying any conversion function or type conversion present in the formal part) does not belong to the element subtype of the actual.

NOTE—For parameters of array and record types, the parameter passing rules imply that if no actual parameter of such a type is accessible by more than one path, then the effect of a subprogram call is the same whether or not the implementation uses copying for parameter passing. If, however, there are multiple access paths to such a parameter (for example, if another formal parameter is associated with the same actual parameter), then the value of the formal is undefined after updating the actual other than by updating the formal. A description using such an undefined value is erroneous.

2.1.1.2 Signal parameter

For a formal parameter of class **signal**, references to the signal, the driver of the signal, or both, are passed into the subprogram call.

For a signal parameter of mode **in** or **inout**, the actual signal is associated with the corresponding formal signal parameter at the start of each call. Thereafter, during the execution of the subprogram body, a reference to the formal signal parameter within an expression is equivalent to a reference to the actual signal.

It is an error if signal-valued attributes 'STABLE, 'QUIET, 'TRANSACTION, and 'DELAYED of formal signal parameters of any mode are read within a subprogram; similarly, it is an error if quantity-valued attributes 'RAMP or 'SLEW are read within a subprogram.

A process statement contains a driver for each actual signal associated with a formal signal parameter of mode **out** or **inout** in a subprogram call. Similarly, a subprogram contains a driver for each formal signal parameter of mode **out** or **inout** declared in its subprogram specification.

For a signal parameter of mode **inout** or **out**, the driver of an actual signal is associated with the corresponding driver of the formal signal parameter at the start of each call. Thereafter, during the execution of the subprogram body, an assignment to the driver of a formal signal parameter is equivalent to an assignment to the driver of the actual signal.

If an actual signal is associated with a signal parameter of any mode, the actual shall be denoted by a static signal name. It is an error if a conversion function or type conversion appears in either the formal part or the actual part of an association element that associates an actual signal with a formal signal parameter.

If an actual signal is associated with a signal parameter of any mode, and if the type of the formal is a scalar type, then it is an error if the bounds and direction of the subtype denoted by the subtype indication of the formal are not identical to the bounds and direction of the subtype denoted by the subtype indication of the actual.

If an actual signal is associated with a formal signal parameter, and if the formal is of a constrained array subtype, then it is an error if the actual does not contain a matching element for each element of the formal. If an actual signal is associated with a formal signal parameter, and if the subtype denoted by the subtype indication of the declaration of the formal is an unconstrained array type, then the subtype of the formal in any call to the subprogram is taken from the actual associated with that formal in the call to the subprogram. It is also an error if the mode of the formal is **in** or **inout** and if the value of each element of the actual array does not belong to the element subtype of the formal.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

A formal signal parameter is a guarded signal if and only if it is associated with an actual signal that is a guarded signal. It is an error if the declaration of a formal signal parameter includes the reserved word **bus** (see 4.3.2).

NOTE—It is a consequence of the preceding rules that a procedure with an **out** or **inout** signal parameter called by a process does not have to complete in order for any assignments to that signal parameter within the procedure to take effect. Assignments to the driver of a formal signal parameter are equivalent to assignments directly to the actual driver contained in the process calling the procedure.

2.1.1.3 File parameters

For parameters of class **file**, references to the actual file are passed into the subprogram. No particular parameter-passing mechanism is defined by the language, but a reference to the formal parameter shall be equivalent to a reference to the actual parameter. It is an error if an association element associates an actual with a formal parameter of a file type and that association element contains a conversion function or type conversion. It is also an error if a formal of a file type is associated with an actual that is not of a file type.

At the beginning of a given subprogram call, a file parameter is open (see 3.4.1) if and only if the actual file object associated with the given parameter in a given subprogram call is also open. Similarly, at the beginning of a given subprogram call, both the access mode of and external file associated with (see 3.4.1) an open file parameter are the same as, respectively, the access mode of and the external file associated with the actual file object associated with the given parameter in the subprogram call.

At the completion of the execution of a given subprogram call, the actual file object associated with a given file parameter is open if and only if the formal parameter is also open. Similarly, at the completion of the execution of a given subprogram call, the access mode of and the external file associated with an open actual file object associated with a given file parameter are the same as, respectively, the access mode of and the external file associated with the associated formal parameter.

2.2 Subprogram bodies

A subprogram body specifies the execution of a subprogram.

```
subprogram_body ::=
    subprogram_specification is
        subprogram_declarative_part
    begin
        subprogram_statement_part
    end [ subprogram_kind ] [ designator ] ;

subprogram_declarative_part ::=
    { subprogram_declarative_item }

subprogram_declarative_item ::=
      subprogram_declaration
    | subprogram_body
    | type_declaration
    | subtype_declaration
    | constant_declaration
    | variable_declaration
    | file_declaration
    | alias_declaration
    | attribute_declaration
    | attribute_specification
```

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

| use_clause
| group_template_declaration
| group_declaration

subprogram_statement_part ::=
{ sequential_statement }

subprogram_kind ::= **procedure** | **function**

The declaration of a subprogram is optional. In the absence of such a declaration, the subprogram specification of the subprogram body acts as the declaration. For each subprogram declaration, there shall be a corresponding body. If both a declaration and a body are given, the subprogram specification of the body shall conform (see 2.7) to the subprogram specification of the declaration. Furthermore, both the declaration and the body shall occur immediately within the same declarative region (see 10.1).

If a subprogram kind appears at the end of a subprogram body, it shall repeat the reserved word given in the subprogram specification. If a designator appears at the end of a subprogram body, it shall repeat the designator of the subprogram.

It is an error if a variable declaration in a subprogram declarative part declares a shared variable. (See 4.3.1.3.)

A *foreign subprogram* is one that is decorated with the attribute 'FOREIGN, defined in package STANDARD (see 14.2). The STRING value of the attribute may specify implementation-dependent information about the foreign subprogram. Foreign subprograms may have non-VHDL implementations. An implementation may place restrictions on the allowable modes, classes, and types of the formal parameters to a foreign subprogram; such restrictions may include restrictions on the number and allowable order of the parameters.

Excepting foreign subprograms, the algorithm performed by a subprogram is defined by the sequence of statements that appears in the subprogram statement part. For a foreign subprogram, the algorithm performed is implementation defined.

The execution of a subprogram body is invoked by a subprogram call. For this execution, after establishing the association between the formal and actual parameters, the sequence of statements of the body is executed if the subprogram is not a foreign subprogram; otherwise, an implementation-defined action occurs. Upon completion of the body or implementation-dependent action, if exclusive access to an object of a protected type was granted during elaboration of the declaration of the subprogram (see 12.5), the exclusive access is rescinded. Then, return is made to the caller (and any necessary copying back of formal to actual parameters occurs).

A process or a subprogram is said to be a *parent* of a given subprogram S if that process or subprogram contains a procedure call or function call for S or for a parent of S.

An *explicit* signal is a signal other than an implicit signal GUARD or other than one of the implicit signals defined by the predefined attributes 'ABOVE, 'DELAYED, 'STABLE, 'QUIET, or 'TRANSACTION. The *explicit ancestor* of an implicit signal is found as follows. All implicit GUARD signals and any signal defined by the predefined attribute 'ABOVE have no explicit ancestor. An explicit ancestor of an implicit signal defined by the predefined attributes 'DELAYED, 'STABLE, 'QUIET, or 'TRANSACTION is the signal found by recursively examining the prefix of the attribute. If the prefix denotes an explicit signal, a slice, or a member (see Clause 3) of an explicit signal, then that is the explicit ancestor of the implicit signal. Otherwise, if the prefix is one of the implicit signals defined by the predefined attributes 'DELAYED, 'STABLE, 'QUIET, or 'TRANSACTION, this rule is recursively applied. If the prefix is an implicit signal GUARD, or a signal defined by the predefined attribute 'ABOVE, then the signal has no explicit ancestor.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

If a pure function subprogram is a parent of a given procedure and if that procedure contains a reference to an explicitly declared signal or variable object, or a slice or subelement (or slice thereof) of an explicit signal, then that object shall be declared within the declarative region formed by the function (see 10.1) or within the declarative region formed by the procedure; this rule also holds for the explicit ancestor, if any, of an implicit signal and also for the implicit signal GUARD. If a pure function is the parent of a given procedure, then that procedure shall not contain a reference to an explicitly declared file object (see 4.3.1.4) or to a shared variable (see 4.3.1.3).

Similarly, if a pure function subprogram contains a reference to an explicitly declared signal or variable object, or a slice or subelement (or slice thereof) of an explicit signal, then that object shall be declared within the declarative region formed by the function; this rule also holds for the explicit ancestor, if any, of an implicit signal and also for the implicit signal GUARD. A pure function shall not contain a reference to an explicitly declared file object.

A pure function shall not be the parent of an impure function.

The rules of the preceding three paragraphs apply to all pure function subprograms. For pure functions that are not foreign subprograms, violations of any of these rules are errors. However, since implementations cannot in general check that such rules hold for pure function subprograms that are foreign subprograms, a description calling pure foreign function subprograms not adhering to these rules is erroneous.

Example:

— The declaration of a foreign function subprogram:

```
package P is
   function F return INTEGER;
   attribute FOREIGN of F: function is
      "implementation-dependent information";
end package P;
```

NOTE 1—It follows from the visibility rules that a subprogram declaration shall be given if a call of the subprogram occurs textually before the subprogram body, and that such a declaration shall occur before the call itself.

NOTE 2—The preceding rules concerning pure function subprograms, together with the fact that function parameters shall be of mode **in**, imply that a pure function has no effect other than the computation of the returned value. Thus, a pure function invoked explicitly as part of the elaboration of a declaration, or one invoked implicitly as part of the simulation cycle, is guaranteed to have no effect on other objects in the description.

NOTE 3—VHDL does not define the parameter-passing mechanisms for foreign subprograms.

NOTE 4—The declarative parts and statement parts of subprograms decorated with the 'FOREIGN attribute are subject to special elaboration rules. See 12.3 and 12.4.5.

NOTE 5—A pure function subprogram shall not reference a shared variable. This prohibition exists because a shared variable cannot be declared in a subprogram declarative part and a pure function cannot reference any variable declared outside of its declarative region.

NOTE 6—A subprogram containing a wait statement shall not have an ancestor that is a subprogram declared within either a protected type declaration or a protected type body.

2.3 Subprogram overloading

Two formal parameter lists are said to have the same *parameter type profile* if and only if they have the same number of parameters, and if at each parameter position the corresponding parameters have the same base type. Two subprograms are said to have the same *parameter and result type profile* if and only if both have the same parameter type profile, and if either both are functions with the same result base type or neither of the two is a function.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

A given subprogram designator can be used to designate multiple subprograms. The subprogram designator is then said to be overloaded; the designated subprograms are also said to be overloaded and to overload each other. If two subprograms overload each other, one of them can hide the other only if both subprograms have the same parameter and result type profile.

A call to an overloaded subprogram is ambiguous (and therefore is an error) if the name of the subprogram, the number of parameter associations, the types and order of the actual parameters, the names of the formal parameters (if named associations are used), and the result type (for functions) are not sufficient to identify exactly one (overloaded) subprogram.

Similarly, a reference to an overloaded resolution function name in a subtype indication is ambiguous (and is therefore an error) if the name of the function, the number of formal parameters, the result type, and the relationships between the result type and the types of the formal parameters (as defined in 2.4) are not sufficient to identify exactly one (overloaded) subprogram specification.

Examples:

— Declarations of overloaded subprograms:

```
procedure Dump (F: inout Text; Value: Integer);
procedure Dump (F: inout Text; Value: String);

procedure Check (Setup: Time; signal D: Data; signal C: Clock);
procedure Check (Hold: Time; signal C: Clock; signal D: Data);
```

— Calls to overloaded subprograms:

```
Dump (Sys_Output, 12);
Dump (Sys_Error, "Actual output does not match expected output");

Check (Setup=>10 ns, D=>DataBus, C=>Clk1);
Check (Hold=>5 ns, D=>DataBus, C=>Clk2);
Check (15 ns, DataBus, Clk) ;
   --  Ambiguous if the base type of DataBus is the same type
   --  as the base type of Clk.
```

NOTE 1—The notion of parameter and result type profile does not include parameter names, parameter classes, parameter modes, parameter subtypes, or default expressions or their presence or absence.

NOTE 2—Ambiguities may (but need not) arise when actual parameters of the call of an overloaded subprogram are themselves overloaded function calls, literals, or aggregates. Ambiguities may also (but need not) arise when several overloaded subprograms belonging to different packages are visible. These ambiguities can usually be solved in two ways: qualified expressions can be used for some or all actual parameters and for the result, if any; or the name of the subprogram can be expressed more explicitly as an expanded name (see 6.3).

2.3.1 Operator overloading

The declaration of a function whose designator is an operator symbol is used to overload an operator. The sequence of characters of the operator symbol shall be one of the operators in the operator classes defined in 7.2.

The subprogram specification of a unary operator shall have a single parameter, unless the subprogram specification is a method (see 3.5.1) of a protected type. In this latter case, the subprogram specification shall have no parameters. The subprogram specification of a binary operator shall have two parameters; unless the subprogram specification is a method of a protected type, in which case, the subprogram specification shall have a single parameter. If the subprogram specification of a binary operator has two parameters, for each use of this operator, the first parameter is associated with the left operand, and the second parameter is associated with the right operand.

Documents
Document Sharing Hub
Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

For each of the operators "+" and "–", overloading is allowed both as a unary operator and as a binary operator.

NOTE 1—Overloading of the equality operator does not affect the selection of choices in a case statement in a selected signal assignment statement, nor does it affect the propagation of signal values.

NOTE 2—A user-defined operator that has the same designator as a short-circuit operator (i.e., a user-defined operator that overloads the short-circuit operator) is not invoked in a short-circuit manner. Specifically, calls to the user-defined operator always evaluate both arguments prior to the execution of the function.

NOTE 3—Functions that overload operator symbols may also be called using function call notation rather than operator notation. This statement is also true of the predefined operators themselves.

Examples:

```
type MVL is ('0', '1', 'Z', 'X');
function "and" (Left, Right: MVL) return MVL;
function "or" (Left, Right: MVL) return MVL;
function "not" (Value: MVL) return MVL;

signal Q,R,S: MVL;

Q <= 'X' or '1';
R <= "or" ('0','Z');
S <= (Q and R) or not S;
```

2.3.2 Signatures

A signature distinguishes between overloaded subprograms and overloaded enumeration literals based on their parameter and result type profiles. A signature can be used in an attribute name, entity designator, or alias declaration.

signature ::= [[type_mark { , type_mark }] [**return** type_mark]]

(Note that the initial and terminal brackets are part of the syntax of signatures and do not indicate that the entire right-hand side of the production is optional.) A signature is said to match the parameter and the result type profile of a given subprogram if, and only if, all of the following conditions hold:

— The number of type marks prior to the reserved word **return**, if any, matches the number of formal parameters of the subprogram.

— At each parameter position, the base type denoted by the type mark of the signature is the same as the base type of the corresponding formal parameter of the subprogram.

— If the reserved word **return** is present, the subprogram is a function and the base type of the type mark following the reserved word in the signature is the same as the base type of the return type of the function, or the reserved word **return** is absent and the subprogram is a procedure.

Similarly, a signature is said to match the parameter and result type profile of a given enumeration literal if the signature matches the parameter and result type profile of the subprogram equivalent to the enumeration literal defined in 3.1.1.

Example:

```
attribute BuiltIn of "or" [MVL, MVL return MVL]: function is TRUE;
   --  Because of the presence of the signature, this attribute
specification
   --  decorates only the "or" function defined in 2.3.1.
```

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

```
attribute Mapping of JMP [return OpCode] :literal is "001";
```

2.4 Resolution functions

A resolution function is a function that defines how the values of multiple sources of a given signal are to be resolved into a single value for that signal. Resolution functions are associated with signals that require resolution by including the name of the resolution function in the declaration of the signal or in the declaration of the subtype of the signal. A signal with an associated resolution function is called a resolved signal (see 4.3.1.2).

A resolution function shall be a pure function (see 2.1); moreover, it shall have a single input parameter of class **constant** that is a one-dimensional, unconstrained array whose element type is that of the resolved signal. The type of the return value of the function shall also be that of the signal. Errors occur at the place of the subtype indication containing the name of the resolution function if any of these checks fail (see 4.2).

The resolution function associated with a resolved signal determines the *resolved value* of the signal as a function of the collection of inputs from its multiple sources. If a resolved signal is of a composite type, and if subelements of that type also have associated resolution functions, such resolution functions have no effect on the process of determining the resolved value of the signal. It is an error if a resolved signal has more connected sources than the number of elements in the index type of the unconstrained array type used to define the parameter of the corresponding resolution function.

Resolution functions are implicitly invoked during each simulation cycle in which corresponding resolved signals are active (see 12.6.1). Each time a resolution function is invoked, it is passed an array value, each element of which is determined by a corresponding source of the resolved signal, but excluding those sources that are drivers whose values are determined by null transactions (see 8.4.1). Such drivers are said to be *off*. For certain invocations (specifically, those involving the resolution of sources of a signal declared with the signal kind **bus**), a resolution function may thus be invoked with an input parameter that is a null array; this occurs when all sources of the bus are drivers, and they are all off. In such a case, the resolution function returns a value representing the value of the bus when no source is driving it.

Example:

```
function WIRED_OR (Inputs: BIT_VECTOR) return BIT is
   constant FloatValue: BIT := '0';
begin
   if Inputs'Length = 0 then
      --  This is a bus whose drivers are all off.
      return FloatValue;
   else
      for I in Inputs'Range loop
         if Inputs(I) = '1' then
            return '1';
         end if;
      end loop;
      return '0';
   end if;
end function WIRED_OR;
```

2.5 Package declarations

A package declaration defines the interface to a package. The scope of a declaration within a package can be extended to other design units.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

package_declaration ::=
  package identifier **is**
    package_declarative_part
  end [**package**] [*package*_simple_name] ;

package_declarative_part ::=
  { package_declarative_item }

package_declarative_item ::=
  subprogram_declaration
| type_declaration
| subtype_declaration
| constant_declaration
| signal_declaration
| *shared*_variable_declaration
| file_declaration
| alias_declaration
| component_declaration
| attribute_declaration
| attribute_specification
| disconnection_specification
| use_clause
| group_template_declaration
| group_declaration
| nature_declaration
| subnature_declaration
| terminal_declaration

If a simple name appears at the end of the package declaration, it shall repeat the identifier of the package declaration.

If a package declarative item is a type declaration (i.e., a full type declaration whose type definition is a protected type definition), then that protected type definition shall not be a protected type body.

Items declared immediately within a package declaration become visible by selection within a given design unit wherever the name of that package is visible in the given unit. Such items may also be made directly visible by an appropriate use clause (see 10.4).

NOTE—Not all packages will have a package body. In particular, a package body is unnecessary if no subprograms, deferred constants, or protected type definitions are declared in the package declaration.

Examples:

— A package declaration that needs no package body:

```
package TimeConstants is
   constant tPLH: Time := 10 ns;
   constant tPHL: Time := 12 ns;
   constant tPLZ: Time := 7 ns;
   constant tPZL: Time := 8 ns;
   constant tPHZ: Time := 8 ns;
   constant tPZH: Time := 9 ns;
end TimeConstants;
```

— A package declaration that needs a package body:

```
package TriState is
   type Tri is ('0', '1', 'Z', 'E');
```

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

```
        function BitVal (Value: Tri) return Bit;
        function TriVal (Value: Bit) return Tri;
        type TriVector is array (Natural range <>) of Tri;
        function Resolve (Sources: TriVector) return Tri;
    end package TriState;
```

2.6 Package bodies

A package body defines the bodies of subprograms and the values of deferred constants declared in the interface to the package.

package_body ::=
  package body *package*_simple_name **is**
    package_body_declarative_part
  end [**package body**] [*package*_simple_name] ;

package_body_declarative_part ::=
  { package_body_declarative_item }

package_body_declarative_item ::=
  subprogram_declaration
  | subprogram_body
  | type_declaration
  | subtype_declaration
  | constant_declaration
  | *shared*_variable_declaration
  | file_declaration
  | alias_declaration
  | use_clause
  | group_template_declaration
  | group_declaration

The simple name at the start of a package body shall repeat the package identifier. If a simple name appears at the end of the package body, it shall be the same as the identifier in the package declaration.

In addition to subprogram body and constant declarative items, a package body may contain certain other declarative items to facilitate the definition of the bodies of subprograms declared in the interface. Items declared in the body of a package cannot be made visible outside of the package body.

If a given package declaration contains a deferred constant declaration (see 4.3.1.1), then a constant declaration with the same identifier shall appear as a declarative item in the corresponding package body. This object declaration is called the *full* declaration of the deferred constant. The subtype indication given in the full declaration shall conform to that given in the deferred constant declaration.

Within a package declaration that contains the declaration of a deferred constant, and within the body of that package (before the end of the corresponding full declaration), the use of a name that denotes the deferred constant is only allowed in the default expression for a local generic, local port, or formal parameter. The result of evaluating an expression that references a deferred constant before the elaboration of the corresponding full declaration is not defined by the language.

Example:

```
package body TriState is
```

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

```
   function BitVal (Value: Tri) return Bit is
      constant Bits : Bit_Vector := "0100";
   begin
      return Bits(Tri'Pos(Value));
   end;

   function TriVal (Value: Bit) return Tri is
   begin
      return Tri'Val(Bit'Pos(Value));
   end;

   function Resolve (Sources: TriVector) return Tri is
      variable V: Tri := 'Z';
   begin
      for i in Sources'Range loop
         if Sources(i) /= 'Z' then
            if V = 'Z' then
               V := Sources(i);
            else
               return 'E';
            end if;
         end if;
      end loop;
      return V;
   end;

end package body TriState;
```

2.7 Conformance rules

Whenever the language rules either require or allow the specification of a given subprogram to be provided in more than one place, the following variations are allowed at each place:

— A numeric literal can be replaced by a different numeric literal if and only if both have the same value.

— A simple name can be replaced by an expanded name in which this simple name is the selector if, and only if, at both places the meaning of the simple name is given by the same declaration.

Two subprogram specifications are said to *conform* if, apart from comments and the preceding allowed variations, both specifications are formed by the same sequence of lexical elements and if corresponding lexical elements are given the same meaning by the visibility rules.

Conformance is likewise defined for subtype indications in deferred constant declarations.

NOTE 1—A simple name can be replaced by an expanded name even if the simple name is itself the prefix of a selected name. For example, Q.R can be replaced by P.Q.R if Q is declared immediately within P.

NOTE 2—The subprogram specification of an impure function is never conformant to a subprogram specification of a pure function.

NOTE 3—The following specifications do not conform since they are not formed by the same sequence of lexical elements:

```
procedure P (X,Y: INTEGER)
procedure P (X: INTEGER; Y: INTEGER)
procedure P (X,Y: in INTEGER)
```

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

3. Types and natures

This clause describes the various categories of types and natures that are provided by the language as well as those specific types that are predefined. The declarations of all predefined types are contained in package STANDARD, the declaration of which appears in Clause 14.

A type is characterized by a set of values and a set of operations. The set of operations of a type includes the explicitly declared subprograms that have a parameter or result of the type. The remaining operations of a type are the basic operations and the predefined operators (see 7.2). These operations are each implicitly declared for a given type declaration immediately after the type declaration and before the next explicit declaration, if any.

A *basic operation* is an operation that is inherent in one of the following:

— An assignment (in assignment statements and initializations)

— An allocator

— A selected name, an indexed name, or a slice name

— A qualification (in a qualified expression), an explicit type conversion, a formal or actual part in the form of a type conversion, or an implicit type conversion of a value of type *universal_integer* or *universal_real* to the corresponding value of another numeric type

— A numeric literal (for a universal type), the literal **null** (for an access type), a string literal, a bit string literal, an aggregate, or a predefined attribute

There are five classes of types. *Scalar* types are integer types, floating-point types, physical types, and types defined by an enumeration of their values; values of these types have no elements. *Composite* types are array and record types; values of these types consist of element values. *Access* types provide access to objects of a given type. *File* types provide access to objects that contain a sequence of values of a given type. *Protected types* provide atomic and exclusive access to variables accessible to multiple processes.

The set of possible values for an object of a given type can be subjected to a condition that is called a *constraint* (the case where the constraint imposes no restriction is also included); a value is said to satisfy a constraint if it satisfies the corresponding condition. A *subtype* is a type together with a constraint. A value is said to *belong to a subtype* of a given type if it belongs to the type and satisfies the constraint; the given type is called the *base type* of the subtype. A type is a subtype of itself; such a subtype is said to be *unconstrained* (it corresponds to a condition that imposes no restriction). The base type of a type is the type itself.

The set of operations defined for a subtype of a given type includes the operations defined for the type; however, the assignment operation to an object having a given subtype only assigns values that belong to the subtype. Additional operations, such as qualification (in a qualified expression) are implicitly defined by a subtype declaration.

The term *subelement* is used in this standard in place of the term element to indicate either an element, or an element of another element or subelement. Where other subelements are excluded, the term *element* is used instead.

A given type shall not have a subelement whose type is the given type itself. Similarly, a given nature shall not have a subelement whose nature is the given nature itself. Natures are introduced in 3.6.

A *member* of an object is one of the following:

— A slice of the object

— A subelement of the object

— A slice of a subelement of the object

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

The name of a class of types or natures is used in this standard as a qualifier for objects and values that have a type or nature of the class considered. For example, the term *array object* is used for an object whose type is an array type or whose nature is an array nature; similarly, the term *access value* is used for a value of an access type.

NOTE—The set of values of a subtype is a subset of the values of the base type. This subset need not be a proper subset.

3.1 Scalar types

Scalar types consist of *enumeration types, integer types, physical types*, and *floating-point types*. Enumeration types and integer types are called *discrete types.* Integer types, floating-point types, and physical types are called *numeric types.* All scalar types are ordered; that is, all relational operators are predefined for their values. Each value of a discrete or physical type has a position number that is an integer value.

scalar_type_definition ::=
    enumeration_type_definition
  | integer_type_definition
  | floating_type_definition
  | physical_type_definition

range_constraint ::= **range** range

range ::=
    *range*_attribute_name
  | simple_expression direction simple_expression

direction ::= **to** | **downto**

A range specifies a subset of values of a scalar type. A range is said to be a *null* range if the specified subset is empty.

The range L **to** R is called an *ascending* range; if L > R, then the range is a null range. The range L **downto** R is called a *descending range*; if L < R, then the range is a null range. The smaller of L and R is called the *lower bound*, and the larger, the *upper bound*, of the range. The value V is said to *belong to the range* if the relations (*lower bound* <= V) and (V <= *upper bound*) are both true and the range is not a null range. The operators >, <, and <= in the preceding definitions are the predefined operators of the applicable scalar type.

For values of discrete or physical types, a value V1 is said to be *to the left* of a value V2 within a given range if both V1 and V2 belong to the range and either the range is an ascending range and V2 is the successor of V1, or the range is a descending range and V2 is the predecessor of V1. A list of values of a given range is in *left to right order* if each value in the list is to the left of the next value in the list within that range, except for the last value in the list.

If a range constraint is used in a subtype indication, the type of the expressions (likewise, of the bounds of a range attribute) shall be the same as the base type of the type mark of the subtype indication. A range constraint is *compatible* with a subtype if each bound of the range belongs to the subtype or if the range constraint defines a null range. Otherwise, the range constraint is not compatible with the subtype.

The direction of a range constraint is the same as the direction of its range.

NOTE—Indexing and iteration rules use values of discrete types.

Documents
Document Sharing Hub
Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

3.1.1 Enumeration types

An enumeration type definition defines an enumeration type.

enumeration_type_definition ::=
(enumeration_literal { , enumeration_literal })

enumeration_literal ::= identifier | character_literal

The identifiers and character literals listed by an enumeration type definition shall be distinct within the enumeration type definition. Each enumeration literal is the declaration of the corresponding enumeration literal; for the purpose of determining the parameter and result type profile of an enumeration literal, this declaration is equivalent to the declaration of a parameterless function whose designator is the same as the enumeration literal and whose result type is the same as the enumeration type.

An enumeration type is said to be a *character type* if at least one of its enumeration literals is a character literal.

Each enumeration literal yields a different enumeration value. The predefined order relations between enumeration values follow the order of corresponding position numbers. The position number of the value of the first listed enumeration literal is zero; the position number for each additional enumeration literal is one more than that of its predecessor in the list.

If the same identifier or character literal is specified in more than one enumeration type definition, the corresponding literals are said to be *overloaded*. At any place where an overloaded enumeration literal occurs in the text of a program, the type of the enumeration literal is determined according to the rules for overloaded subprograms (see 2.3).

Each enumeration type definition defines an ascending range.

Examples:

```
type MULTI_LEVEL_LOGIC is (LOW, HIGH, RISING, FALLING, AMBIGUOUS);

type BIT is ('0','1');

type SWITCH_LEVEL is ('0','1','X');     --  Overloads '0' and '1'
```

3.1.1.1 Predefined enumeration types

The predefined enumeration types are CHARACTER, BIT, BOOLEAN, SEVERITY_LEVEL, FILE_OPEN_KIND, and FILE_OPEN_STATUS.

The predefined type CHARACTER is a character type whose values are the 256 characters of the ISO/IEC 8859-1:1998 [B7][5] character set. Each of the 191 graphic characters of this character set is denoted by the corresponding character literal.

The declarations of the predefined types CHARACTER, BIT, BOOLEAN, SEVERITY_LEVEL, FILE_OPEN_KIND, and FILE_OPEN_STATUS appear in package STANDARD in Clause 14.

[5]The numbers in brackets correspond to those of the bibliography in Annex F.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

NOTE 1—The first 33 nongraphic elements of the predefined type CHARACTER (from NUL through DEL) are the ASCII abbreviations for the nonprinting characters in the ASCII set (except for those noted in Clause 14). The ASCII names are chosen as ISO/IEC 8859-1:1998 [B7] does not assign them abbreviations. The next 32 (C128 through C159) are also not assigned abbreviations, so names unique to VHDL are assigned.

NOTE 2—Type BOOLEAN can be used to model either active high or active low logic depending on the particular conversion functions chosen to and from type BIT.

3.1.2 Integer types

An integer type definition defines an integer type whose set of values includes those of the specified range.

integer_type_definition ::= range_constraint

An integer type definition defines both a type and a subtype of that type. The type is an anonymous type, the range of which is selected by the implementation; this range shall be such that it wholly contains the range given in the integer type definition. The subtype is a named subtype of this anonymous base type, where the name of the subtype is that given by the corresponding type declaration and the range of the subtype is the given range.

Each bound of a range constraint that is used in an integer type definition shall be a locally static expression of some integer type, but the two bounds need not have the same integer type. (Negative bounds are allowed.)

Integer literals are the literals of an anonymous predefined type that is called *universal_integer* in this standard. Other integer types have no literals. However, for each integer type there exists an implicit conversion that converts a value of type *universal_integer* into the corresponding value (if any) of the integer type (see 7.3.5).

The position number of an integer value is the corresponding value of the type *universal_integer*.

The same arithmetic operators are predefined for all integer types (see 7.2). It is an error if the execution of such an operation (in particular, an implicit conversion) cannot deliver the correct result (that is, if the value corresponding to the mathematical result is not a value of the integer type).

An implementation may restrict the bounds of the range constraint of integer types other than type *universal_integer*. However, an implementation shall allow the declaration of any integer type whose range is wholly contained within the bounds –2147483647 and +2147483647 inclusive.

Examples:

```
type TWOS_COMPLEMENT_INTEGER is range -32768 to 32767;

type BYTE_LENGTH_INTEGER is range 0 to 255;

type WORD_INDEX is range 31 downto 0;

subtype HIGH_BIT_LOW is BYTE_LENGTH_INTEGER range 0 to 127;
```

3.1.2.1 Predefined integer types

The only predefined integer type is the type INTEGER. The range of INTEGER is implementation dependent, but it is guaranteed to include the range –2147483647 to +2147483647. It is defined with an ascending range.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

NOTE—The range of INTEGER in a particular implementation is determinable from the values of its 'LOW and 'HIGH attributes.

3.1.3 Physical types

Values of a physical type represent measurements of some quantity. Any value of a physical type is an integral multiple of the primary unit of measurement for that type.

physical_type_definition ::=
    range_constraint
        units
            primary_unit_declaration
            { secondary_unit_declaration }
        end units [*physical_type*_simple_name]

primary_unit_declaration ::= identifier ;

secondary_unit_declaration ::= identifier = physical_literal ;

physical_literal ::= [abstract_literal] *unit*_name

A physical type definition defines both a type and a subtype of that type. The type is an anonymous type, the range of which is selected by the implementation; this range shall be such that it wholly contains the range given in the physical type definition. The subtype is a named subtype of this anonymous base type, where the name of the subtype is that given by the corresponding type declaration and the range of the subtype is the given range.

Each bound of a range constraint that is used in a physical type definition shall be a locally static expression of some integer type, but the two bounds need not have the same integer type. (Negative bounds are allowed.)

Each unit declaration (either the primary unit declaration or a secondary unit declaration) defines a *unit name*. Unit names declared in secondary unit declarations shall be directly or indirectly defined in terms of integral multiples of the primary unit of the type declaration in which they appear. The position numbers of unit names need not lie within the range specified by the range constraint.

If a simple name appears at the end of a physical type declaration, it shall repeat the identifier of the type declaration in which the physical type definition is included.

The abstract literal portion (if present) of a physical literal appearing in a secondary unit declaration shall be an integer literal.

A physical literal consisting solely of a unit name is equivalent to the integer 1 followed by the unit name.

There is a position number corresponding to each value of a physical type. The position number of the value corresponding to a unit name is the number of primary units represented by that unit name. The position number of the value corresponding to a physical literal with an abstract literal part is the largest integer that is not greater than the product of the value of the abstract literal and the position number of the accompanying unit name.

The same arithmetic operators are predefined for all physical types (see 7.2). It is an error if the execution of such an operation cannot deliver the correct result (i.e., if the value corresponding to the mathematical result is not a value of the physical type).

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Documents
Document Sharing Hub
Full document details: IEC/IEEE 61691-6-2009

An implementation may restrict the bounds of the range constraint of a physical type. However, an implementation shall allow the declaration of any physical type whose range is wholly contained within the bounds –2147483647 and +2147483647 inclusive.

Examples:

```
type DURATION is range -1E18 to 1E18
      units
         fs;                          --femtosecond
         ps     =   1000 fs;          --picosecond
         ns     =   1000 ps;          --nanosecond
         us     =   1000 ns;          --microsecond
         ms     =   1000 us;          --millisecond
         sec    =   1000 ms;          --second
         min    =   60 sec;           --minute
      end units;

type DISTANCE is range 0 to 1E16
      units
      -- primary unit:
         Å;                           --angstrom

      -- metric lengths:
         nm     =   10 Å;             --nanometer
         um     =   1000 nm;          --micrometer (or micron)
         mm     =   1000 um;          --millimeter
         cm     =   10 mm;            --centimeter
         m      =   1000 mm;          --meter
         km     =   1000 m;           --kilometer

      -- English lengths:
         mil    =   254000 Å;         --mil
         inch   =   1000 mil;         --inch
         ft     =   12 inch;          --foot
         yd     =   3 ft;             --yard
         fm     =   6 ft;             --fathom
         mi     =   5280 ft;          --mile
         lg     =   3 mi;             --league
      end units DISTANCE;

variable x: distance;
variable y: duration;
variable z: integer;

x := 5 Å + 13 ft - 27 inch;
y := 3 ns + 5 min;
z := ns / ps;
x := z * mi;
y := y/10;
z := 39.34 inch / m;
```

NOTE 1—The 'POS and 'VAL attributes may be used to convert between abstract values and physical values.

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009

NOTE 2—The value of a physical literal, whose abstract literal is either the integer value zero or the floating-point value zero, is the same value (specifically zero primary units) no matter what unit name follows the abstract literal.

3.1.3.1 Predefined physical types

The only predefined physical type is type TIME. The range of TIME is implementation dependent, but it is guaranteed to include the range –2147483647 to +2147483647. It is defined with an ascending range. All specifications of delays and pulse rejection limits shall be of type TIME. The declaration of type TIME appears in package STANDARD in Clause 14.

By default, the primary unit of type TIME (1 femtosecond) is the *resolution limit* for type TIME. Any TIME value whose absolute value is smaller than this limit is truncated to zero (0) time units. An implementation may allow a given execution of a model (see 12.6) to select a secondary unit of type TIME as the resolution limit. Furthermore, an implementation may restrict the precision of the representation of values of type TIME and the results of expressions of type TIME, provided that values as small as the resolution limit are representable within those restrictions. It is an error if a given unit of type TIME appears anywhere within the design hierarchy defining a model to be executed, and if the position number of that unit is less than that of the secondary unit selected as the resolution limit for type TIME during the execution of the model, unless that unit is part of a physical literal whose abstract literal is either the integer value zero or the floating-point value zero.

NOTE—By selecting a secondary unit of type TIME as the resolution limit for type TIME, it may be possible to simulate for a longer period of simulated time, with reduced accuracy, or to simulate with greater accuracy for a shorter period of simulated time.

Cross-references: Delay and rejection limit in a signal assignment, 8.4; disconnection, delay of a guarded signal, 5.3; function NOW, 14.2; predefined attributes, functions of TIME, 14.1; simulation time, 12.6.2 and 12.6.3; type TIME, 14.2; updating a projected waveform, 8.4.1; wait statements, timeout clause in, 8.1; Elaboration of a declarative part, 12.3.

3.1.4 Floating-point types

Floating-point types provide approximations to the real numbers.

floating_type_definition ::= range_constraint

A floating type definition defines both a type and a subtype of that type. The type is an anonymous type, the range of which is selected by the implementation; this range shall be such that it wholly contains the range given in the floating type definition. The subtype is a named subtype of this anonymous base type, where the name of the subtype is that given by the corresponding type declaration and the range of the subtype is the given range. The tolerance group of the subtype (see 4.2) is a value of type STRING equal to an empty string literal.

Each bound of a range constraint that is used in a floating type definition shall be a locally static expression of some floating-point type, but the two bounds need not have the same floating-point type. (Negative bounds are allowed.)

Floating-point literals are the literals of an anonymous predefined type that is called *universal_real* in this standard. Other floating-point types have no literals. However, for each floating-point type there exists an implicit conversion that converts a value of type *universal_real* into the corresponding value (if any) of the floating-point type (see 7.3.5).

The same arithmetic operations are predefined for all floating-point types (see 7.2). A design is erroneous if the execution of such an operation cannot deliver the correct result (that is, if the value corresponding to the mathematical result is not a value of the floating-point type).

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Documents
Document Sharing Hub
Full document details: IEC/IEEE 61691-6-2009

An implementation shall choose a representation for all floating-point types except for *universal_real* that conforms either to IEEE Std 754™-1985 [B2] or to IEEE Std 854™-1987 [B3]; in either case, a minimum representation size of 64 bits is required for this *chosen representation*.

An implementation may restrict the bounds of the range constraint of floating-point types other than type *universal_real*. However, an implementation shall allow the declaration of any floating-point type whose range is wholly contained within the bounds allowed by the chosen representation.

NOTE—An implementation is not required to detect errors in the execution of a predefined floating-point arithmetic operation, since the detection of overflow conditions resulting from such operations might not be easily accomplished on many host systems.

3.1.4.1 Predefined floating-point types

The only predefined floating-point type is the type REAL. The range of REAL is host-dependent, but it is guaranteed to be the largest allowed by the chosen representation. It is defined with an ascending range.

NOTE—The range of REAL in a particular implementation is determinable from the values of its 'LOW and 'HIGH attributes.

3.2 Composite types

Composite types are used to define collections of values. These include both arrays of values (collections of values of a homogeneous type) and records of values (collections of values of potentially heterogeneous types).

composite_type_definition ::=
    array_type_definition
  | record_type_definition

An object of a composite type represents a collection of objects, one for each element of the composite object. It is an error if a composite type contains elements of file types or protected types. Thus an object of a composite type ultimately represents a collection of objects of scalar or access types, one for each noncomposite subelement of the composite object.

3.2.1 Array types

An array object is a composite object consisting of elements that have the same subtype. The name for an element of an array uses one or more index values belonging to specified discrete types. The value of an array object is a composite value consisting of the values of its elements.

array_type_definition ::=
  unconstrained_array_definition | constrained_array_definition

unconstrained_array_definition ::=
  array (index_subtype_definition { , index_subtype_definition })
    of *element*_subtype_indication

constrained_array_definition ::=
  array index_constraint **of** *element*_subtype_indication

index_subtype_definition ::= type_mark **range** <>

index_constraint ::= (discrete_range { , discrete_range })

Published by IEC under licence from IEEE. © 2007 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 25,2026 at 20:14:45 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEC/IEEE 61691-6-2009