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INTERNATIONAL STANDARD

IEEE Std 1505.1™

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Standard for the common test interface pin map configuration for high-density, single-tier electronics test requirements utilizing IEEE Std 1505™

IEC 63003:2015-12(en) IEEE Std 1505.1-2008

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Approved 26 September 2008

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Abstract: This standard represents an extension to the IEEE 1505 receiver fixture interface (RFI) standard specification. Particular emphasis is placed on defining within the IEEE 1505 RFI standard a more specific set of performance requirements that employ a common scalable: (a) pin map configuration; (b) specific connector modules; (c) respective contacts; (d) recommended switching implementation; and (e) legacy automatic test equipment (ATE) transitional devices. This is intentionally done to standardize the footprint and assure mechanical and electrical interoperability between past and future automatic test systems (ATS).

Keywords: ATE, ATS, fixture, ICD, IEEE 1505.1™, interface, ITA, mass termination, receiver, scalable, TPS, UUT

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IEEE Introduction

This introduction is not part of IEEE Std 1505.1-2008, IEEE Standard for the Common Test Interface Pin Map Configuration for High-Density, Single-Tier Electronics Test Requirements Utilizing IEEE Std 1505™.

This standard stems from the history of ATE implementations having unique input/output (I/O) pin out definitions. This uniqueness has prevented the interoperability of test program sets (TPSs) among different ATEs within the same organizations. Even if the same RFI was used by the target ATE, the signals I/O could not be guaranteed to be at the same pin location. This is due to there being no suitable standard pin out definition for general purpose electronic testing applications.

IEEE Std 1505-2006[a] has addressed part of the interoperability problem by defining the common mechanical interface for the ATE. This project takes the TPS interoperability problem one step further toward completion by standardizing the electrical signal I/O pin map for general purpose electronic testing applications.

Particular emphasis is placed on defining within the IEEE 1505 RFI standard a more specific set of performance requirements that employ a common scalable: (a) framework; (b) pin map configuration; (c) specific connector modules; (d) respective contacts; (e) recommended switching implementation; and (f) legacy ATE transitional devices. This is intentionally done to standardize the footprint and assure mechanical and electrical interoperability between past and future ATS. The suggested mechanical and electrical requirements necessary to implement a specific IEEE 1505 RFI product in support of a common test interface (CTI) across all U.S. Department of Defense (DoD) defense agencies, related aerospace industry, and a variety of non-U.S. government agencies such as the U.K. Ministry of Defense (MoD) is provided.

The DoD is a major buyer and user of ATE; however, existing acquisition guidance desires the use of commercial standards and/or best practices for these systems. Suitable standards currently do not exist in the commercial marketplace; therefore, this standard will provide such specification.

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1. Overview

1.1 Scope

The scope of this standard is the definition of a pin map utilizing the IEEE 1505™ [1] receiver fixture interface (RFI). The pin map defined within this standard shall apply to military and aerospace automatic test equipment (ATE) testing applications.

[1] Information on references can be found in Clause 2.

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1.2 Purpose

Standardization of a common input/output (I/O) will enable the interoperability of IEEE 1505 compliant interface fixtures [also known as *interface test adapters* (ITA), *interface devices* (IDs), or *interconnecting devices* (ICDs)] on multiple ATE systems utilizing the IEEE 1505 RFI.

1.3 Statement of the problem

1.3.1 U.S. Government guidance

From 1980 to 1992, the U.S. Department of Defense (DoD) investment in field, depot, and factory automatic test systems (ATS) exceeded $35 billion with an additional $15 billion for associated support. Most of this test capability was acquired as part of individual weapon system procurements. This led to a proliferation of different custom equipment types with unique interfaces. Recent policy decisions have changed the direction of the purchase of test equipment towards a standards based approach with both hardware and software critical interface requirements.

The U.S. DoD Instruction 5000.2-R1 ATS Policy states: "ATS capabilities shall be defined through critical hardware and software elements" (see [B2][2]). This policy however, did not define these critical elements. The Critical Interfaces Project was created to define critical ATS elements.

1.3.2 Critical Interfaces Project

The Factory-to-Field Integration of Defense Test Systems Project (commonly referred to as the *Critical Interfaces Project*) was started in the latter part of 1995. The Critical Interfaces Working Group (CIWG) within the Joint-Service ATS Research and Development Integrated Product Team (ARI) was established to perform the project. The ATS Executive Agent Office (EAO) has provided project management and coordination among the Air Force, Army, Marine Corps, and Navy participants. In addition, many industry representatives have participated. The CIWG published their findings in the Automatic Test System Critical Interfaces Report [B1] and this report served as the basis for the development of the RFI architecture and subsequent specification.

The objective of the Critical Interfaces Project was to demonstrate the feasibility of reducing the cost to re-host test program sets (TPSs) and increase the interoperability of TPS software among the military services by using standardized interfaces.

Interfaces that offer the potential to achieve this objective are deemed critical. Potential savings will be quantified through demonstration. The Automatic Test System Critical Interfaces Report [B1] is maintained by the ATS EAO and provides guidance to DoD ATE acquisition programs. This document also addressed the requirements of DoD Regulation 5000.2-R1 [B2] and assisted in migrating the DoD designated tester families towards a common solution. The Hardware Interfaces (HI) Subcommittee of the IEEE Standards Coordinating Committee on Test and Diagnosis for Electronic Systems (SCC20) applied the recommendations of the report as it related to the RFI, to the extent that the current RFI standard is in full compliance with the report.

1.3.3 CTIWG guidance recommendations

During the Common Test Interface Working Group (CTIWG) October 2003 meeting, the DoD provided the following recommendations as guidance for the Working Group's success:

[2] The numbers in brackets correspond to those of the bibliography in Annex B.

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a) Identify a modular/scaleable interface

b) Allow use of different size ID/fixture on the same general purpose interface (GPI)

c) Ensure TPS hardware compatibility as interface grows

d) Provide legacy system support

e) Provide a transition path to support legacy TPS hardware

f) Adhere to an open architecture system

g) Built to one specification

h) Multiple sources

i) Non-proprietary design and components

j) Ensure capabilities that provision for growth and special requirements

k) Provide room for future expansion and TPS requirements

l) Support and Promote the use of commercial-off-the-shelf (COTS) interconnect components

m) Use industry standard connector technology

1.3.4 CTIWG legacy test program set support

In support of these recommendations, the CTI architecture shall assure past legacy and future TPS *plug and play* compatibility between defense agencies and defense-aerospace suppliers. Areas addressed by the CTIWG include:

a) Pin mapping

b) Scalability

c) TPS legacy support

d) Connector parametric (dc to light)

e) Reliability and maintainability

f) Physical

g) Switching

h) Design-to-cost factors

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated referenced, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1505-2006, IEEE Standard for Receiver Fixture Interface.[3, 4]

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3. Definitions, acronyms, and abbreviations

3.1 Definitions

For the purposes of this document, the following terms and definitions apply. *The Authoritative Dictionary of IEEE Standards Terms* [B5] should be referenced for terms not defined in this clause.

3.1.1 pin map: The data table and explanatory text that provides the assignment of electrical characteristics or instrument I/O to specific pins.

3.2 Specification terms

The specification terms used throughout this standard are described as follows.

Rule: Rules *shall* be followed to ensure compatibility to the standard. A rule is characterized by the use of the words *shall* and *shall not*. These words are not used for any other purpose other than stating rules.

Recommendation: Recommendations consist of advice to applicants that will affect the usability of the final device. Discussions of particular hardware to enhance throughput would fall under a recommendation. These should be followed to avoid problems and to obtain optimum performance.

Suggestion: A suggestion contains advice that is helpful but not vital. The reader is encouraged to consider the advice before discarding it. Suggestions are included to help the novice designer with problematic areas of the design.

Permission: Permissions are included to clarify the areas of the specification that are not specifically prohibited. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. The word *may* is reserved for indicating permissions.

Observation: Observations spell out implications of rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules, so that the reader understands why the rule must be followed.

3.3 Acronyms and abbreviations

ACPS	alternating current power supply
ADC	analog-to-digital converter
AI	analog instrument
AM	amplitude modulation
ATE	automatic test equipment
ATS	automatic test system
AWG	arbitrary waveform generator, American wire gauge

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CAL	calibration
CAN	controller-area network
CASS	Consolidated Automated Support System[5]
CH	channel
CIWG	Critical Interfaces Working Group
CLK	clock
COTS	commercial-off-the-shelf
CSW	coax switch
CTI	common test interface
DAC	digital-to-analog converter
DAS	display analyzer-simulator
DCPS	direct current power supply
DMM	digital multi-meter
DoD	U.S. Department of Defense
DTC	design-to-cost
ECL	emmitter-coupled logic
ESTS	Electronic Systems Test Set[6]
ETE	end to end
EXT	external
freq	frequency
FTIC	frequency time interval counter
GND	ground
GPI	general purpose interface
HPL	high-power load
IAIS	improved avionics intermediate shop
ICD	interconnecting device

[5] US Navy Tester, AN/USM-636 (V).
[6] US Air Force Tester, AN/GSM-397 (V).

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ID	interface device
IFTE	Integrated Family of Test Equipment [7]
Instr	instrument
I/O	input/output
ITA	interface test adapter
JTAG	Joint Testability Action Group
LCC	life-cycle costs
LFC	low-frequency calibrator
LM-STAR®	Lockheed Martin Star[8]
LPL	low-power load
LXI	LAN extensions for instrumentation
max	maximum
min	minimum
MOD	modulation
MoD	Ministry of Defense (UK)
MOD SRC	modulation source
MRK	marker
MTA	microwave transition analyzer
MTBF	mean time between failures
MUX	multiplexer
NOM	nominal
OCD	open-collector driver
ORD	Operational Requirements Document
PAM	phase-angle modulation
PCI	Peripheral Component Interface

[7] US Army Tester, AN/USM-632 (V)3.
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PECL	positive emmitter-coupled logic
PGEN	pulse generator
PH	phase
PM	pulse (or phase) modulation, power meter
Prog	programmable
PS	power supply
PSW	power switch
PXI	PCI Extensions for Instrumentation (compact PCI format)
RAF	Royal Air Force
ResLoad	resistive load
RF	radio frequency
RFI	receiver fixture interface
RSIA	raster stroke image acquisition
SAMe	sistema automatico de mantenimiento estandar
Spec An	spectrum analyzer
STA	system trigger assembly
Std	Standard
Sync	synchronizer
TETS	Third Echelon Test System[9]
TPS	test program set
Trig	trigger
TSP	twisted shielded pair
TTL	transistor-transistor logic
UBIC	universal bus interface controller
USB	Universal Serial Bus
UUT	unit under test
VGA	Versatile Graphics Adapter

[9] US Marine Tester, AN/USM-657 (V)1, (V)2, (V)3.

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VME versa-module extended

VXI VME extended for instrumentation

4. Common test interface requirements

4.1 Introduction

The following subclauses and illustrations describe the requirements for this standard, IEEE Std 1505.1-2008, to support military/aerospace test requirements. This information is supplemental and not stand-alone and shall coexist with that presented in the IEEE Std 1505 RFI specifications, Clause 1 through Clause 6.

The IEEE 1505.1 standard for the use of IEEE 1505 RFI to support military/aerospace test requirements represents a higher order subset of cost/physical/signal performance requirements to meet specific industry and defense agency goals of a common test interface (CTI). These high order requirements expand on the previously defined RFI: (a) framework; (b) connector modules and respective contacts; to meet objectives for: (c) a common scalable pin map configuration; (d) switching; and (e) legacy ATS transitional device for Third Echelon Test System (TETS), Consolidated Automated Support System (CASS), Integrated Family of Test Equipment (IFTE), and others as deemed necessary by the cognizant agencies. This is intentionally done to standardize the footprint and assure mechanical and electrical interoperability between past and future ATS.

4.2 CTI open system requirements

4.2.1 Government “open system” policy

On 29 November 1994, the Honorable Paul G. Kaminski, Under Secretary of Defense for Acquisition and Technology, directed acquisition executives in the DoD to use “open systems” specifications and standards (electrical, mechanical, thermal, etc.), for acquisition of all weapon systems electronics to the greatest extent practical. The Open Systems Joint Task Force (OS-JTF) was formed in September 1994 to: “Sponsor and accelerate the adoption of open systems in weapons systems and subsystems electronics to reduce life-cycle costs (LCC) and facilitate effective weapon system intra- and interoperability.”

4.2.2 CTI “open” architecture

Rule 4.2.2: An open standard CTI *architecture* shall identify components, the relationship between components, and the rules for the architecture’s composition.

Recommendation 4.2.2: Typical guidelines for addressing the CTI architecture should include:

a) Define and describe a system architecture that is traceable to the Operational Requirements Document (ORD).

b) A preferred architecture is modular, hierarchical and layered, and is based on open standards at its interfaces.

c) Selection of an architecture shall be a cooperative process between government and industry.

d) Specify key performance attributes of system building blocks including internal interface standards.

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e) Where a new system is contemplated, consensus among potential contractors and their key suppliers on application of widely accepted standards is desirable.

f) Identify aspects of the program that might limit the use of an open systems approach.

g) Determine the level at which the architecture will be defined for the system.

h) Architecture approach resulting from a system engineering process shall be linked to a business case analysis.

i) Decisions about architecture shall be linked to performance, LCC, schedule, and risk.

j) Identify opportunities for reuse of hardware and software configuration items and dependence upon interfaces.

4.3 CTI cost requirements

Recommendation 4.3a: Fundamental to the implementation of the CTI recommended practice should be the paramount need to address design-to-costs (DTC) and LCC attributed to test interface and TPS requirements.

Recommendation 4.3b: CTI should improve the test acquisition process by creating a competitive multi-vendor environment that provisions common module components that can be procured as COTS, at pricing that benefits from industry economics-of-scale production/quality processes, and improved time-to-market availability.

Recommendation 4.3c: CTI should meet advanced functional and technological needs through shared industry R&D, multi-functional/virtual modules that can be replicated, distributed, and reconfigured to meet a broad set of applications without customization. Extend legacy system life through technology insertion of plug and play enhancements based upon standardized infrastructure, and related cost-avoidance of ATS obsolescence.

Recommendation 4.3d: CTI should minimize configuration variations and related software customization and adjustments between unique test assets, integration methods, and signal routing schemes.

Recommendation 4.3e: CTI should promote cooperative design, design reuse, shared design data models, automation in software development, rehostability and portability of TPSs, implementation of lessons learned, and enhance long-term support between vendors, integrators and users. Standards also promote common fabrication processes, signal routing schemes, canned solutions that could reduce TPS engineering integration time and cost.

4.4 Vertical integration test support requirements

Recommendation 4.4: The implementation of the CTI/RFI standard as common *vertical integrated test support* through the product cycle and various maintenance levels assures the greatest benefits of common system implementation and cost savings. Specific benefits include the shared development/manufacturing of ATS and TPS assets, enhanced TPS verification and refinements, and transitional improvements in lessons learned, hands-on training and asset management.

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4.5 CTI configuration/interoperability requirements

Rule 4.5: CTI *pin map requirements,* as defined by *general pin map requirements* in Annex A, and subsequent detailed *CTI pin map input/output (I/O) configuration*, shall be implemented to assure test interface interoperability between agencies and ATS configurations.

Recommendation 4.5: A common CTI pin map configuration has been recommended across government multi-agencies, to stimulate greater use of common assets, which reduces proliferation and support duplication. By satisfying interoperability requirements between government agencies TPS development, deployment and asset duplication can be eliminated and related weapon system support enhanced.

4.6 Maintainability/end-user support requirements

Rule 4.6: The general pin map requirements in Annex A, and subsequent detailed CTI pin map I/O configuration, as part of this IEEE 1505.1 CTI document, shall be maintained/upgraded through IEEE standards revision processes.

Recommendation 4.6: The CTI implementation within industry and the government, utilizing standard product configurations, multi-vendor interchangeable parts, calibration, and maintenance support is recommended.

Observation 4.6: Applying common CTI products to ATS and CTI fixture deployment would dramatically reduce duplicative requirements for unique system development, validation, production, deployment, configuration product management, and long-term support. This approach would further enhance asset availability/uptime mean time between failures (MTBF), calibration/spares consolidation, and mean-time-to-repair (MTTR) results. Users could also benefit from common maintenance practices, tooling, and training costs. CTI implementation would also focus product management/feedback on a smaller number of unique installed systems, their related failures/lessons learned, and iterative improvements, resulting in improved reliability, less obsolescence, and longer life cycles.

4.7 Scaleable architecture requirements

4.7.1 Overview

Rule 4.7.1: CTI shall support modular and scaleable concepts as illustrated in Figure 1. Based upon the IEEE 1505 RFI standard, CTI shall support upward scalable compatibility without modification or added extensions of a low-end (4-slot CTI configuration), and a mid-sized (20-slot CTI configuration), to a high-end (29-slot CTI configuration) test system capability.

Observation 4.7.1: Scalability—"Serves to minimize or eliminate the costs of fixturing by scaling the requirements to minimum framework and related pin map configuration. This minimizes the size, storage requirements, and complexity of fixturing, as well as related receiver and fixture(s) costs, to only what is necessary to interface the unit under test (UUT) to the ATS (e.g., a cable assembly can be plugged into the receiver without a fixture box being applied). This also permits an avionics board manufacturer to develop a compatible TPS for factory test and allow the Government to utilize that same fixture on the high-end depot tester without modifications/adapters. Such capabilities demand that the mechanism support engagement actuators at incremental points to pull smaller fixtures into the receiver."

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4.7.2 General building block architecture

Rule 4.7.2: CTI shall support a scalable building block architecture with common I/O pin map that remains upwardly compatible with matched connector/contact configuration and scalable application levels described in Table 1.[10]

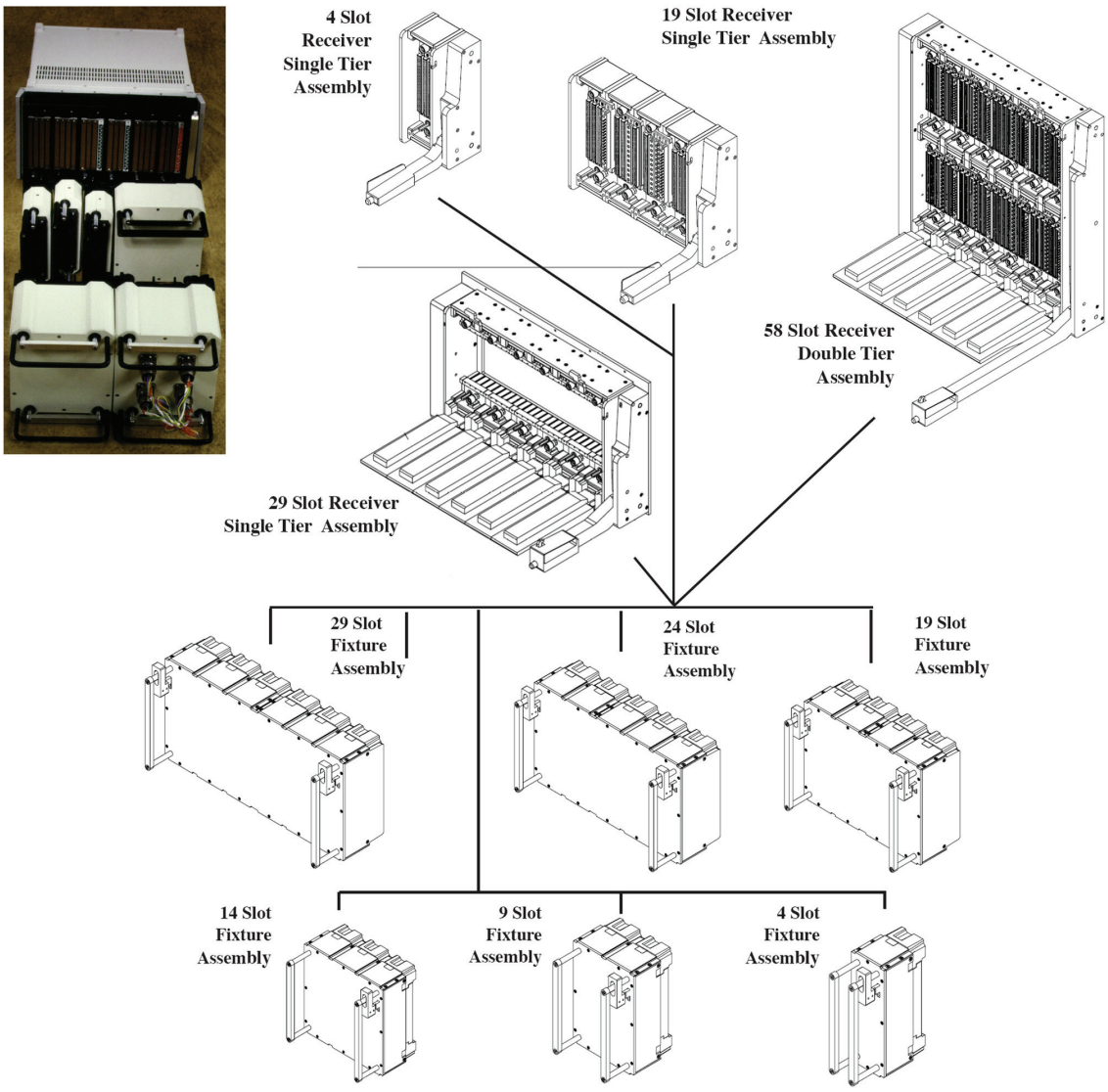

Figure 1—CTI system receiver modular scalable framework architecture

[10] Notes in text, tables, and figures of a standard are given for information only and do not contain requirements needed to implement this standard.

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4.8 Physical framework requirements

4.8.1 IEEE 1505 RFI standard compliance

Rule 4.8.1: The CTI shall be fully compliant with IEEE Std 1505 RFI standard framework specifications, Clause 5, expandable to two tiers, to a maximum of 29 slots per tier (26 slots usable for connector mounting, see Figure 2 and Figure 3).

Table 1—CTI building block suggested configuration

Worse case: High-end test system application—26 connector slots/3 blanks	
Signal contacts:	3200 pos, 0-3A/200 pos module
Lo / hi power contacts:	270 pos 23 A / 152-59 pos
Lo / hi coax contacts:	363 pos 3 GHz / 152-59 pos
Typical: Mid-range test system application—18 connector slots/2 blanks	
Signal contacts:	2800 pos, 0-3 A/200 pos module
Lo / hi power contacts:	211 pos 23 A / 152-59 pos
Lo / hi coax contacts:	59 pos 3 GHz / 152-59 pos
Basic: Low-end test system application—4 connector slots	
Signal contacts:	600 pos, 0-3 A/200 pos module
Lo / hi power contacts:	59 pos 23 A / 152-59 pos
Lo / hi coax contacts:	0 pos 3 GHz / 152-59 pos
NOTE—pos = position (interchangeable with term *contact* in this context)	

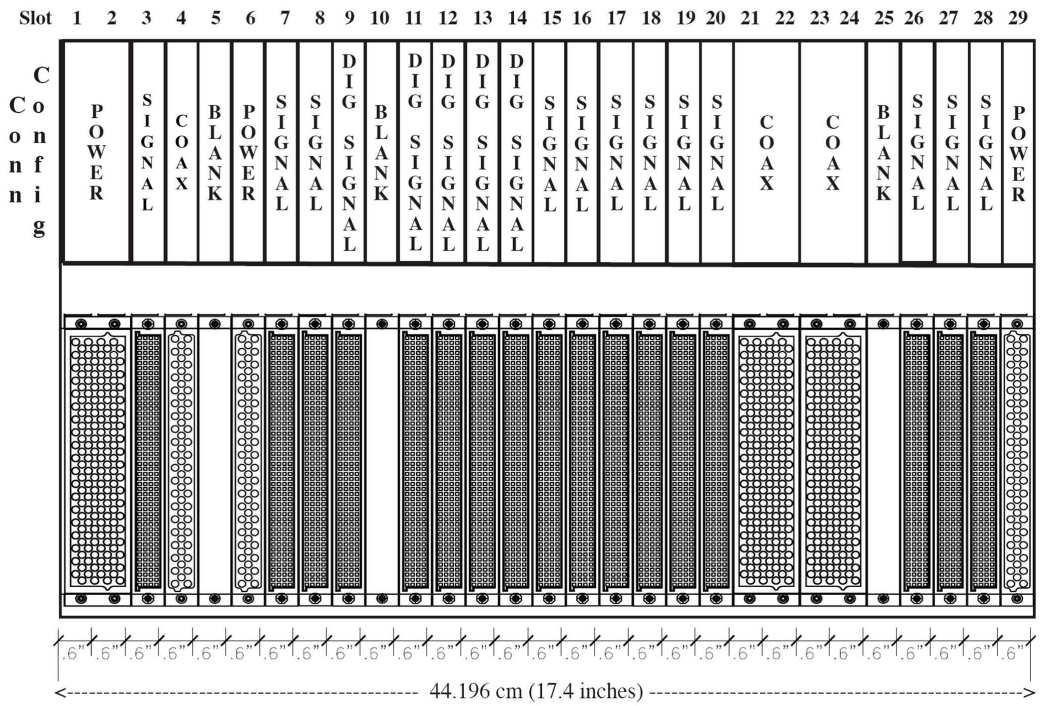

Figure 2—CTI system 29-slot receiver connector configuration

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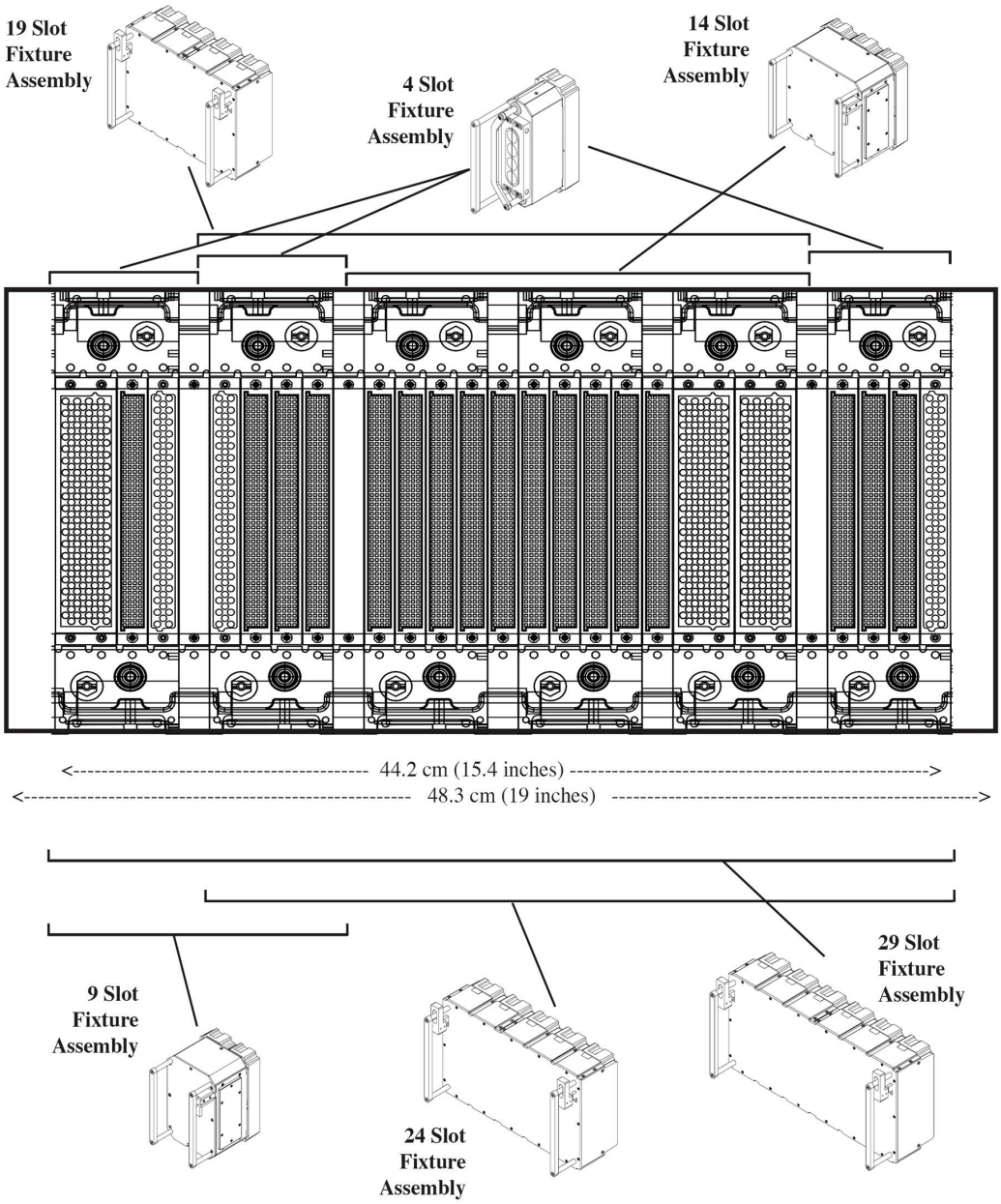

Figure 3—CTI system configuration to fixture options

4.8.2 CTI modular combination framework design

Rule 4.8.2: Under IEEE Std 1505 *combination framework specification* (detailed in the RFI framework specification, Clause 5), the CTI *framework* shall provision three (3) blanks at slot 5, 10, and 25 to provision a 1.524 cm (0.6 in) spacing for the protective shrouds of two adjoining fixtures.

Permission 4.8.2: Combinational framework requirement can be implemented in any of two methods: (a) combining *segmented and continuous framework* (illustrated in Figure 6), to form a 29-slot configuration

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made up of three (3) segmented 5.6 cm (3 in) wide frames, with four (4) connector slots each, and one (1) continuous 22.9 cm (9 in) wide frame, that supports fourteen (14) connector slots that supports frame/blank spacing at slots 5, 10, 25; or (b) modifying a 29-slot continuous framework (illustrated in Figure 5 and Figure 6), to provision three blanks at slots 5, 10, 25.

4.8.3 CTI receiver footprint/scaleable requirements

Rule 4.8.3a: CTI receiver framework footprint shall be a scaleable combinational implementation that can be incremented from the smallest footprint of a segmented framework of four (4) connector slots, and expandable to 29 slots by adding segmented and/or continuous framework intervals, while maintaining downward compatibility with any smaller fixture increments (26 slots for connectors and 3 slots for shroud spacings). Either of the framework implementations can be reduced to any interval segmented at slot 5, 10, and 25 with combinations that can support 4, 8, 14, 18, or 22 slots usable for connector mounting. All connector configurations shall satisfy the IEEE Std 1505 framework/connector specifications, Clause 5 and Clause 6, and CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.8.3b: Physical footprint of the CTI *receiver framework* shall be in accordance with framework specification, Clause 5, that describes receiver framework under IEEE Std 1505 segmented and continuous framework layouts, as the examples in Figure 4 and Figure 6 further illustrate. Although the receiver drive system implementation is supplier dependent, the CTI receiver mechanical drive system shall not extend beyond the dimensional envelope of a standard 48.3 cm (19 in) rack width or height of 35.6 cm (14 in) (including handle height);

Rule 4.8.3c: The CTI specification permits integrators or users to add incremental receiver framework, anytime, to satisfy any mix of fixture requirements, as shown in Figure 1 and Figure 3, that includes multiple tier increments (two tier shown in Figure 1), in accordance with the CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.8.3d: Overall physical size of each CTI *receiver tier,* including drive assemblies, shall not exceed standard 19 in equipment rack width in accordance with EIA/ECA-310-E (2005) [B3], or 35.56 cm (14 in) height, or protrude from the mounting plate more than 8.89 cm (3.5 in).

4.8.4 CTI receiver physical weight requirements

Rule 4.8.4: Physical weight of the CTI receiver framework shall not exceed a maximum of 5.63 kg (8.0 lb) per 7.62 cm (3 in) frame interval and 21.8 kg (48.0 lb) for each CTI 29-slot tier, including fully populated connector modules and the engagement mechanism.

4.8.5 CTI mechanical engagement requirements

Rule 4.8.5: The CTI *receiver mechanical engagement system* shall be in accordance with framework specification, IEEE Std 1505, Clause 5, and provide sufficient mechanical advantage to overcome the physical mating insertion force of a fully-populated interface and the cantilevered fixture weight requirements, and apply sufficient mechanical advantage to assure a 15.9 kg (35 lb) of handle force is not exceeded.

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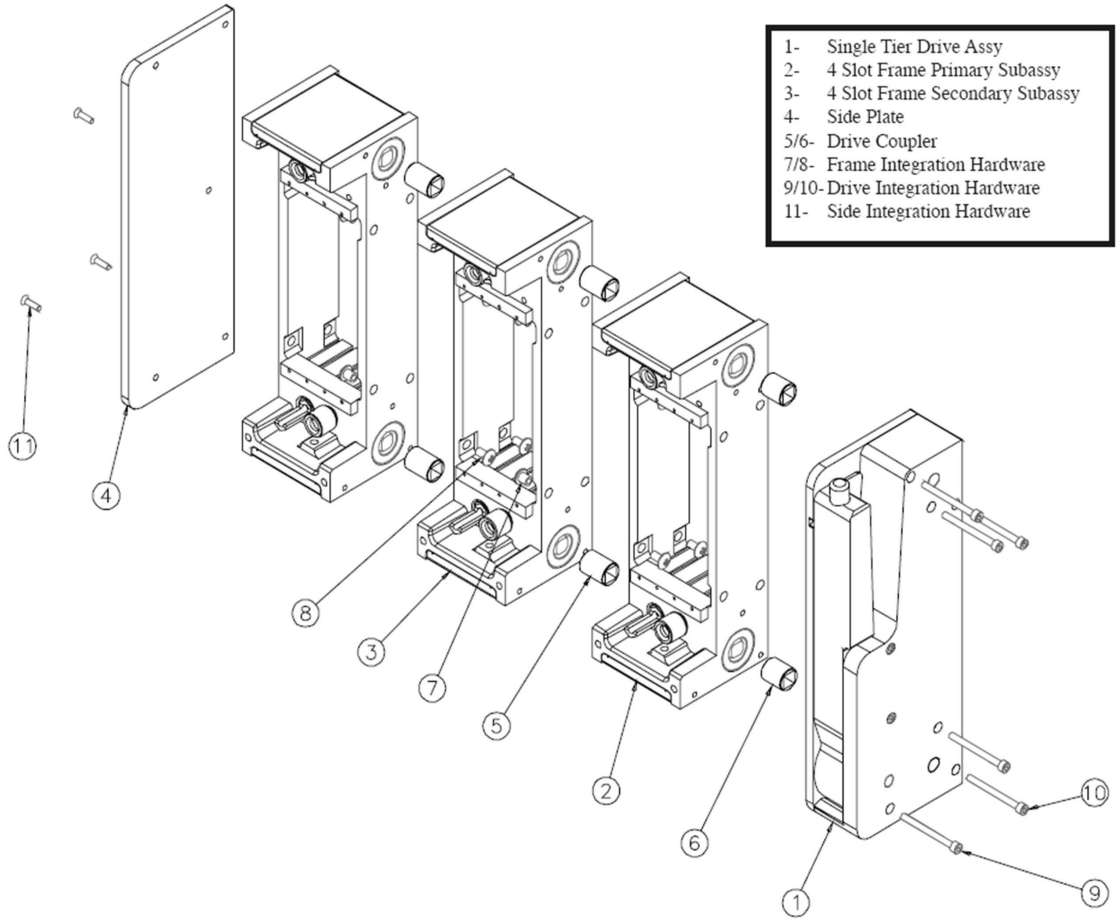

Figure 4—IEEE 1505 receiver segmented framework example

4.8.6 CTI fixture weight requirements

Rule 4.8.6: Each CTI receiver 4-slot *frame increment* shall support a maximum static fixture weight (fixture fully engaged to receiver) of 4.54 kg (10 lb) cantilevered at 38.1 cm (15 in) from receiver mating interface while meeting cycle life, interface insertion force, and electrical parametric requirements. In increments of 4.54 kg (10 lb) per 7.62 cm (3 in) frame interval, a CTI 29-slot receiver with six frame intervals shall support a maximum of 22.68 kg (50 lb) at 38.1 cm (15 in).

NOTE—Implementers/users shall provide additional safety support to assist operators during lift, and prevent injury or damage to equipment, when engaging/disengaging heavy fixture applications.

4.8.7 Oversized fixture keep-out area

Rule 4.8.7: Fixture manufacturers that offer large (oversize) fixture footprints shall not intrude on the dimensional areas annotated in Figure 5.

Observation 4.8.7: The area to the right is reserved for operation of the engaging handle. The area below the fixture is reserved for fixture support facilities.

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CAUTION
Manufacturers should be cognizant of cantilevered weight and other surrounding interference factors that may impact implementation when standard footprints are exceeded.

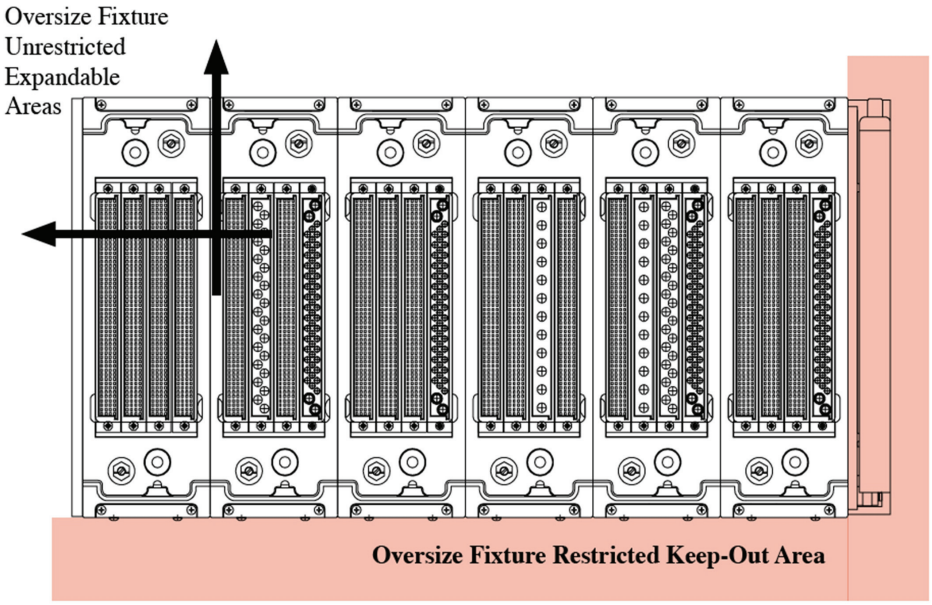

Figure 5—Fixture (ITA) footprint restricted areas

4.8.8 Transportability/mobility requirements

Rule 4.8.8: CTI shall meet transportability/mobility requirements per the IEEE Std 1505 RFI environmental/quality specifications, defined in Clause 4 and Clause 5 of the standard. A fully assembled CTI (framework, connector modules, contacts, and engagement mechanism) shall withstand a 5 ms of 49 m/s for shock drop test.

Observation: 4.8.8: The intent of the drop test is to ensure the assembled interface does not deform or otherwise become unusable if it is "dropped" during assembly or repair. The condition of this test includes the interface as a stand-alone object, impacted on all corners and faces at a 5 ms of 49 m/s for shock drop test force.

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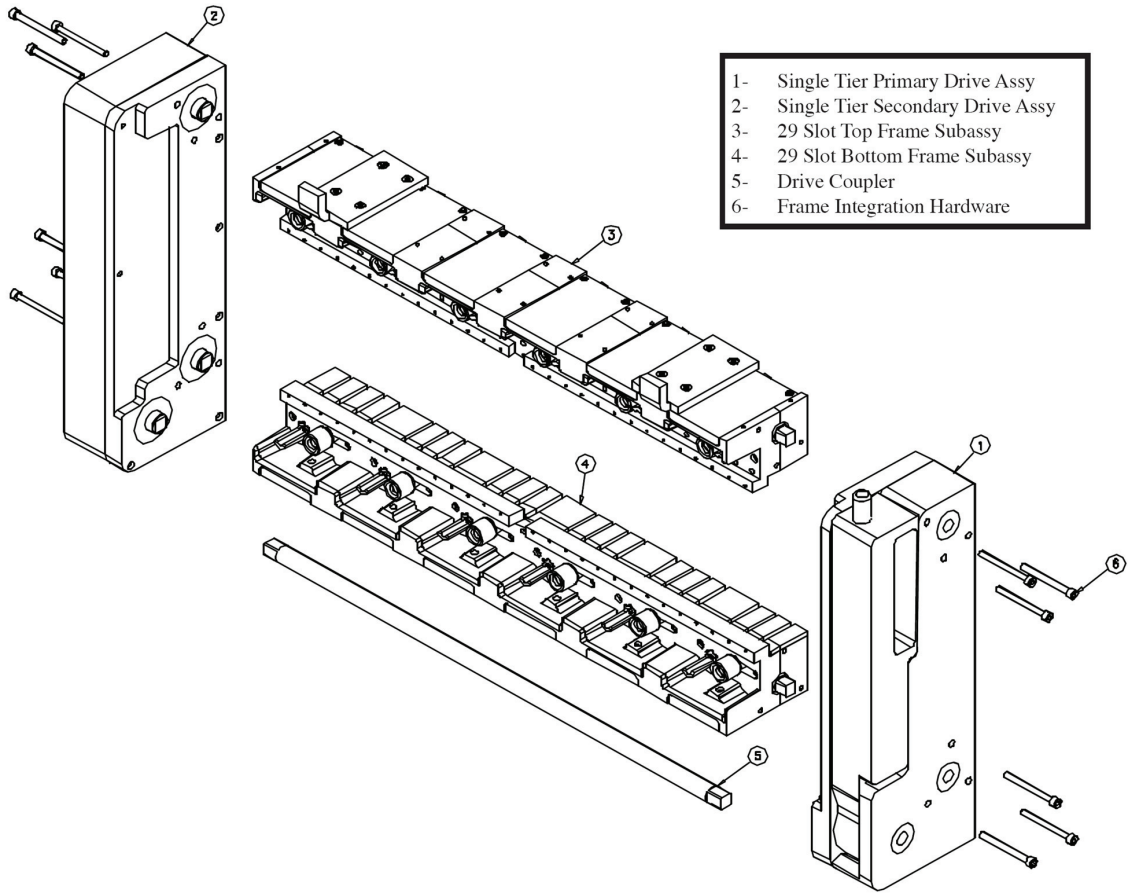

Figure 6—IEEE 1505 receiver continuous framework example

4.9 Reliability requirements

4.9.1 Repeatability/reproducibility/interchangeability

Rule 4.9.1: CTI design shall conform to dimensional and functional requirements defined in IEEE Std 1505 RFI environmental/quality specifications, described in Clause 5 and Clause 6, in order to assure component part interchangeability/intermateability and interoperability between components from multiple vendors. Component parts shall remain "operational" through life of the program. Any part changes that affect form, fit, or function cannot obsolete existing parts.

4.9.2 Mean time between failures requirements

Rule 4.9.2: CTI components shall be designed and produced to perform without failure between established durability/life-cycle requirements. Failures shall be assessed to determine cause and corrective actions. MTBF data for the CTI components shall be calculated in accordance with MIL-HDBK-217 [B21].

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4.9.3 Durability and cycle life

Rule 4.9.3: Durability and cycle life for CTI receiver/fixture mechanism shall have a minimum durability rating of 25 000 cycles. Connector module contacts shall have a minimum durability rating of 10 000 cycles. Cycle limits are considered end of life requiring replacement of wearable items. Manufacturers shall validate conformance to this specification in accordance with the IEEE Std 1505 RFI qualification requirements, Clause 4, cycle testing, and per framework specifications, Clause 5.

4.10 CTI connector footprint/parametric requirements

4.10.1 IEEE 1505 RFI standard compliance

Rule 4.10.1a: CTI shall be compliant with the IEEE Std 1505 RFI standard connector specifications, Clause 6, that establishes the Eurocard DIN standard connector footprint as the basis of CTI architecture.

Observation 4.10.1: Both commercial and ruggedized versions (under MIL-C-55302/179-180 [B20]) were available in a 200-pin, 4-row connector by two of the three primary interface suppliers. Signal module meets the highest levels for open system, low-cost, performance, COTS acceptance, and level of applicability, receiving more than 25% higher grade over any of the other connectors reviewed.

Rule 4.10.1b: CTI shall implement three DIN connector types: (a) signal; (b) power; and (c) RF coax; as defined in IEEE Std 1505 RFI standard connector specifications, Clause 6, and related connector specifications, Clause 7 through Clause 12.

4.10.2 CTI requirements for compliance

Rule 4.10.2: Suppliers of systems shall state their degree of compliance to IEEE Std 1505.1 using the definitions of compliance in 4.10.2.1 and 4.10.2.2.

4.10.2.1 Mechanical compliance

Rule 4.10.2.1: To meet this criteria, a manufacturer shall at the minimum supply an IEEE 1505 RFI compliant interface that conforms to a connector per slot type that matches the configuration shown in Figure 2. That is, the power connector is used in slot ½, the 200-pin signal module in slot 3, etc.

Observation 4.10.2.1: This level of compliance only ensures that physical connector damage will not result from installing a fixture (ITA/ID) from one minimum level compliant system onto a different minimum level compliant system's receiver. It does *not* ensure that the proper signals will be routed.

4.10.2.2 Full compliance

This is the highest degree of compliance and requires full slot-by-slot mechanical and electrical compatibility for the stated compliance categories defined as follows.

Rule 4.10.2.2a: To state full compliance, a manufacturer shall meet all the requirements for the signals for each slot as identified in Annex A, except for the columns labeled "Recommended attributes." Non-populated modules should be blank (e.g., if block is "blank," it can be keyed normally; if block has different pin out, it shall be keyed differently). Both the full compliance and the following category shall be stated.

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The following are the defined categories:

a) Category 1—This is defined as mechanically and electrically compliant with the Annex A slots 6 through 9. This is the basic *stimulus-measurement* section of the pin map.

b) Category 2—This is defined as mechanically and electrically compliant with Annex A slots 1 through 9. This is the basic stimulus-measurement plus power supplies and switching of the pin map.

c) Category 3—This is defined as mechanically and electrically compliant with Annex A slots 6 through 24. This is the basic stimulus-measurement plus digital, switching, and additional analog of the pin map.

d) Category 4—This is full slot compliance (mechanical and electrical) for slots 1 through 24 of the Annex A pin map.

e) Category 5—This is full slot compliance (mechanical and electrical) for all 29 slots of the Annex A pin map.

NOTE—Partially compliant approaches shall rotate keys 180 degrees to insure that physical and/or electrical damage is not incurred.

Observation 4.10.2.2: This level of compliance ensures both mechanical compatibility between systems *and* electrical signal compatibility/interoperability between systems for the slots included in the categories. The categories represent scalable increments based on the segmented architecture and the electrical signals included in the scalable options.

Permission 4.10.2.2a: Pins may also have lesser or higher capability as identified in Annex A tables as long as the pin mapping of Annex A is met and the capability is of the same/similar functionality. For example, an identified dc power supply (DCPS) capability identified in Annex A should be matched with a DCPS, not an ac supply.

Permission 4.10.2.2b: The designer of a compliant system is allowed to implement capability identified in Annex A with non-classical instruments.

4.10.3 Standardized keying

A standardized keying arrangement is required to support the compliant interfaces. Each 4-slot section of the IEEE 1505 RFI interface has a top and bottom key as shown in Figure 7. Each key is set in a hexagonal socket that allows one of six rotational positions. Therefore, with the top and bottom key being independently variable, the keying of one 4-slot segment can have one of 36 different keying arrangements.

Rule 4.10.3a: Systems (receivers and ITAs) that implement a mechanically or fully compliant interface as defined in 4.10.2 and subparagraphs shall implement the keying as shown in Figure 7.

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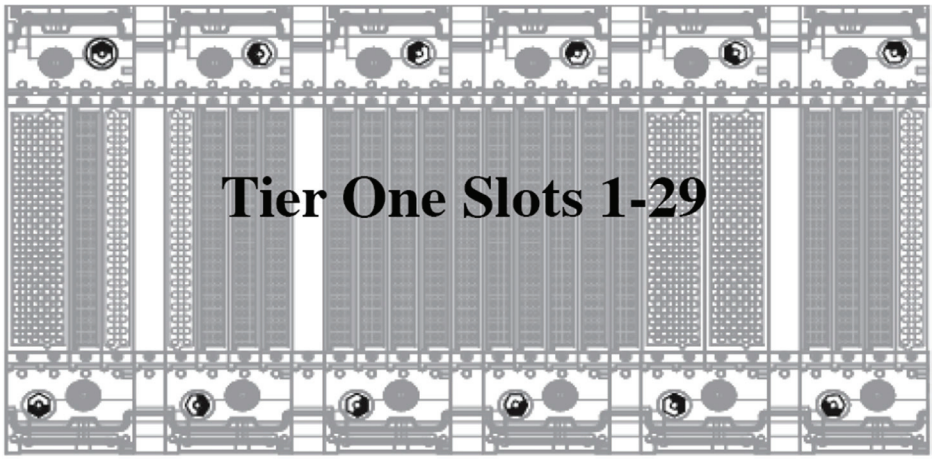

Figure 7—Standardized keying for compliant systems (receiver view)

Rule 4.10.3b: Systems that have segments that are non-compliant per the definition of 4.10.2 shall implement a different keying option. The option used shall *not* duplicate any of the keying options shown for a compliant interface for any section. The goal is to *prevent* any ability to mount a compliant ITA on any non-compliant receiver or a non-compliant ITA on a compliant receiver.

4.10.4 Population policy

Rule 4.10.4a: A test system developer shall follow a set order of precedence in the selection of test assets and the associated pins from the pin map. The following process shall be followed:

a) Identify an unused test asset/instrument that meets the *minimum* test requirements.

b) If the asset/instrument is part of a group of like-capability assets, use the lowest numbered, available (unused) asset for the test.

c) Proceed in like fashion for the entire group of similar assets

d) If the *minimum* required capability assets become completely used (implemented) in the TPS, proceed to utilize the next highly capability asset/instrument.

e) If this asset/instrument is part of a group, follow the same rules in which the lowest numbered is utilized first.

Rule 4.10.4b: A TPS developer shall follow a set order of precedence in the selection of test assets and pins from the pin map. The following process shall be followed:

1) Select an unused test asset/instrument that meets the *minimum* requirements for the test.

2) If the asset/instrument is part of a group of like-capability assets, use the lowest numbered, available (unused) asset for the test.

3) Proceed in like fashion for the entire group of similar assets

4) If the *minimum* required capability assets become completely used (implemented) in the TPS, proceed to utilize the next highly capability asset/instrument. These should also be implemented from lowest numbered asset to higher numbered asset.

5) If this asset/instrument is part of a group, follow the same rules in which the lowest numbered is utilized first.

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Recommendation 4.10.4: Refer to Annex A tables for clarification of asset capabilities and how assets are numbered.

4.10.5 CTI connector parametric requirements

Rule 4.10.5: CTI connector module with contacts shall comply with the definitions contained in IEEE Std 1505 RFI connector specifications, Clause 6, and related connector specifications, Clause 7 through Clause 12, that satisfies the respective parametric requirements defined by Table 2.

Table 2—CTI connector module/contact module performance requirements

Signal contact/module	
Operating voltage:	300 Vdc max
Operating current:	3.0 Adc continuous
Contact resistance:	10 mΩ max
Insulation resistance:	5.0 x 10e9 Ω min
Capacitance:	10 pF max
Reliability:	10 000 engagement cycles
Footprint:	025 in square pins on 0.1 in centers arranged in 4 row x 50 pin multiples
Mating force:	2.0 oz/pin max
Module footprint:	200 positions in 4 columns
Power module/contact	
Operating voltage:	300 Vdc max
Operating current:	23 A dc/ac rms continuous/free stdg/ambient air
Contact resistance:	5 mΩ max
Characteristic imped:	n/a
Insulation resistance:	5.0 x 10e9 Ω min
Capacitance:	10 pF max
Reliability:	10 000 engagement cycles
Contact:	Size 16 DIN requirements
Mating force:	18 oz/pin max
Module footprint:	59 positions in 3 columns, or 152 positions in 8 columns

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Table 2–CTI connector module/contact module performance requirements *(continued)*

Coax module/contact	
Frequency bandwidth:	dc 3 GHz
Operating voltage:	150 V ac, rms
Contact resistance:	10 mΩ max
Voltage standing wave ratio (VSWR):	1:1.22 + 0.52 f (GHz)
RF insertion loss:	.03√f (GHz)
RF leakage:	– 90dB at 2.5 GHz
Contact resistance:	Center contact; straight 6.0 mΩ max
Crosstalk:	Less than or equal to – 90 dB to 2 GHz
Characteristic imped:	50 ± 2 Ω
Insulation resistance :	1000 MΩ min
Capacitance:	15 pF max
Reliability:	10 000 engagement cycles
Contact:	Size 16 DIN requirements
Mating force:	18 oz max
Module footprint:	59 positions in 3 columns or 152 positions in 8 columns

4.11 CTI pin map requirements

4.11.1 CTI scaleable/modular pin map configuration

Rule 4.11.1a: The CTI scaleable pin map configuration shall support scalability (the use of less than a full tier interface as previously discussed in 4.8.3), through the distribution of station resources as defined in CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.11.1b: The CTI configuration shall apply the five (5) connector modules: (a) signal, single slot 200 position; (b) power, single slot 59 position; (c) power, double slot 152 position; (d) RF coax, single slot 59 position; and (e) RF coax, double slot 152 position; in the configuration shown in Figure 2, and in accordance with RFI connector specification, connector specifications, Clause 7 through Clause 12 of IEEE Std 1505.

Rule 4.11.1c: The CTI configuration shall be implemented in intervals conforming to framework segmentation in accordance with RFI framework specification, Clause 5 of IEEE Std 1505, that supports mounting of connector types in intervals of four (4), four (4), fourteen (14), and four (4) slots, or any reduced footprint, as determined by the specific application.

4.11.2 CTI pin map I/O categories

Rule 4.11.2: The CTI connector configuration, as illustrated in Figure 2, shall be implemented in accordance with detailed CTI pin map I/O configuration and general pin map requirements, Annex A. These requirements shall be divided into several I/O parametric categories, described as follows, and distributed in scaleable segments, to assure test signal mapping is a maintained for all CTI applications.

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The following describes the general pin map categories:

a) Digital I/O
b) Analog instrumentation
c) Programmable ac/dc load
d) Programmable ac/dc power supplies
e) Bus I/O
f) Switching implementation

4.11.2.1 Digital I/O

Rule 4.11.2.1a: CTI shall implement a scaleable digital I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.11.2.1b: CTI digital I/O shall be applied utilizing Eurocard DIN/MIL-DTL-55302/180 4-row 200 position connector design specifications in accordance with IEEE Std 1505 RFI standard connector specifications, Clause 7 through Clause 12.

Suggestion 4.11.2.1: Digital I/O signal channel may be implemented with 200 discrete wires, 100 twisted pairs, or two pins per channel of precision point-to-point 50 Ω matched impedance wiring having a bandwidth from dc to 750 MHz to a maximum of 100 channels increments (200 pins), as necessary to meet selected ATE digital requirements.

4.11.2.2 Analog instrumentation

Rule 4.11.2.2a: CTI shall implement a scaleable AI (AI) I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A, and subsequent requirements. CTI AI I/O shall be implemented utilizing either the CTI signal or coax connectors as subsequently described.

Rule 4.11.2.2b: If implemented, the CTI AI I/O shall apply Eurocard DIN/MIL-DTL-55302/180 4-row 200 position connector design specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12.

Suggestion 4.11.2.2: AI I/O signal channel may be implemented with 200 discrete wires, 100 twisted pairs, or two pins per channel of precision point-to-point 50 Ω matched impedance wiring having a bandwidth from dc to 750 MHz to a maximum of 100 channels increments (200 pins), or as necessary to meet selected ATE digital requirements.

Rule 4.11.2.2c: If implemented, the CTI AI I/O shall apply RF coaxial size 16 contact with RF coax size 16 connector module design and wiring specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12.

4.11.2.3 Programmable ac/dc load

Rule 4.11.2.3a: CTI shall implement a scaleable programmable dc load I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A.

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Rule 4.11.2.3b: CTI programmable dc load I/O shall be applied utilizing the CTI power connector using 23 amp contact in a 59 or 152 positions power module connector design in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12. These contacts shall be derated to 18 A, when six or more are clustered adjacent to each other and operating simultaneously and continuously at that current level.

Suggestion 4.11.2.3: Discrete 23 amp pins should be implemented with 14 AWG MIL-spec (high temperature and flammable resistant) discrete or twisted pair wiring.

Permission 4.11.2.3: CTI programmable dc load I/O where applicable may utilize low level (current <3 A) discrete I/O signal pins using Eurocard DIN 41612 and MIL-C-179/180 5 row 200 position connector design specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12, and the CTI pin map I/O configuration and general pin map requirements, Annex A. Discrete pins may be implemented with 24 AWG discrete or twisted pair wiring.

4.11.2.4 Programmable ac/dc power supply

Rule 4.11.2.4a: CTI shall implement a scaleable programmable dc/ac power supply I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.11.2.4b: CTI programmable dc/ac power supply I/O shall be normally applied utilizing the CTI power connector using 23 amp contact in a 59 or 152 positions power module connector design specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 6 and Clause 8. These contacts shall be derated to 18 A, when six or more are clustered adjacent to each other, and operating simultaneously and continuously at that current level.

Suggestion 4.11.2.4: Discrete 23 amp pins should be implemented with 14 AWG MIL-spec (high temperature and flammable resistant) discrete or twisted pair wiring.

Permission 4.11.2.4: CTI programmable dc/ac power supply I/O where applicable may utilize low-level (current <3 A) discrete I/O signal pins using Eurocard DIN/MIL-DTL-55302/179/180 4-row 200 position connector design specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12. Discrete pins shall be implemented with 24 AWG discrete or twisted pair wiring.

4.11.2.5 Bus I/O

Rule 4.11.2.5a: CTI shall implement a scaleable bus I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.11.2.5b: CTI bus capability shall be applied utilizing Eurocard DIN/MIL-DTL-55302/180 4-row 200 position connector design specifications in accordance with IEEE Std 1505 RFI standard connector specifications, Clause 7 through Clause 12.

Suggestion 4.11.2.5: Bus I/O signal channels may be implemented with 200 discrete wires, 100 twisted pairs, or two pins per channel of precision point-to-point 50 Ω matched impedance wiring having a bandwidth from dc to 500 MHz to a maximum of 100 channels increments (200 pins), as necessary to meet selected ATE bus requirements.

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4.11.2.6 Switching implementation

4.11.2.6.1 General requirements

These interfaces describe the hardware requirements necessary to switch stimulus, response, and power signals between the UUT and the test instrumentation. The switching may be implemented in various ways.

Observation 4.11.2.6.1: The combination of the switch and CTI I/O provides the ATS developer the ability to select various signal paths between the instrument and UUT. Examples of switch implementations are shown in Figure 8 as: (a) benchtop units; (b) integrated switch cards; (c) rack-mounted units; and (d) switch modules meeting published industry standards such as (but not limited to) LXI, USB, VME, VXI, and PXI.

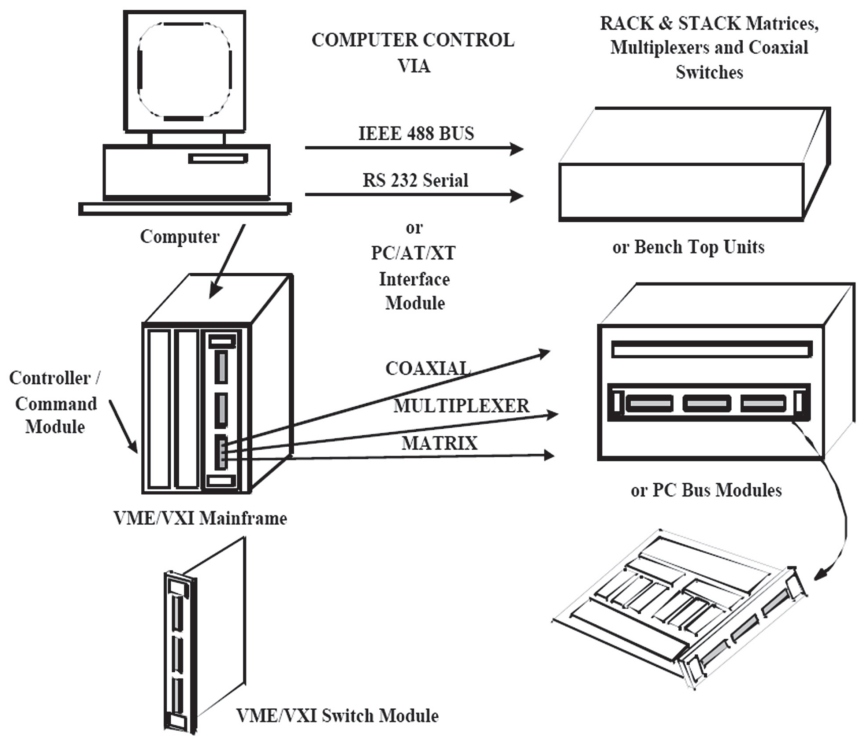

Figure 8—Switching product designs

4.11.2.6.2 Switch concerns

Observation 4.11.2.6.2: General requirements for the switch interface, described in Table 3 and Table 4, were derived from many sources representing general industry needs, Government and commercial interests, Government open-system directives, industry technology trends, Government/aerospace test requirements previously described (functional test requirements), and test industry switch defacto standards. The CIWG and CTI Switching Task Group reviewed the widest spectrum of requirements, legacy support requirements, and other interests to assure switch elements were addressed. These requirements were extracted from the envelope of the cases reviewed. This is expected to provide capability for almost every requirement the solution will encounter. During the review process standards or products that could meet these requirements were sought. The switching philosophies considered in the analysis are the following:

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a) Switching outside ATE—This approach incorporates switching into the test fixture based on the UUT requirements. This places financial burden on the end user since switching needs to be incorporated in many test fixtures. This is a significant recurring cost.

b) Switching in the ATE—This approach integrates the switching capability into the ATE and treats it as additional instrumentation. This simplifies test fixture design, reduces TPS cost, and places the switching under control of the ATE system software. This can be accomplished in one of two ways:

1) *Internal hardwiring* of instrumentation to ATE switching. The internal approach simplifies test fixture design and implementation; however, a performance trade-off discussion resulted in providing instrument parts directly at the CTI. Costs associated with connecting the instruments to the switch are relegated to the electrical connectivity within the ATS-to-UUT interface adapter.

2) *External hardwiring* of instrumentation to ATE switching in the test fixture. The external approach will greatly increase test fixture complexity, however; the TPS developer has greater flexibility should higher performance instrumentation require uncompromising access at the tester interface.

4.11.2.6.3 CIWG recommended switch requirements

Suggestion 4.11.2.6.3: The Critical Interface Working Group (CIWG) Report suggested certain switch requirements that could implement COTS solutions and preserve the needs of the Government legacy programs. The following goals were utilized in assessing switching candidates:

a) Is widely accepted by industry with multi-vendor sources.

b) Has established design definitions.

c) Offers a full range of options to meet signal, power, and coax requirements.

d) Supports high life-cycle performance and maintainability.

e) Is available today in volume production and is in its early product life-cycle phase.

f) Provides a scaleable switch with a modular framework design that permits ATS integrators to incrementally augment their systems through add-on/duplicative features. This will enable them to meet worst case requirements while maintaining downward compatibility with any smaller I/O increment.

g) Establishes a common switch specification that offers multi-vendor sources, is flexible enough to support a wide variety of signal performance/switch configurations (1x2, 1x4, 1x8), and can evolve with new test needs.

h) Minimizes pin out configuration to effect greater transportability and reconfigurability is not impaired.

i) Reduces the proliferation of switch designs.

j) Defines a minimum set of performance requirements that will meet the Government I/O basic switch needs. Common I/O basic switch envelope that supports legacy 1x2, 1x4, 1x8 wrap-around signal cascade TPS requirements.

Recommendation 4.11.2.6.3: The integrator determines switch requirements based on the number of instruments and the flexibility with which they must be applied. Switch designs require a compromise between direct wire performance and switch flexibility. The CIWG concluded that switching in the ATS with internal hard wiring should be required to achieve greater cost-effectiveness and minimize fixture complexity.

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4.11.2.6.4 CTI switch requirements

Rule 4.11.2.6.4: The CTI shall employ a scaleable switch that applies high performance analog switch cards for any general purpose high-end ATE system. All switch functional requirements shall be implemented directly through the CTI to support legacy switch requirements, in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A. The detailed descriptions of Table 3, Table 4, Table 5, and Table 6, as well as Figure 9, provide additional switch definition/requirements to be implemented under the CTI Specification.

Table 3—Signal switch performance requirements

Switch type	Characteristic	Requirement
Signal 1x2, 2A	Time, switch	<3ms
	Crosstalk	<–60 dB (adj channels)
	Current	2.0 A
	Isolation	>=100 MΩ
	Isolation	>45 dB @ 10 MHz
	Isolation	<1E9 Ω @ dc
	Power, switched	30 Wdc, 62.5 VA ac
	Resistance to ground	>100 MΩ
	Resistance, path	<0.2 Ω
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	300 Vdc/300 Vac
Signal 1x2, 4A	Time, switch	<3 ms
	Crosstalk	<–60 dB (adj channels)
	Current, switched	4 A ac/dc
	Isolation	>=100 MΩ
	Isolation	>45 dB @ 10 MHz
	Isolation	<1E9 Ω @ dc
	Power, switched	90 Wdc, 1000 VA ac
	Resistance to ground	>100 MΩ
	Resistance, path	< 0.2 Ω
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	300 Vdc/300 Vac

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Table 3–Signal switch performance requirements *(continued)*

Switch type	Characteristic	Requirement
Signal 1x4	Time, switch	<3 ms
	Crosstalk	<–60 dB (adj channels)
	Current, switched	2A
	Isolation	>=100 MΩ
	Isolation	>45 dB @ 10 MHz
	Power, switched	30 Wdc, 62.5 VA ac
	Resistance, path	< 0.3 Ω
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	300 Vdc/300 Vac
Signal 1x8	Bandwidth (–3dB)	<100 MHz
	Time, switch	<3 ms
	Current, switched	2 A
	Isolation	<–45dB @ 10MHz
	Resistance, path	<1E9 MΩ
	Voltage, switched	300 Vdc/300 Vac
Signal 8x24	Bandwidth (–3dB)	20 MHz
	Time, switch	<3 ms
	Capacitance, CH to CH	<0.36 µF
	Crosstalk	<–60 dB @ 1 MHz
	Current, steady state	2.0 A
	Current, switched	2 A ac/dc
	Impedance, shunt cap	<0.5 µF
	Impedance	50 Ω
	Isolation	<–50 dB @ 10 MHz >=100 MΩ
	Resistance to ground	>100 MΩ
	Resistance, path	< 1.0 Ω
	Voltage, switched	300 Vdc/300 Vac
	Voltage, unswitched	350 Vac/dc

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Table 4—Power switch performance requirements

Switch type	Characteristic	Requirement
Power 1x1, 10 A	Time, switch	<20 ms
	Current, steady state	10.0 A
	Current, switched	10 A ac/dc
	Isolation	>45 dB @ 5 kHz <1E9 Ω @ dc
	Power load rating	300 Wdc, 2000 VA/CH
	Resistance to ground	>100 MΩ
	Resistance, path	< 0.1 Ω
	Voltage, switched	220 V ac/dc
Power 1x2, 10 A	Time, switch	<20 ms
	Current, switched	10 A ac/dc
	Isolation	>45 dB @ 5 kHz <1E9 Ω @ dc
	Noise floor	<=–100 dBm @ quiescent
	Power, switched	300 Wdc, 2000 VA/CH
	Resistance to ground	>100 MΩ
	Resistance, path	< 0.1 Ω
	Voltage, switched	220 Vac/dc
Power 1x2, 10 A, low-R	Time, switch	<20 ms
	Current, contact rating	9 A
	Isolation	>=10 000 MΩ
	Power, switched	300 Wdc, 2000 VA/CH
	Resistance to ground	>100 MΩ
	Resistance, path	< 40 mΩ @ 9 A, < 500 mΩ @ 1 mAdc
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	250 Vac/125 Vdc
Power 1x2, 20 A	Time, switch	<20 ms
	Current, switched	20 A
	Power, switched	4800 Vac/560 Wdc
	Resistance to ground	>100 MΩ
	Resistance, path	0.05 Ω to 0.1 Ω
	Voltage, switched	240 Vac/220 Vdc

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Table 4—Power switch performance requirements *(continued)*

Switch type	Characteristic	Requirement
Power 1x2, 20 A, low-R	Time, switch	<20 ms
	Current, contact Rating	18.75 A
	Current, switched	20 A
	Isolation	>=10 000 MΩ
	Power, switched	4800 Vac/560 Wdc
	Resistance, path	<20 mΩ @ 18.75 A, <250 mΩ @ 1 mAdc
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	240 Vac/220 Vdc
Power 1x4, 20 A,	Time, switch	<20 ms
	Current, switched	20 A
	Power, switched	560 Wdc/4800 Vac
	Resistance to ground	>100 MΩ
	Resistance, path	< 0.1 Ω
	Voltage, switched	240 Vac/220 Vdc
Power 1x4, 20 A, low-R	Time, switch	<20ms
	Current, contact rating	18.75 A
	Current, switched	20 A
	Isolation	>=10 000 MΩ
	Power, switched	4800 Vac/560 Wdc
	Resistance to ground	>100 MΩ
	Resistance, path	<20 mΩ @ 18.75 A, <250 mΩ @ 1 mAdc
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	240 Vac/220 Vdc
Power DPDT, 20A, low-R	Time, switch	<20 ms
	Current, contact Rating	18.75 A
	Current, switched	20 A
	Isolation	>=10 000 MΩ
	Power, switched	4800 Vac/560 Wdc
	Resistance to ground	>100 MΩ
	Resistance, path	<20 mΩ @ 18.75 A, <250 mΩ @ 1 mAdc
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	240 Vac/220 Vdc

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Table 5—Coax switch performance requirements

Switch type	Characteristic	Requirement
Coax 1x2	Frequency range	DC to 1.3 GHz
	Bandwidth loss	<0.2 dB @ 100 MHz <0.5 dB @ 500 MHz <2.0 dB @ 1 GHz
	Time, switch	<=15 msec
	Crosstalk	<–65 dB @ 100Mz <–60 dB @ 500Mz <–55 dB @ 1 GHz
	Isolation, input to output	<–70 dB @ 100 MHz; <–65 dB @ 500 MHz <–55 dB @ 1 GHz
	VSWR	<1.2:1 @ 100 MHz <1.5:1 @ 1 GHz
	Characteristic impedance	50 Ω
	Current, switched	0.5 A
	Power, max	+33 dBm (2 W into 50 Ω)
	Power, switched	10 Wdc
	Power, unswitched	10 Wdc
	Resistance, dc path	<1 Ω
Coax 1x4	Frequency Range	DC to 1.3 GHz
	Bandwidth Loss	<0.2 dB @ 100 MHz <0.5 dB @ 500 MHz <2.0 dB @ 1 GHz
	Time, switch	<=15 msec
	Crosstalk	<–65 dB @ 100 MHz <–60 dB @ 500 MHz <–55 dB @ 1 GHz
	Isolation, Input to Output	<–70 dB @ 100 MHz <–65 dB @ 500 MHz <–55 dB @ 1 GHz
	VSWR	<1.2:1 @ 100 MHz <1.5:1 @ 1 GHz
	Characteristic impedance	50 Ω
	Capacitance	<0.25 µF
	Current, switched	1.0 A @ 28 Vdc
	Current, Steady State	2 A
	Power, max	+33 dBm (2 W into 50 Ω)
	Power, switched	10 Wdc
	Power, unswitched	10 Wdc
	Resistance, dc path	<1 Ω
	Resistance, to ground	>100 MΩ

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Table 6—CTI switch configuration requirements

Switch nomenclature	Quantity	Power	Signal	Coax
Signal 1x2, 2 A	50		150	
Signal 1x2, 4 A	50		150	
Signal 1x4	16		80	
Signal 8x24	6		312	
Signal 8x8	16		288	
Power 1x1, 10 A	12	24		
Power 1x2, 10 A	12	36		
Power 1x2, 10 A low-R	12	36		
Power 1x2, 20 A	3	9		
Power 1x2, 20 A low-R	1	3		
Power DPDT, 20 A low-R	2	12		
Power 1x4, 20 A	1	5		
Power switch 1x4, 20A low-R	5	25		
Coax 1x2	9			27
Coax 1x4	48			240
Totals	**243**	**150**	**980**	**267**

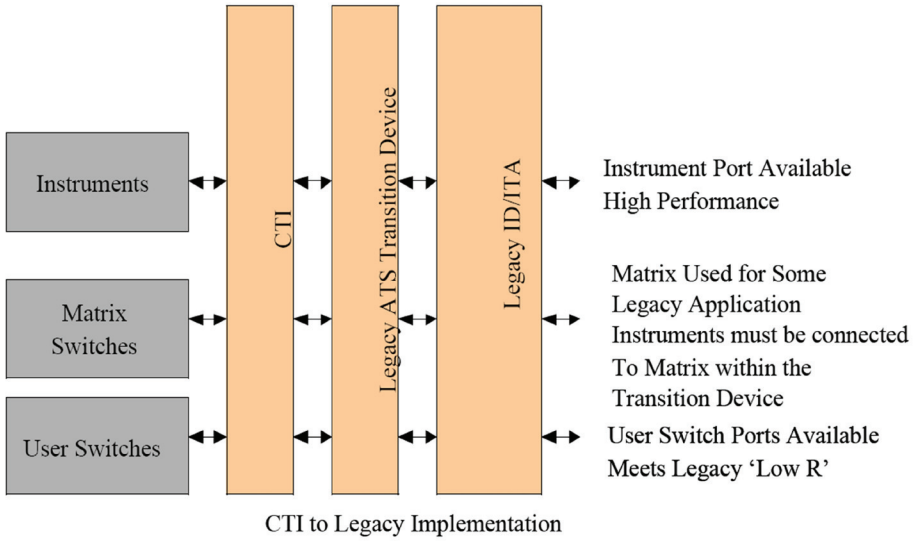

Figure 9—CTI switch architecture

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4.12 CTI pin map input/output configuration

Rule 4.12: The CTI connector configuration and related CTI pin map I/O configuration and general pin map requirements, as defined in Annex A, shall be implemented in accordance with interconnect specifications detailed therein. These requirements within Annex A shall be divided into several I/O parametric categories/signal definitions, related legacy pin map I/O, and distributed in functional scaleable segments, to assure test signal mapping is maintained for all CTI applications. Pin map I/O descriptions for respective legacy systems shall be provided within Annex A to support legacy TPS and transition device requirements.

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Annex A

(normative)

Common test interface signal definitions for pin map

A.1 Analog instruments (AI)

A.1.1 Analog-to-digital converter (ADC) analog-in (Table A.1)

Sixteen channels plus a trigger channel are mapped to 34 pins to support a 2-wire interface for each, i.e., Ch+, Ch–. Six shield pins are provided.

A.1.2 AI multi-parallel (Table A.2, Table A.3, and Table A.4)

Ninety-six channels are mapped to 192 pins to support a 2-wire interface for each. Thirty-two channels are mapped in the core. Each of the channels is capable of stimulus or measurement. As stimulus channels (function generator), capabilities include dc, sine, triangle, pulse, and arbitrary waveform generation. As measurement channels, capabilities include timer/counter, digitizer, digital multi-meter (DMM) and limit detect.

A.1.3 AWG (Table A.5)

The composite *arbitrary waveform generator* is comprised of 4 AWGs providing a total of 6 output channels: 1A, 1B, 2A, 2B, 3A, and 4A. Each of the 4 AWGs provide for external inputs. AWGs 1 and 2 allow for mark, trigger, and sync. AWG 3 allows for trigger and sync. AWG 4 allows trigger. These 15 interfaces are mapped to 30 pins to support a 2-wire interface for each. Two additional interfaces to the AWGs (DiffGate and DataGate) are mapped to 4 pins to support a 2-wire interface. These main functions are mapped to a total of 34 pins.

A.1.3.1 AWG emitter-coupled logic (ECL) outputs

Twenty-four differential, digital data bits provided by AWGs 1 and 2 (12 each) are mapped to 48 pins to support a 2-wire interface for each data bit. An AWG GND pin is mapped for each of these ports. These output ports are mapped to a total of 50 pins.

A.1.3.2 AWG-5

A fifth AWG adds the following 6 ports to the interface: Out, Out/7, Marker, ref, Start/Arm, StopTrigFsk. These ports are mapped to 6 coax contacts.

A.1.3.3 AWG function generator

The function generator has the following I/O: Out, Sync, Trig, Clock, and PM. These channels are mapped to 5 coax contacts.

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A.1.4 AWG520 (Table A.6)

This unique capability AWG has 2 channels, 4 markers, 10 digital, an input trigger, 4 event triggers, clock-in, clock-out, and noise-gen. These 26 interfaces are mapped to 52 pins to support a 2-wire interface for each.

A.1.5 Digital-to-analog converter (DAC) analog-out (Table A.7)

A.1.5.1 DAC 1

DAC 1 has 16 channels, a trigger, and 8 keys. The first 12 channels provide for remote sense as these have 100 mA drive capability. The channels, trigger, and sense lines are collocated and are mapped as 2-wire interfaces to 58 pins. The keys are collocated and mapped as 2-wire interfaces to 16 pins. Two shield pins are provided.

A.1.5.2 DAC 2

DAC 2 has 16 channels and a trigger. The channels and trigger are collocated and are mapped as 2-wire interfaces to 34 pins. Six shield pins are provided.

A.1.6 Digitizer (Table A.8)

Four digitizer channels are mapped. Three supporting interfaces are mapped: dc Cal, ExtTrig, and Trig out. These 7 interfaces are mapped to 14 pins to support a 2-wire interface for each.

A.1.7 DMM (Table A.9)

The DMM has the customary Hi, Lo, Sense+, Sense–, and trigger paths. Two additional paths are mapped: Probe and DMM Done. These 7 interfaces are mapped to 14 pins to support a 2-wire interface for each. A Guard pin and Current pin round out the total to 16 pins.

A.1.8 Frequency time interval counter and RF counter (Table A.10)

The frequency time interval counter (FTIC) has 2 channels plus a single trigger/gate channel. These 3 interfaces are mapped to 6 pins to support a 2-wire interface for each. The RF counter has 2 interfaces: inhibit and threshold.

A.1.9 Low-frequency calibrator (Table A.11)

The low-frequency calibrator is mapped to 4 pins: Hi, Lo, Sense+, and Sense–. A guard pin and shield pin are mapped for a total of 6 pins.

A.1.10 Open-collector driver (Table A.12)

Ninety-six channels of open-collector drivers (OCDs) are mapped to 192 pins to support the 2-wire interface approach. Twelve I/O-control and 12 clock channels are mapped to 24 pins for a single wire

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implementation. Two additional pins are mapped anticipating the need for returns for the I/O-control and clock channels, bringing the total for the OCD to 218 pins.

A.1.11 Pulse generator 1 (Table A.13)

Pulse generator 1 has 2 channels plus an external trigger-in and a trigger-out. These 4 interfaces are mapped to 8 pins to support a 2-wire interface for each.

A.1.12 Pulse generator 2 (Table A.14)

Pulse generator 2 has 2 channels plus an external trigger-in and a trigger-out. These 4 interfaces are mapped to 8 pins to support a 2-wire interface for each.

A.1.13 Resistive load (Table A.15)

The resistive load is mapped to 2 pins.

A.1.14 Scope (Table A.16)

Four oscilloscope channels plus an aux-out channel are mapped to 5 coax contacts.

A.1.15 Syncro-resolver (Table A.17)

Sixty-five pins are mapped for the syncro-resolver.

A.1.16 Video (Table A.18)

Two-hundred pins are mapped for video.

A.2 Bus

A.2.1 Programmable bus (Table A.19)

Sixty-four programmable bus channels are mapped to 128 pins. The programmable channels support standard serial and parallel bus formats. Four additional pins are provided as GND pins to support 1553 GND pin requirements.

A.2.2 IEEE 1149.1™ boundary scan (Table A.20)

Twenty-one pins are mapped for IEEE Std 1149.1-2001 [B13].

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A.3 Digital

A.3.1 Channels (Table A.21)

Four hundred forty-eight channels are mapped to 896 pins to support a 2-wire interface for each, and 3 Kelvin grounds are mapped to 6 pins.

A.3.2 Clocks (Table A.22)

Six control clocks, one reference, 4 sync, one Kelvin ground, 4 clocks, and 6 miscellaneous signals are mapped to 22 coax pins.

A.3.3 External control (Table A.23)

Fifty-four channels are mapped to 108 pins to allow external control of the digital channels.

A.4 Instrument control

A.4.1 Spectrum analyzer (Table A.24)

Four channels, trigger, detected video, RF measure in, and 321.4 MHz IF are mapped to 4 coax contacts.

A.4.2 Modulation source (Table A.25)

Thirteen modulation sources are mapped to 13 coax contacts. RF Source 1 has 4 channels: pulse amplitude modulation (PAM) trigger, amplitude modulation (AM), frequency modulation (FM), and an External Trigger IN. RF Source 2 also has RF AM, RF FM, RF PM, and an External Trigger IN. RF Source 3 has 4 channels: AM, FM, PAM, and an External Trigger IN. There is also a microwave transition analyzer (MTA) External Trigger IN, which rounds the total to 13.

A.4.3 Power meter (Table A.26)

There are 4 power meter control interfaces. Three interfaces are mapped as: Ext Trig in, Video1, and Video2. These 3 interfaces are mapped to 3 coax contacts. The fourth interface, power meter recorder, is mapped to a coax contact.

A.5 Power loads

A.5.1 Hi current ac/dc load (Table A.27)

Two high current power loads are mapped to 8 power pins to support the high current path. Each of the high current loads has 2 Load (+) pins and 2 Load (–) pins.

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A.5.2 AC/DC load (Table A.28)

Six power loads are mapped to 12 power pins. Each of the current loads has a Load (+) pin and Load (–) pin.

A.5.3 Load modulation (Table A.29)

A load modulation channel is mapped to 2 pins as Load Mod (+) and Load Mod (–). Load modulation allows a signal to vary the load about a programmed nominal value. (This applies to active loads only.)

A.6 Power supplies

A.6.1 DC

A.6.1.1 High current DCPS (Table A.30)

Ten high current DCPS are mapped to 40 power pins to support the current path. Each of the high current supplies has 2 DCPS (+) pins and 2 DCPS (–) pins.

A.6.1.2 DCPS (Table A.31)

Twelve DCPS are mapped to 24 power pins. Each of the supplies has a DCPS (+) pin and a DCPS (–) pin.

A.6.2 AC

A.6.2.1 AC power supply (ACPS) three phase (Table A.32)

A three-phase source is mapped to 10 power pins. Phases A, B, and C, plus neutral and ground are mapped to 2 pins each to support the high current paths.

A.6.2.2 ACPS programmable (Table A.33)

Four programmable ac sources are mapped to 10 power pins. Each source has a complementary return. Two pins are mapped as ground. Four auxiliary power sources are mapped to 8 signal pins. Each source has a complementary return.

A.7 Sense and control, DCPS, and loads

A.7.1 DCPS sense (Table A.34)

Forty-four pins are mapped as sense lines for the 11 DCPS. Sense lines are paired as DCPS Sense (+) and DCPS Sense (–).

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A.7.2 ACPS sense (Table A.35)

Eight pins are mapped as sense lines for the 4 programmable ac sources.

A.7.3 Load sense (Table A.36)

Two pins are mapped as sense lines for one of the high power loads: High Power Load Sense (+) and High Power Load Sense (–). Two additional pins are mapped as *chassis* ground.

A.7.4 28V Control (Table A.37)

Two pins are mapped as control lines. Control 28 (+) and Control 28 (–) are inputs to the system to command a DCPS to the turn on.

A.8 Switch

Three types of switches are mapped: coax, power, and signal.

NOTE—The selection of the matrix switches was mapped to meet legacy requirements. A system integrator can choose to populate a system with, for example, 2x8 switches that meet the recommend attributes vice 1x4 switches, wire them to the CTI and still be compliant, as long as the superset contains the required subset.

A.8.1 Coax switch (CSW)

Two types of CSWs are mapped: 1x4 and 1x2.

A.8.1.1 1x8

1x8 CSWs can be created from 1x4 and 1x2 by appropriate wiring in an ITA/ID or transition adapter.

A.8.1.2 1x4 (Table A.38)

Forty-eight 1x4 CSWs are mapped to 240 coax contacts.

A.8.1.3 1x2 (Table A.39)

Nine 1x2 CSWs are mapped to 27 coax contacts.

A.8.2 Power switch

Four types of power switches are mapped: 1x4, 1x2, DPDT, and 1x1.

A.8.2.1 1x4 (Table A.40)

Six 1x4 switches are mapped to 30 power pins. These are 20 A relays, however the CTI interface has a thermal restriction of 18 A in a cluster of 6 adjacent pins. Five of the six are low-R.

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