

PUBLICLY AVAILABLE SPECIFICATION

PRE-STANDARD



**Printed boards –
Part 14: Device embedded substrate – Terminology / reliability / design guide**

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**Printed boards –
Part 14: Device embedded substrate – Terminology / reliability / design guide**

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The text of this PAS is based on the following document:

This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document

Draft PAS	Report on voting
91/893/PAS	91/910/RVD

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PRINTED BOARDS – Part 14: Device embedded substrate – Terminology / reliability / design guide

1 Scope

This PAS is applicable to device embedded substrates fabricated by embedding discrete active and passive electronic devices into an inner layer of a substrate with electric connections by vias, conductor plating, conductive paste, and printing. The device embedded substrate may be used as a substrate to mount SMDs to form electronic circuits, as conductor and insulator layers may be formed after embedding electronic devices.

The purpose of this PAS is to obtain common understanding in design, fabrication and use of device embedded substrates in the industry.

This PAS describes the substrate embedding devices including but not limited to module, integrated passive device (IPD), microelectrochemical systems (MEMS), discrete component formed in the fabrication process of the electronic wiring board, and sheet form component. Figure 1 shows examples of device embedding in the fabrication process of the device embedded substrate. Active and passive devices are connected to each other by interlayer vias and/or conductor patterns. Insulating layers are formed using insulating materials with vias for the connection of inside conductor patterns to the conductor patterns formed on the surface(s) of the substrate. Figure 2 shows the substrate with connections using pads, and Figure 3 shows the board using via connections.

The insulating layer includes rigid and flexible insulating resins such as phenol resin, epoxy resin, polyimide resin and modified polyimide resin, which are reinforced with glass cloth, aramid cloth or paper, and resins without reinforcement. Interconnections to the input and output terminals to the embedded device and the surface conductor pattern include conventional interconnection of the terminals of the embedded device to an interconnecting land for SMD, and formation of terminals on the surface of an embedded device by copper plating or vias using conductive paste.

This PAS does not specify the fabrication process of device embedded substrates, via diameter/via land diameter, conductor width/conductor spacing nor conductor line density.

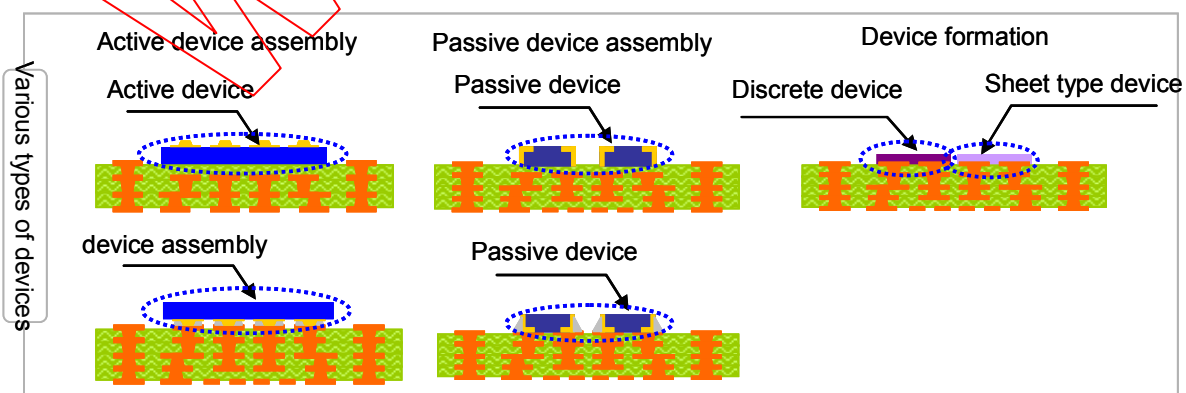


Figure 1 – Examples of device embedded substrate

2 Normative references

Void

3 General definitions

3.1 Technology of the device embedded substrate

There are two types of device embedded substrates: one type consists in embedding an active and/or passive discrete device on a base substrate and covering it with organic resin and the other consists in forming a device on a substrate and then covering it with organic resin. The device embedded substrate also includes composite type substrates which consist of mass produced inorganic ceramic including LTCC (low temperature co-fired ceramics) substrates (hereafter they are called just ceramics) on which passive devices are embedded as shown in Figure 4, and the other type as shown in Figure 5 where the ceramic substrate is used as a base on which active and passive devices are mounted and the entire body is covered by organic resin; details of inorganic ceramics are not specified in this document. Such a ceramic is treated just handled as a base of a device embedded module.

Classification of device embedding is given in Table 1. Active devices include bare die, wafer-level package (WLP), BGA, LGA, and QFN. Passive devices include chip component, complex chip component like an array and integrated passive device (IPD). Module and MEMS are embedded onto the substrate after packaging and moulding into module and MEMS. The component formed during substrate formation is not covered in this document but also included in Table 1. There are two types of formed passive component embedding, one is to form passive components using thick film or thick film technology on the base of a silicon or compound semiconductor and/or on the stacked chip at the wafer level or on package-on-package (PoP), and the other is to use a sheet-type passive device on an organic substrate first and then to embed the other devices.

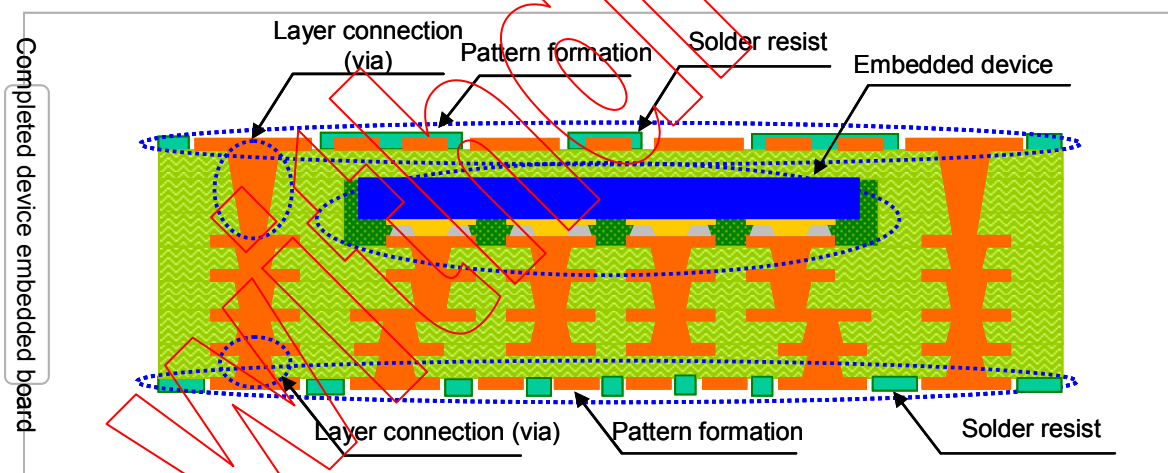


Figure 2 – Completed device embedded substrate (pad connection)

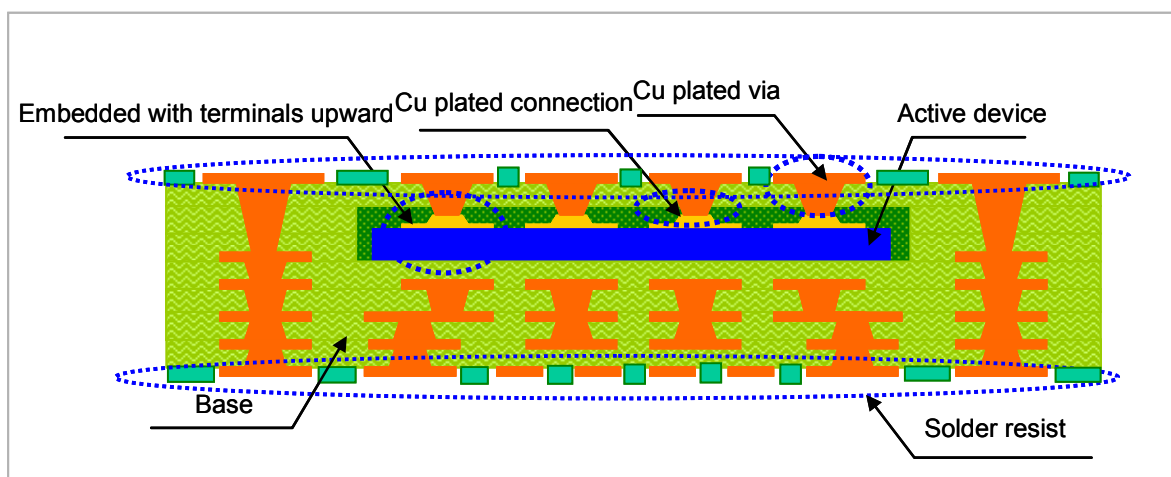


Figure 3 – Completed device embedded substrate (via connection)

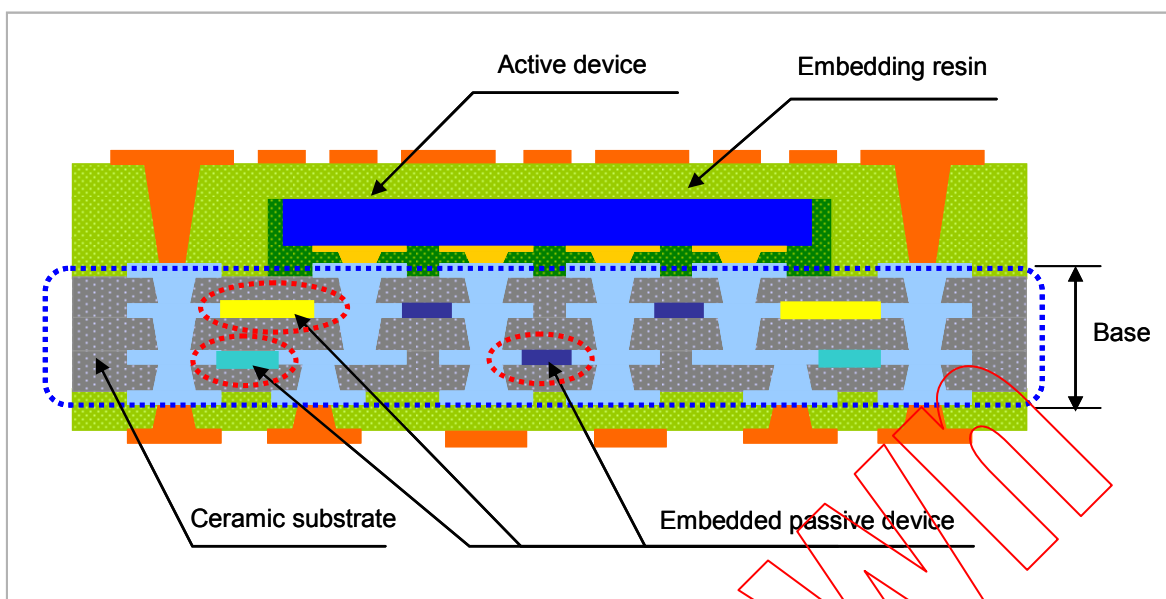


Figure 4 – Structure of a device embedded substrate using a passive device embedded substrate as a base and then a active and/or a passive device is mounted and then covered by resin (Pad connection type)

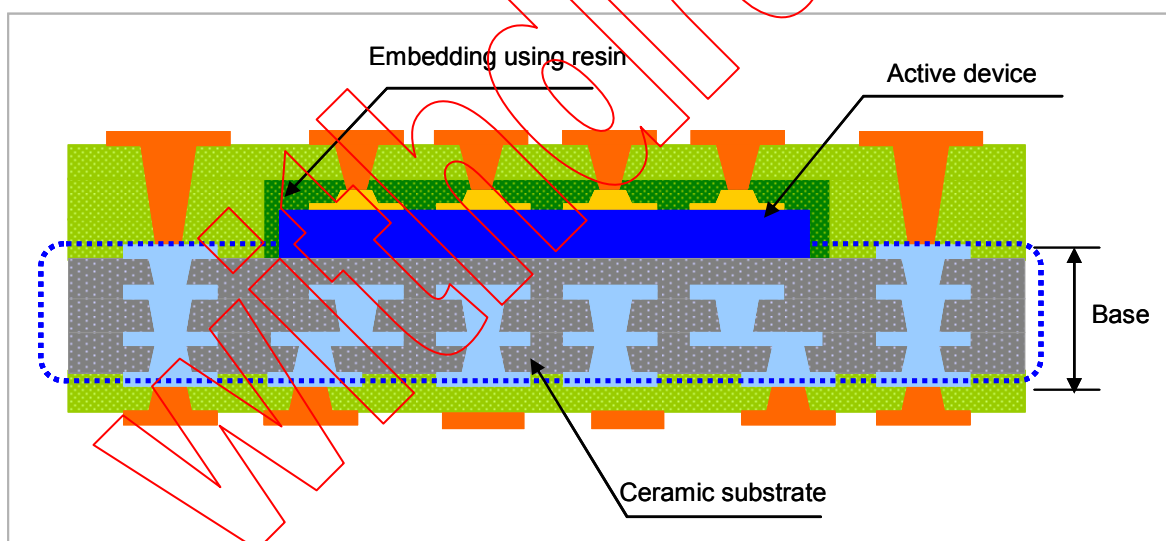


Figure 5 – Structure of a device embedded substrate using a ceramic board as the base (via connection type)

Table 1 – Classification of device embedding

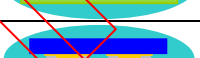
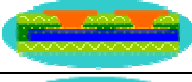
Classification	Item	Embedding	Device terminals	Bonding	Schematics
Active device	Bare die	Die bonding	Peripheral	Wire bonding	
		Flip chip bonding	Peripheral area array	Flip chip bonding	
		Die bonding	Peripheral area array	Via connection (plating, paste)	
	Wafer level package	Mounting	Peripheral area array	Soldering conductive paste	
		Die bonding	Peripheral area array	Via connection (plating, paste)	
	Package	Mounting	BGA, LGA, QFN	Soldering conductive paste	
		Mounting	BGA, LGA, QFN	Via connection (plating, paste)	
Passive device	Chip component	Mounting	Rectangular chip Rod type chip	Through hole	
		Mounting	Rectangular chip Rod type chip	Soldering conductive paste	
		Mounting	Rectangular chip	Via connection (plating, paste)	
	Module chip component	Mounting	Rectangular chip	Soldering conductive paste	
		Mounting	Rectangular chip	Via connection (plating, paste)	
	Integrated passive device	Mounting	IPD	Soldering conductive paste	
		Mounting	IPD	Via connection (plating, paste)	
Module	Packaging and moulding	Mounting	Arbitrary	Soldering conductive paste	
		Mounting	Arbitrary	Via connection (plating, paste)	
MEMS	Packaging and moulding	Mounting	Arbitrary	Soldering conductive paste	
		Mounting	Arbitrary	Via connection (plating, paste)	

Table 1 – Classification of device embedding *(continued)*

Classification	Item	Embedding	Device terminals	Bonding	Schematics
Active device	Formed	Thin film Sputtering	Silicon	Via connection (plating, paste)	
		Thick film Screen printing	Semiconducting polymer	Via connection (plating, paste)	
Passive device	Formed	Double through hole	Copper plating	Via connection (plating, paste)	
		Etching	Laminate material	Via connection (plating, paste)	
		Etching	Film	Via connection (plating, paste)	
		Screen printing	Polymer	Via connection (plating, paste)	
		Transfer	Ferromagnetic Ceramics	Via connection (plating, paste)	
		Lamination	Seeding	Via connection (plating, paste)	
		Spin coating	Polymer	Via connection (plating, paste)	

3.2 Substrate

Structures and fabrication processes of device embedded substrates are illustrated in Table 2. A base substrate is necessary for the device embedded substrate to embed active and passive devices. Most of the base substrates are multilayer substrates and build-up substrates, but an insulating resin board, insulating sheet, metal sheet or film carrier can certainly also be used. Table 2 shows the method to embed the active or passive device and then connect the device to the surface conductor by vias made of copper plating and conductive paste and checking items during the fabrication process.

This document, however, does not cover active devices formed on a silicon interposer, a compound semiconductor substrate or a printed wiring board and passive device (resistor, capacitor or inductor) but it does cover inductors formed together with a conductor pattern and capacitor in its structure.

Table 2 – Embedded device structure and fabrication process

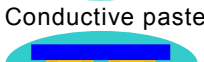
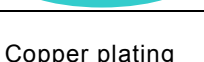
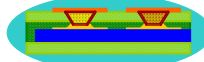
Process	Item	Structure		To check
		Pad bonding	Via connection	
1	Base			Opening, short
2	Mounting			Position accuracy
3	Pad bonding		—	Connection, conduction
4	Embedding			Microvoid Board thickness Flatness
5	Via hole			Hole position Terminal position Resistance to chemicals
6	Via hole	—		Thicknesses of Cu plating & conductive paste Micro void
7	Pattern formation (multi-layer)			Open, short
8	Surface treatment (solder mask, etc.)			Observation

3.3 Jisso mounting and interconnection

There are two types of terminal connections; one is to connect terminals of an embedded device to connecting pads formed on the base, and the other is to form connecting vias on the device after embedding. The device is connected to the pads on the base using conventional semiconductor and SMD mounting techniques and then the device is embedded. The device is connected to the conductor pattern in the second case after embedding by copper plating or conductive paste.

Both of the device mountings can be classified into die-bonding and mounting methods as shown in Table 3.

Table 3 – Jisso mounting and interconnection of the device embedded substrate

Jisso mounting		Device	Interconnection		Structure	
			Process	Interconnection		
Pad bonding	Die bonding	Chip	Wire bonding	Wire melt-connection		
			Flip-chip bonding	Metal bonding Contact connection	Metal bonding  Contact 	
		Mounting	Wafer level packaging (WLP)	Reflow Polymer bonding	Soldering Conductive paste	Soldering  Conductive paste 
	Package		Reflow Polymer bonding	Soldering Conductive paste	 Conductive paste 	
	Rectangular chip		Reflow Polymer bonding	Soldering Conductive paste	Soldering  Conductive paste 	
	Rod-type chip		Reflow Polymer bonding	Soldering Conductive paste	 Conductive paste 	
	Module		Reflow Polymer bonding	Soldering Conductive paste	Soldering  Conductive paste 	
	MEMS		Reflow Polymer bonding	Soldering Conductive paste	 Conductive paste 	
	Via bonding		Die bonding	Chip	Via connection	Copper plating Conductive paste
		Wafer level package (WLP)		Via connection	Copper plating Conductive paste	 Conductive paste
Mounting		Package	Via connection	Copper plating Conductive paste	 Conductive paste 	
		Rectangular chip	Via connection	Copper plating Conductive paste	Copper plating Conductive paste 	
		Rod-type chip	Via connection	Copper plating Conductive paste	 Conductive paste 	
		Module	Via connection	Copper plating Conductive paste	 Conductive paste 	
		MEMS	Via connection	Copper plating Conductive paste	 Conductive paste 	
NOTE The shape and surface treatment of the terminals of the embedding device should be agreed upon between the user and the supplier of the device.						

3.4 Structure and terminology

3.4.1 General

Figure 6 shows each section of the device embedded substrate and its name. See JPCA-TD01-2008, Terms and definitions in electronic circuits, and JIS C 5603, Terms and definitions in printed wiring boards. The number of layers is counted after completion of the device embedding as L1, L2 ~ L6 (in case of 6 layers) from the top layer.

The structure of the device embedded substrate is illustrated by means of the structure of the build-up substrate. See JPCA-BU01-2007, Build-up wiring board (Terms and test methods). Figure 7 shows the typical structure of the base and Figure 8 the cavity structure. Other structures are shown in Figure 9 with the insulating base, in Figure 10 for the base using a conductive carrier or a metal sheet. Figure 11 shows the structure of the device embedded ceramics and Figure 12 shows the standard ceramic board as the wiring board base.

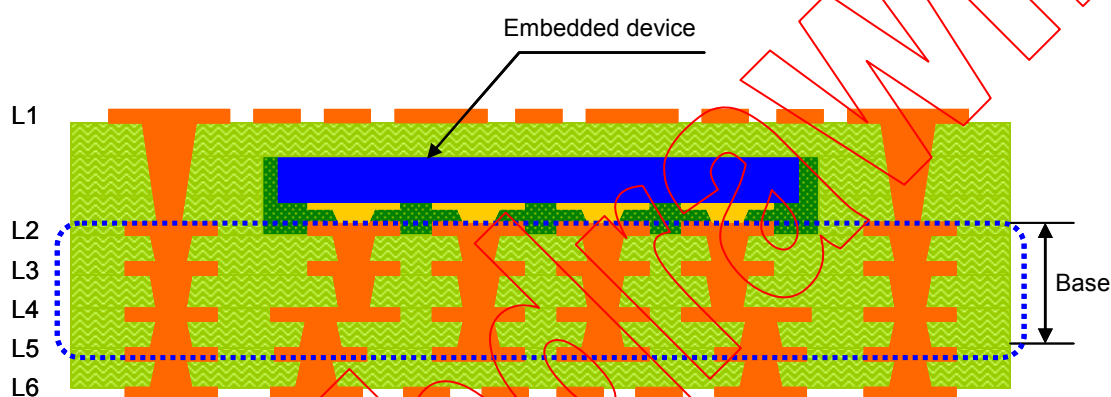


Figure 6 – Entire structure of device embedded substrate

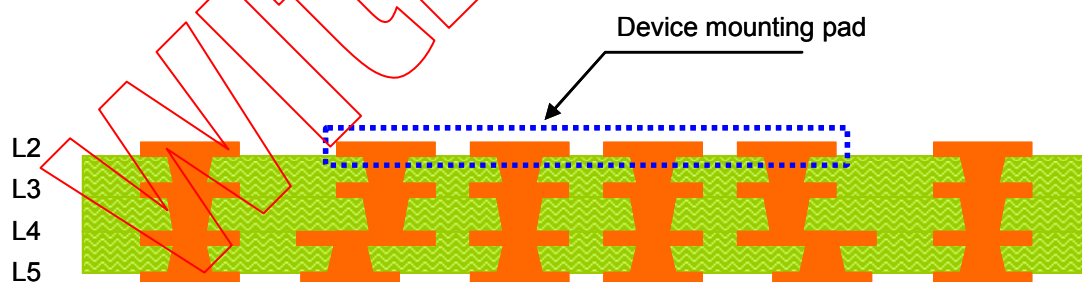


Figure 7 – Base (typical structure)

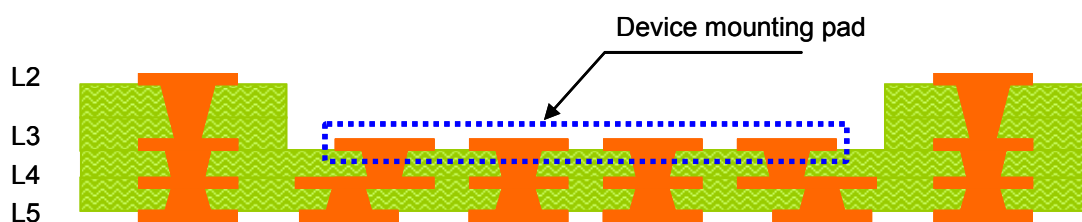
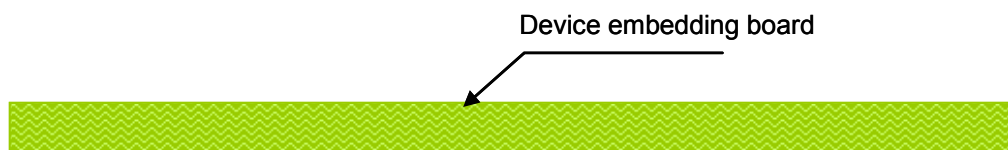


Figure 8 – Base (Cavity structure)



* Used for terminal connection in electronic circuit board

Figure 9 – Base (insulator)



Figure 10 – Base (conductive carrier – metal plate)

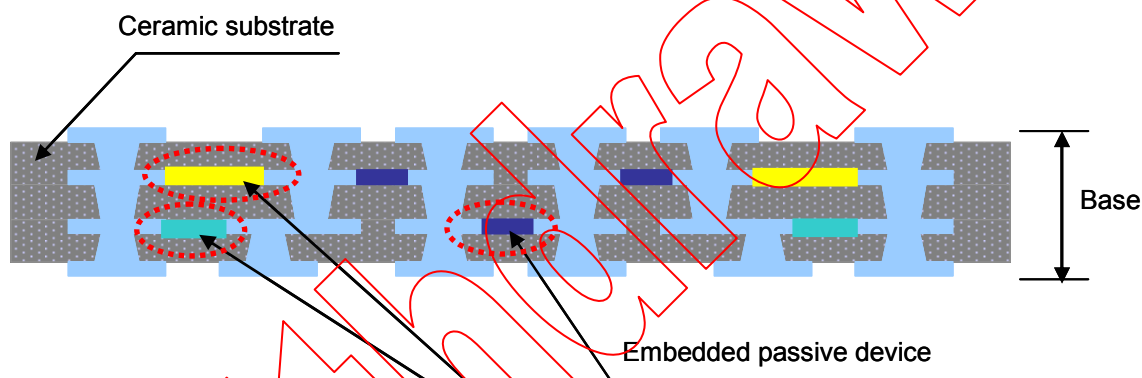


Figure 11 – Passive device embedded ceramic substrate used as a base

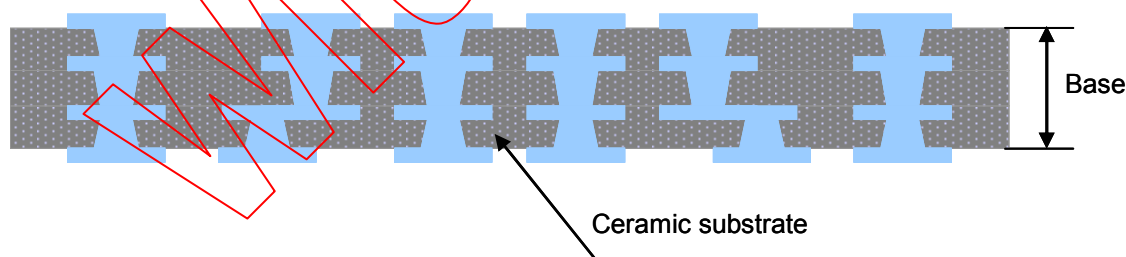


Figure 12 – Ceramic board used as base

Figure 13 to Figure 19 show various cases of device embedding in conventional mounting technique, electric connection after embedding various types of devices, embedding device over more than one layer, device embedding with resin base, and use of conductor layer and metal sheet/copper foil.

3.4.2 Device embedding by conventional process

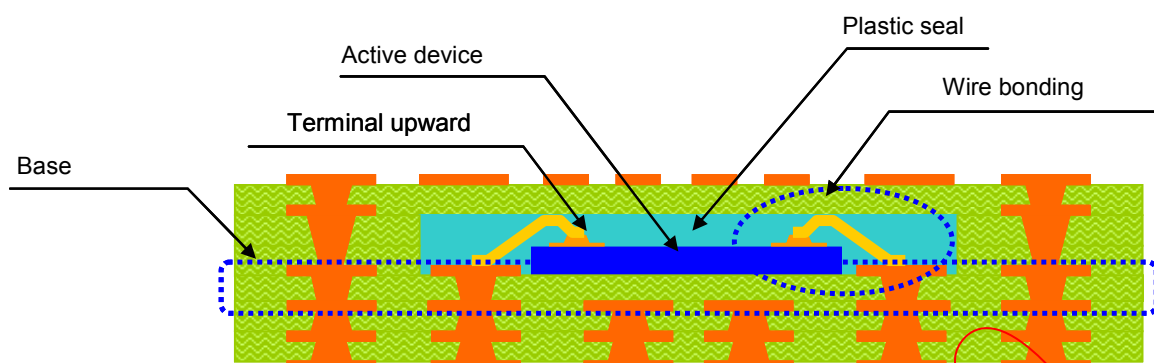


Figure 13a – Wire bonding connection and embedding of active device bear chip

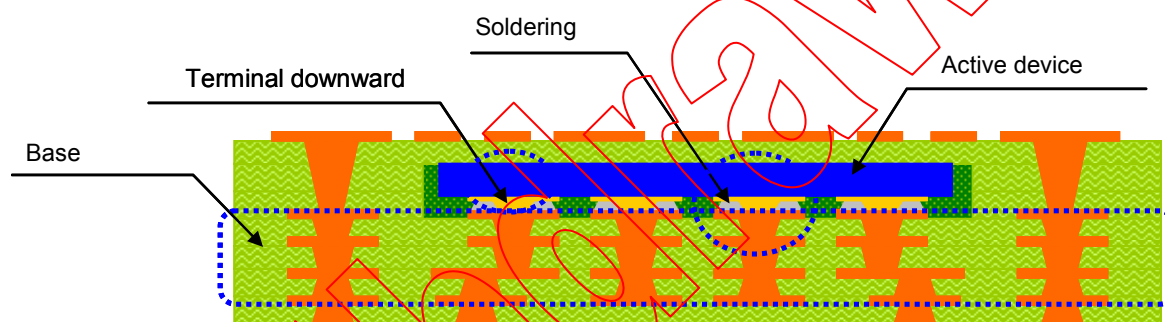


Figure 13b – Soldering connection and embedding of active device

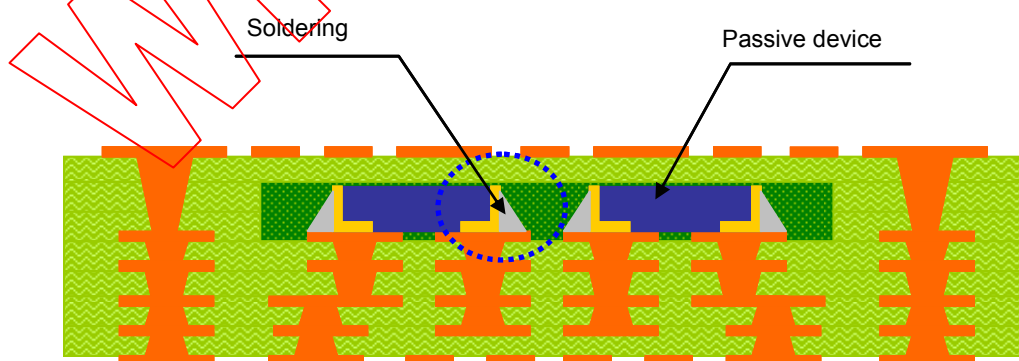


Figure 13c – Soldering connection of square type passive device

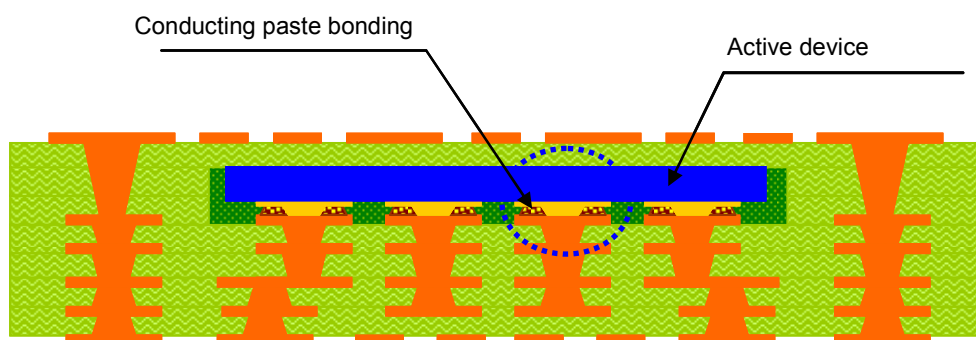


Figure 13d – Conductive resin connection and embedding of active device

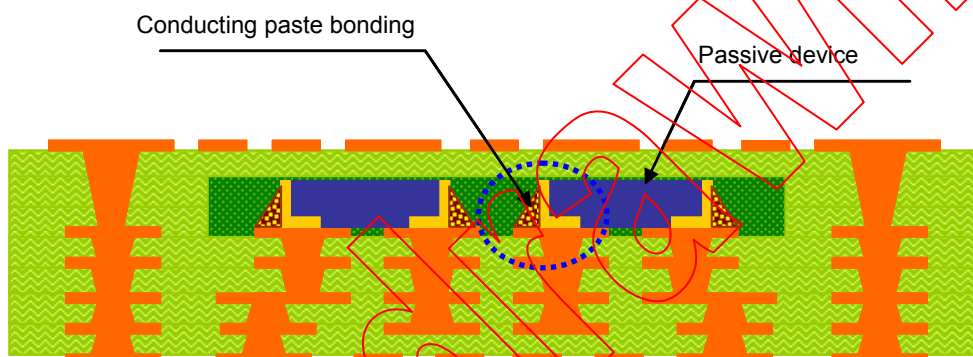


Figure 13e – Conductive resin connection and embedding of square type passive device

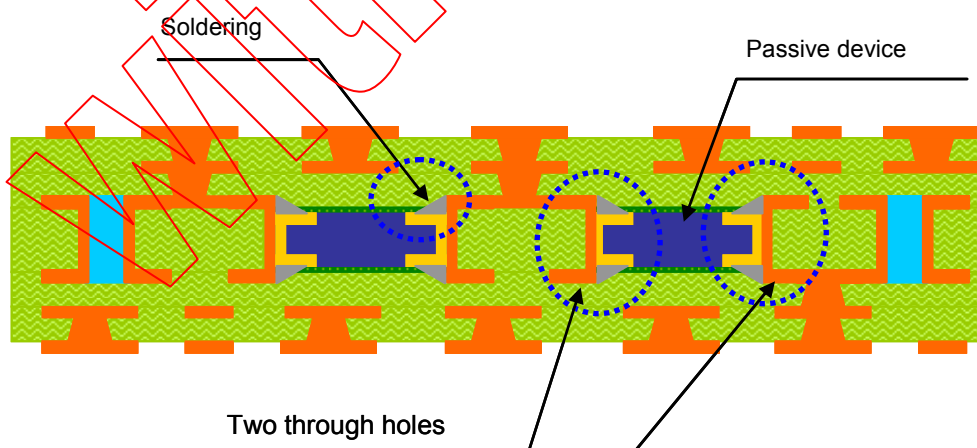


Figure 13f – Soldering connection into through hole and embedding of passive device

Figure 13 – Embedding of device by conventional methods