IEC TR 61191-8

Edition 1.0 2021-03

TECHNICAL REPORT

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Printed board assemblies –
Part 8: Voiding in solder joints of printed board assemblies for use in automotive electronic control units – Best practices

IEC TR 61191-8:2021-03(en)

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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 31.180; 31.190

ISBN 978-2-8322-9575-5

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

PRINTED BOARD ASSEMBLIES –

Part 8: Voiding in solder joints of printed board assemblies for use in automotive electronic control units – Best practices

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IEC TR 61191-8, which is a technical report, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this technical report is based on the following documents:

DTR	Report on voting
91/1665/DTR	91/1689/RVDTR

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

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A list of all parts in the IEC 61191 series, published under the general title *Printed board assemblies*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

This document applies to electronic and electromechanical automotive printed board assemblies and describes current best-practices for dealing with voiding in solder joints of surface-mount components soldered onto printed boards.

This document is an informative document which serves to illustrate the technically feasible options and to provide a basis for customer and supplier discussions and agreements. It is not intended to be regarded as a specification or standard.

Related standards are gathered in the bibliography.

This document has been prepared based on material provided by the working group DKE AK682.0.7 (Assembly and interconnect technology in automotive electronics).

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PRINTED BOARD ASSEMBLIES –

Part 8: Voiding in solder joints of printed board assemblies for use in automotive electronic control units – Best practices

1 Scope

This part of IEC 61191 gives guidelines for dealing with voiding in surface-mount solder joints of printed board assemblies for use in automotive electronics. This technical report focuses exclusively on voids in solder joints connecting packaged electronic or electromechanical components with printed boards (PBs). Voids in other solder joints (e.g. in a joint between a silicon die and a substrate within an electronic component, solder joints of through-hole components, etc.) are not considered. The technical background for the occurrence of voids in solder joints, the potential impact of voiding on printed board assembly reliability and functionality, the investigation of voiding levels in sample- and series-production by use of X-ray inspection as well as typical voiding levels in different types of solder joints are discussed. Recommendations for the control of voiding in series production are also given.

Annex A collects typical voiding levels of components and recommendations for acceptability.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
design authority
individual, organization, company, contractually designated authority, or agency responsible for the design of electrical / electronic hardware, having the authority to define variations or restrictions to the requirements of applicable standards, i.e., the originator/custodian of the applicable design standard and the approved or controlled documentation

3.2
manufacturer
individual, organization, or company responsible for the assembly process and verification operations

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3.3
preballed component
component delivered with solder balls attached, as ball-grid arrays

3.4
solder coverage
ratio of the overlapping area between parallel and wettable surfaces of printed board and component termination covered with a vertically continuous layer of solder divided by the total overlapping area between parallel and wettable surfaces of printed board and component termination

Note 1 to entry: Voids and empty space are not part of the vertically continuous layer of solder and therefore do not contribute to the solder coverage.

3.5
user
individual, organization, company or agency responsible for the procurement of electrical/electronic hardware, and having the authority to define any variation or restrictions to the requirements of applicable standards, i.e., the originator/custodian of the contract detailing these requirements

4 Technical background of voiding in solder joints and potential impact on assembly reliability

4.1 Void categories

Different categories of voids exist (see also Annex A). Those are illustrated in Figure 1 to Figure 7:

a) Inclusions / macro voids (type I)

Voids generated by the evolution of volatiles during the reflow process when the solder is molten. The sources of volatiles are fluxes and solder paste, absorbed moisture in laminates or resulting from oxide reduction during the flux reaction. See Figure 1 for an example.

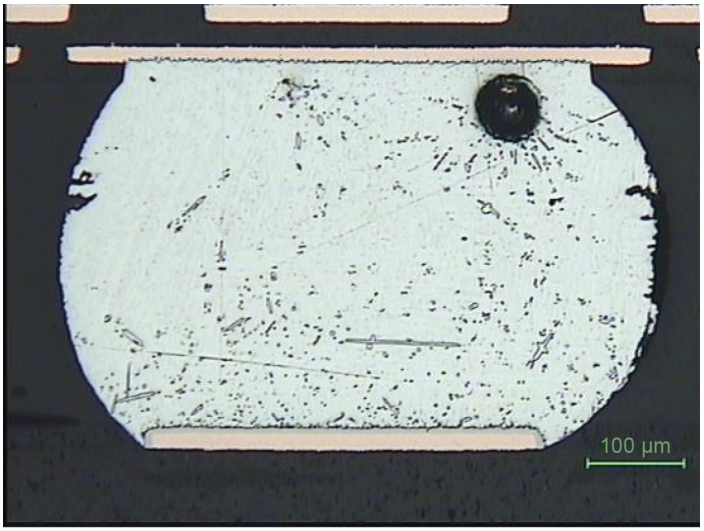

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Figure 1 – Example of inclusion/macro void

b) Design induced voids, (type II)

Voids generated due to the presence of microvia(s) in the land pattern (via in pad design). During reflow, the microvia traps the volatile gases and prevents them from escaping from the solder joint. See Figure 2 for an example.

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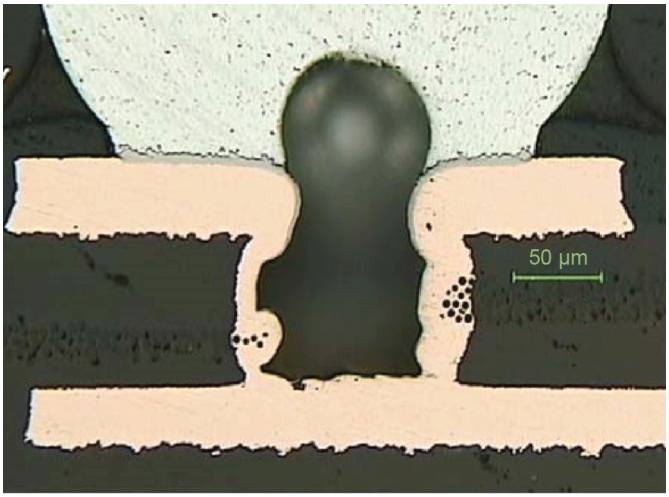

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Figure 2 – Example of design induced void

c) Shrinkage voids (type III)

Voids caused by the reduction in solder volume when the solder is in the process of solidification from liquid to solid. See Figure 3 for an example.

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Figure 3 – Example of shrinkage void

d) Planar micro voids (type IV)

Small voids (typically < 20 µm in diameter) residing substantially at the interface between PB land or component termination and solder; this type of voiding is sometimes also known as "champagne voids". See Figure 4 for an example.

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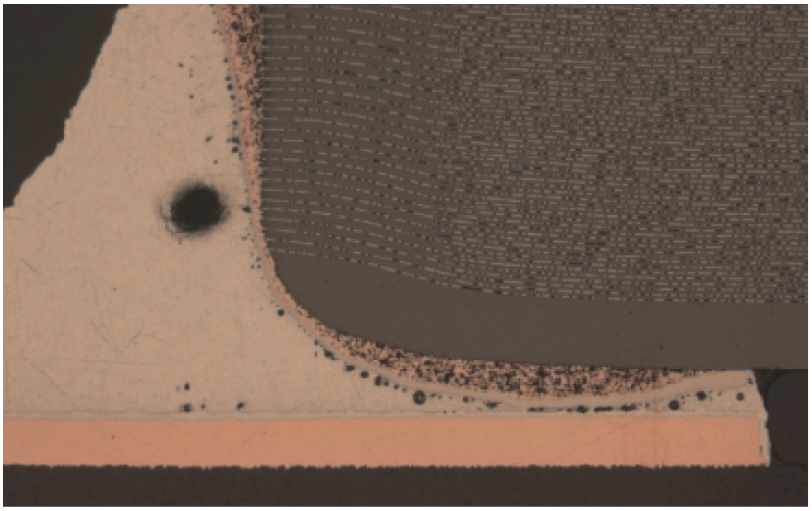

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Figure 4 – Example of planar micro voids

e) Intermetallic micro voids (type V)

Voids formed within intermetallic layers, between base metal and component termination, due to organic impurities in the Cu during electroplating. See Figure 5 for an example.

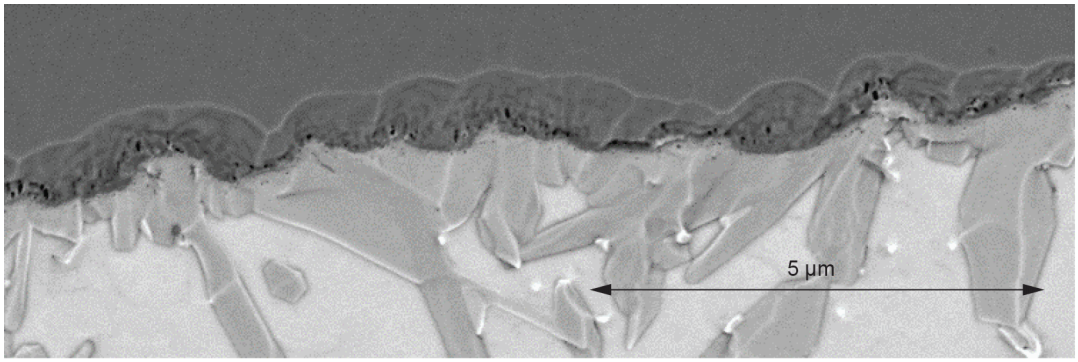

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Figure 5 – Example of intermetallic voids

f) Pinhole micro voids (type VI)

Micron-sized voids within the intermetallic compound (IMC), between the IMC and the PB Cu land or (rarely) close to the IMC in the solder; these are due to an unstable plating process, which can lead to chemicals becoming entrapped during the PB fabrication process. See Figure 6 for an example.

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