

TECHNICAL REPORT

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TR 62017-1

First edition
2001-04

Documentation on design automation subjects –

Part 1: EDA Industry standards roadmap

*Documentation sur les sujets d'automatisation
de la conception –*

*Partie 1:
EDA Industry standards roadmap*



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

DOCUMENTATION ON DESIGN AUTOMATION SUBJECTS – Part 1: EDA Industry Standards Roadmap

FOREWORD

- 1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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The main task of IEC technical committees is to prepare International Standards. However, a technical committee may propose the publication of a technical report when it has collected data of a different kind from that which is normally published as an International Standard, for example "state of the art".

IEC 62017-1, which is a technical report, has been prepared by IEC technical committee 93: Design automation.

It is based on the *EDA Industry Standards Roadmap - 1996* developed jointly by Silicon Integration Initiative Inc. (formerly CAD framework initiative, Inc.), EDAC and SEMATECH.

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
93/97/CDV	93/113/RVC

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This publication has not been drafted in accordance with the ISO/IEC Directives, Part 3.

This document which is purely informative is not to be regarded as an International Standard.

The committee has decided that the contents of this publication will remain unchanged until 2004. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

How this Book is Organized

This book contains six chapters, summarized below:

- Chapter 1, “Introduction,” describes the charter, the three working groups that contributed to the roadmap, and the scope of the work is detailed.
- Chapter 2, “Executive Summary,” summarizes the key messages to the industry council regarding the requirements and the status of EDA standards with respect to those requirements, the recommendations for standards convergence, acceleration, and new standards work, and the recommended standards roadmaps for each category of requirements. The Executive Summary is designed to summarize the information in the chapters that follow that expand upon the Electronic Design and Test area, discussing the environment, the requirements, and the status, recommendations, and roadmaps in more detail.
- Chapter 3, “Electronic Design and Test Environment,” reviews environmental topics that are relevant to the effective design of complex electronic systems. Key emerging paradigm shifts in the EDA industry and many of the pressures on design and CAD integrator teams are identified and discussed.
- Chapter 4, “The Design System (Infrastructure and Tools),” includes the computing environment and user interface, design tool communication, extension language, software development environment, and the design and data management areas. These topics are primarily domain-independent topics, but with an EDA focus.
- Chapter 5, “The Design Information (Design Data Representation),” addresses the key standards related to design data representations for all key design activities, including system level design (architectural and high level design activities) and detailed design (both logical and physical design in a given technology), as well as preparation for manufacturing build and test.
- Chapter 6, “Key Electronic Design and Test Interfaces,” discusses the interfaces to other design (or co-design) disciplines, and the key standards that relate to those interfaces. Manufacturing build and test Interfaces, software interfaces, and mechanical design interfaces are discussed.

How to Find the Information You Want

Below are some quick access tips to help you find the information you want to read about in this book.

- To access the *key roadmap recommendations*, their priority and timeframe, read Section 2 “Executive Summary”.
- To access a given topic’s detailed information including the *environment, requirements, recommendations and roadmap tasks* with descriptions, find the topic in the table of contents and go to the referenced page.
- Those topics that relate to *Design and Data Management* are located in Chapter Four, since they are related to the general design system environment.
- Topics related to *Technology Libraries and Models* are located in Chapter Five, as they are specific representations of EDA design data.

DOCUMENTATION ON DESIGN AUTOMATION SUBJECTS -

Part 1: EDA Industry Standards Roadmap

1 Introduction

1.1 Charter

The EDA Standards Roadmap Workshop was sponsored by the CAD Framework Initiative (CFI), Electronic Design Automation Companies (EDAC), and SEMATECH with participation by interested industry groups. The Workshop was specifically aimed at developing an industry-wide roadmap for development of design and test standards within Electronic Design Automation (EDA).

There were three working groups, each charged with identifying requirements, understanding the current standards environment, and developing a roadmap to improved standards across the next decade for their area of focus:

- EDA Interoperability and Integration Working Group (EII)
- Technology Libraries and Models Working Group (TLM)
- Design and Data Management Working Group (DDM).

The charter of these working groups is discussed below.

1.1.1 Identify the EDA Industry Requirements on EDA Systems

A primary goal was to identify the target requirements of the EDA industry on EDA Systems over the following timeframes:

- Immediate (Short) Term (1995-1998)
- Near Term (1999-2001)
- Long Term (2002-2004 and Beyond).

1.1.2 Review Status and Current Plans of Related Standards

With an understanding of the EDA industry requirements, develop a mapping to the relevant standards involved in supporting those requirements, and review the status and plans of current EDA standards that relate to those requirements.

1.1.3 Determine How to Coexist and Migrate to Improved Standards

Identify the standards changes necessary to meet the requirements, as well as the appropriate coexistence and migration plans from today's current situation to the target EDA system standards structure.

1.1.4 Identify Standards Areas Requiring Improvement

Identify potential standards convergence opportunities, areas where new focus on existing

standards work is needed, and areas where acceleration of planned standards work is required. Clearly identify elements of the standards roadmap in the following categories:

- Convergence of Standards in Areas of Overlap
- New Focus on New Work
- Areas Requiring Acceleration.

1.1.5 Develop a Roadmap to Future Standards

Keeping in mind that the perspective of the roadmap should be a global one, develop and deliver a roadmap of key action plans to support the requirements, and itemize the standards-related work tasks required over time (using the definition of timeframe above). The roadmap should include task descriptions of each of the work items in the roadmap.

The task descriptions have different levels of precision depending on the timeframe for implementation. Those tasks required in the Immediate or Short Term (i.e., end of 1998 to coincide with next generation of CMOS.25um) will have more detail than tasks in later timeframes.

The roadmap for the short term (immediate) timeframe should define the steps that the standards organizations must take to achieve the recommended convergent state of standards to support the Technology Roadmaps. The roadmap steps will define the detailed implementation plan for items in the short term. Roadmap items that are targeted for the near or long term may be less defined.

1.1.6 Deliver Recommendations and Roadmap Contributions

CFI, EDAC and SEMATECH will assist the work groups and provide the lead for the final integration of the individual workgroup recommendations and contributions into an overall EDA Standards Roadmap. Tasks will include:

- Prioritize recommended actions
- Document the needed timeframe for implementation
- Seek approval of the Roadmap and its recommendations by the EDA Industry Council.

1.1.7 EDA Standards Industry Council

The Industry Council is comprised of individuals with the credentials and influence to support the roadmap and promote industry adoption. The membership represents a broad range of geographic, academic, and government interests and reflects the major constituencies of the EDA industry. Industry Council members include:

- Joseph Borel, SGS Thomson Microelectronics
- Ron Collett, Collett International
- Joseph Costello, Cadence Design Systems, Inc.
- John Darringer, IBM

- Aart deGeus, Synopsys, Inc.
- William Evans, AT&T
- Richard Goering, EE Times
- Andrew Graham, CAD Framework Initiative, Inc.
- Alain Hanover, EDAC and Viewlogic Systems, Inc.
- Randy Harr, ARPA
- Lambert van den Hoven, Philips Semiconductor
- Lance Mills, Hewlett-Packard
- L.J. Reed, Motorola
- Wally Rhines, Mentor Graphics, Inc.
- Robert Rozeboom, Texas Instruments, Incorporated
- Greg Ledenbach, SEMATECH
- Gadi Singer, Intel Corporation
- Gary Smith, Dataquest
- Kinya Tabuchi, Mitsubishi
- Hitoshi Yoshizawa, NEC.

1.2 Background

The initial input to the working groups included several documents. The requirements described in chapters 4, 5, and 6 represent a summarization of the key requirements identified in these documents and other sources. The key documents include:

- SIA National Technology Roadmap for Semiconductors¹
- SRC White Paper²
- IPC OEM Requirements³

As indicated in the SIA National Technology Roadmap for Semiconductors (aka, the SIA Roadmap), the U.S. semiconductor community faces new challenges as it moves towards design and manufacturing of chip feature sizes less than .50 microns. This is not unique to the U.S. and is in fact a global problem. A few of these challenges span the entire spectrum of technology including chip cores, chips, MCMs, and boards (PCAs/PCBs), and they require major industry initiatives to develop effective solutions. The SIA Roadmap states that the magnitude of the challenges listed below demands the special attention of the semiconductor industry leadership.

1. The National Technology Roadmap for Semiconductors, 1994
 2. Design Needs for the 21st Century: White Paper, Edited by Dr. James Freedman, VP of Research Integration, Semiconductor Research Corporation, 9/94
 3. OEM Requirement as Input to National Technology Roadmap for Electronic Interconnection, 3/14-16/95

1.2.1 Productivity Improvement

The SIA Roadmap suggests that the semiconductor industry will require productivity gains greater than the 30% historical per-year, per-function cost reduction. Achieving projected densities and projected growth will require unprecedented industry cooperation and standardization through consensus. Many standards are required to achieve cost-effective factories; but the EDA standards are key to the success of future design teams struggling to achieve the productivity and density objectives.

1.2.2 Complexity Management

The years 2007-2010 will see maximum chip sizes increase to 350-800M million transistors for microprocessor designs, and 210M-430M gates¹ for ASIC designs. Successful development of designs this size will:

- require very large design teams and enormous effort,
- involve considerable design complexity, and
- result in a huge amount of design data to manage.

Maintaining control of these designs requires innovative design approaches and tools that support hierarchical and incremental design changes. EDA systems need to provide sophisticated design process and information management capabilities well beyond today's. To support the rapid evolution of design environments, new and innovative EDA solutions must be inserted into complex design processes. Widespread use of design re-use technology and complex intellectual property for data and tools, within and between companies, will be a major enabling technology for designs of such complexity.

EDA systems must be put together in ways that allow "technology insertion" of new EDA innovations as they become available. EDA standards that support an evolving design environment are imperative.

1.2.3 Advanced Technology Development

Funding for high cost and long-term research efforts has been reduced both in the U.S. and the rest of the world. The resulting gap in infrastructure must be filled by members of the semiconductor R&D community.

Improvements in software engineering are required; software applications are now fundamental to design, manufacturing, and business processes. Software development is the least perfected of engineering disciplines.

Increasingly, design and manufacturing of complex electronic systems requires a cultural change, from local optimization, to global optimization of technology solutions across multiple engineering disciplines. Changing industrial cultures is a formidable and time-consuming task.

1. The National Technology Roadmap for Semiconductors, Table 2, p. 16, SIA, 1994

1.2.4 Technology Development Funding

Meeting the challenges of the SIA Roadmap will require an increased expenditure of resources on research and development of technology from the already heavy levels of today. The key challenge is to clearly define requirements and find funding strategies that cover all critical needs.

Items 1.2.3 "Advanced Technology Development" and 1.2.4 "Technology Development Funding" above are not primarily within the scope of this work; however, 1.2.1 "Productivity Improvement" and 1.2.2 "Complexity Management" are clearly contained within the scope of work for this EDA Industry Standards for Design and Test Roadmap.

1.3 Scope

This section defines the scope of the EDA Industry Standards Roadmap for the SIA Electronic Design and Test Areas. It includes strategic direction for key electronic design and test standards, with specific focus on the design system infrastructure, tools and design data, and key packaging technologies, across all key design phases.

The scope is focused on EDA, and is specifically focused on:

- EDA *systems and software* standardization (NOT standardization of electronics hardware)
- EDA and key *interfaces* to the EDA domain (NOT standardization of other CAD domains)
- EDA *Roadmap* for standards development (NOT actual development of the standards)
- EDA *standards* roadmap (NOT a design process or algorithm development roadmap)

1.3.1 Electronic Design and Test Standards Focus

Electronic design and test standards focus includes: infrastructure and tools, design and data management, design data representation, and technology libraries and models.

1.3.1.1 The Design System

This section summarizes the standards for the infrastructure surrounding and supporting Electronic Design and Test systems and tools. It also covers all design and data management standards relating to the definition, execution, and management of the electronic design process.

- Infrastructure and Tools

This includes all standards dealing with the infrastructure surrounding and supporting Electronic Design and Test systems and tools. The subject addresses platform operating systems, communications environment, user interfaces, tool encapsulation, inter-tool communication, and general EDA development environment. These standards promote innovation of new processes and methods for electronic design and test, that can be easily inserted into the design environment (i.e., plug and play). Such standards operate at various levels to bind tools together into design flows, and enable cost-effective multi-vendor flows without requiring tight integration of tools.

- Design and Data Management

This area includes all design and data management standards areas relating to the definition, execution, and management of the electronic design process and its associated work-flows and data across the enterprise. EDA design tool integration and general tool management standards are also discussed in this area.

1.3.1.2 The Design Information

This section addresses Design and Test design information (data) and the definition and re-use of design technology libraries and models.

- Design Data Representation

This area includes all standards areas relating to the definition and representation of Electronic Design and Test design information (data) created and used by EDA design tools and/or the design team in the execution of the design process. Examples include such items as netlists, libraries, test benches, and many kinds of in-process data. The purpose of this area is to identify standards for EDA and point tool suppliers in order to support high quality information exchange and data sharing throughout the design process and across a geographically dispersed enterprise.

- Technology Libraries and Models

Included in this area are all standards relating to the definition and re-use of design technology libraries and models. Key library standards or standards requirements are identified, and focus areas and a roadmap for the next decade is described.

1.3.2 Technology Packages

The following technology and package types are addressed in this roadmap:

- Technology Cores, Cells, and Macrocells (i.e., subsets of chips)
- Chips
- MCMs
- Boards (PCAs, PCBs, backplanes, subassemblies of various types).

1.3.3 Design Phases

The key design phases involved in design and test processes will be addressed, including:

- System Level Design (i.e., Architectural and High Level Design), and
- Detailed Design (i.e., Detailed Logic Design and Detailed Physical Design).

1.3.4 Key Electronic Design and Test Interfaces

The key interfaces involved between electronic design and test and other related disciplines will be addressed, including:

- Manufacturing Build Interface
- Manufacturing Test Interface
- Mechanical Design Interface
- Software Design Interface.

2 Executive Summary

This chapter of the document summarizes the findings of the working groups, and provides the essential information from which the Industry Council review presentations were drawn. Highlights and key messages to the industry council are included for:

- recommended standards roadmaps for each of the key areas,
- recommendations for standards convergence, acceleration, and new areas for development,
- recommendations for a modernized standards development process.

2.1 Roadmaps

The working groups and the charter are briefly reviewed below, along with an overview of the categories of roadmaps developed, and then the roadmaps for each category.

2.1.1 Introduction to Roadmap

The roadmap is designed to be a high level plan for the Electronic Design Automation (EDA) industry to converge on a common set of standards for the next decade. A summary of the charter and scope of this work is summarized below.

The EDA Standards Roadmap Workshop was sponsored by the CAD Framework Initiative (CFI), Electronic Design Automation Companies (EDAC), and SEMATECH with participation by interested industry groups. The Workshop was specifically aimed at developing an industry-wide roadmap for development of design and test standards within EDA.

There were three working groups, each charged with identifying requirements, understanding the current standards environment, and developing a roadmap to improved standards over the next decade in their area of focus:

- EDA Interoperability and Integration Working Group (EII)
- Technology Libraries and Models Working Group (TLM)
- Design and Data Management Working Group (DDM).

The charter of these working groups was as follows:

- Identify the EDA Industry Requirements on EDA Systems over time
 - Immediate (Short) Term (1995-1998)
 - Near Term (1999-2001)
 - Long Term (2002-2004 and Beyond).
- Review Status and Current Plans of Related Standards
- Determine How to Coexist and Migrate to Improved Standards
- Identify Standards Areas Requiring Improvement

- Convergence of Standards in Areas of Overlap
- New Focus on New Work
- Areas Requiring Acceleration.
- Develop a Roadmap to the Future Standards.

2.1.2 Overview of Design and Test Categories

The information in this document and in this executive summary section is organized into categories as follows:

- Design System (Infrastructure and Tools)

This part of the executive summary highlights the key roadmap items for standards related to the

- Computing Environment and User Interface,
- Design Tool Communication,
- EDA System Extension Language,
- EDA Standards-Based Software Development Environment, and
- Design and Data management areas.

- Design Information (Design Data Representations)

This part of the executive summary highlights the key roadmap items for standards in the following design information areas:

- Common topics across all design information (such as incremental processing, hierarchical processing, and design object naming),
- Common topics across all design steps (such as timing, simulation controls),
- System Level Design (i.e. architectural and high level design standards)
- Detailed Design (i.e., detailed logical and physical design standards)
- Design and Technology Re-Use topics, including Technology Libraries and Models.

- Key Design and Test Interfaces

In this section, we summarize the key roadmap items relative to the key interfaces associated with the general area of “design and test”. The interfaces to manufacturing build and test are discussed, as well as high level roadmaps for mechanical design and software/hardware codesign.

2.1.3 Design System Roadmaps

This section summarizes the specific roadmaps for each of the categories. Details on each of the roadmap items can be found in chapters 4-6. Note that each roadmap item as shown in the figures is numbered according to the roadmap chapter and section. In the figures, the following scheme is used to indicate priority

- High priority items are indicated by the darkest fill color (or red)
- Medium priority items are indicated by a lighter fill color (or blue)
- Low priority items are indicated by the lightest fill color (or white).

Note: *All* items are considered important or they would not be in the roadmap.

The start and stop points for items in the roadmaps indicate a mapping of the consensus of the workgroups as to the priority of the requirements (high, medium, low) and the timeframe for the item (i.e., short term, near term, long term).

Design System Roadmap			
	Short Term (1995-1998)	Near Term (1999-2001)	Long Term (2002-2004+)
4.1 <u>Computing Environment & User Interface</u>			
- Standard Unix GUI	Adopt CDE		
- Standard Non-Unix GUI	Adopt Windows		
- Standards-Based EDA Env't	Certified EDA Toolbox		
- Req'ts Path to OS Providers	Formalize EDA Industry Requirements		
4.2 <u>Design Tool Communication</u>			
- Tool to Tool Communication	Adopt ToolTalk		
- Unix-Windows Communication	ToolTalk to Windows OLE		
4.3 <u>EDA System Extension Language</u>			
- Ext Language Functions Library	Multiple EL Support		
- Strategic Ext Language	Re-evaluate Strategic EL(s)		
4.4 <u>EDA Standards-Based Software Development</u>			
- EDA Standards Environment	EDA Standards Architecture Guide		
4.5 <u>Design Management</u>			
- Portable Process Description	Standard Process Description		
- Tool Interface to Design Mgr	Standard Interface Design Tools to Design Mgr		
4.6 <u>Design Data Management</u>			
- Tool Interface to Data Mgr	Standard Interface Design Tools to Data Mgr		
- Access to Data via Metadata	Standard Metafile Interface		
4.7 <u>Design Decision Mgmt</u>			
- Process Metrics Definition	Standard Process Metrics		
- Metrics Collection	Standard I/F to Metrics Collection		
4.8 <u>Design Tool Management</u>			
- Intertool Communications	Adopt ToolTalk, Provide Windows Interoperability		
- Tool Encapsulation	Adopt CFI TES		
- Tool License Management	Establish EDA Industry License Mgr/Use Policy		
4.9 <u>Resource Management</u>	No Roadmap Recommendation		

Figure 2.1—Design System Roadmap

2.1.4 Design Information Roadmaps

In this section, the roadmaps that pertain to the standards for design data representation are addressed. The roadmap shown in Figure 2.2— "Design Information Roadmap" includes standards for the following areas:

- Common Topics Across All Design Information, which include:
 - Incremental Processing
 - Hierarchical Processing
 - Design Object Naming
- Common Topics Across All Design Steps, which include:
 - Timing Information
 - Simulation/Test Control
- System Level Design (i.e. architectural and high level design standards)
- Detailed Design (i.e., detailed logical and physical design standards)
- Design and Technology Re-Use topics, including Technology Libraries and Models.

Design Information Roadmap			
	Short Term (1995-1998)	Near Term (1999-2001)	Long Term (2002-2004+)
5.1 Common Topics - All Info			
- Incremental Processing	Support Incremental Processing		
- Hierarchical Processing	Support Hierarchical Processing		
- Design Object Naming	Support Design Object Naming Std		
5.1 Common Topics - All Steps			
- Timing Information	Support Common Timing Model		
- Simulation/Test Control	Common Simulation/Test Control		
5.3 System Level Design			
- System Design Use Model Standard	System Design Use Model Standard		
- Synthesis Support	Standards for Synthesizable Primitives		
- HDL Interfaces to Tools	Standard Interface to Simulation - OMF		
- Constraint Driven Design Support	Standard Controls for Constraint Driven Design		
- Floorplanning Support	Standards to Support Floorplanning Loop		
5.4 Detailed Design			
- Converged Connectivity Standard	Converged Connectivity Standard		
- Converged Board Standard	Converged PCA/PCB Standard		
- Converged MCM Standard	Converged MCM Standard		
- Converged Chip/Core Standard	Converged Chip/Core Standard		
- Testability Analysis	Standards to Support Test Analysis		
- Manufacturability Analysis	Standards to Support Mfg Analysis		
5.5 Design/Technology Re-Use			
- Data Dictionary	Standard EDB Dictionary/Classifications		
- Design Object “Datasheet”	Standard DesignObject Specification		
- Reusable Functions (Logical)	Standards Reusable Function Taxonomy		
- Reusable Components (Physical)	Standards Reusable Components		
- Library of Reusable Objects	Standards Based Library Building		

Figure 2.2—Design Information Roadmap

2.1.5 Key Electronic Design and Test Interface Roadmaps

Key Electronic Design and Test Interface Roadmaps shown in Figure 2.3— "Key Design and Test Interfaces Roadmap" include:

- Manufacturing Build Interface
- Manufacturing Test Interface
- Mechanical Design Interface
- Software Design Interface.

Key Design and Test Interfaces Roadmap			
	Short Term (1995-1998)	Near Term (1999-2001)	Long Term (2002-2004+)
6.1 <u>Manufacturing Build I/F</u> - Chips and Macrocells (Cores) - Boards (PCA/PCB) - MCMs		Std Interface - See Chip Standard	
		Std Interface - See PCB Standard	
		Std Interface - See MCM Standard	
6.2 <u>Manufacturing Test I/F</u> - Test Interface		Standard Interface for Test	
6.3 <u>Mechanical Design</u> - Mechanical Design Interface		Standard Interface for Mechanical Design	
6.4 <u>Hardware/Software I/F</u> - Hardware/Software Interface		Standard Interface for Co-Design	

Figure 2.3—Key Design and Test Interfaces Roadmap

2.2 Recommendations

In this section, the key recommendations are summarized. Additional information which provides backup and support for these recommendations is detailed in chapters 4-6 of this book.

2.2.1 Key Roadmap Recommendations

The key recommendations of the EDA Industry Standards Roadmap are highlighted in Figure 2.4— "The EDA Industry Standards Roadmap". Along the roadmap on the chart are the time-frames; short term (through 1998), near term (through 2001), and long term (2004 and beyond). The column entitled "Current Standards" lists key current standards in use by the

EDA industry today, arranged in groups entitled “Systems Design” and “Detailed Design.” Along the bottom of the roadmap, we see “Co-Existence”, “Migration”, and “Evolution” which characterize some of the key goals of the roadmap strategy. As we move along the roadmap from left to right, there are a series of recommended EDA Industry Standards:

- Common Connectivity Standard

In this initial release, which is based on the common core information model from the EDIF - CFI DR converged model work, the base is created from which *all* the other design data representation standards developments evolve. This release establishes, for the first time, a file format (in this case an interchange language format, based on EDIF 3 0 0), and a programming interface (based on CFI DR 1.X) which are based upon the *same* information model. In addition, note the “Hierarchical, Incremental, Naming” at the base of the diagram; this is denoting the significant importance of providing support for the hierarchical and incremental processing of design data in *all* future standards developments.

From this point forward, the idea is to add functionality to the base connectivity standard for various “use models,” based on such design topics as timing or package type (e.g., PCB or chip), or even system design models (based on VHDL or Verilog use models), including the necessary support for hierarchical and incremental processing, and at all times have a matched pair of file format and programming interface (PI). Section 2.3.2.1 “Technical Approach” discusses this approach to standards development in more detail. Refer to 5.4.4.1 “Converged Industry Standard for Logical Connectivity” for additional information on this specific roadmap item.

- PCBs and MCM Standards

In this phase, the physical information required to support board level packages including PCBs (printed circuit boards) and MCMs (multi-chip modules) is added to the common information model for connectivity developed in the previous step. There are two standards (or use models) released in this phase; one for boards, and one for MCMs. A file format and PI are both available and are based on the extensions made to the common information model as described above. This work should begin as soon as possible, and the physical information should be initially based on the EDIF 3 5 0 for PCB (and eventually EDIF 4 0 0 for MCM) information models.

- Chips and Cores/Macrocells Standard

Similarly, in this phase, use model standards for physical design data for chips and subsets of chips (cores or macrocells) are supported. A file format and PI are both available and are based on the extensions made to the common information model.

Over time, the defacto standards of today which contain chip/core information will converge into this industry wide standard. For example, the roadmap says that the timing information which is today contained in SDF files, could in the future be contained in a “chip/core” standards-compliant applications database. Because of the standards strategy of information modeling, followed by a file format (or language) and a PI, it is possible to co-exist with legacy standards (e.g., the SDF), while migrating to a new standard (the chip/core standards). It is imperative that vendor tools be developed as soon as possible to this new standard to meet the design requirements detailed in Chapter 5; however, because

of the ability to co-exist with legacy standards while migrating towards new standards, new tools which operate from the new standard can exchange information with legacy tools. EDA vendors can migrate to the new standard when their business situation dictates. At any point in time, the industry would have some vendor tools which operate on legacy standards, and other tools which capitalize on the new standard, and the strategy recognizes the reality of this, and supports it.

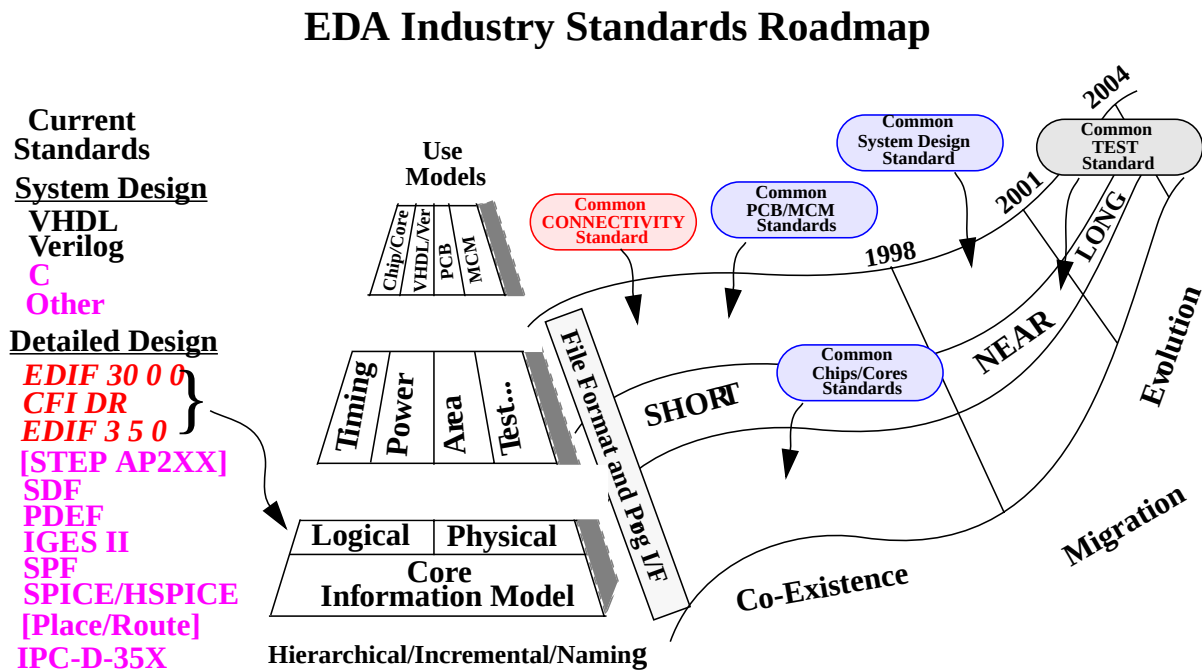


Figure 2.4—The EDA Industry Standards Roadmap

- System Design Standards

In this phase, which is envisioned later in this decade, such as in the near term, a common information model and *standard for system level design* is developed and added to the information model base from the previous step. Because VHDL is significantly more comprehensive than Verilog for system design, it is recommended that we start to build the initial system design standard base using VHDL as a base from which to determine the information model. Similarly, the information model developed from the above step can be extended if necessary to completely cover the information model requirements for Verilog. Additional requirements to support any additional new system design language requirements can also be factored into the information model as well in a similar fashion. From this converged information model, a system design standard with a PI can be developed, with appropriate mappings to any HDL (e.g., VHDL and Verilog).

Using this strategy, for VHDL as an example, would allow the vision to be realized for a new VHDL use model standard; i.e., there is an information model, from which a file for-

mat (i.e., the language, which in this example is VHDL and already defined) and a programming interface is developed. A new VHDL use model standard can be released in the near term which includes both the language and a PI to access that information in PI-compliant tools. Over the long term, the strategy states that for the file format, the system design standard should move to a common exchange file format which supports incremental processing.

It is important to note that to the extent that the information modeling efforts between VHDL and Verilog overlap (i.e., the information being modeled is the same information), then the PI to access that information is *identical*. Over time, as extensions are made to the system design information model (e.g., for analog support), the PI for those extensions is the same for both VHDL-based and Verilog-based customers, even though the file format representations (i.e., the languages) are different. It is anticipated that over time, more and more applications will migrate to the PI approach for data access in cases where data sharing is desired. It would be *very desirable* that the information modeling efforts described above be converged between VHDL and Verilog, but it is not required to achieve VHDL-based or Verilog-based use model standards which have a PI as well as a language.

It should also be noted that this strategy for standards development supports the identification of areas where VHDL and Verilog have a direct mapping (e.g., the areas where the information model and PI are the same), and also those areas where the information models are different, and hence where their use model standards would be different. The creation of language translators would also be facilitated by this information modeling work; however, it must also be noted that because of the differences in VHDL and Verilog, translation between those languages is definitely not automatic, and human intervention may well be required in such translation. Of course, the goal is really to not require data translation, but to use the information modeling based strategy to help us co-exist with the existing legacy languages while we migrate towards an information and data sharing approach.

Defining an information model derived file format (designed for effective tool to tool data exchange of incremental design information, not designed to be human readable) would make it possible for any *specific* language dependency to be reduced over time, and this strategy enables new HDL languages, including graphical representations (non-textual) to be directly supported by the system design standard and PI, and thus be less dependent on language form. Refer to Figure 4.2— "Open EDA Data Interoperability Architecture" for additional comments on co-existing with legacy languages and file formats. Ultimately, it will be a combination of the users and the tool developers who will determine the rate of movement from the traditional system design language based approach to more picture-based system design approaches which are to be supported by the system design standards. Again, this strategy for standards evolution is independent of that rate of change.

- Common Test Standard

In the area of test, it is also envisioned that later in the decade, perhaps in the near term, a common test information model for test information should be developed, from which existing legacy test standards can be supported, and yet a common test standard can be developed to enable new design and test support software and hardware to be developed to

meet emerging design and test requirements. In the same fashion as in the other standards, the test standard also would have a file format and PI available based on the common test information model.

2.2.2 Coexistence and Migration

The roadmap recommendations described above would be extremely difficult to achieve without an effective method to coexist with today's standards while we are attempting to migrate to a better standards-based future.

In order to support coexistence and migration, it must be possible to support legacy standards such as SDF, PDEF, and other file formats, while the industry migrates to a more focused strategic standard such as a common PI and related file format(s)/languages. To support co-existence and migration, a family of translators from each important legacy language (file format) to information model compliant design data repositories must be developed and made available to the industry at large. With this approach, there would be a need for only *one* certified translator for each language in each direction (i.e., one for import, and one for export).

This strategy also makes it possible to gracefully coexist with and migrate to new standards-based design data repositories which include *mixtures* of legacy data and data based upon the new standards roadmap. For example, tools which depend upon SDF files today can still operate without change, and new PI-based design data repositories can import/export SDF transparently through the PI (i.e., the PI knows where and how the data is to be stored or retrieved). Tools which are being rewritten (e.g., to support incremental or hierarchical design) can access that data directly via a PI, or via a common standards-based file format.

To the extent that this standards development process (i.e., information modeling, file format and PI) approach is adopted by industry, it would enable legacy design languages and interchange file formats to eventually phase out as primary design representations. Coexistence with legacy formats would be supported by the translator set, and new tool development would be done totally to a new file format and PI based on the information model. The PI approach also insulates the tool developers from the specific technology used to actually store and retrieve the information, such as relational data base technology, object oriented technology, (e.g., OMG CORBA), and so on. Client applications are also completely insulated from the specifics of the database implementation, and may be distributed across a LAN or WAN, through the use of the PI approach. As a result of this approach, innovation is enabled, yet tools can be implemented in an open EDA environment.

2.2.3 Areas of Convergence

This section summarizes areas where ongoing standards work has considerable overlap. This overlap has been identified, and the recommendations contained here are that certain standards be strategically converged. Table 2.1: "Areas of Recommended Standards Convergence" summarizes the recommended convergence of standards.

As indicated in Figure 2.4— "The EDA Industry Standards Roadmap", examples where standards efforts must be converged include:

- The convergence of EDIF 3 0 0 and CFI DR 1.X into an industry standard which encom-

passes both of them. In the figure, the base core information model and the common connectivity standard reflect this approach.

- The convergence of common design topics such as timing and physical parameters including parasitics and floorplanning, and placement and wiring information must be converged over time into the common information model. Over time, this would imply the *gradual phaseout* of several current standards, including:

- SDF
- PDEF
- IGESII
- SPF
- potentially SPICE/HSPICE
- various floorplanning, and place and wire file formats.

Note that the phaseout of the above standards was described as gradual; this is because the strategy allows this to be achieved over time, based upon EDA vendor development capabilities and user demand, with the “coexist and migrate” strategy described above. The proposed strategy enables all EDA tools to be based on the file (or PI) based interface to design data, as long as they have value to users; but the goal is to get to the PI.

- The convergence of standards for all types of packages and levels of design based on a common information model from which various “use models” for each package type are developed. Use models for boards (PCA/PCB), MCMs, one for chips/cores/macrocells, and a system design language are recommended.
- The convergence of standards related to the manufacturing test interface is also possible (but less studied and understood) and is based on the same strategy as for the design and build standards for packages; i.e., determine the information model requirements based on existing or legacy standards, and develop a file format and PI which supports the converged information model. As in the package standards convergence examples above, the test standards in use today should converge with potential phaseout of selected test-related standards, including:
 - STEP AP211
 - WAVES
 - IEEE DASC short term common chip tester interface.

Table 2.1: Areas of Recommended Standards Convergence

Current Standard	Recommended Standards Convergence
EDIF	5.4.4.1 “Converged Industry Standard for Logical Connectivity
CFI DR	5.4.4.1 “Converged Industry Standard for Logical Connectivity
SDF	5.4.4.1 “Converged Industry Standard for Logical Connectivity
PDEF	5.4.4.1 “Converged Industry Standard for Logical Connectivity
IGES II	5.4.4.1 “Converged Industry Standard for Logical Connectivity

Table 2.1: Areas of Recommended Standards Convergence

Current Standard	Recommended Standards Convergence
SPF	5.4.4.1 “Converged Industry Standard for Logical Connectivity
SPICE/HSPICE	5.4.4.1 “Converged Industry Standard for Logical Connectivity

2.2.4 Areas of Acceleration of Work

In this section are areas of ongoing standards work which need an accelerated rate of development to meet current and future design requirements. A boost in funding and/or resources or EDA vendor focus may be required to accelerate the work of development or adoption of a standard. Refer to Table 2.2: "Areas of Recommended Standards Acceleration" for a list of areas where standards work should be accelerated.

Table 2.2: Areas of Recommended Standards Acceleration

Current Work	Recommended Standards Acceleration
OMF	5.3.4.3 “Standard Interfaces to Design Analysis Tools”
ToolTalk	4.9.4.1 “Intertool Communications: Adopt ToolTalk...”, others
Tool Management	4.9.4.3 “Establish EDA Industry License Manager/Use Policy
DCL Project	5.2.1.4.3 “Complete Delay Project and Extend Beyond ASICs”

Examples in this category include: development of HDL independent standards (e.g., OMF).

2.2.5 Areas Where New Standards Work is Required

In this section are areas where gaps exist in standards, or there are no standards at all. New standards are required to meet critical design requirements, now and in the future. Refer to Table 2.3: "Areas of Recommended New Standards Work" for a list of areas where new standards work is required.

Table 2.3: Areas of Recommended New Standards Work

Related Standards	Recommended New Standards Work
ToolTalk, OLE 2	4.2.4.2 “Provide Windows Interoperability for ToolTalk”
VHDL, Verilog, C	5.3.4.1 “Standards for System Level Design”
Library Standards	5.5.4 “Roadmap - Design and Technology Re-Use”

2.2.6 Areas Where Additional Roadmap Work is Required

In this section, areas which require additional study to complete a detailed roadmap are described. In these areas, the working groups ran out of time and/or resources, and it was determined that additional follow-on work is required before conclusions can be reached. Refer to Table 2.4: "Areas of Recommended Additional Roadmap Development" for a list of areas where additional roadmap development work is required.

Table 2.4: Areas of Recommended Additional Roadmap Development

Related Standards	Recommended Additional Roadmap Development Work
Library Standards	5.5.4 "Roadmap - Design and Technology Re-Use"
Board Standards	5.4.4.2 "Converged Industry Standard for Board Packages"
Data Management	Chapter 4 Design Data, Resource, and Release Management
Manufacturing Test	6.2 Manufacturing Test Interface
Mechanical Interface	6.3 Mechanical Design Interface
Software Interface	6.4 Software Design Interface (Hardware/Software Co-Design)

2.3 The Standards Development Process

This section describes the current standards environment and provides recommendations for the future.

2.3.1 Current Standards Development Environment

The most widely used standards support tool interoperability through the use of "standard" interface file formats. Standards efforts working on the definition of these file formats tend to be somewhat disjointed, and to a degree, competitive. This leads to the necessity for industry players to either support all of these different standards, or pick the one(s) they feel most likely to satisfy their customers. To complicate matters, the standards tend to differ not only in format, but also in content and in the basic structure of their information models. For example, the basic information model for EDIF 3 0 0 electrical connectivity is different from that of CFI DR 1.X or STEP AP2XX. This leads to a further need for translation software to convert between these different standards, which is costly, short lived, and prone to errors.

To meet the challenges of the future, there are a number of standards related needs that must get into focus:

- EDA standards efforts must be harmonized in line with a single "roadmap" (as described in this document). Some harmonization efforts have started, such as between CFI and EDIF, but this is "ad hoc" and without long term targets or goals. There is considerable confusion and frustration across the EDA industry, the ASIC suppliers, and the end-user design community. A roadmap-driven standards effort will offer a strong and stabilizing base from

which to build more effective long term set of standards.

- The time period from standardization to the appearance in commercial products is much too long. A considerable reduction in this time should be a mandatory requirement in reforming the standards development process. The time required for standard identification, definition, industry acceptance, and certifiably accurate implementation needs to be addressed, and requires much closer cooperation between EDA industry participants.

2.3.2 Standards Development Process Recommendations

This section describes the technical vision of standards development and proposes a management model for standardization of future developments.

2.3.2.1 Technical Approach

This section describes the vision and the idealized model of standards development from a technical viewpoint, and the strategy for coexistence and migration towards the ideal model from today's situation.

In general, for a given EDA standards area that needs significant work (and where it makes sense), the conceptual process of building a standard should include:

- Definition of an information model (in EXPRESS)
- A programming interface (built from the information model)

A software programming interface (PI) is designed to support an access method for data *sharing* and direct data access (i.e., no data exchange required). This approach can also be used for high performance data *transfer* between PI-compliant tools. When implemented as a programming interface appropriately, this approach is inherently hierarchical and incremental in nature. This approach can also be used to provide a strategic PI interface between client and provider applications which enables the support of legacy file formats while coexisting and migrating to more strategic forms of design data and PI access. This means that a client application can request design data through a PI interface, and be relatively independent from the actual source of the data (e.g., an SDF or a new converged standard which contains the timing information).

- A file format (built from the same information model)

The file format approach is designed to support the *exchange/archival* of design information where that makes sense; e.g., when passing data between two companies, or a development site and a manufacturing site (where the programming interface concept of data sharing may not apply). Clearly, file formats also provide a base from which to *translate* design data where translation is an effective mechanism.

It is possible that a binary computer readable (not human readable) file format which is based on the information model can be developed which is suitable for data archival and incremental data exchange between information model compliant applications.

Both the file format and the programming interface should be developed and *delivered simultaneously*, as new releases of the standard evolve.

To better convey this concept, refer to Figure 2.5— "Vision of Standards Development". The concept is as follows:

- The Common Connectivity Model

A common core information model is developed (in EXPRESS) for fundamental design connectivity (which is the same connectivity model for all package types). That common connectivity model must also ensure and record the mapping and relationship of all logical and physical information about the entities being connected.

- The Design Topics Model

In this layer, the idea of various design topics such as timing, power, area, and test information get modeled (also in EXPRESS). Each additional design topic for which a standard is required get added in this fashion. As an example, in the illustration, a timing value for a net is shown as .5ps; this timing information would be “annotated” to the base connectivity model as information regarding the net timing information between a specific output net of one block and a specific input pin of another block.

- The “Use Model” Standards

In addition to the information modeled in the previous layers, there is certain additional information required to support “use models” for specific types of packages and the release to manufacturing of design information for those package types. For example, there is information that is unique to board (PCA/PCB) packages, MCMs, and also for chips/cores/Macrocells. The example in the diagram is one of a PCB. Therefore, in general, there is a subset of the information in the common connectivity model, the design topics layer, and the physical package type, that when considered collectively make up the use model for that type of package.

Similarly, there could also be a use model for system design (e.g., a VHDL use model).

Any test of compliance to a “use model” standard actually implies compliance to proper processing of the information per the use model involved.

The concept here is one where the design data information model evolves from a common core information model, upon which specific design topics can extend that core model (e.g., timing), and from which various use models (e.g. a package type such as “chip”) can be further developed. Similarly, a use model for system level design can be developed. From each of these use models a “standard” can be developed.

Vision of Standards Development

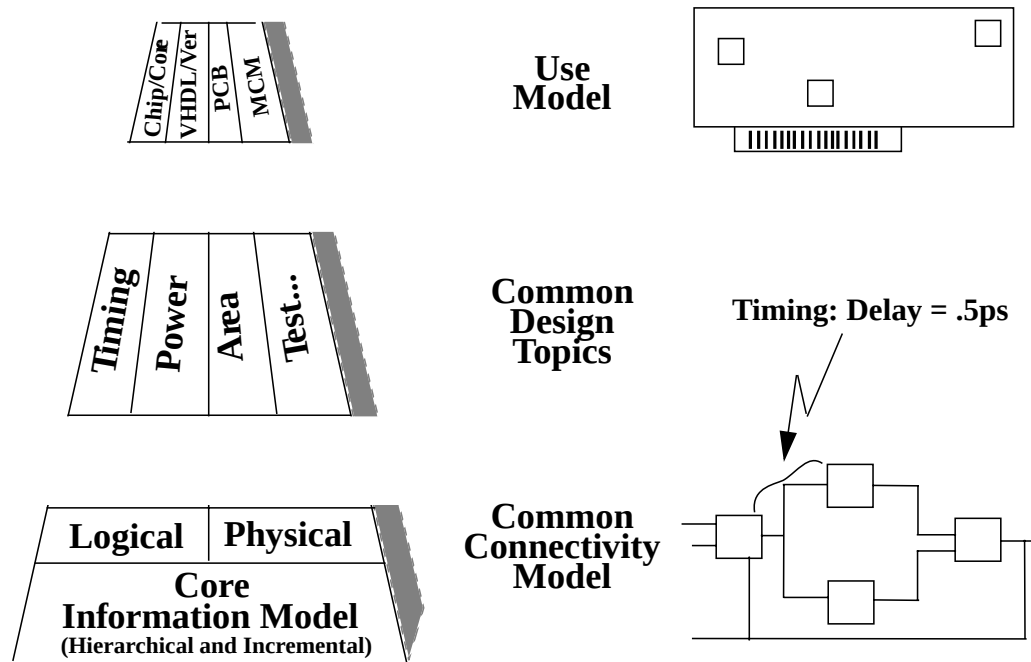


Figure 2.5—Vision of Standards Development

2.3.2.2 Standards Management Model

This section overviews the existing standards situation, and proposes a management strategy supporting the cooperative and focused development and adoption of future standards.

It is easy to observe that there are many standards organizations with standards that they develop and promote. It is also clear that there is confusion in the EDA marketplace, and unnecessary overlap and competition in selected standards areas. This problem must be addressed by the industry council.

It is recommended that the industry council come to a common agreement that *all* design data representation standards developed for the EDA industry be developed under the process described in this document, and when ready (i.e., accepted by industry), be submitted to a *single* standards body (e.g., IEEE, EIA, etc.) for formal standardization process and life cycle management.

2.3.2.3 Pilot Programs and Prototype Development

Any new standard or significant new release of a standard should have a prototype implementation using the draft level of the standard to form a candidate standard.