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# IEEE Standard for System, Software, and Hardware Verification and Validation

IEEE Computer Society

Sponsored by the
Software and Systems Engineering Standards Committee




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**IEEE Std 1012™-2016**
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Approved 28 September 2017

**IEEE-SA Standards Board**

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**Abstract:** Verification and validation (V&V) processes are used to determine whether the development products of a given activity conform to the requirements of that activity and whether the product satisfies its intended use and user needs. V&V life cycle process requirements are specified for different integrity levels. The scope of V&V processes encompasses systems, software, and hardware, and it includes their interfaces. This standard applies to systems, software, and hardware being developed, maintained, or reused (legacy, commercial off-the-shelf [COTS], non-developmental items). The term *software* also includes firmware and microcode, and each of the terms *system, software*, and *hardware* includes documentation. V&V processes include the analysis, evaluation, review, inspection, assessment, and testing of products.

**Keywords:** acceptance testing, architecture evaluation, component testing, concept documentation evaluation, criticality, criticality analysis, design evaluation, disposal plan evaluation, environmental verification and validation (V&V) factors, hardware life cycle, hardware V&V, hardware verification and validation, hazard analysis, IEEE 1012, implementation evaluation, independent verification and validation (IV&V), integration testing, integrity level, interface analysis, IV&V, minimum V&V tasks, nth of a kind, objective evidence, operating procedure evaluation, qualification testing, quality assurance, regression analysis, regression testing, requirements allocation analysis, requirements evaluation, reuse software, risk analysis, security analysis, software life cycle, software quality assurance (SQA), software V&V, software verification and validation, source code documentation evaluation, source code evaluation, SQA, stakeholder needs and requirements evaluation, system element interaction analysis, system life cycle, system maintenance strategy assessment, system of interest, system requirements evaluation, system V&V, system verification and validation, testing, traceability analysis, V&V, V&V measures, validation, verification

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## Introduction

This introduction is not part of IEEE Std 1012™-2016, IEEE Standard for System, Software, and Hardware Verification and Validation.

The Verification and Validation processes are technical processes of systems, software, and hardware engineering. The Verification process and the Validation process are interrelated and complementary processes, and are referenced together as *verification and validation (V&V)*. The purpose of V&V is to help the organization build quality into the system during the life cycle. V&V processes provide an objective assessment of products and processes throughout the life cycle. This assessment demonstrates whether the requirements are correct, complete, accurate, consistent, and testable. The V&V processes determine whether the development products of a given activity conform to the requirements of that activity and whether the product satisfies its intended use and user needs. The determination includes the assessment, analysis, evaluation, review, inspection, and testing of products and processes. V&V is performed in parallel with all life cycle stages, not at their conclusion.

V&V is an extension of program management and systems, software, and hardware engineering that employs a rigorous methodology to identify objective data and conclusions to provide feedback about quality, performance, and schedule to the supplier. This feedback consists of anomaly resolutions, performance improvements, and quality improvements not only for expected operating conditions but also across the full spectrum of the system and its interfaces. Early feedback results allow the organization to modify the products in a timely fashion and thereby reduce overall project and schedule impacts. Without a proactive approach, the anomalies and associated system changes are typically delayed to later in the program schedule, resulting in greater program costs and schedule delays.

IEEE Std 1012 is a process standard that defines the V&V processes in terms of specific activities and related tasks. The standard also defines the contents of the V&V plan (VVP), including example formats.

V&V may be performed at the level of the system, software element, or hardware element, or on any combination of these. V&V may also be performed on an element of a system, including a subordinate system (i.e., subsystem). Throughout this standard, the term *hardware* means an electronic or mechanical hardware element. In each case, the V&V processes are invoked, either in parallel or recursively, across the full life cycle of the system or element.

This version of the standard is a revision to IEEE Std 1012-2012 [B5].[1] The earliest version of this standard (1986) described the content of a software V&V plan, with subsequent versions (1998 and 2004) changing the focus from the software V&V plan to software V&V processes. The 2012 revision expanded the scope of the V&V processes to include systems and hardware as well as software. This revision aligns more completely with the terminology and structure of ISO/IEC/IEEE 15288:2015(E) [B16] and ISO/IEC 12207:2008 [B11]. The following is a summary of the changes made in this version:

— No new V&V activities or tasks have been added other than to address the new or modified processes from ISO/IEC/IEEE 15288:2015(E) [B16], and conformance to this standard can be readily aligned with conformance to the V&V clauses of ISO/IEC/IEEE 15288. Some V&V activities and tasks have been rearranged to facilitate understanding and ease of use.

— The terminology, structure, and mappings were revised to be consistent with ISO/IEC/IEEE 15288:2015(E) [B16].

The following key concepts are emphasized in this standard:

— Integrity levels. Defines four integrity levels to describe the importance of the system, software, and hardware, varying from high integrity to low integrity, to the user.

[1] The numbers in brackets correspond to those of the bibliography in Annex N.


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— Minimum V&V tasks for each integrity level. Defines the minimum V&V tasks required for each of the four integrity levels.

— Optional V&V tasks. Includes a table of optional V&V tasks for tailoring the V&V effort to address the project needs and application-specific characteristics.

— Intensity and rigor applied to V&V tasks. Includes the concept that the intensity and rigor applied to the V&V tasks vary according to the integrity level. Higher integrity levels require the application of greater intensity and rigor to the V&V task. Intensity includes a greater scope of analysis across all normal and abnormal system operating conditions. Rigor includes more formal techniques and recording procedures.

— Detailed criteria for V&V tasks. Defines specific criteria for each V&V task, including minimum criteria for correctness, consistency, completeness, accuracy, readability, and testability. The V&V task descriptions include a list of the required task inputs and outputs.

— Systems viewpoints. Includes minimum software and hardware V&V tasks to address system issues. These tasks include hazard analysis, security analysis, risk analysis, migration assessment, and retirement assessment. Specific system issues are contained in individual V&V task criteria.

— Conformance to international and IEEE standards. Defines the V&V processes to conform to life cycle process standards such as ISO/IEC/IEEE 15288:2015(E) [B16] and ISO/IEC 12207:2008 [B11], as well as the entire family of IEEE software engineering standards. This standard addresses all system and software life cycle processes, including the Agreement, Organizational Project-Enabling, Project, Technical, Software Implementation, Software Support, and Software Reuse process groups. This standard is compatible with all life cycle models; however, not all life cycle models use all of the life cycle processes described in this standard.


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# IEEE Standard for System, Software, and Hardware Verification and Validation

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## 1. Overview

### 1.1 Scope

This verification and validation (V&V) standard is a process standard that addresses all system, software, and hardware life cycle processes including the Agreement, Organizational Project-Enabling, Project, Technical, Software Implementation, Software Support, and Software Reuse process groups. This standard is compatible with all life cycle models (e.g., system, software, and hardware); however, not all life cycle models use all of the processes listed in this standard.

V&V processes determine whether the development products of a given activity conform to the requirements of that activity and whether the product satisfies its intended use and user needs. This determination may include the analysis, evaluation, review, inspection, assessment, and testing of products and processes.

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The user of this standard may invoke those life cycle processes and the associated V&V processes that apply to the project. A description of system life cycle processes may be found in ISO/IEC/IEEE15288:~~2008~~ 2015(E) [B16], [1] and a description of software life cycle processes may be found in ISO/IEC 12207:2008 [B11] ~~and IEEE Std 1074™ 2006 [B9]~~. Annex A maps ISO/IEC/IEEE 15288:~~2008~~2015(E) [B16] (Table A.1 and Table A.2) and ISO/IEC 12207:2008 [B11] (Table A.3 and Table A.4) to the V&V activities and tasks defined in this standard.

This standard defines the verification and validation processes that are applied to the system, software, and hardware development throughout the life cycle, including acquisition, supply, development, operations, maintenance, and retirement. This standard applies to the system, software, and hardware being acquired, developed, maintained, or reused. The term *software* also includes firmware and microcode (e.g., Field Programmable Gate Arrays and Programmable Logic Devices). Each of the terms *system*, *software*, and *hardware* includes its associated documentation.

V&V processes consist of the Verification process and the Validation process. The Verification process provides objective evidence for whether the products ~~perform the following~~:

— Conform to requirements (e.g., for correctness, completeness, consistency, and accuracy) for all activities during each life cycle process.

— Satisfy the standards, practices, and conventions during life cycle processes.

— Successfully complete each life cycle activity and satisfy all the criteria for initiating succeeding life cycle activities (i.e., builds the product correctly).

The Validation process provides evidence for whether the products ~~perform the following~~:

— Satisfy system requirements allocated to the products at the end of each life cycle activity.

— Solve the right problem (e.g., correctly model physical laws, implement business rules, and use the proper system assumptions).

[1] The numbers in brackets correspond to those of the bibliography in Annex ~~M~~ N.

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— Satisfy intended use and user needs in the operational environment (i.e., builds the correct product).

The Verification process and the Validation process are interrelated and complementary processes that use each other's process results to establish better completion criteria and analysis, evaluation, review, inspection, assessment, and test V&V tasks for each life cycle activity. The V&V task criteria described in Table 1a through Table 1d explicitly define the conformance requirements for V&V processes.

The development of a sufficient body of evidence requires a trade-off between the amount of time spent and a finite set of system conditions and assumptions against which to perform the V&V tasks. Each project should define criteria for a sufficient body of evidence (~~i.~~e.g., selecting an integrity level ~~establishes one of~~), the ~~basic parameters), time~~ schedule, and the scope of the V&V analysis and test tasks ~~(i.e., range of system conditions and assumptions)~~.

This standard does not assign the responsibility for performing the V&V tasks to any specific organization. The analysis, evaluation, and test activities may be performed by multiple organizations; however, the methods and purpose will differ for each organization's functional objectives.

ISO/IEC/IEEE 15288:~~2008~~ 2015(E) [B16] ~~and ISO/IEC 12207:2008 [B11] require that the developer perform various testing and evaluation~~ includes tasks ~~as an integral part of implementation~~ for the supplier to execute the agreement according to established project plans and to deliver the product or service in accordance with the agreement criteria. The techniques described in this standard ~~may be~~ are useful in performing the ~~developer's~~ supplier's tests and evaluations. Therefore, whenever this standard mentions the ~~developer's~~ supplier's performance of a verification or validation activity, it is to be understood that the reference applies to the test and evaluation tasks of ~~implementation~~ system development.

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## 1.2 Purpose

The purpose of ~~the~~ this standard is to ~~perform the following~~:

— Establish a common framework of the V&V processes, activities, and tasks in support of all system, software, and hardware life cycle processes.

— Define the V&V tasks, required inputs, and required outputs in each life cycle process.

— Identify the minimum V&V tasks corresponding to a four-level integrity ~~scheme~~ schema.

— Define the content of the Verification and Validation Plan.

## 1.3 Field of application

This standard applies to all applications of systems. When conducting V&V of a system, software, or hardware element, it is important to examine the interactions with the system of which the element is a part. This standard identifies the important system considerations that V&V processes and tasks address in determining correctness and other V&V attributes (e.g., completeness, accuracy, consistency, and testability).

The dynamics of complex systems and the multitude of different logic paths available within the system in response to varying stimuli and conditions demand that the V&V effort examines the correctness of the system for each possible variation in conditions. The ability to model complex, real-world conditions will be limited, and thus, the V&V effort examines whether the limits of the modeling are realistic and reasonable for the desired solution. The unlimited combination of system conditions presents the V&V effort with the challenge of using a finite set of analytical, test, simulation, and demonstration techniques to establish a reasonable body of evidence that the system is correct.

A system provides a capability to satisfy a stated need or objective by combining one or more of the following: processes, hardware, software, facilities, and people. These relationships require that V&V processes consider interactions among all system elements (software and hardware). The V&V processes address the following interactions with the system:

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— Environment: Determines that the system correctly accounts for all conditions, natural phenomena, physical laws of nature, business rules, and physical properties and the full ranges of the system operating environment.

— Operators/users: Determines that the system communicates the proper status/condition of the system to the operator/user and correctly processes all operator/user inputs to produce the required results. For incorrect operator/user inputs, ~~assure~~ assures that the system is protected from entering into a dangerous or uncontrolled state. ~~Validate~~ Validates that operator/user policies and procedures (e.g., security, interface protocols, data representations, and system assumptions) are consistently applied and used across each component interface.

— Other software, hardware, and systems: Determines that the software or hardware component interfaces correctly with other components in the system in accordance with requirements and that errors are not propagated between components of the system.

The scope of V&V processes includes the operational environment, operators and users, hardware, software, data processes (e.g., processes for providing service to users), procedures (e.g., operator instructions), and facilities. The user of this standard should consider V&V as part of the life cycle processes defined by industry standards, such as ISO/IEC 12207:2008 [B11]~~, IEEE Std 1074-2006 [B9],~~ or ISO/IEC/IEEE15288:~~2008~~ 2015(E) [B16].

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To address the systems perspective, system, software, and hardware V&V ~~effort~~ efforts should provide an integrated analysis where the V&V tasks are interrelated, providing input and insight into other V&V tasks. The results from completed life cycle processes provide valuable and necessary inputs to V&V tasks in other life cycle processes. The results and findings from one V&V task may cause previously completed V&V tasks to be analyzed again with the new data. This relationship among V&V tasks (including feedback to the Technical and Software/Hardware Specific processes) employing rigorous systems engineering techniques is a key approach to an integrated systems, software, and hardware V&V. The V&V results provide the other ISO/IEC/IEEE 15288:2015(E) [B16] life cycle processes (agreement, organizational project-enabling, technical management, and technical) with an early detection of anomalies and potential process trends that may be used for process improvement. The V&V processes and tasks described in this standard may be used in conjunction with systems engineering and process improvement models, such as the CMU/SEI-2010-TR-033 [B1].

## 1.4 V&V objectives

V&V processes provide an objective assessment of products and processes throughout the life cycle. This assessment demonstrates whether the requirements are correct, complete, accurate, consistent, and testable. The V&V processes determine whether the products of a given activity conform to the requirements of that activity and whether the product satisfies its intended use and user needs. The determination includes assessment, analysis, evaluation, review, inspection, and testing of products and processes. V&V tasks ~~shall be~~ are performed in parallel with all life cycle stages, not at their conclusion.

The results of V&V provide the following benefits to the program:

— Facilitate early detection and correction of anomalies.

— Enhance management insight into process and product risks.

— Support the life cycle processes to assure conformance to program performance, schedule, and budget.

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— Provide an early assessment of performance.

— Provide objective evidence of conformance to support a formal certification process.

— Improve the products from the acquisition, supply, development, and maintenance processes.

— Support process improvement activities.

## 1.5 Organization of the standard

The Verification and Validation processes described in this standard are constructed to be consistent with ISO/IEC/IEEE 15288:2015(E) [B16] and ISO/IEC Std 12207:2008 [B11].

This standard is organized into clauses (Clause 1 through Clause 12), tables (Table 1 through Table 3, and their respective subparts a–d), figures (Figure 1 and Figure 2, and their respective subparts a–d), and annexes (Annex A through Annex ~~M~~ N). Clause 2 through Clause 12 and Table 1a through Table 1d and Table 2a through Table 2d provide the mandatory V&V requirements for this standard. Table 1a through Table 1d and Table 2a through Table 2d are the focal point of this standard, containing detailed V&V activity and task requirements. Table 1a through Table 1d and Table 2a through Table 2d ~~are broken into four subtables~~ address the following:

— Common V&V tasks in Table 1a and Table 2a

— System V&V tasks in Table 1b and Table 2b

— Software V&V tasks in Table 1c and Table 2c

— Hardware V&V tasks in Table 1d and Table 2d

Each clause containing V&V activities and tasks has the subset of Table 1a through Table 1d and Table 2a through Table 2d associated with the V&V requirements for that clause. Figure 1a through Figure 1d, Figure 2a through Figure 2d, and Table 3a through Table 3d contain informative material that provides examples of V&V processes and provides guidance for using this standard, and they are similarly organized. All annexes are informative.

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— Clause 1 provides guidance for using this standard.

— Clause 2 is reserved for normative references; however, this standard does not prescribe any normative references.

— Clause 3 provides a definition of terms, abbreviations, and conventions.

— Clause 4 describes the relationships between the V&V processes and the life cycle processes from ISO/IEC/IEEE 15288:~~2008~~2015(E) [B16] and ISO/IEC 12207:2008 [B11], and it describes how the V&V standard is applied recursively within the concept of a system of systems and from system to software or hardware components.

— Clause 5 describes the use of integrity levels to determine the scope and rigor of V&V processes.

— Clause 6 explains how V&V tasks are described within this standard.

— Clause 7 describes common V&V tasks~~;~~. The common V&V tasks are invoked for any V&V that is~~, tasks that are common across application of this standard to~~ performed (system, software, or hardware).

1) Table 1a contains the V&V tasks and activities and their criteria for common V&V tasks and activities.

2) Table 2a contains the minimum tasks for each integrity level for common V&V tasks.

3) Table 3a contains the optional common V&V tasks.

4) Figure 1a depicts a summary of common V&V activities and tasks.

5) Figure 2a depicts a summary of V&V test products and tasks.

— Clause 8 describes system V&V tasks.

1) Table 1b contains the V&V tasks and activities and their criteria for system V&V tasks and activities.

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2) Table 2b contains the minimum tasks for each integrity level for system V&V tasks.

3) Table 3b contains the optional system V&V tasks.

4) Figure 1b depicts a summary of system V&V activities and tasks.

5) Figure 2b depicts a summary of system V&V test products and tasks.

— Clause 9 describes software V&V tasks.

1) Table 1c contains the V&V tasks and activities and their criteria for software V&V tasks and activities.

2) Table 2c contains the minimum tasks for each integrity level for software V&V tasks.

3) Table 3c contains the optional software V&V tasks.

4) Figure 1c depicts a summary of software V&V activities and tasks.

5) Figure 2c depicts a summary of software V&V test products and tasks.

— Clause 10 describes hardware V&V tasks.

1) Table 1d contains the V&V tasks and activities and their criteria for hardware V&V tasks and activities.

2) Table 2d contains the minimum tasks for each integrity level for hardware V&V tasks.

3) Table 3d contains the optional hardware V&V tasks.

4) Figure 1d depicts a summary of hardware V&V activities and tasks.

5) Figure 2d depicts a summary of hardware V&V test products and tasks.

— Clause 11 describes V&V reporting, administrative, and documentation requirements.

— Clause 12 describes the content of a V&V plan.

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This standard is organized so that the V&V processes (system, software, or hardware) may be invoked separately or in any combination. V&V processes may be accomplished in any of the following combinations: system V&V (Clause 8), software V&V (Clause 9), hardware V&V (Clause 10), system/software V&V (Clause 8 and Clause 9), system/hardware V&V (Clause 8 and Clause 10), software/hardware V&V (Clause 9 and Clause 10), and system/software/hardware V&V (Clause 8 ~~through~~, Clause 9, and Clause 10). Some V&V tasks are common to systems, software, and hardware V&V; in order not to repeat these V&V tasks in each part, the common V&V tasks are listed once in Clause 7. The common V&V tasks are invoked for any V&V that is performed. These combinations are illustrated in Figure 3.

| V&V Scope | Common Clause 7 | System Clause 8 | Software Clause 9 | Hardware Clause 10 |
|---|---|---|---|---|
| System only | X | X | | |
| Software only | X | | X | |
| Hardware only | X | | | X |
| System and software | X | X | X | |
| System and hardware | X | X | | X |
| Software and hardware | X | | X | X |
| System, software, and hardware | X | X | X | X |

(New)

~~| V&V Scope | Common | System | Software | Hardware |~~
~~| --- | --- | --- | --- | --- |~~
~~| System only | X | X | | |~~
~~| Software only | X | | X | |~~
~~| Hardware only | X | | | X |~~
~~| System and software | X | X | X | |~~
~~| System and hardware | X | X | | X |~~
~~| Software and hardware | X | | X | X |~~
~~| System, software, and hardware | X | X | X | X |~~

~~(Deleted)~~

**Figure 3—V&V effort combinations**

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NOTE—References to Table 1 and Table 2 without a suffix a, b, c, or d are understood to include those parts of the table that correspond to the parts of the V&V scope being invoked (i.e., Common, System, Software, or Hardware). References to Figure 1 and Figure 2 that do not have a suffix a, b, c, or d are similarly understood to include those parts of the figure that correspond to the parts of the V&V scope being invoked.[2]

Clause 4 through Clause 6 contain guidance that is applicable to all combinations of the V&V scope. Clause 11 contains reporting requirements for all combinations of V&V scope. Clause 12 ~~contains~~ describes the content of the V&V plan and provides a sample V&V plan outline.

Table 1a through Table 1d provide V&V task descriptions, inputs, and outputs for each life cycle process. Table 2a through Table 2d list minimum V&V tasks required for different integrity levels. Table 3a through Table 3d provide a list of optional V&V tasks and their suggested applications in the system life cycle. These optional V&V tasks may be added to the minimum V&V tasks to tailor the V&V effort to project needs.

Figure 1a through Figure 1d provide an example of an overview of the V&V inputs, outputs, and minimum V&V tasks for integrity level 4. Figure 2a through Figure 2d provide guidelines for scheduling V&V test planning, execution, and verification activities. An example of a phased life cycle model was used in Figure 1a through Figure 1d and Figure 2a through Figure 2d to illustrate a mapping of the ISO/IEC 12207:2008 [B11] life cycle processes to the V&V activities and tasks described in this standard.

[2] Notes in text, tables, and figures of a standard are given for information only and do not contain requirements needed to implement this standard.

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Annex A describes the mapping of ISO/IEC 12207:2008 [B11] and ISO/IEC/IEEE 15288:~~2008~~2015(E) [B16] to this standard's V&V activities and tasks. Annex B provides an example of a risk-based, four-level integrity ~~scheme~~ schema. Annex C ~~provides a~~ describes the degrees ~~definition~~ of ~~independent~~ independence in verification and validation ~~(IV&V)~~. Annex D provides guidelines for conducting V&V of reuse software. Annex E describes V&V measures. Annex F illustrates an example of the V&V organizational relationship to other project responsibilities. Annex G describes optional V&V tasks. Annex H describes environmental factors that should be considered when conducting V&V. Annex I discusses potential issues with interactions among system, software, and hardware. Annex J describes hazard analysis, security analysis, and risk analysis and their role in V&V. Annex K provides an example of assigning and changing the integrity level of supporting system functions. Annex L maps the process outcomes from ISO/IEC 12207:2008 [B11] and ISO/IEC/IEEE 15288:~~2008~~2015(E) [B16] to associated V&V tasks. Annex M describes V&V for $n^{th}$ of a kind systems. Annex N provides a bibliography of the informative standards referenced in this standard.

## 1.6 Audience

The audience for this standard includes system, software, and hardware suppliers, acquirers, developers, maintainers, V&V practitioners, operators, users, and managers in both the supplier and acquirer organizations.

## 1.7 Conformance

The word *shall* identifies the mandatory requirements to be followed to conform to this standard. The words *should* and *may* indicate optional tasks that are not required to claim conformance to this standard.

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Not all V&V efforts are initiated at the start of the life cycle process of acquisition and continued through the maintenance process. If a project uses only selected life cycle processes, then conformance to this standard is achieved if the minimum V&V tasks are implemented for all of the associated life cycle processes selected for the project. ~~Any~~ A claim of conformance to this standard ~~shall identify~~ includes identification of the applicable life cycle processes. As in all cases, the minimum V&V tasks are defined by the integrity level assigned to the system, software, or hardware. For life cycle processes that are not used by the project, the V&V requirements and tasks for those life cycle processes are optional V&V tasks invoked as needed at the discretion of the project. Specific development methods and technologies (such as automated code generation from detailed design) may eliminate development steps or combine several development steps into one; therefore, a corresponding adaptation of the minimum V&V tasks is permitted and ~~shall be~~ is documented in any claim of conformance to this standard.

When this standard is invoked for existing systems, software, or hardware and the required V&V inputs are not available, then the V&V tasks may use other available project input sources or may reconstruct the needed inputs to achieve conformance to this standard.

Clause 2 through Clause 12, Table 1a through Table 1d, and Table 2a through Table 2d provide the mandatory V&V requirements for this standard. System, software, or hardware conformance to this standard can be achieved by demonstrating that all the "shall" requirements in the specified clauses are met as defined below:

— System V&V conformance: Clause 7 and Clause 8

— Software V&V conformance: Clause 7 and Clause 9

— Hardware V&V conformance: Clause 7 and Clause 10

All conformance waivers need to be approved by the acquiring organization and ~~shall be~~ described in the verification and validation plan (VVP). The information required for deviations and waivers ~~shall include~~ includes the task identification, rationale, and the effect on quality.

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## 1.8 Disclaimer

This standard establishes minimum criteria for V&V processes, activities, and tasks. However, implementing these criteria does not automatically ensure conformance to system or mission objectives, or prevent adverse consequences (e.g., loss of life, mission failure, loss of system safety or security, or financial or social loss). Conformance to this standard does not absolve any party from any social, moral, financial, or legal obligations.

# 2. Normative references

This standard does not require the use of any normative references. Standards useful for the implementation and interpretation of this standard are listed in Annex ~~M~~ N, Bibliography.

# 3. Definitions~~, abbreviations,~~ and acronyms

## 3.1 Definitions

For the purposes of this document, the following terms and definitions apply. ~~ISO/IEC/~~The *IEEE* ~~24765-2010 *IEEE Standard Glossary of Software Engineering Terminology* [B19] and the *IEEE* *Standards Dictionary*: *Glossary of Terms and Definitions*~~ *Online* [B2] should be consulted for terms not defined in this clause.[3] ~~A note following a definition indicates the source of the definition.~~

**acceptance testing: (A)** ~~Formal~~ Testing conducted to determine whether a system satisfies its acceptance criteria and to enable the customer to determine whether to accept the system. **(B)** Formal testing conducted to enable a user, customer, or other authorized entity to determine whether to accept a system or component.

[3]IEEE Standards Dictionary Online subscription is available at:

http://www.ieee.org/portal/innovate/products/standard/standards_dictionary.html.

~~[3] *IEEE Standard Glossary of Software Engineering Terminology* and *IEEE Standards Dictionary: Glossary of Terms and Definitions* are available at http://shop.ieee.org/. Definitions of individual terms may also be obtained free of charge at http://www.computer.org/sevocab.~~

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NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**acquirer:** Stakeholder that acquires or procures a product or service from a supplier. Other terms commonly used for an acquirer are buyer, customer, owner, or purchaser.

NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**anomaly:** Anything observed in the documentation or operation of a system that deviates from expectations based on previously verified system, software, or hardware products or reference documents.

NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**asset:** An item (e.g., design, specifications, source code, documentation, test suites, or manual procedures) that has been designed for use in multiple contexts.

NOTE—See IEEE Std 1517™-2010 [B10].

**baseline:** Any agreement or result designated and fixed at a given time, from which changes require justification and approval.

NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**component:** One part that makes up a system. A component may be hardware or software and may be subdivided into other components.

NOTE 1—The terms *module, component,* and *unit* are often used interchangeably or defined to be subelements of one another in different ways depending on the context. The relationship of these terms is not yet standardized.

NOTE 2—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**component testing:** Testing of individual hardware or software components.

NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

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**criticality:** The degree of impact that a requirement, module, error, fault, failure, or other item has on the development or operation of a system.

NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**domain:** A problem space.

NOTE—See IEEE Std 1517-2010 [B10].

**domain analysis: (A)** The analysis of systems within a domain to discover commonalities and differences among them. **(B)** The process by which information used in developing software systems is identified, captured, and organized so that it can be reused to create new systems, within a domain. **(C)** The result of the process in (A) and (B).

NOTE—See IEEE Std 1517-2010 [B10].

**domain engineering:** A reuse-based approach to defining the scope (i.e., domain definition), specifying the structure (i.e., domain architecture), and building the assets (e.g., requirements, designs, software code, and documentation) for a class of systems, subsystems, or applications. Domain engineering may include the following activities: domain definition, domain analysis, developing the domain architecture, and domain implementation.

NOTE—See IEEE Std 1517-2010 [B10].

**firmware:** The combination of a hardware device and computer instructions and data that reside as read-only software on that device.

NOTE 1—This term is sometimes used to refer only to the hardware device or only to the computer instructions or data, but these meanings are deprecated.

NOTE 2—The confusion surrounding this term has led some to suggest that it be avoided altogether.

NOTE 3—See ISO/IEC/IEEE 24765:2010 [B~~19~~ 20].

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**hazard: (A)** An intrinsic property or condition that has the potential to cause harm or damage. **(B)** A source of potential harm or a situation with a potential for harm in terms of human injury, damage to health, property, or the environment, or some combination of these.

NOTE—~~For (A),~~ See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**hazard identification:** The process of recognizing that a hazard exists and defining its characteristics.

NOTE—~~For (A),~~ See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**independent verification and validation (IV&V):** V&V performed by an organization that is technically, managerially, and financially independent of the development organization.

NOTE 1— See Annex C for a description of the degrees of independence for V&V.

NOTE 2— See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**integration testing:** Testing in which software components, hardware components, or both are combined and tested to evaluate the interaction between them.

NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**integrity level:** A value representing project-unique characteristics (e.g., complexity, criticality, risk, safety level, security level, desired performance, and reliability) that define the importance of the system, software, or hardware to the user.

**interface design document (IDD):** Documentation that describes the architecture and design interfaces between system and components. These descriptions include control algorithms, protocols, data contents and formats, and performance.

NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**interface requirements specification (IRS):** Documentation that specifies the requirements for the interfaces between systems and components. These requirements include constraints on formats and timing.

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NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**life cycle processes:** A set of interrelated or interacting activities that result in the development or assessment of system, software, or hardware products. Each activity consists of tasks. The life cycle processes may overlap one another. For verification and validation (V&V) purposes, no life cycle process is concluded until its development products are verified and validated according to the defined tasks in the verification and validation plan (VVP).

NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**microcode:** A collection of microinstructions, comprising part of, all of, or a set of microprograms.

NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**microprogram:** A sequence of instructions, called microinstructions, specifying the basic operations needed to carry out a machine language instruction.

NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**minimum tasks:** Those verification and validation (V&V) tasks required ~~for~~ by the integrity level assigned to the system, software, or hardware to be verified and validated.

**n$^{th}$ of a kind component/system:** a re-manufacturing or re-installation of a previously verified and validated hardware and/or software design. The n$^{th}$ of a kind component/system is equivalent to the first application in all relevant aspects, including functional and performance requirements, design documentation, environment, and regulatory constraints.

NOTE—See Annex M for a discussion of V&V of n$^{th}$ of a kind systems.

**optional tasks:** Those verification and validation (V&V) tasks that may be added to the minimum required V&V tasks to address specific application requirements.

**qualification testing:** Testing conducted on a hardware element, software element, or system to evaluate conformance with specified requirements.

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NOTE—See ISO/IEC/IEEE 24765:2010 [B20].

**required inputs:** The set of items necessary to perform the minimum verification and validation (V&V) tasks mandated within any life cycle activity.

**required outputs:** The set of items produced as a result of performing the minimum verification and validation (V&V) tasks mandated within any life cycle activity.

**reusable product:** A system, software, or hardware product developed for one use but having other uses, or one developed specifically to be usable on multiple projects or in multiple roles on one project. Examples include, but are not limited to, commercial off-the-shelf (COTS) software products, acquirer-furnished software products, software products in reuse libraries, and preexisting developer software-

products. Each use may include all or part of the software product and may involve its modification. This term can be applied to any software product (for example, requirements, architectures), not just to software itself.

NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**risk: (A)** The combination of the likelihood of occurrence and the consequences of a given future undesirable event. Risk can be associated with products and/or projects. **(B)** The combination of the likelihood of an abnormal event or failure and the consequence(s) of that event or failure to a system's components, operators, users, or environment.

NOTE—See ISO/IEC 16085-2006 [~~B18~~ B19]. ISO/IEC 16085 provides examples of risk categories, but does not provide a complete taxonomy. By its nature, V&V will typically identify risks that are technical, safety, or engineering, but may also identify other types, including legal, organizational, cost, or schedule risks.

**security: (A)** The protection of computer hardware or software from accidental or malicious access, use, modification, destruction, or disclosure. Security also pertains to personnel, data, communications, and the physical protection of computer installations. **(B)** The protection of information and data so that unauthorized persons or systems cannot read or modify them and authorized persons or systems are not denied access to them.

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NOTE—See ISO/IEC/IEEE 24765-:2010 [B19 B20].

**software design description (SDD):** A representation of software created to facilitate analysis, planning, implementation, and decision-making. The software design description is used as a medium for communicating software design information and may be thought of as a blueprint or model of the system.

NOTE—See ISO/IEC/IEEE 24765-:2010 [B19 B20].

**software requirements specification (SRS):** Documentation of the essential requirements (functions, performance, design constraints, and attributes) of the software and its external interfaces.

NOTE—See ISO/IEC/IEEE 24765-:2010 [B19 B20].

**system of interest:** System whose life cycle is under consideration in the application of one instance of this verification and validation (V&V) standard.

NOTE—See ISO/IEC/IEEE 15288:20082015(E) [B16].

~~**system testing:** Testing conducted on a complete, integrated system to evaluate the system's compliance with its specified requirements.~~

~~NOTE—See ISO/ISO/IEC/IEEE 24765-2010 [B19].~~

**test case: (A)** A set of test inputs, execution conditions, and expected results developed for a particular objective, such as to exercise a particular program path or to verify compliance with a specific requirement. **(B)** Documentation specifying inputs, predicted results, and a set of execution conditions for a test item.

NOTE—See ISO/IEC/IEEE 24765-:2010 [B19 B20].

**test design:** Documentation specifying the details of the test approach for a system, software, or hardware feature or combination of features and identifying the associated tests.

NOTE—See ISO/IEC/IEEE 24765-:2010 [B19 B20].

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**test plan: (A)** A document describing the scope, approach, resources, and schedule of intended test activities. It identifies test items, the features to be tested, the testing tasks, who will do each task, and any risks requiring contingency planning. **(B)** A document that describes the technical and management approach to be followed for testing a system or component. Typical contents identify the items to be tested, tasks to be performed, responsibilities, schedules, and required resources for the testing activity.

NOTE—See ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**test procedure: (A)** Detailed instructions for the setup, execution, and evaluation of results for a given test case. **(B)** A document containing a set of associated instructions as in (A). **(C)** Documentation that specifies a sequence of actions for the execution of a test.

NOTE—See IEEE Std 982.1™-2005 [B4].

**validation: (A)** The process of evaluating a system or component during or at the end of the development process to determine whether it satisfies specified requirements. **(B)** The process of providing evidence that the system, software, or hardware and its associated products satisfy requirements allocated to it at the end of each life cycle activity, solve the right problem (e.g., correctly model physical laws, implement business rules, and use the proper system assumptions), and satisfy intended use and user needs.

NOTE—For (A), see ISO/IEC/IEEE 24765-:2010 [~~B19~~ B20].

**verification: (A)** The process of evaluating a system or component to determine whether the products of a given development phase satisfy the conditions imposed at the start of that phase. **(B)** The process of providing objective evidence that the system, software, or hardware and its associated products conform to requirements (e.g., for correctness, completeness, consistency, and accuracy) for all life cycle activities during each life cycle process (acquisition, supply, development, operation, and maintenance); satisfy standards, practices, and conventions during life cycle processes; and successfully complete each life cycle activity and satisfy all the criteria for initiating succeeding life cycle activities. Verification of interim work products is essential for proper understanding and assessment of the life cycle phase product(s).

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NOTE—For (A), see ISO/IEC/IEEE 24765-:2010 [B19 B20].

**verification and validation (V&V) effort:** The work associated with performing the V&V processes, activities, and tasks.

## 3.2 Abbreviations and Acronyms

The following acronyms and abbreviations appear in this standard:

| | |
|---|---|
| COTS | commercial off-the-shelf |
| CPU | central processing unit |
| GOTS | government off-the-shelf |
| HDD | hardware design description |
| HRS | hardware requirements specification |
| HW | hardware |
| IDD | interface design document |
| IRS | interface requirements specification |
| IV&V | independent verification and validation |
| N/A | not applicable |
| N/R | not required |
| OCD | operational concept document |
| QA | quality assurance |
| RFP | request for proposal (tender) |
| SDD | software design description |
| SRD | system requirements document |

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SRS software requirements specification

SW software

TRA threat and risk assessment

VVP verification and validation plan

V&V verification and validation

WBS work breakdown structure

## 4. Relationships between verification and validation (V&V) and life cycle processes

This standard is structured to enable a V&V practitioner to use Clause 7 (common V&V) and any of Clause 8 (system V&V), Clause 9 (software V&V), or Clause 10 (hardware V&V) in performing V&V for a particular product. V&V on a system is performed using Clause 7 and Clause 8 (common and system), on software using Clause 7 and Clause 9 (common and software), and on hardware using Clause 7 and Clause 10 (common and hardware).

Most systems consist of more than a single hardware or a single software element. A depiction of a more complex system with subsystems and system elements (i.e., software or hardware, shown as shaded boxes) is shown in Figure 4. The system life cycle processes are applied recursively from the system of interest to the systems at the next level, with the recursion continuing until a system element is reached. For software system elements, the software life cycle processes are applied, and for hardware system elements, the hardware life cycle processes are applied. The life cycle processes at the system, software, or hardware levels may be conducted in parallel for systems or system elements at the same level. The full set of life cycle processes (system, software, or hardware, as appropriate) are applied to each product. In the same way, system V&V is applied recursively for each system of the system of interest, and software or hardware V&V is applied to each system element. For V&V purposes, no life cycle process is concluded until its development products are verified and validated according to the defined tasks in the verification and validation plan (VVP).

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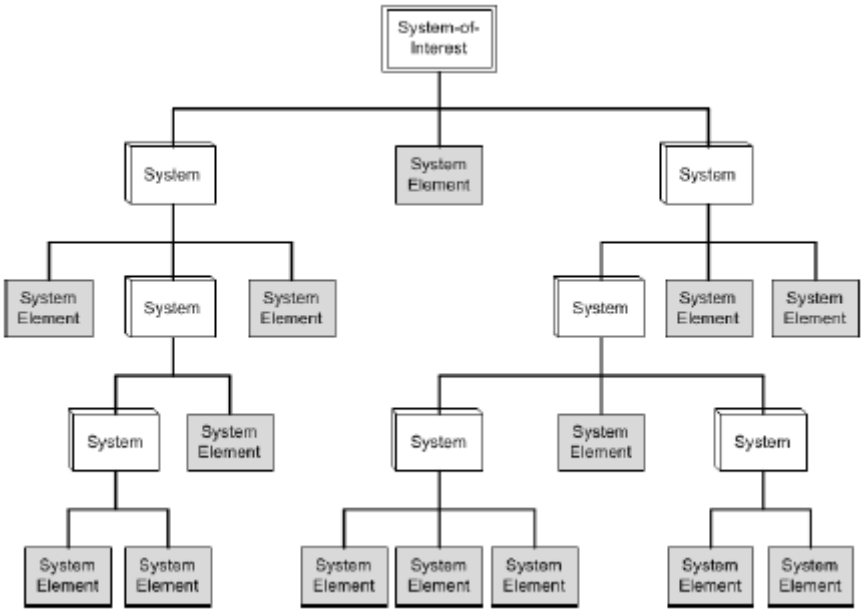
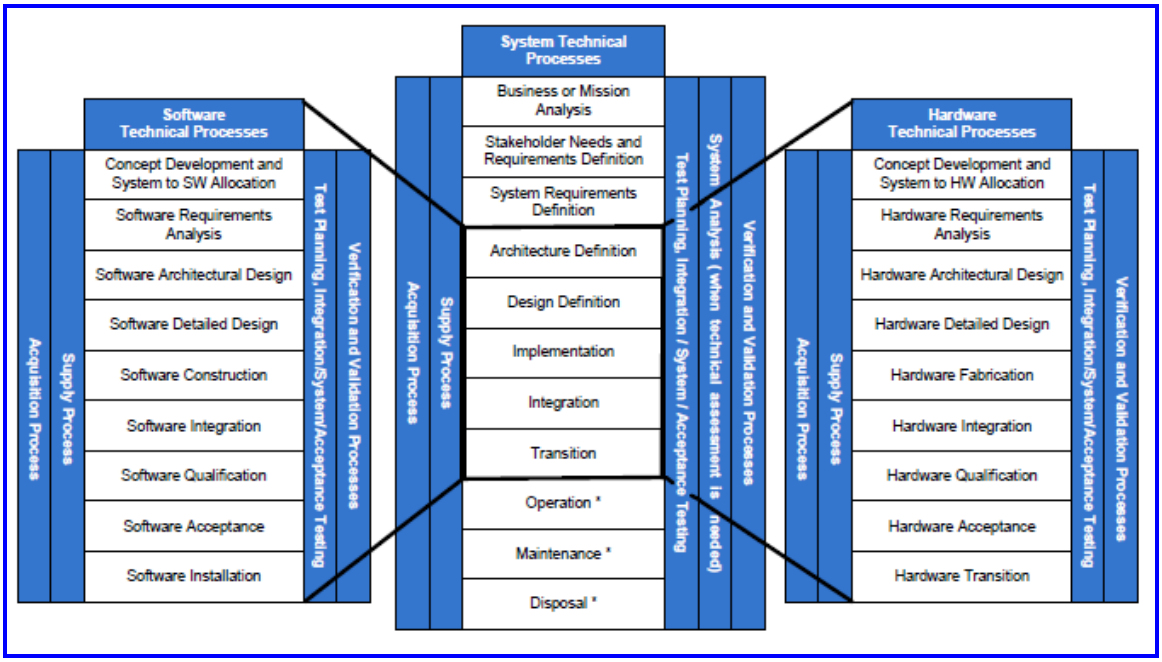



**Figure 4—Example system-of-interest structure**

The Verification process and the Validation process are two processes within the Technical processes group of the System Life Cycle processes defined in ISO/IEC/IEEE 15288:~~2008~~2015(E) [B16]. System V&V as described in this V&V standard is a conforming instance of the Verification and Validation processes in ISO/IEC/IEEE 15288:~~2008~~2015(E) [B16] (i.e., conducting system V&V as described in this V&V standard enables the V&V practitioner to claim full conformance with those two System Life Cycle processes, although other approaches may also be in conformance). In a similar fashion, software V&V as described in this V&V standard is a conforming instance of the Software Verification and Software Validation processes within the Software Support processes group of the Life Cycle processes defined in ISO/IEC 12207:2008 [B11].

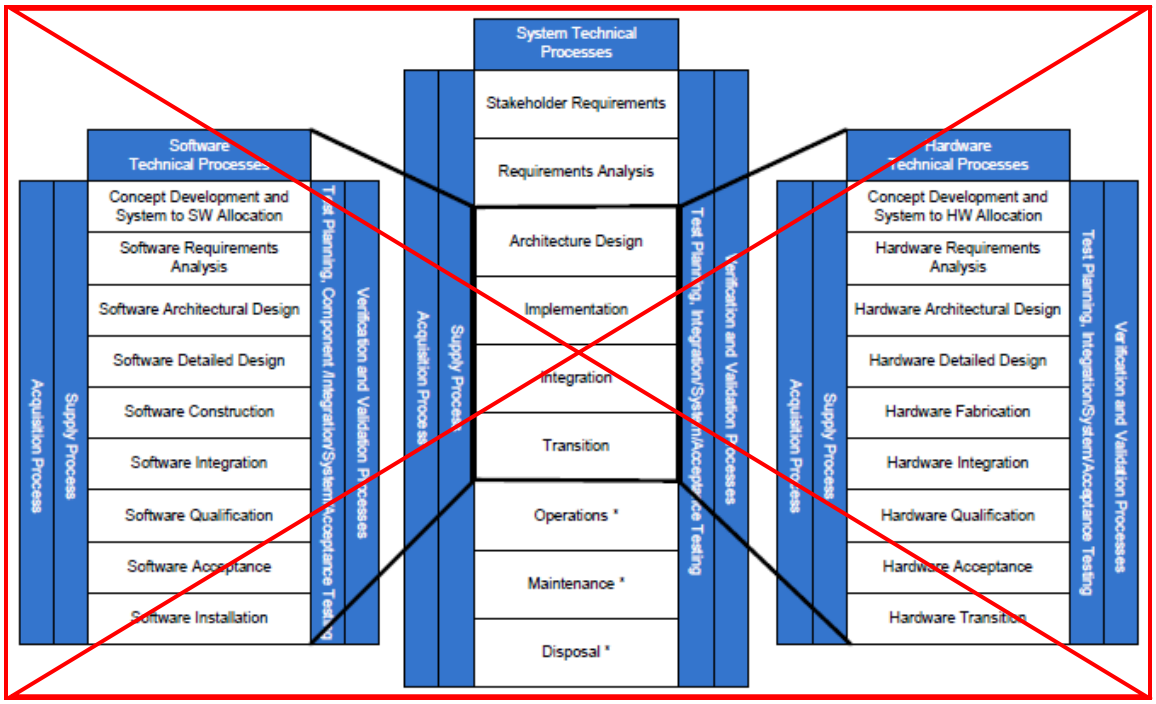
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The purpose of the system Implementation process is to produce a specified system element implemented as a software and hardware product or service. Within the system Implementation process, each software and hardware element is developed using the full software or hardware life cycle (requirements, design, implementation/construction, integration, and test). This concept is reflected in Figure 5, which also illustrates that the Technical processes for software and hardware overlap with the system Architecture Definition, Design ~~Process~~ Definition, System Analysis, Integration, and ~~the System~~ Transition processes. At the system element level, the implementation will be realized by the Software ~~Implementation~~ Construction process (described in Clause 9) or the Hardware Fabrication process (described in Clause 10).




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NOTE 1—The layout of the processes is not intended to specify an ordering of processes. V&V activities may be applied to any life cycle process.

NOTE 2—The ~~Operations~~ Operation, Maintenance, and Disposal processes within the System Technical processes are marked with an asterisk (*) to indicate that there are Software and Hardware V&V activities and tasks that support these System Technical processes but are not shown in Figure 5.

NOTE 3—Management of V&V activity is concurrent with all V&V activities.

NOTE 4—The task description, inputs, and outputs of all V&V tasks are included in Table 1a through Table 1d.

## Figure 5 —Relationship of system, software, and hardware processes

~~The following cross-reference~~ Figure 6 maps the V&V activities to those processes for which this V&V standard calls out specific activities and tasks.

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| V&V activity<br>IEEE 1012 | System processes<br>(ISO/IEC/IEEE 15288:2015(E) [B16]) | Software processes<br>(ISO/IEC 12207:2008 [B11]) | Hardware processes<br>(NOTE 4) |
|---|---|---|---|
| V&V Management | Verification, Validation | Software Verification, Software Validation | |
| Acquisition Support V&V | Acquisition | Acquisition | Acquisition |
| Supply Planning V&V | Supply | Supply | Supply |
| Project Planning V&V | Project Planning | Project Planning | Project Planning |
| Configuration Management V&V | Configuration Management | Software Configuration Management | Hardware Configuration Management |
| Business or Mission Analysis V&V | Business or Mission Analysis | | |
| Stakeholder Needs and Requirements Definition V&V | Stakeholder Needs and Requirements Definition | Stakeholder Requirements Definition | Stakeholders Requirements Definition |
| System Requirements Definition V&V | System Requirements Definition | System Requirements Analysis | System Requirements Analysis |
| Architecture Definition V&V | Architecture Definition | | |
| Design Definition V&V | Design Definition | | |
| System Analysis V&V | System Analysis | | |
| Implementation V&V<br>Software/Hardware V&V Activities<br>Software/Hardware Concept V&V<br>Software/Hardware Requirements Analysis V&V<br>Software/Hardware Design V&V<br>Software Construction/Hardware Fabrication V&V<br>Software/Hardware Integration V&V<br>Software/Hardware Qualification Testing V&V<br>Software/Hardware Acceptance Testing V&V | Implementation | Software Implementation | Hardware Implementation |
| Integration V&V | Integration | Support System Integration | Support System Integration |
| All verification activities of the IEEE 1012 life cycle | Verification | Software Verification | Hardware Verification |
| Transition V&V<br>Software Installation and Checkout V&V<br>Hardware Transition V&V | Transition | Software Installation | Hardware Transition |
| All validation activities of the IEEE 1012 life cycle | Validation | Software Validation | Hardware Validation |
| Operation V&V<br>Software Operation V&V<br>Hardware Operation V&V | Operation | Software Operation | Hardware Operation |
| Maintenance V&V<br>Software Maintenance V&V<br>Hardware Maintenance V&V | Maintenance | Software Maintenance | Hardware Maintenance |
| Disposal V&V<br>Software Disposal V&V<br>Hardware Disposal V&V | Disposal | Software Disposal | Hardware Disposal |

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| V&V Activity IEEE 1012 | System Processes (ISO/IEC 15288:2008 [B16]) | Software Processes (ISO/IEC 12207:2008 [B11]) | Hardware Processes (NOTE 3) |
|---|---|---|---|
| Management of V&V | Not specified | Not specified | Not specified |
| Acquisition Support V&V | Acquisition Process | Acquisition Process | Acquisition |
| Supply Planning V&V | Supply Process | Supply Process | Supply |
| Project Planning V&V | Project Planning Process | Project Planning Process | Project Planning Process |
| Configuration Management V&V | Configuration Management Process | Software Configuration Management Process | Hardware Configuration Management |
| System Stakeholder Requirements Definition V&V | Stakeholder Requirements Definition Process | Stakeholder Requirements Definition Process | Stakeholders Requirements Definition Process |
| System Requirements Analysis V&V | System Requirements Analysis Process | System Requirements Analysis Process | System Requirements Analysis Process |
| System Architecture Design V&V<br>Software Concept V&V<br>Hardware Concept V&V | System Architectural Design Process | System Architectural Design Process | System Architectural Design Process |
| System Implementation V&V<br>Software/Hardware V&V Activities<br>— Concept V&V<br>— Requirements V&V<br>— Design V&V<br>— Implementation/Fabrication V&V<br>— Integration Test V&V<br>— Qualification Test V&V<br>— Acceptance Test V&V | System Implementation Process | Software Requirements Analysis Process<br>Software Architectural Design Process<br>Software Detailed Design Process<br>Software Construction Process<br>Software Integration Process<br>Software Qualification Testing Process | Hardware Requirements Analysis Process<br>Hardware Architectural Design Process<br>Hardware Fabrication Process<br>Hardware Test Process<br>Hardware Integration Test Process<br>Hardware Qualification Test Process |
| System Integration V&V | System Integration Process | Support System Integration Process | Support System Integration Process |
| All verification activities of the IEEE 1012 life cycle | System Verification Process | Software Verification Process | Hardware Verification Process |
| System Transition V&V<br>Software Installation and Checkout V&V (Transition)<br>Hardware Transition V&V | System Transition Process | Software Installation Process | Hardware Transition Process |
| All validation activities of the IEEE 1012 life cycle | System Validation Process | Software Validation Process | Hardware Validation Process |
| System Operation V&V<br>Software Operation V&V<br>Hardware Operation V&V | System Operation Process | Software Operation Process | Hardware Operation Process |
| System Maintenance V&V<br>Software Maintenance V&V<br>Hardware Maintenance V&V | System Maintenance Process | Software Maintenance Process | Hardware Maintenance Process |
| System Disposal V&V<br>Software Disposal V&V<br>Hardware Disposal V&V | System Disposal Process | Software Disposal Process | Hardware Disposal Process |

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NOTE 1—Not all life cycle processes from ISO/IEC/IEEE 15288:~~2008~~2015(E) [B16] and ISO/IEC 12207:2008 [B11] have V&V tasks specified in this standard. The V&V processes also interact with the other system and software processes not included in this table, such as providing inputs and receiving outputs that are used in the V&V effort.

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NOTE 2—V&V practitioners provide feedback on noted deficiencies or areas for improvement ~~(e.g., a life cycle model that does not produce a product needed to perform V&V tasks and activities).~~

~~NOTE 3—There are no applicable IEEE or International Standards for hardware lifecycle processes.~~

NOTE 3—Each ~~IEEE~~ ISO/IEC 12207 software specific process is a specialization of its corresponding process in ISO/IEC~~-~~/IEEE

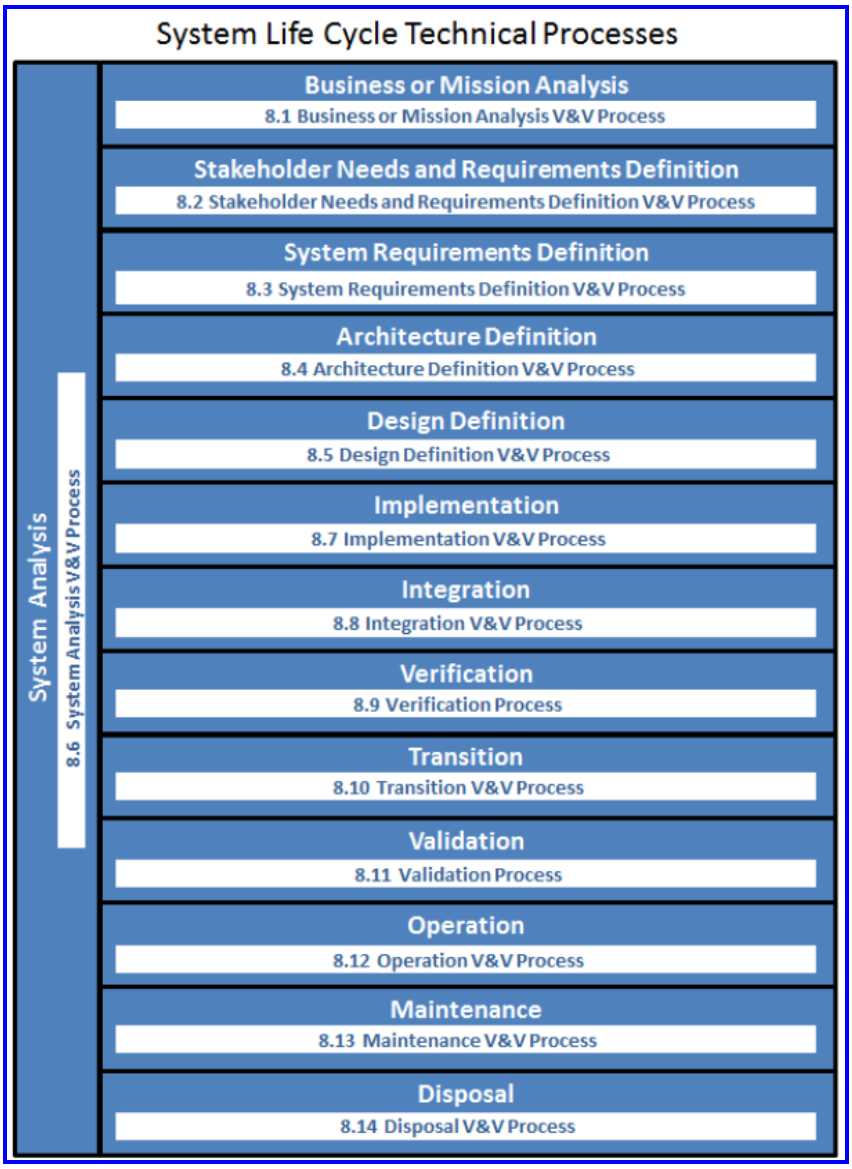
15288:~~2008~~2015(E) [B16]. Users may consider claiming conformance to the ISO/IEC/IEEE 15288 process rather than the ~~IEEE~~ ISO/IEC 12207 process.

NOTE 4—Each hardware process that corresponds to an ~~IEEE~~ ISO/IEC 12207 software specific process is a specialization of its corresponding process in ISO/IEC/IEEE 15288.

## Figure 6 —Mapping of V&V activities to system, software, and hardware processes

The life cycle model, including selected processes, defines the evolution of the system, software, and hardware elements throughout life cycle stages. To achieve the verification and validation processes outcomes for each life cycle process, this standard is organized by life cycle process, and within each life cycle process the verification and validation activities and tasks for that life cycle process are identified. Figure 7 illustrates that organization for system life cycle processes. The listing of all verification and validation activities and tasks to specific system, software, or hardware life cycle processes are depicted in Figure 1a (Common V&V), Figure 1b (System V&V), Figure 1c (Software V&V), and Figure 1d (Hardware V&V). The mappings of ISO/IEC/IEEE 15288 processes and activities with IEEE Standard 1012 V&V activities and of ISO/IEC 12207 processes and activities with IEEE Standard 1012 V&V activities are shown in Annex A.

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NOTE—Each system, software, and hardware life cycle process defines the evolution of the system, software, and hardware elements throughout life cycle stages. To achieve the verification and validation process outcomes for each life cycle process, the standard is organized by life cycle process and within each life cycle process the verification and validation activities and tasks are identified. This figure illustrates that organization for system life cycle processes.

**Figure 7 —V&V processes align with other technical life cycle processes**

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## 5. Integrity levels

Integrity level determination ~~quantifies~~ establishes the importance of the system to the user and acquirer based on complexity, criticality, risk, safety level, security level, desired performance, reliability, or other system-unique characteristics ~~based on the importance of the system to the user and acquirer~~. Integrity levels are used to determine the V&V tasks, activities, rigor, and the level of intensity of the V&V to be performed.

The following is a result of the integrity level determination:

a) An integrity schema is defined.

b) Integrity levels for all system entities are assigned.

c) Integrity assignments are used to determine V&V activities and tasks using Table 2a through Table 2d.

d) A basis is established to review and revalidate the integrity levels throughout the V&V effort.

The degree of rigor and intensity in performing and documenting ~~the task~~ any V&V task associated with a system, software, or hardware work product shall be commensurate with the integrity level. As the integrity level decreases, so does the required scope, intensity, and degree of rigor associated with the V&V task. For example, ~~a hazard analysis performed~~ system integration testing for integrity level 4 ~~software might~~ systems must be ~~formally documented and consider failures at~~ performed independently by the ~~module level; a hazard analysis~~ V&V organization, whereas for an integrity level 3 ~~software may consider~~ system the V&V organization need only ~~significant software failures and be documented informally as part of the design~~ review ~~process~~ the results from systems integration testing.

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Use the integrity schema established for the system, software, or hardware, if one exists. An integrity level ~~scheme~~ schema shall be specified if one is not already defined. Establish gradations of criticality ~~and~~ or integrity to assure complete ~~partitioning~~ coverage of the ~~potential effects space~~ risk classes from ~~"~~possible system behaviors from no ~~effect"~~ risk to ~~"~~worst case risk.~~"~~ The integrity levels established for a system element by the developer should result from agreements among the acquirer and the supplier and remain consistent with ~~the~~ regulatory requirements.

This standard was developed with a four-level schema to explain the minimum normative V&V requirements. Other integrity schemas are acceptable. For any selected integrity schema, the selected integrity levels shall be mapped into this standard's four-level schema (and associated V&V criteria) to demonstrate that the minimum V&V requirements are satisfied. Because V&V is applied recursively from the system of interest down to each of the subsystems or elements at the next level, it is not necessary to use the same integrity level schema for all the subsystems or elements of the system of interest.

NOTE—A process for developing an integrity schema can be found in ISO/IEC 15026~~-~~:2011 [~~B12~~ B14].

The V&V criticality analysis task is used to classify the integrity level of every system (e.g., subsystem) or element in the system of interest. Integrity levels are assigned to requirements, functions, groups of functions, components, or subsystems. The integrity levels characterize and quantify the potential for undesirable effects and consequences resulting from integrity lapse, unintended effects, failure mode effects, and unverified performance effects. The characteristics that determine integrity level vary depending on the intended application and use of the system.

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Integrity level assignments shall be applied recursively to the components of each system element. As the development stages progressively decompose the solution into more details, the criticality analysis performed at each development stage assigns integrity levels to each function. By recursively assigning integrity levels to individual solution parts, greater rigor and intensity is applied to the higher integrity level elements. Progressive decomposition for criticality analysis and assignment of integrity levels shall be applied to segregate parts that warrant high-integrity V&V tasks from those parts that do not. This recursive assignment of integrity levels to solution parts keeps the V&V effort focused on the high-integrity elements, making the V&V effort cost efficient and technically effective.

From the system perspective, during integrity level analysis, software and hardware are treated as functional elements. Subsystem components cannot have a higher criticality or integrity level than the parent subsystem. The system shall be assigned the same integrity level as the highest level assigned to any individual element. The integrity level assigned to the parent shall be as high as the highest integrity level of the system elements. The system elements can have the integrity level of the system parent or lower depending on the critical functions it supports.

The integrity level assigned to reused, COTS, and government off-the-shelf (GOTS) components shall be in accordance with the integrity level ~~scheme~~ schema adopted for the system element into which COTS or GOTS may be integrated for the project. The reused COTS or GOTS component shall be evaluated for use in the context of its application. The design, development, procedural, and technology features implemented in the system can raise or lower the assigned integrity levels.

The V&V criticality analysis task is used to classify the integrity level of enabling systems. The tools that insert or translate code (e.g., optimizing compilers and auto-code generators) shall be assigned the same integrity level as the integrity level assigned to the software element that the tool affects. If the tool cannot be verified and validated, then the output of the tool shall be subject to the same level of V&V as the software element.

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