

# IEEE Standard VHDL Synthesis Packages

Sponsor

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**Abstract:** The current interpretation of common logic values and the association of numeric values to specific VHDL array types is described. This standard provides semantic for the VHDL synthesis domain, and enables formal verification and simulation acceleration in the VHDL based design. The standard interpretations are provided for values of standard logic types defined by IEEE Std 1164-1993, and of the BIT and BOOLEAN types defined in IEEE Std 1076-1993. The numeric types SIGNED and UNSIGNED and their associated operators define integer and natural number arithmetic for arrays of common logic values. Two's complement and binary encoding techniques are used. The numeric semantic is conveyed by two VHDL packages. This standard also contains any allowable modifications.

**Keywords:** interpretations, metalogical values, numeric VHDL vector types, signed, synthesis, unsigned

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# Introduction

(This introduction is not a part of IEEE Std 1076.3-1997, IEEE Standard VHDL Synthesis Packages.)

This standard, IEEE Std 1076.3-1997, supports the synthesis and verification of hardware designs, by defining vector types for representing signed or unsigned integer values and providing standard interpretations of widely used scalar VHDL values.

The standardization activity started during the development of IEEE Std 1076-1993, IEEE Standard VHDL Language Reference Manual, to address a number of issues in the synthesis area that could not be adequately addressed within the scope of the main 1076 project.

The initial Synthesis Special Interest Group (SSIG) analyzed a wide range of requirements and grouped them in four categories:

- a) Standard Interpretations of IEEE Std 1164-1993 values for synthesis
- b) Numeric types for synthesis
- c) Special attribute semantics
- d) Constraint specification

Consensus was reached only on solutions presented for categories a) and b). The large working group then commissioned a Pilot Team to drive the standardization effort. The three standardization chapters (North America, Europe, and Asia-Pacific) were all represented in the Pilot Team. The active members of the Pilot Team were the following:

**Alex N. Zamfirescu, Chair**

|                    |                                          |
|--------------------|------------------------------------------|
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| James H. Vellenga  | Documentation and Pilot Team Co-Chair    |
| Rob Dekker         |                                          |
| Bob Flatt          |                                          |
| Chris Kingsley     |                                          |

The hard work and professionalism of the Pilot Team members contributed significantly to the final result. Although the Working Group met regularly and voted on all major issues, the Pilot Team also extensively used electronic mail, a common repository, and several World Wide Web pages to accelerate the completely voluntary standardization process of the IEEE. A simple VHDL test suite (not part of the standard) that exercises and verifies the packages was also produced during standardization. A set of axioms and formal properties involving standard operators has been formally proven.

Individuals from many organizations participated in the development of IEEE Std 1076.3-1997. In addition to members of the Pilot Team, the following individuals attended meetings of the Synthesis Working Group:

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The following persons were on the balloting committee:

|                       |                         |                        |
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# IEEE Standard VHDL Synthesis Packages

## 1. Overview

### 1.1 Scope

This standard defines standard practices for synthesizing binary digital electronic circuits from VHDL source code. It includes the following:

- a) The hardware interpretation of values belonging to the BIT and BOOLEAN types defined by IEEE Std 1076-1993<sup>1</sup> and to the STD\_ULOGIC type defined by IEEE Std 1164-1993.
- b) A function (STD\_MATCH) that provides “don’t care” or “wild card” testing of values based on the STD\_ULOGIC type.
- c) Standard functions for representing sensitivity to the edge of a signal.
- d) Two packages that define vector types for representing signed and unsigned arithmetic values, and that define arithmetic, shift, and type conversion operations on those types.

This standard is designed for use with IEEE Std 1076-1993. Modifications that may be made to the packages for use with the previous edition, IEEE Std 1076-1987, are described in 7.2.

### 1.2 Terminology

The word *shall* indicates mandatory requirements strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*). The word *should* is used to indicate that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (*should* equals *is recommended that*). The word *may* indicates a course of action permissible within the limits of the standard (*may* equals *is permitted*).

A synthesis tool is said to *accept* a VHDL construct if it allows that construct to be legal input; it is said to *interpret* the construct (or to provide an *interpretation* of the construct) by producing something that represents the construct. A synthesis tool is not required to provide an interpretation for every construct that it accepts, but only for those for which an interpretation is specified by this standard.

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<sup>1</sup>Information on references can be found in Clause 2.

## 1.3 Conventions

This standard uses the following conventions:

- a) The body of the text of this standard uses boldface to denote VHDL reserved words (such as **downto**) and upper case to denote all other VHDL identifiers (such as REVERSE\_RANGE or FOO).
- b) The text of the VHDL packages defined by this standard, as well as the text of VHDL examples and code fragments, is represented in a fixed-width font. All such text represents VHDL reserved words as lower case text and all other VHDL identifiers as upper case text.
- c) In the body of the text, italics denote words or phrases that are being defined by the paragraph in which they occur.
- d) VHDL code fragments not supported by this standard are denoted by an italic fixed-width font.

## 2. References

This standard shall be used in conjunction with the following publications. When the following standards are superseded by an approved revision, the revision shall apply.

IEEE Std 1076-1993, IEEE Standard VHDL Language Reference Manual (ANSI).<sup>2</sup>

IEEE Std 1164-1993, IEEE Standard Multivalued Logic System for VHDL Model Interoperability (Std\_logic\_1164) (ANSI).

## 3. Definitions

Terms used in this standard, but not defined in this clause, are assumed to be from IEEE Std 1076-1993 and IEEE Std 1164-1993.

**3.1 argument:** An expression occurring as the actual value in a function call or procedure call.

**3.2 arithmetic operation:** An operation for which the VHDL operator is +, -, \*, /, **mod**, **rem**, **abs**, or \*\*.

**3.3 assignment reference:** The occurrence of a literal or other expression as the waveform element of a signal assignment statement or as the right-hand side expression of a variable assignment statement.

**3.4 don't care value:** The enumeration literal '-' of the type STD\_ULOGIC defined by IEEE Std 1164-1993.

**3.5 equality relation:** A VHDL relational expression in which the relational operator is =.

**3.6 high-impedance value:** The enumeration literal 'Z' of the type STD\_ULOGIC defined by IEEE Std 1164-1993.

**3.7 inequality relation:** A VHDL relational expression in which the relational operator is /=.

**3.8 logical operation:** An operation for which the VHDL operator is **and**, **or**, **nand**, **nor**, **xor**, **xnor**, or **not**.

**3.9 metalogical value:** One of the enumeration literals 'U', 'X', 'W', or '-' of the type STD\_ULOGIC defined by IEEE Std 1164-1993.

<sup>2</sup>IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.

**3.10 ordering relation:** A VHDL relational expression in which the relational operator is `<`, `<=`, `>`, or `>=`.

**3.11 shift operation:** An operation for which the VHDL operator is `sll`, `srl`, `sla`, `sra`, `rol`, or `ror`.

**3.12 standard logic type:** The type `STD_ULOGIC` defined by IEEE Std 1164-1993, or any type derived from it, including, in particular, one-dimensional arrays of `STD_ULOGIC` or of one of its subtypes.

**3.13 synthesis tool:** Any system, process, or tool that interprets VHDL source code as a description of an electronic circuit in accordance with the terms of this standard and derives an alternate description of that circuit.

**3.14 user:** A person, system, process, or tool that generates the VHDL source code that a synthesis tool processes.

**3.15 vector:** A one-dimensional array.

**3.16 well-defined:** Containing no metalogical or high-impedance element values.

## 4. Interpretation of the standard logic types

This clause defines how a synthesis tool shall interpret values of the standard logic types defined by IEEE Std 1164-1993 and of the `BIT` and `BOOLEAN` types defined by IEEE Std 1076-1993. Simulation tools, however, shall continue to interpret these values according to the standards in which the values are defined.

### 4.1 The `STD_LOGIC_1164` values

IEEE Std 1164-1993 defines the standard logic type:

```
type STD_ULOGIC is ( 'U', -- Uninitialized
                    'X', -- Forcing Unknown
                    '0', -- Forcing 0
                    '1', -- Forcing 1
                    'Z', -- High Impedance
                    'W', -- Weak Unknown
                    'L', -- Weak 0
                    'H', -- Weak 1
                    '-' -- Don't care
                    );
```

The *logical values* '1', 'H', '0', and 'L' are interpreted as representing one of two logic levels, where each logic level represents one of two distinct voltage ranges in the circuit to be synthesized.

IEEE Std 1164-1993 also defines a resolution function named `RESOLVED` and a subtype `STD_LOGIC` that is derived from `STD_ULOGIC` by using `RESOLVED`. The resolution function `RESOLVED` treats the values '0' and '1' as *forcing values* that override the *weak values* 'L' and 'H' when multiple sources drive the same signal.

The values 'U', 'X', 'W', and '-' are *metalogical values*; they define the behavior of the model itself rather than the behavior of the hardware being synthesized. The value 'U' represents the value of an object before it is explicitly assigned a value during simulation; the values 'X' and 'W' represent forcing and weak values, respectively, for which the model is not able to distinguish between logic levels.

The value '-' is also called the *don't care value*. This standard treats it in the same way as the other metalogical values except when it is furnished as an argument to the `STD_MATCH` functions in the

IEEE.NUMERIC\_STD package. The STD\_MATCH functions use ‘-’ to implement a “match all” or “wild card” matching.

The value ‘Z’ is called the *high-impedance value*, and represents the condition of a signal source when that source makes no effective contribution to the resolved value of the signal.

## 4.2 Static constant values

Wherever a synthesis tool accepts a reference to a locally static or globally static named constant, it shall treat that constant as the equivalent of the associated static expression.

## 4.3 Interpretation of logic values

This subclause describes the interpretations of logic values occurring as literals (or in literals) after a synthesis tool has replaced named constants by their corresponding values.

### 4.3.1 Interpretation of the forcing and weak values (‘0’, ‘1’, ‘L’, ‘H’, FALSE, TRUE)

A synthesis tool shall interpret the following values as representing a logic value 0:

- The BIT value ‘0’.
- The BOOLEAN value FALSE.
- The STD\_ULOGIC values ‘0’ and ‘L’.

It shall interpret the following values as representing a logic value 1:

- The BIT value ‘1’.
- The BOOLEAN value TRUE.
- The STD\_ULOGIC value ‘1’ and ‘H’.

This standard makes no restriction as to the interpretation of the relative strength of values.

### 4.3.2 Interpretation of the metalogical values (‘U’, ‘W’, ‘X’, ‘-’)

#### 4.3.2.1 Metalogical values in relational expressions

If the VHDL source code includes an equality relation (=) for which one operand is a static metalogical value and for which the other operand is not a static value, a synthesis tool shall interpret the equality relation as equivalent to the BOOLEAN value FALSE. If one operand of an equality relation is a vector, and one element of that vector is a static metalogical value, a synthesis tool shall interpret the entire equality relation as equivalent to the BOOLEAN value FALSE.

A synthesis tool shall interpret an inequality relation (/=) for which one operand is or contains a static metalogical value, and for which the other operand is not a static value, as equivalent to the BOOLEAN value TRUE.

A synthesis tool shall treat an ordering relation for which at least one operand is or contains a static metalogical value as an error.

#### 4.3.2.2 Metalogical values as a choice in a case statement

If a metalogical value occurs as a choice, or as an element of a choice, in a case statement that is interpreted by a synthesis tool, the synthesis tool shall interpret the choice as one that can never occur. That is, the inter-

pretation that is generated is not required to contain any constructs corresponding to the presence or absence of the sequence of statements associated with the choice.

Whenever a synthesis tool interprets a case statement alternative that associates multiple choices with a single sequence of statements, it shall produce an interpretation consistent with associating the sequence of statements with each choice individually.

Whenever a synthesis tool interprets a selected signal assignment statement, it shall interpret the selected signal assignment statement as if it were the case statement in the equivalent process as defined by IEEE Std 1076-1993.

#### **4.3.2.3 Metalogical values in logical, arithmetic, and shift operations**

When a static metalogical value occurs as all of, or one element of, an operand to a logical, arithmetic, or shift operation, and when the other operand to the operation is not a static value, a synthesis tool shall treat the operation as an error.

#### **4.3.2.4 Metalogical values in concatenate operations**

If a static metalogical value occurs as all of, or as one element of, an operand to the concatenate (&) operator, a synthesis tool shall treat it as if it had occurred as the corresponding element of the expression formed by the concatenate operation.

#### **4.3.2.5 Metalogical values in type conversion and sign-extension functions**

If a static metalogical value occurs as all of, or as one element of, the value argument to a type conversion or sign-extension function, a synthesis tool shall treat it as if it had occurred as the corresponding element of the expression formed by the function call.

#### **4.3.2.6 Metalogical values used in assignment references**

A synthesis tool shall accept a static metalogical value used as all of, or as one element of, an assignment reference, but is not required to provide any particular interpretation of that metalogical value.

#### **4.3.3 Interpretation of the high-impedance value ('Z')**

If the static value 'Z' occurs as an assignment reference in a signal assignment statement, a synthesis tool shall interpret the assignment as implying the equivalent of a three-state buffer that is disabled when the conditions under which the assignment occurs is true. The output of the three-state buffer is the target of the assignment. The input of the three-state buffer is the logic network that represents the value of the target apart from any assignments to 'Z'.

If the 'Z' occurs as one or more elements of an assignment reference in a signal assignment statement, a synthesis tool shall interpret each such occurrence as implying the equivalent of a three-state buffer in the manner defined by the preceding paragraph.

This standard does not specify an interpretation when a static value 'Z' occurs as all of, or one bit of, an assignment reference in a variable assignment statement.

Whenever a static high-impedance value occurs in any context other than an assignment reference, a synthesis tool shall treat it as equivalent to a static metalogical value.

NOTE—A signal assignment statement that assigns one or more bits of a signal to 'Z' unconditionally implies the equivalent of a three-state buffer that is always disabled. A synthesis tool may choose to ignore such assignments.

## 5. The STD\_MATCH function

The NUMERIC\_STD package defined by this standard defines functions named STD\_MATCH to provide wild card matching for the don't care value. Whenever the STD\_MATCH function compares two arguments which are STD\_ULOGIC values, it returns TRUE if and only if:

- Both values are well-defined and the values are the same, or
- One value is '0' and the other is 'L', or
- One value is '1' and the other is 'H', or
- At least one of the values is the don't care value ('-').

Whenever the STD\_MATCH function compares two arguments which are vectors whose elements belong to the STD\_ULOGIC type or to one of its subtypes, it returns TRUE if and only if:

- a) The operands have the same length, and
- b) STD\_MATCH applied to each pair of matching elements returns TRUE.

When one of the arguments to the STD\_MATCH function is a static value and the other is not, a synthesis tool shall interpret the call to the STD\_MATCH function as equivalent to an equality test on matching elements of the arguments, excepting those elements of the static value which are equal to '-'.

NOTE—If any argument value passed to STD\_MATCH is or contains a metalogical or high-impedance value other than '-', the function returns FALSE.

## 6. Signal edge detection

Wherever a synthesis tool interprets a particular expression as the edge of a signal, it shall also interpret the function RISING\_EDGE as representing a rising edge and the function FALLING\_EDGE as representing a falling edge, where RISING\_EDGE and FALLING\_EDGE are the functions declared either by the package STD\_LOGIC\_1164 of IEEE Std 1164-1993 or by the NUMERIC\_BIT package of this standard.

## 7. Standard arithmetic packages

Two VHDL packages are defined by this standard. The NUMERIC\_BIT package is based on the VHDL type BIT, while the second package, NUMERIC\_STD, is based on the subtype STD\_LOGIC of the type STD\_ULOGIC. Simulations based on the subprograms of the NUMERIC\_BIT package ordinarily require less execution time, because the subprograms do not have to deal with operands containing metalogical or high-impedance values. Use of the subprograms of the NUMERIC\_STD package allow simulation to detect the propagation or generation of metalogical values.

Each package defines a vector type named SIGNED and a vector type named UNSIGNED. The type UNSIGNED represents an unsigned binary integer with the most significant bit on the left, while the type SIGNED represents a two's-complement binary integer with the most significant bit on the left. In particular, a one-element SIGNED vector represents the integer values -1 and 0.

The two packages are mutually incompatible, and only one shall be used in any given design unit. To facilitate changing from one package to the other, most of the subprograms declared in one package are also declared for corresponding arguments in the other. Exceptions are when:

- a) The NUMERIC\_BIT package declares the functions RISING\_EDGE and FALLING\_EDGE; the corresponding functions for STD\_ULOGIC are declared by the STD\_LOGIC\_1164 package.

- b) The NUMERIC\_STD package declares the STD\_MATCH functions, which give special treatment to the don't care value, whereas the BIT-based types of the NUMERIC\_BIT package have no don't care values.
- c) The NUMERIC\_STD package declares the TO\_01 functions, which may be applied to SIGNED and UNSIGNED vector values, and which map the element values of the vectors to the STD\_ULOGIC values '0' and '1' and to a third value representing metalogical or high-impedance values.

Table 1 shows the order of the function declarations within the package declarations.

**Table 1—Order of functions within packages**

| Function Id(s)                                                                        | NUMERIC_BIT                                                                                     | NUMERIC_STD                                                                                     |
|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|
| A.1<br>A.2                                                                            | <b>abs</b><br>unary –                                                                           | <b>abs</b><br>unary –                                                                           |
| A.3–A.8<br>A.9–A.14<br>A.15–A.20<br>A.21–A.26<br>A.27–A.32<br>A.33–A.38               | binary +<br>binary –<br>*<br>/<br><b>rem</b><br><b>mod</b>                                      | binary +<br>binary –<br>*<br>/<br><b>rem</b><br><b>mod</b>                                      |
| C.1–C.6<br>C.7–C.12<br>C.13–C.18<br>C.19–C.24<br>C.25–C.30<br>C.31–C.36               | ><br><<br><=<br>>=<br>=<br>/=                                                                   | ><br><<br><=<br>>=<br>=<br>/=                                                                   |
| S.1, S.3<br>S.2, S.4<br>S.5, S.7<br>S.6, S.8                                          | SHIFT_LEFT<br>SHIFT_RIGHT<br>ROTATE_LEFT<br>ROTATE_RIGHT                                        | SHIFT_LEFT<br>SHIFT_RIGHT<br>ROTATE_LEFT<br>ROTATE_RIGHT                                        |
| S.9, S.10<br>S.11, S.12<br>S.13, S.14<br>S.15, S.16                                   | (predefined in VHDL)                                                                            | <b>sll</b><br><b>srl</b><br><b>rol</b><br><b>ror</b>                                            |
| R.1–R.2                                                                               | RESIZE                                                                                          | RESIZE                                                                                          |
| D.1–2<br>D.3<br>D.4                                                                   | TO_INTEGER<br>TO_UNSIGNED<br>TO_SIGNED                                                          | TO_INTEGER<br>TO_UNSIGNED<br>TO_SIGNED                                                          |
| E.1<br>E.2                                                                            | RISING_EDGE<br>FALLING_EDGE                                                                     | (defined by the<br>STD_LOGIC_1164<br>package)                                                   |
| L.1, L.8<br>L.2, L.9<br>L.3, L.10<br>L.4, L.11<br>L.5, L.12<br>L.6, L.13<br>L.7, L.14 | <b>not</b><br><b>and</b><br><b>or</b><br><b>nand</b><br><b>nor</b><br><b>xor</b><br><b>xnor</b> | <b>not</b><br><b>and</b><br><b>or</b><br><b>nand</b><br><b>nor</b><br><b>xor</b><br><b>xnor</b> |
| M.1–M.5                                                                               |                                                                                                 | STD_MATCH                                                                                       |
| T.1–T.2                                                                               |                                                                                                 | TO_01                                                                                           |

If a null array is furnished as an input argument to any subprogram declared by NUMERIC\_BIT or NUMERIC\_STD, a synthesis tool shall treat it as an error.

All vector return values that are not null array values are normalized so that the direction of the index range is **downto** and the right bound is 0. A vector return value that is a null array has the index range “0 **downto** 1”.

The package declarations use the following format to declare each function:

```
-- Id: <id_nr>
function <designator> (<formal_parameter_list>) return <type_mark>;
-- Result Subtype: <subtype_indication>
-- Result: <description of function>
```

The elements of this format have the following meanings:

<id\_nr>

A unique identifier of the form *letter.number*. A corresponding identifier appears at the beginning of the corresponding function body in the package body for the same package.

<designator>

The function designator as defined by IEEE Std 1076-1993.

<formal\_parameter\_list>

The formal parameter list for the function as defined by IEEE Std 1076-1993.

<type\_mark>

A type mark denoting the result subtype of the function as defined by IEEE Std 1076-1993.

<subtype\_indication>

The subtype of the value returned by the function. If the result subtype of the function denotes an unconstrained vector subtype, <subtype\_indication> also includes an index constraint defining the index range of the returned value in terms of sizes and values of the input parameters. <subtype\_indication> is syntactically a subtype indication as defined by IEEE Std 1076-1993.

<description of function>

An English language description of the operation performed by the function.

Both packages shall be analyzed into the library symbolically named IEEE.

## 7.1 Allowable modifications

Vendors of tools conforming to this standard shall not modify the package declarations for NUMERIC\_BIT or NUMERIC\_STD. However, a vendor may provide package bodies for either or both packages in which subprograms are rewritten for more efficient simulation or synthesis, provided that the behavior of the rewritten subprograms remains the same under simulation. The behavior of the original and rewritten subprograms are the same if, for any combination of input values, they return the same return values. The text of messages associated with assertions may differ in the rewritten subprogram.

The package bodies for both packages declare a constant named NO\_WARNING that has the value FALSE. A user may set NO\_WARNING to TRUE and reanalyze the package body to suppress warning messages generated by calls to the functions in these packages. For this reason:

- A tool vendor who rewrites the package body shall preserve the declaration of the NO\_WARNING constant to allow a user to suppress warnings by editing and reanalyzing the package body.
- A simulation tool vendor who provides a preanalyzed version of the package body should also provide a mechanism for suppressing warning messages generated by the package functions.

## 7.2 Compatibility with IEEE Std 1076-1987

The following functions from the NUMERIC\_STD package are compatible with IEEE Std 1076-1993 but not with the previous edition, IEEE Std 1076-1987:

- a) "xnor"
- b) "sll"
- c) "srl"
- d) "rol"
- e) "ror"

To use these functions with a VHDL-based system that has not yet been upgraded to be compatible with IEEE Std 1076-1993, a user or vendor may comment out the subprogram declarations and subprogram bodies.

In addition, IEEE Std 1076-1993 supports a character set that includes the copyright symbol (©). However, IEEE Std 1076-1987 does not support this same character set. Therefore, in order to use the NUMERIC\_BIT and NUMERIC\_STD packages with a system that has not yet been upgraded to be compatible with IEEE Std 1076-1993, a user or vendor may replace the copyright symbol within the sources of those packages by a left parenthesis, a lowercase "c," and a right parenthesis.

## 7.3 The package texts

The texts of the NUMERIC\_BIT and NUMERIC\_STD packages (both package declarations and package bodies) are on the diskette that is included with this standard. Those texts are an official part of this standard. For the convenience of users, the package declarations are also included in the printed form of the standard. Please consult the diskette for the contents of the package bodies.