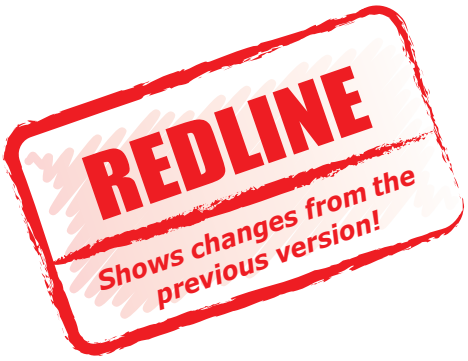
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IEEE Standard for Test Access Port and Boundary-Scan Architecture

IEEE Computer Society

Sponsored by the
Test Technology Standards Committee



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USA

13 May 2013

IEEE Std 1149.1™-2013
(Revision of
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Approved 6 February 2013

IEEE-SA Standards Board

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Abstract: Circuitry that may be built into an integrated circuit to assist in the test, maintenance and support of assembled printed circuit boards and the test of internal circuits is defined. The circuitry includes a standard interface through which instructions and test data are communicated. A set of test features is defined, including a boundary-scan register, such that the component is able to respond to a minimum set of instructions designed to assist with testing of assembled printed circuit boards. Also, a language is defined that allows rigorous structural description of the component-specific aspects of such testability features, and a second language is defined that allows rigorous procedural description of how the testability features may be used.
Keywords: boundary scan, boundary-scan architecture, Boundary-Scan Description Language (BSDL), boundary-scan register, circuit boards, circuitry, IEEE 1149.1™, integrated circuit, printed circuit boards, Procedural Description Language (PDL), test, test access port (TAP), very high speed integrated circuit (VHSIC), VHSIC Hardware Description Language (VHDL)

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Introduction

This introduction is not part of IEEE Std 1149.1-2013, IEEE Standard for Test Access Port and Boundary-Scan Architecture.

This standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. The facilities defined by the standard seek to provide a solution to the problem of testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques. They also provide a means of accessing and controlling design-for-test features built into the digital integrated circuits themselves. Such features might, for example, include internal scan paths and self-test functions as well as other features intended to support service applications in the assembled product.

In addition, two languages are provided to describe both the structure of the test logic and the procedures needed to use the test logic.

History of the development of this standard

The process of developing this standard began in 1985 when the Joint European Test Action Group (JETAG) was formed in Europe. During 1986, this group expanded to include members from both Europe and North America and, as a result, was renamed the Joint Test Action Group (JTAG). Between 1986 and 1988, the JTAG Technical Subcommittee developed and published a series of proposals for a standardized form of boundary scan. In 1988, the last of these proposals, JTAG Version 2.0, was offered to the IEEE Testability Bus Standards Committee (P1149) for inclusion in the standard then under development. The Testability Bus Standards Committee accepted this approach. It decided that the JTAG proposal should become the basis of a standard within the Testability Bus family, with the result that the P1149.1 project was initiated. Following these decisions, the JTAG Technical Subcommittee became the core of the IEEE Working Group that developed this standard.

After the initial approval of this standard in February 1990 and its subsequent publication, the Working Group immediately began efforts to develop a supplement for the purpose of correction, clarification, and enhancement. This effort, spurred and guided by interaction between developers and users of the original standard, culminated in IEEE Std 1149.1a™-1993, which was approved in June 1993.

The major changes to this standard introduced by IEEE Std 1149.1a-1993 were as follows:

— The addition of two optional instructions, *CLAMP* and *HIGHZ*, which standardized the names and specifications of features often implemented as design-specific features.

— The addition of an optional facility to switch a component from a mode in which it complies to this standard into one in which it supports another design-for-test approach.

Furthermore, starting with a proposal made by Kenneth P. Parker and Stig Oresjo in 1990, an effort was undertaken to develop a language to describe components that conform to this standard. This effort concluded in the approval of IEEE Std 1149.1b™-1994 in September 1994.

The major change introduced to this standard by IEEE Std 1149.1b-1994 was the addition of Annex B, which defines the Boundary-Scan Description Language. All other changes were minor and were strictly for clarification.

The 2001 revision was primarily a housekeeping update, designed to incorporate learning from the first 10 years of the standard's use into the standard document. The principal changes introduced were as follows:

— To reduce the risk of accidental entry into test mode, the requirement that a binary code for the *EXTEST* instruction be {000...0} was removed and use of this binary code for other instructions that result in entry to test mode was deprecated.

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— To increase the flexibility with which instructions may be implemented and merged, the implicitly merged *SAMPLE/PRELOAD* instruction was redefined as two separate instructions: *SAMPLE* and *PRELOAD*. *These instructions can continue to share a single binary code*, effectively resulting in a merged *SAMPLE/PRELOAD* instruction, but alternatively, they may now share binary codes with other instructions, provided that no rules applying to any of the merged instructions are violated.

— To enable more efficient implementation of boundary-scan register cells provided at system logic outputs, the source of data to be captured in such cells in response to the *SAMPLE* instruction was allowed to be at the connected system pin. Additionally, three new cell types based on this implementation (**BC_8, BC_9,** and **BC_10**) were added to the standard Boundary-Scan Description Language (BSDL) Package and Package Body.

— To permit more flexible boundary-scan register cell implementations, sharing of circuitry between the boundary-scan register and other elements of the test and/or system logic were allowed in limited cases.

— To support more complete description of IC pin drivers with bus keeper circuits, a new value for <disable result> was defined (**KEEPER**).

— To track the widespread acceptance of BSDL, the language was made a normative part of this standard and its use for documentation was mandated.

Additionally, a number of minor changes were made to correct and clarify the language of this standard.

Changes introduced by this revision

First, this version of the standard affirms what had been required in the previous (2001) version. There are only minor clarifications or relaxations to the rules that are already established. It is expected that components currently compliant with the previous version of this standard will remain compliant with this one. The one exception is that the previously deprecated **BC_6** boundary-scan cell is no longer supported or defined, and the component supplier must provide a user-supplied BSDL package defining the **BC_6** cell for any component using the **STD_1149_1_2013** standard Package and still using that cell.

Second, while this is a major revision, items introduced in this version are optional and intended to provide test improvements for the complex components being created today and in the foreseeable future. There are also significant improvements in documentation capability, including the introduction of a new language to document test procedures unique to the component.

The major changes, listed in the order in which they appear in this standard, are as follows:

In the standard body:

— A new, optional, test mode persistence controller that can maintain the IEEE 1149.1 test logic in test mode even if the active instruction does not force test mode. Clause 6 is now split into 6.1 for the TAP controller and 6.2 for the test mode persistence controller. In support of this new controller, there are three new instructions: *CLAMP_HOLD* and *TMP_STATUS* in 8.20, with the new TMP status test data register in Clause 16; and *CLAMP_RELEASE* in 8.20.

— A new, optional *ECIDCODE* instruction in 8.15 and its electronic chip identification test data register in Clause 13 to supplement the existing *IDCODE* and *USERCODE* instructions and allow for the recovery of an Electronic Chip Identification value used to identify and track individual integrated circuits.

— A new, optional, component initialization mechanism to provide more flexibility in preparing the component for test. The *INIT_SETUP, INIT_SETUP_CLAMP,* and *INIT_RUN* instructions in 8.17, 8.18, and 8.19, and their new initialization data and initialization status test data registers in Clause 14 and Clause 15, respectively. This will allow programmable input/output (I/O) to be set up prior to board or system testing, as well as any tasks required to put the system logic into a safe state for test.

— A new, optional, *IC_RESET* instruction in 8.21 and its reset_select test data register in Clause 17 to provide control of component reset functions through the TAP.

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— In 9.2, an optional standard TAP to test data register interface is recommended, and examples of different types of test data register cells using this interface are shown. In addition, the concept of register segments is expanded to allow for segments that may be excluded or included. This is introduced to support power domains that may be powered down, and yet may have a segment of a test data register within that domain. However, the capability was kept general.

— In the new 9.4, the rules for defining and controlling the new excludable and selectable segments are established.

— Boundary-scan register description in Clause 11 has been updated to support:

  i) Optional excludable (but not selectable) boundary-scan register segments
  ii) Optional observe-only boundary-scan register cells to redundantly capture the signal value on all digital pins except the TAP pins
  iii) Optional observe-only boundary-scan register cells to capture a fault condition on all pins, including nondigital pins, except the TAP pins

— Documentation requirements in Clause 18 have been updated for the new capabilities.

Note that where rules were removed or moved in this version of this standard, a placeholder was left behind ("Removed in this version ...." or "Moved to Permision ....") in order to preserve the rule numbering from previous versions. This is intended to simplify the transition for both users and tool vendors in supporting what is a significant change.

In Annex B (Boundary Scan Description Language):

— The entire annex was rewritten for:

  i) Increased clarity of what was normative versus descriptive text
  ii) Increased consistency in presentation

— BSDL is no longer a "proper subset" of VHDL, but it is now "based on" VHDL. See B.4. In particular, new pin type keywords were introduced in B.8.3 that are not needed in VHDL but give a more accurate description of each port in BSDL.

— Formal definitions of language elements are included in B.5 instead of reliance on inheritance from VHDL.

— Some changes to the BNF notation used, including definition of all the special character tokens, are in B.6.

— Pin mapping in B.8.7 now allows for documenting that a port is not connected to any device package pin in a specific mapped device package.

— The boundary-scan register description in B.8.14 introduces new attributes for defining boundary-scan register segments, and introduces a requirement for documenting the behavior of an undriven input.

— New capabilities are introduced for documenting the structural details of test data registers:

  i) Subclause B.8.18 introduces the definition of mnemonics that may be associated with register fields.
  ii) Subclause B.8.19 introduces the ability to name fields within a register or segment.
  iii) Subclause B.8.20 introduces the ability to define the types of cells used in a test data register (TDR) field.
  iv) Subclause B.8.21 introduces the ability to hierarchically assemble segments into larger segments or whole registers.
  v) Subclause B.8.22 introduces the ability to define constraints on the values to be loaded in a register or register field.
  vi) Subclause B.8.23 introduces the ability to associate a register field or bit to specific ports and other information, and to associate a power port to other ports.

— The role of a User Defined Package defined in B.10 has been expanded to support logic IP providers who may need to document test data register segments contained within their IP.

A new annex, Annex C, codifies the Procedural Description Language (PDL), a new language for documenting the procedural and data requirements for some of the new instructions. As mentioned, this version of the standard introduces new instructions for configuring complex I/Os prior to entering the *EXTEST* instruction. As the data required for initialization could vary for each use of the component on each distinct board or system design, this

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created the need for a new language for setting internal TDR register fields in order to configure the I/O. It was decided to adopt PDL and tailor it to the BSDL register descriptions and IEEE 1149.1 needs.

A new informative annex, Annex D, shows extended examples of BSDL and PDL used together to describe the structure and the procedures for use of new capabilities.

A new informative annex, Annex E, shows example pseudo-code for the execution of the PDL iApply command, the most complex of the new commands in PDL.

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IEEE Standard for Test Access Port and Boundary-Scan Architecture

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1. Overview

1.1 Scope

This standard defines test logic that can be included in an integrated circuit to provide standardized approaches to:

— Testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate

— Testing the integrated circuit itself~~; and~~

— Observing or modifying circuit activity during the component's normal operation

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The test logic consists of a boundary-scan register and other building blocks and is accessed through a test access port (TAP).

1.2 Purpose

1.2.1 ~~An~~ Overview of the operation of this standard ~~IEEE Std 1149.1~~

This subclause provides a general overview of the operation of a component compatible with this standard and provides a background to the detailed discussion in later clauses ~~subclauses~~.

The circuitry defined by this standard allows test instructions (which take control of the component outputs and observe the component inputs) and associated test data to be fed into a component and, subsequently, allows the results of execution of such instructions to be read out. All information (instructions, test data, and test results) is communicated in a serial format.

The sequence of operations would be controlled by a bus master, which could be either an automatic test equipment (ATE) or a component that interfaces to a higher level test bus as a part of a complete system maintenance architecture. Control is achieved through signals applied to the test mode select (TMS) and test clock (TCK) inputs of the various components connected to the bus master. Starting from an initial state in which the test circuitry defined by this standard is inactive, a typical sequence of operations would be as follows.

The first steps would be, in general, to load serially into the component the instruction binary code for the particular operation to be performed. The test logic defined by this standard is designed such that the serial movement of instruction information is not apparent to those circuit blocks whose operation is controlled by the instruction. The instruction applied to these blocks changes only on completion of the shifting (instruction load) process.

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Once the instruction has been loaded, the selected test circuitry is configured to respond. In some cases, however, it is necessary to load data into the selected test circuitry before a meaningful response can be made. Such data are ~~is~~ loaded into the component serially in a manner analogous to the process used previously to load the instruction. Note that the movement of test data has no effect on the instruction present in the test circuitry.

After execution of the test instruction, based where necessary on supplied data, the results of the test can be examined by shifting data out of the component to or through the bus master.

Note that in cases where the same test operation is to be repeated but with different data, new test data can be shifted into the component while the test results are shifted out. There is no need for the instruction to be reloaded.

Operation of the test circuitry may proceed by loading and executing several further instructions in a manner similar to that described and would conclude by returning control from the test circuitry to ~~and, where required, on chip~~ system circuitry. Note that the ~~to its initial~~ state of the system logic may be indeterminate, and care is required in returning to system operation.

1.2.2 ~~The~~ Use of this standard ~~IEEE Std 1149.1~~ to test an assembled product

This subclause outlines the use of the boundary-scan circuitry defined by this standard during the process of testing an assembled product such as a printed circuit board.

The test problem for any product constructed from a collection of components can be decomposed into three goals:

a) To confirm that each component performs its required function

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b) To confirm that the components are interconnected in the correct manner

c) To confirm that the components in the product interact correctly and that the product performs its intended function

This approach can be applied to a board constructed from integrated circuits, to a system constructed from printed circuit boards, or to a complex integrated circuit constructed from a set of simpler functional modules. To simplify the discussion, this description henceforth will concentrate on the case of an assembled printed circuit board constructed from a collection of digital integrated circuits.

At the board level, the second goal ~~a) and~~ [goal b)] may be ~~typically are~~ achieved ~~by~~ using in-circuit test techniques; the first and third goals [goal a) and ~~for~~ goal c)] require a functional test ~~is required~~. However in-circuit test techniques have significant limitations when viewed against evolving surface-mount interconnection technology, for example, the difficulty of making reliable contact to miniaturized features of the printed circuit board using a bed-of-nails fixture. How, then, might these ~~the above~~ three test goals be achieved if test access becomes limited to the normal circuit connections, plus a relatively small number of special-purpose test connections?

Considering goal a), it is clear that the vendor of an integrated circuit used in the board-level design will have an established test methodology for that component. The components could be tested on a proprietary ATE system or by using a self-test procedure embedded in the design. Information on the test methodology adopted is typically not available to the component purchaser. Even where self-test modes of operation are known to exist, they may not be documented and therefore are not available to the component user. Alternative sources of test data for the board test engineer may be the component test libraries supplied with in-circuit test systems or the test programs developed by component users for incoming inspection of delivered devices.

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Wherever the test data for a component originates, the next step is to use it once the component has been assembled onto the printed circuit board. If access is limited to the normal connections of the assembled circuit, this task may be far from simple. This is particularly true if the surrounding components are complex or if the board designer has tied some of the components' connections to fixed logic levels or has left component pins unconnected. Even for slow speed tests, it will not normally be possible to test the component in the same way that it was tested in isolation unless an in-circuit test is achievable.

To help ensure that built-in test facilities can be used or that preexisting test patterns can be applied, a framework is needed that can be used to convey test data to or from the boundaries of individual components so that they can be tested as if they were freestanding. This framework will also allow access to and control of built-in test facilities of components. A boundary scan coupled with a test access bus provides such a framework.

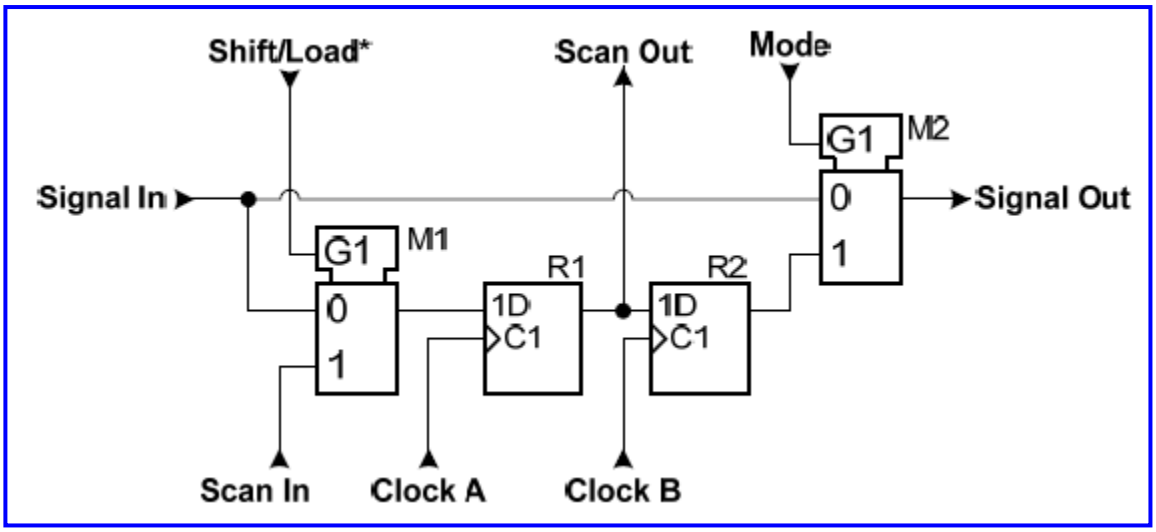
The objective of this standard is to define a boundary-scan architecture that can be adopted as a standard feature of integrated circuit designs, thus, allowing the required test framework to be created on assembled printed circuit boards and other products.

1.2.3 What is a boundary scan?

The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan register cell) adjacent to each component pin so that signals at component boundaries can be controlled and observed using scan testing principles.

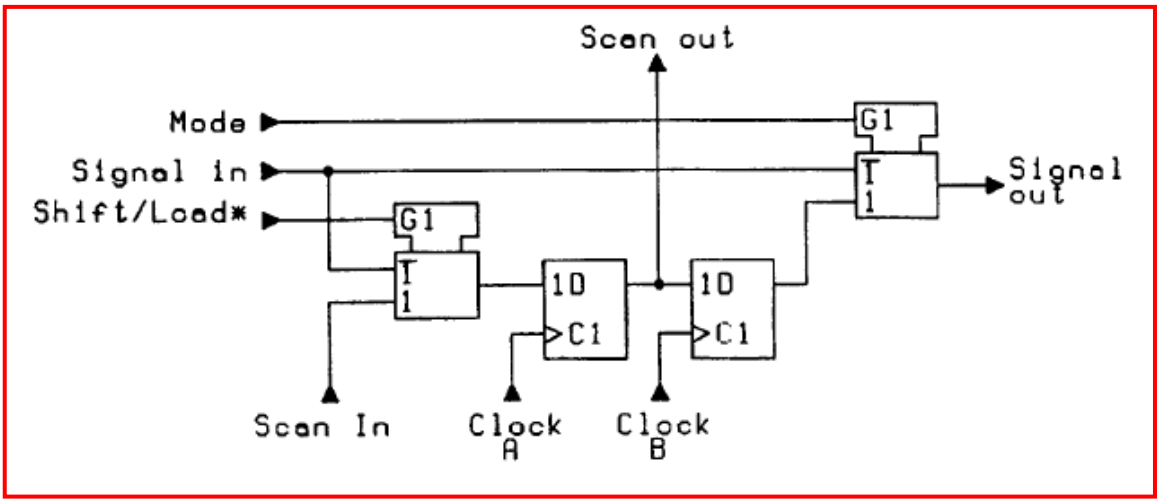
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Figure 1-1 illustrates an example implementation for a boundary-scan register cell that could be used for an input or output connection to an integrated circuit. If it is used for an input, data can either be loaded into the scan register from the input pin through the signal-in port or be driven from the register through the Signal-out port of the cell into the core of the component design, depending on the control signals applied to the multiplexers. Similarly, if it is used for an output, data can either be loaded into the scan register from the core of the component or be driven from the register to an output pin. As will be discussed in detail in Clause 11, the second flip-flop (controlled by input Clock B) is provided to hold ~~ensure that~~ the signal value driven out of the cell ~~in the latter case are held~~ while new data are ~~is~~ shifted into the cell using input Clock A. This flip-flop is not required in all cases but is included in Figure 1-1 to simplify the discussion.



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~~(Deleted)~~

Figure 1-1—~~A~~ Boundary-scan register cell

The boundary-scan register cells for the pins of a component are interconnected to form a shift-register chain around the border of the design, and this path is provided with serial input and output connections and appropriate clock and control signals. Within a product assembled from several integrated circuits, the boundary-scan registers for the individual components could be connected in series to form a single path through the complete design, as illustrated in Figure 1-2. Alternatively, a board design could contain several independent boundary-scan paths.

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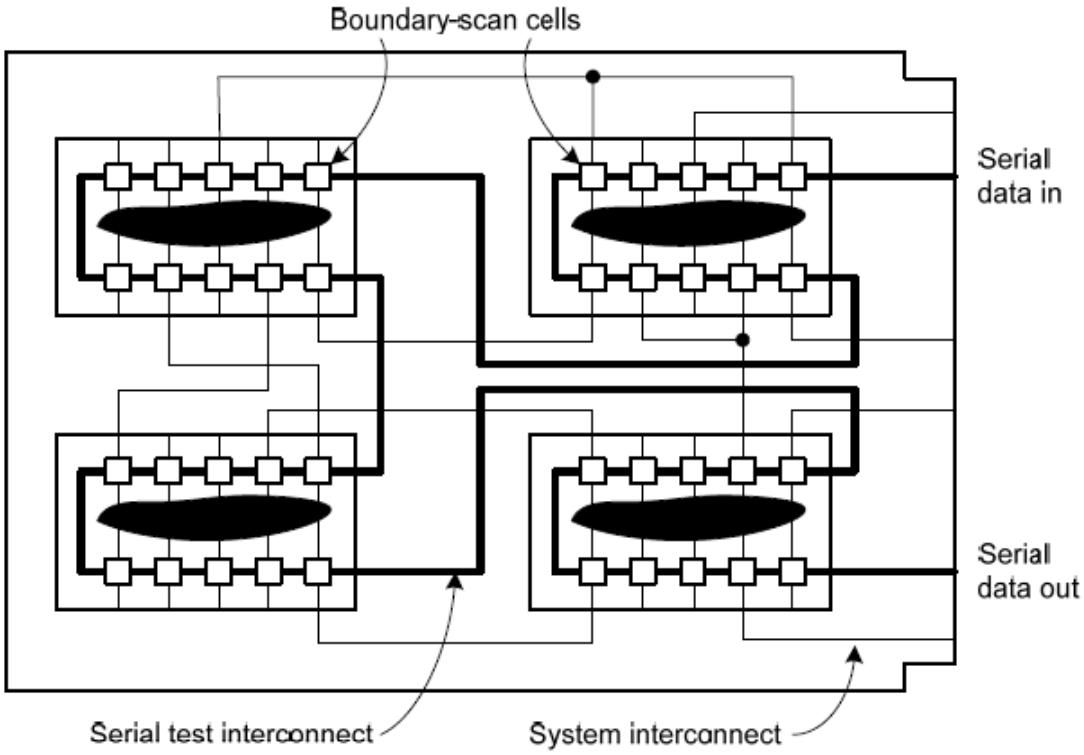


Figure 1-2—~~A~~ Boundary-scannable board design

If all ~~the~~ components used to construct a circuit have a boundary-scan register, then the resulting serial path through the complete design can be used in two ways:

a) To allow the interconnections between the various components to be tested, test data can be shifted into all the boundary-scan register cells associated with component output pins and loaded in parallel through the component interconnections into those cells associated with input pins.

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b) To allow the components on the board to be tested, the boundary-scan register can be used as a means of isolating ~~on-chip~~ system logic from stimuli received from surrounding components while an internal self-test is performed. Alternatively, if the boundary-scan register is suitably designed, it can permit a limited slow- speed static test of the ~~on-chip~~ system logic because ~~since~~ it allows delivery of test data to the component and examination of the test results.

These tests allow the first two goals discussed earlier to be achieved through the use of the boundary-scan register. In effect, tests applied using the register can detect many of the faults that in-circuit testers currently address, but without the need for extensive bed-of-nails access. The third goal—to test the operation of the complete product functionally—remains and can be achieved either ~~by~~ using a functional (through the pins) ATE system or ~~by~~ using a system-level self-test, for example.

Note also that by parallel loading the cells at both the inputs and outputs of a component and shifting out the results, the boundary-scan register provides a means of "sampling" the data flowing through a component without interfering with the behavior of the component or the assembled board. This mode of operation is valuable for design debugging and fault diagnosis because ~~since~~ it permits examination of connections not normally accessible to the test system.

1.2.4 ~~The~~ Use of this standard ~~IEEE Std 1149.1~~ to achieve other test goals

In addition to its application in testing printed circuit assemblies and other products containing multiple components, the test logic defined by this standard can be used to provide access to a wide range of design-for-test features built into the components themselves. Such features might include internal scan paths, self-test functions [e.g., memory ~~using~~ built-in self test (MBIST) or logic built-in self-test (Logic BIST)], ~~block observer (BILBO) elements],~~ or other support functions.

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Design-for-test features such as these can be accessed and controlled using the data path between the serial test data pins of the TAP defined by this standard. Instructions that cause internal reconfiguration of the component's system logic such that the test operation is enabled may be shifted into the component through the TAP.

1.3 Document outline

Circuit designs such as that defined by this standard are more easily understood if their specifications are accompanied by general descriptive material that places the details of the various parts of the design in perspective and provides examples of implementation. Clause 1 therefore contains an overview of the application of this standard to the testing of the digital portions of an electronic product consisting of many integrated circuits.

Subsequent clauses of this document contain the specifications for particular features of this standard. Two classes of material are contained in these clauses~~:~~.

1.3.1 Specifications

Material titled ~~Subclauses entitled~~ "Specifications" contain the rules, recommendations, and permissions that define this standard:

a) *Rules* specify the mandatory aspects of this standard. ~~Subclauses that are~~ Rules contain the word **shall.**

b) *Recommendations* indicate preferred practice for designs that seek to conform to this standard. ~~Subclauses that are~~ Recommendations contain the word **should.**

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c) *Permissions* show how optional features may be introduced into a design that seeks to conform to this standard. These features will extend the application of the test circuitry defined by this standard. ~~Subclauses that are~~ Permissions contain the word **may.**

1.3.2 Descriptions

CAUTION

The descriptive material contained in this standard is for illustrative purposes only and does not define a preferred implementation. Examples are provided throughout this standard to illustrate possible circuit implementations. Where discrepancies between examples and specifications may occur, the specifications always take precedence. Readers should exercise caution when using these examples ~~to ensure full compliance~~ in their specific applications. In particular, it is emphasized that the examples are designed to communicate effectively the meaning of this standard. As such, they are logically correct; however, as always, a particular implementation may not operate properly with respect to timing and other parametric characteristics. One example of this concern is that the example ~~sample~~ TAP Controller implementation depicted in Figure 6-5 reasonably assumes a significantly greater delay in the flip-flop sourcing signal A, for instance, ~~A and A*~~ than in the inverter sourcing TCK*. It is possible to design a circuit where this assumption is violated, causing a critical race to occur that would invalidate the behavior of the TAP controller. Therefore, it is highly recommended that implementations be fully verified for ~~to ensure~~ compliance under required operating conditions.

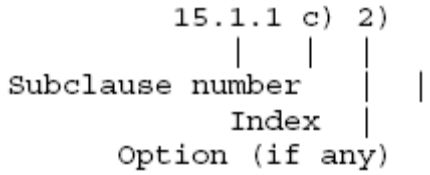
Material not contained in ~~subclauses entitled~~ "Specifications" is descriptive material that illustrates the need for the features being specified or their application. This material includes schematics that illustrate a possible implementation of the specifications in this standard. ~~Annex A to this standard contains an alternative implementation example.~~ The descriptive material also discusses design decisions made during the development of this standard.

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1.4 Text conventions

The following conventions are used in this standard:

a) The rules, recommendations, and permissions in ~~each~~ "Specifications ~~subclause~~" are contained in a single alphabetically indexed list. References to each rule, recommendation, or permission are shown in the form:



b) Instruction and state names defined in this standard are shown in *italic* type in the text ~~of this standard~~.

c) Names of states and signals that control ~~pertain to~~ the test data registers defined by this standard contain the characters DR, while those that control ~~pertain to~~ the instruction register contain the characters IR.

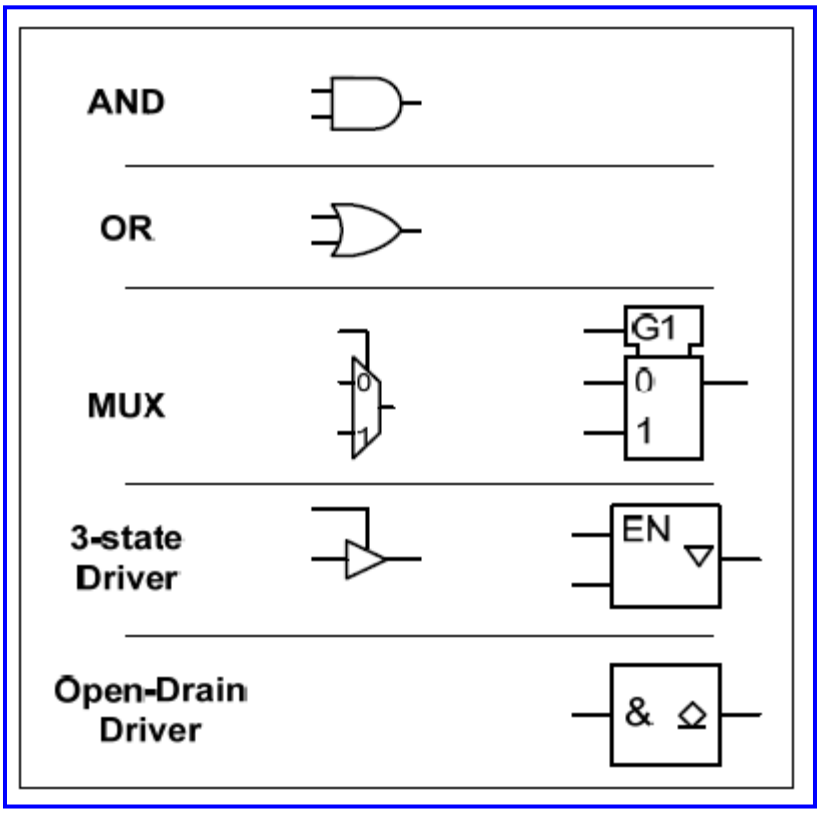
d) Names for signals that are active in their low state have an asterisk as the final character, e.g., TRST*.

e) A positive logic convention is used; i.e., a logic 1 signal is conveyed as the more positive of the two voltages used for logic signals.

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1.5 Logic diagram conventions

During the different iterations of this standard, logic diagram figures have been added in various styles with differing logic symbols. Figure 1-3 shows the symbologies currently used for the common combinational logic elements. Symbols for storage elements (generally edge-sensitive flip-flops) are reasonably consistent, although pin names on the element may vary from figure to figure.



(New)

Figure 1-3—Logic symbology used in this standard

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2. Normative references

The following referenced documents are indispensable for the application of this standard (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

~~This standard shall be used in conjunction with the following standards. When the following standards are superseded by an approved revision, the revision shall apply.~~

EIA/JEP106, JEDEC Publication 106, Standard Manufacturer's Identification Code.[1]

~~IEEE 100, *The Authoritative Dictionary of IEEE Standards Terms*, Seventh Edition~~[2]

IEEE Std 1076~~-1993~~, IEEE Standard VHDL Language Reference Manual.[2,3]

IEEE Std 1451.0, IEEE Standard for a Smart Transducer Interface for Sensors and Actuators—Common Functions, Communication Protocols, and Transducer Electronic Data Sheet (TEDS) Formats.

The following referenced documents provide extensions to this standard and should be referenced when dealing with analog, capacitively coupled, and differential inputs and outputs.

[1] EIA publications are available from Global Engineering Documents (http://global.ihs.com/)

~~[1]Copies can be obtained from EIA/JEDEC, 2500 Wilson Blvd., Arlington, VA 22201-3834, USA (www.jedec.org).~~

[2] IEEE publications are available from The Institute of Electrical and Electronics Engineers ~~, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA~~ (http: //standards .ieee. org/).

[3] The IEEE standards or products referred to in this clause are trademarks of The Institute of Electrical and Electronics Engineers, Inc.

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IEEE Std 1149.4 ~~1999~~, IEEE Standard for a Mixed-Signal Test Bus.

IEEE Std 1149.6, IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks.

IEEE Std 1149.8.1, IEEE Standard for Boundary-Scan-Based Stimulus of Interconnections to Passive and/or Active Components.

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3. Definitions, abbreviations, acronyms, and special terms

For the purposes of this document ~~standard~~, the following terms and definitions apply. ~~IEEE 100,~~ The ~~*Authoritative Dictionary of*~~ *IEEE Standards Dictionary Online* ~~*Terms,* Seventh Edition~~ should be consulted ~~referenced~~ for terms not defined in this clause.[4]

3.1 Definitions

active: When associated with a logic level (e.g., active-low), this term identifies the logic level to which a signal shall be set to cause the defined action to occur. When referring to an output driver (e.g., an active drive), this term describes the state in which the driver is capable of determining the voltage of the network to which it is connected.

bidirectional pin: A component pin that can either drive or receive signals from external connections.

blind interrogation: The act of discovering the identity of an unknown component, or discovering the basic construction of a chain of unknown components, by reading out data that are deterministically set by the devices in the chain when reset. For example, devices may have a documented identification (ID) code, which is selected for scan by the default instruction in such devices, so that a user can identify each unknown component in the chain and the user's position within the chain ~~Access to a facility (e.g., the device identification register) without prior knowledge of the test logic operation of the specific component being accessed~~.

~~**3.1.4 built-in logic block observer (BILBO):** A shift-register-based structure used in some forms of self-testing circuit design.~~

[4] The *IEEE Standards Dictionary Online* subscription is available at http://www. ieee.org/portal/inn ovate/products/standard/standards dictionary.html.

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capture: Load a value into a data register or the instruction register as a consequence of entry into the *Capture-DR* or *Capture-IR* controller state, respectively.

chip: Typically mounted on a board or some other package with other components. The more general term "component" is normally used in this standard for a compliant object as there may be multiple integrated circuits in a package, even when they behave as a single object. *Syn.:* **integrated circuit (IC).**

chip-on-board testing: A test of a component after it has been assembled onto a printed circuit board or other substrate. For example, the facilities defined by this standard may be used.

clock: A signal where transitions between the low and high logic levels (or vice versa) are used to indicate when a stored-state device, such as a flip-flop or latch, may perform an operation.

component: An active or passive electronic part. For the sake of this standard, this usually refers to an integrated circuit, although it could include non-integrated-circuit devices mounted on a board. *See also:* **chip.**

deprecate: To discourage the use of configurations or modes of operation that might reduce reliability or create problems in usage. *Syn.:* disapprove, discourage, disparage.

falling edge: A transition from a high to a low logic level. In positive logic, a change from logic 1 to logic 0. Events that are specified to occur on the rising (falling) edge of a signal should be completed within a fixed (frequency-independent) delay specified by the component supplier.

field: In reference to a register or register segment, a logical set of bits within a defined register or segment, which may be addressed or treated as a unit for specific purposes. *Contrast:* **segment.**

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hierarchy: Objects may be contained (used) in other objects in a tree-type arrangement with no loops; that is, no circular references. The containing (outer, higher) object is referred to as the parent, and the contained (inner, lower) object is referred to as the child, and they are said to be in a parent-to-child relationship. In this standard, only user Packages and Test Data Registers have hierarchy. Packages may "use" (refer to) other packages. Test data registers may be composed of segments and fields, where segments may be composed of other segments and fields. Fields may not contain other objects. *See also:* **instance and instantiation.**

high: The higher of the two voltages used to convey a single bit of information. For positive logic, a logic 1.

inactive: When referring to an output driver (e.g., an inactive drive), this term describes the state in which the driver is not capable of determining the voltage of the network to which it is connected.

input pin: A component pin that receives signals from an external connection.

instance and instantiation: These terms refer to the hierarchical inclusion of an object within another object. For the normative purpose of this standard, these terms are used in the documentation of Test Data Registers, which may be composed of segments and fields, and of segments that may be composed of other segments and fields. A single field or segment definition is an object that may be used multiple times, and each use is termed an *instance* of that object. An *instantiation* is the statement that creates and names an instance of a child object within the definition of the parent object. (Similar terminology is used when discussing "instances" or "instantiations" of components on a board.) *See also:* **hierarchy.**

instruction: A binary data word shifted serially into the test logic in order to define its subsequent operation.

integrated circuit (1C): A collection of transistors, resistors, and capacitors and their interconnections constructed to perform specific functions on a single thin slice of a semiconductor crystal.

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least significant bit (LSB): The digit in a binary number representing the lowest numerical value. For shift-registers, the bit located nearest to the serial output, or the first bit to be shifted out. The least significant bit of a binary word or shift-register is numbered 0.

level-sensitive scan design (LSSD): A variant of the scan design technique that results in race-free, testable digital electronic circuits.

low: The lower of the two voltages used to convey a single bit of information. For positive logic, a logic 0.

most significant bit (MSB): The digit in a binary number representing the greatest numerical value. For shift-registers, the bit farthest from the serial output, or the last bit to be shifted out. Logic values expressed in binary form are shown with the most significant bit on the left.

nonclock: A signal where the transitions between the low and high logic levels do not themselves cause operation of stored-state devices. The logic level is important only at the time of a transition on a clock signal.

no-connect: A signal of the component, which is brought to an input-output pad of the die but not connected to a package pin due, for instance, to a constrained pin-count for the package.

output pin: A component pin that drives signals onto external connections.

pin: The point at which connection is made between the integrated circuit and the substrate on which it and other components are ~~is~~ mounted (e.g., the printed circuit board). For packaged components, this would be the package pin; for components mounted directly on the substrate, this would be the bonding pad. The actual form of connection (bonding wire, landing pad, solder ball, or metal pin inserted into a via) is not material to the definition.

prime source: In the event that several vendors offer pin-for-pin compatible components, the prime source is the vendor that introduced the component type. *Contrast:* **second source.**

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private: An optional ~~A design~~ feature intended solely for use by the component manufacturer. In the context of this standard, an instruction can be defined as private in the Boundary-Scan Description Language (BSDL). *Contrast:* **public.**

power-up reset: A reset of test or system logic that occurs when the power supply goes from OFF to ON. This can be achieved by design of latches that causes them to always power up in a specific state, or by an ON-component or OFF-component circuit that generates an asynchronous reset signal that stays active for some nontrivial time after the power supply has reached its operating voltage. *Syn.:* power-on reset (FOR).

public: A design-specific feature, documented in the component data sheet or in the Boundary-Scan Description Language (BSDL), that may be used by purchasers of the component. In the context of this standard, any instruction not defined as private is public. *Contrast:* **private.**

register: Most often a Test Data Register, which is accessed by one or more specific instructions. (See Clause 9.)

reset: The establishment of an initial logic condition that can be either logic 0 or logic 1, as determined by the context.

rising edge: A transition from a low to a high logic level. In positive logic, a change from logic 0 to logic 1. Events that are specified to occur on the rising (falling) edge of a signal should be completed within a fixed (frequency-independent) delay, specified by the component supplier.

sample: To capture the value of a signal at a specific moment in time, such as defined by a clock edge.

scan design: A design technique that introduces shift-register paths into digital electronic circuitry, providing controllability and observability in deeply embedded regions of circuity and thereby ~~improves their~~improving testability.

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scan path: The shift-register path through a circuit designed using the scan design technique.

second source: In the event that several vendors offer pin-for-pin compatible components, second-source suppliers are vendors of the component other than the prime source.

segment: A set of contiguous (in terms of the scan chain) register bits obeying the rules for Test Data Registers and from which a Test Data Register may be assembled. *Contrast:* **field.** (See Clause 9.)

selected test data register: A test data register is selected when it is required to operate by an instruction supplied to the test logic.

Signature ~~analysis~~: A result of a technique for compressing a sequence of logic values output from a circuit under test into a small number of bits of data (the signature) that, when compared with ~~to~~ stored known-good data, will indicate the presence or absence of faults in the circuit.

stand-alone testing: A test of a component performed before it is assembled onto a board or other substrate, for example, using automatic test equipment (ATE).

stuck-at fault: A failure in a logic circuit that causes a signal connection to be fixed at 0 or 1 regardless of the operation of the circuitry that drives it.

system: Pertaining to the nontest function of the circuit. *Contrast:* **test logic.**

system logic: Any item of logic that is dedicated to realizing the nontest function of the component or is at the time of interest configured to achieve some aspect of the nontest function.

system pin: A component pin that feeds, or is fed from, the on-chip system logic and carries a digital signal. This term does not include analog signals, voltage references, or power sources.

test logic: Any item of logic that is a dedicated part of the test logic architecture or is at the time of interest configured as ~~a~~ part of the test logic architecture.

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test mode: The state of a component in which the component's test logic interferes with the flow of signals to and from the system logic. In addition, the system logic may be controlled as needed to prevent an undesired response to system inputs, excessive heating, and so on.

three-state pin: A component output pin where the drive may be either active or inactive (for example, at high impedance).

update: Transfer ~~of~~ a logic value from the shift-register stage of a data register cell or an instruction register cell into the latched parallel output stage of the cell as a consequence of the falling edge of the test clock input in the *Update-DR* or *Update-IR* controller state, respectively.

~~**3.1.37 3-state pin:** A component output pin where the drive may be either active or inactive (for example, at high impedance).~~

3.2 Abbreviations and acronyms

ASIC	application-specific integrated circuit
ATE	automatic test equipment
ATPG	automatic test pattern generation
BIST	built-in self-test
BNF	Backus-Naur form
BSDL	Boundary-Scan Description Language (see Annex B) or a file containing BSDL statements

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CMOS	complementary metal-oxide semiconductor
DC	direct current
ECID	electronic chip identification
ECL	emitter coupled logic
1C	integrated circuit
I/O	input or output
IP	intellectual property, commonly used to refer to a reusable design element
IR	infrared
~~BILBO~~	~~built-in logic block observer~~
LSB	least significant bit
LSSD	level-sensitive scan design
LVDS	low-voltage differential signaling
MEMBIST	memory built-in self-test
MSB	most significant bit
PDL	Procedural Description Language (see Annex C) or a file containing PDL statements

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PGA pin-grid array

PLL phase-locked loop

FOR power-on reset

PRBS pseudo-random binary sequence

RAM random access memory

SOC system-on-a-chip

TAP test access port (see Clause 4)

TCK test clock input (see 4.2)

Tel Tool Command Language (see Annex C) or a file containing Tel statements

TDI test data input (see 4.4)

TDO test data outputs (see 4.5)

TDR test data register (see Clause 9)

TEDS tranducer electronic data sheet

TMP test mode persistence (see 6.2)

TMS test mode select (see 4.3)-

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TRST*	test reset (see 4.6)
TTL	transistor-transistor logic
UUT	unit under test
VHDL	VHSIC Description Language
VHSIC	very high speed integrated circuit
WBR	wrapper boundary register
WBY	wrapper bypass
WDR	wrapper data register
WIR	wrapper instruction register
WSC	wrapper serial control
WSI	wrapper scan in
WSO	wrapper scan out
WSP	wrapper serial port

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3.3 Special terms

design specific: For the purpose of this standard, a test-logic element, permitted by and conforming to the rules of this standard, added to a specific component implementation in addition to the elements required or defined by this standard.

redundant: When applied to an element of the test logic, and in particular to boundary-scan register cells, implies that the element could be omitted from the component without jeopardizing compliance with this standard.

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