



IEEE Standard for a Mixed-Signal Test Bus

IEEE Computer Society

Developed by the
Test Technology Standards Committee

IEEE Std 1149.4™-2024
(Revision of IEEE Std 1149.4™-2010)

STANDARDS

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Test Technology Standards Committee
of the
IEEE Computer Society

Approved 26 September 2024

IEEE SA Standards Board

Abstract: The testability structure for digital circuits described in IEEE Std 1149.1™ has been extended to provide similar facilities for mixed-signal circuits. The architecture is described, together with the means of control of and access to, both analog and digital test data. Sample implementation and application details (which are not part of the standard) are included for illustration. Also, extensions to the standard Boundary-Scan Description Language (BSDL) are defined that allow description of key component-specific aspects of such testability features.

Keywords: analog test, board testing, boundary scan, Boundary-Scan Description Language (BSDL), design for testability, IEEE 1149.4™, in-circuit test, mixed-signal test

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Introduction

This introduction is not part of IEEE Std 1149.4-2024, IEEE Standard for a Mixed-Signal Test Bus.

The development of this standard began with a preliminary meeting in the summer of 1991 when the need was recognized for a standardized structure to be incorporated into mixed-signal circuits to combat the testability problems posed by such circuits. This meeting adopted the following mission:

To define, document, and promote the use of a standard mixed-signal test bus that can be used at the device and assembly levels to improve the controllability and observability of mixed-signal designs and to support mixed-signal built-in test structures in order to reduce both test development time and testing costs and to improve test quality.

The original draft of IEEE Std 1149.4 was accepted on 26 August 1999 and published 28 March 2000. A language extension to Boundary-Scan Description Language (BSDL) called Analog Boundary-Scan Description Language (ABSDL), was added to the revision of the standard approved on 9 December 2010, which was then published 18 March 2011.

This version addresses changes introduced in IEEE Std 1149.1-2013 on which this standard builds. These are mostly addressed by removing specific standard publication dates from the references noted within this standard. All other modifications to this version are editorial in nature.

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IEEE Standard for a Mixed-Signal Test Bus

1. Overview

1.1 Scope

This standard defines a mixed-signal test bus architecture that provides the means of control and access to both analog and digital test signals such that the testability structure for digital circuits described in IEEE Std 1149.1⁶ has been extended effectively to provide similar facilities for mixed-signal circuits. In addition to testing interconnections in the conventional sense of IEEE Std 1149.1, the mixed-signal test bus defined by this standard also provides the means for parametric testing and, optionally, the means to access internal test structures. The standard does not mandate implementation details of the test circuitry, although examples of conformant implementations are given for illustration. Further, the standard develops extensions to Boundary-Scan Description Language (BSDL) to describe key aspects of implementing this standard within a particular component. At present, the extensions to BSDL defined by this standard specifically omit the description of any and all analog parameters defined by the standard.

1.2 Purpose

Where structures defined by this standard are incorporated into mixed-signal circuits, the testability problems posed by such circuits are mitigated by way of improving the controllability and observability of mixed-signal designs and supporting mixed-signal built-in test structures to reduce both test development time and testing costs and to improve test quality. In particular, these standardized test features allow mixed-signal (analog and/or digital) electronic components, printed circuit assemblies, and electronic systems to be accessible to external or built-in test equipment for interconnect test, parametric test, and internal test. A further purpose of this standard is to define the descriptive elements of BSDL and specified extensions sufficient to support the development of automated test algorithms used for testing interconnections between devices that adhere to this standard and, where practical, between such devices intermixed with devices that incorporate IEEE Std 1149.1 or IEEE Std 1149.6TM as well. The descriptive elements defined by this standard also largely support the automated construction of analog tests for external components attached to or between components that implement this standard with the caveat that such tests may subsequently require modification to account for undocumented analog features within the conformant components.

⁶ Information on references can be found in Clause 2.

1.3 Word usage

The word *shall* indicates mandatory requirements strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*).^{7, 8}

The word *should* indicates that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required (*should* equals *is recommended that*).

The word *may* is used to indicate a course of action permissible within the limits of the standard (*may* equals *is permitted to*).

The word *can* is used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

1.4 Organization of the standard

This standard is divided into ten clauses.

Clause 1 describes the scope and objectives of the standard and explains how the material of the standard is organized.

Clause 2 lists references to related standards necessary for the understanding of this standard, while Clause 3 defines terms and acronyms.

Clause 4 through Clause 8 contain specifications for the particular features of this standard and contain descriptive material that illustrates the need for the specified features or their application. This descriptive material is intended to place the details of various parts of the design in perspective and to provide examples of implementation and use.

Clause 9 addresses some of the practical issues that could arise in the implementation of the standard. In particular, it defines the performance required from a compliant part and describes how the performance limits can be measured.

Clause 10 summarizes the conditions under which any particular component can claim conformance to the standard and defines the documentation that shall be provided by the manufacturer to allow test equipment to make use of the test features. This clause also defines extensions to BSDL for describing concepts and structures introduced by this standard.

1.5 Context

Figure 1 illustrates the context within which this standard is intended to operate. It shows an electrical circuit constructed as a printed circuit assembly (PCA) consisting of a substrate carrying a pattern of conductors (the interconnect) on which separately manufactured components are mounted so that the component pins make electrical contact with the interconnect. In normal functional operation, the PCA connects to other parts of the system by way of a set of contacts, such as the edge-connector shown in Figure 1.

⁷ The use of the word *must* is deprecated and cannot be used when stating mandatory requirements, *must* is used only to describe unavoidable situations.

⁸ The use of *will* is deprecated and cannot be used when stating mandatory requirements, *will* is only used in statements of fact.

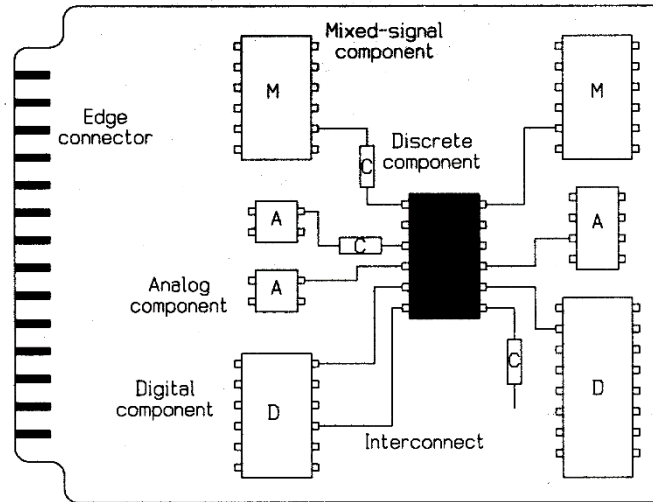


Figure 1—Mixed-signal printed circuit assembly

In Figure 1, the component that is the subject of this standard is shown shaded. In a typical mixed-signal analog and digital PCA, the pins of the component could be connected to:

- Other mixed-signal components (labeled M), which may or may not conform to this standard;
- Digital components (labeled D), which may or may not conform to IEEE Std 1149.1;
- Analog components (labeled A), which could be anything from a single transistor to an operational amplifier or an analog signal processing circuit, but which would be unlikely to contain any associated testability features; or
- Discrete components (labeled C), such as pull-up resistors or coupling capacitors, which will not have any associated testability features.

The PCA is tested, both in production (to verify correct manufacture) and in field service (to detect and locate faults), using automatic test equipment (ATE) to supply test signals to, and to collect test responses from, some or all of the component pins. The aim of the test structures described in this standard is to provide test access to individual component pins from the edge-connector to reduce or eliminate the need for the ATE to make direct physical contact via mechanical probes. The extent to which this aim can be satisfied will depend on the make-up of the PCA: The pins of components that conform either to this standard or to IEEE Std 1149.1 could be accessible from the edge-connector, providing at least partial access to the pins of some non-conformant components. If this access is inadequate for testing purposes, additional probe access would need to be employed.

1.6 Test features

1.6.1 Aims

This standard defines test features to be included in a mixed-signal (analog and digital) component, together with associated test protocols, to provide standardized approaches to:

- Interconnect test: Testing for opens and shorts among the interconnections in a PCA;
- Parametric test: Making analog characterization measurements and testing for the presence and value of discrete components in a PCA; and
- Internal test: Testing the internal circuitry of the mixed-signal component itself, regardless of whether it is part of a PCA.

The standard does not mandate implementation details of the test circuitry, although examples of conformant implementations are given for illustration.

1.6.2 Interconnect testing

IEEE Std 1149.1 provides an effective mechanism for interconnect testing of a PCA populated with digital components. The first objective of IEEE Std 1149.4 is to provide a similar capability for an assembly such as the one illustrated in Figure 1, populated with analog, digital, and mixed-signal components and discrete components.

To satisfy this objective, one of the fundamental requirements is to provide the ability to detect open circuits in the interconnections between integrated circuits and to detect and diagnose bridging faults anywhere in the interconnect regardless of whether they normally carry digital or analog signals. The aim is also to provide a structure that allows testing in full compatibility with IEEE Std 1149.1 to permit mixed-signal interconnect testing to take place at the same time using the same procedures as digital interconnect testing.

The range of problems is illustrated in Figure 2, which shows a group of interconnected components mounted on a board or other substrate, and analog and digital pins are represented by “A” and “D,” respectively. The left side of Figure 2 shows open circuits in analog and digital lines and in an analog interconnection network. The right side of Figure 2 shows a number of short circuits: It is worth noting that short circuits can occur between analog and analog, digital and digital, and analog and digital lines, as well as across discrete components in interconnection networks.

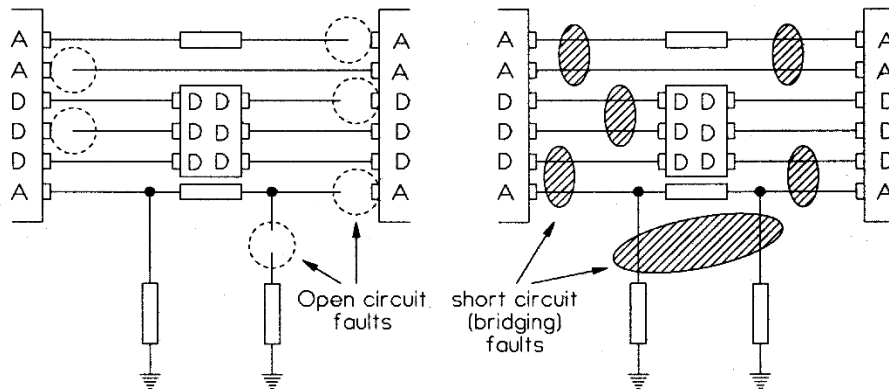


Figure 2—Defects on a mixed-signal printed circuit assembly (PCA)

1.6.3 Parametric test

The second objective of this standard, the parametric test, recognizes that groups of one or more discrete components are often interposed between integrated circuits, performing functions such as level shifting, passive filtering, and ac coupling. The inclusion of discrete components in the interconnection pathway gives rise to the concept of “extended” (as opposed to “simple”) interconnect, as illustrated in Figure 3. To provide for the testing of components in an extended interconnect, the standard defines a framework to support analog measurements, allowing, for example, impedances of discrete components to be computed. Meeting this objective also allows the testing of components such as pull-ups and filter capacitors associated with either analog or digital components.

Also illustrated in Figure 3 is an example of a differential interconnect, which is a pair of pathways carrying signals whose information content is defined by the pair of signals rather than by either one signal individually. In the case of a digital differential interconnect, these pathways would normally be excited by a single signal and the activity would be converted back to a single signal after reception. An analog

differential interconnect could follow the same pattern, but conversion from or to a single-ended form might take place within the core, or it might not take place at all. A differential interconnect can be treated either as two separate simple interconnects, testing the structural connection between pins, or as a single extended interconnect, testing the functional connection between a single-ended transmission point and a single-ended reception point.

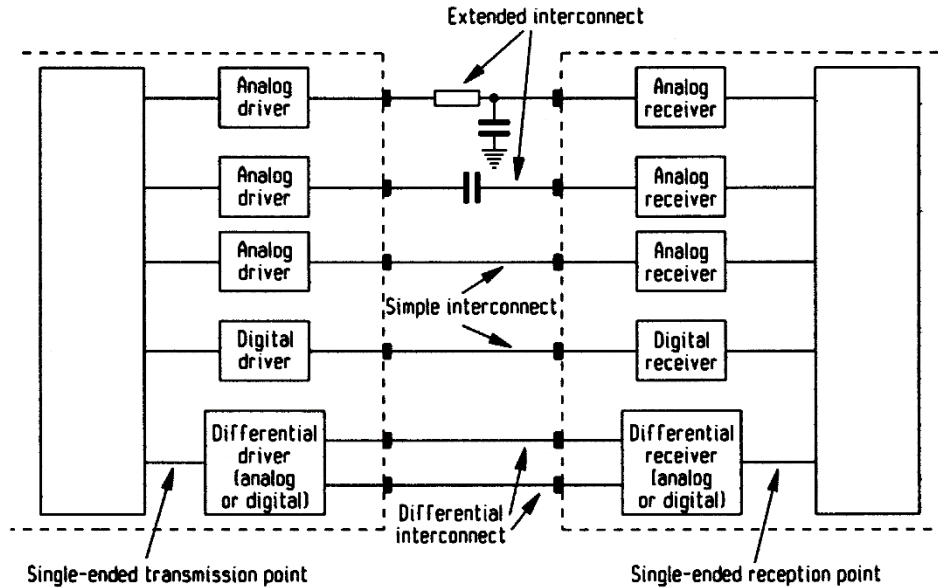


Figure 3—Simple, extended, and differential interconnect

A similar situation from the testing point of view is illustrated in Figure 4, where an analog signal to be transmitted is passed through an analog-to-digital converter, transmitted as a parallel set of digital signals, and passed through a digital-to-analog converter to form a received analog signal. Again, the interconnect can be tested by treating it as several separate simple digital interconnects and then by treating it as if it were a single analog connection between the transmitted and received signals, thereby allowing the overall transmission properties of the system to be assessed.

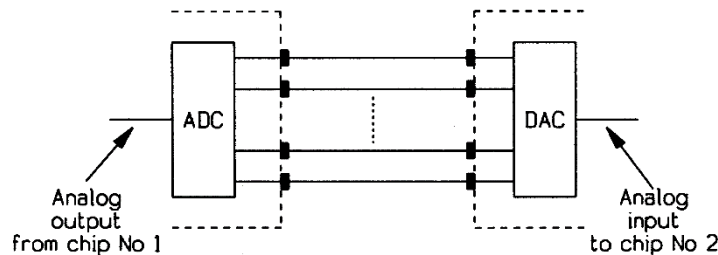


Figure 4—Multiple digital interconnect

1.6.4 Internal test

The third objective of this standard, internal test, relates to the ability to perform comprehensive tests on the components either in isolation or while mounted on a substrate. Since the incorporation of internal test structures, whose impact on the cost and performance of the circuit could be deemed unacceptable, this aspect of the standard is not mandatory. The addition of designer-defined test functions is not limited by this

standard, which allows for the incorporation of ad hoc testability features within the internal core structure. To make such features accessible to the end-user, it is important that they are fully documented (see 10.2).

1.7 Background reading

Readers unfamiliar with IEEE Std 1149.1 might find it helpful to study some relevant books and papers, some of which also discuss mixed-signal testing using structures related to this standard. See Annex A for an annotated bibliography of such items.

1.8 Logic diagram conventions

Table 1 shows the symbologies used for various elements that appear within this standard. Symbols for various elements are reasonably consistent, but can vary from figure to figure.

Table 1—Logic symbology used in this standard

Symbol name	Symbol in this document	Common logic symbol
Switch (transmission gate)		
Tristate buffer		
Multiplexer		
D flip-flop		

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1149.1™, IEEE Standard Test Access Port and Boundary-Scan Architecture.^{9, 10}

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3. Definitions, acronyms and abbreviations, and voltage source symbols

3.1 Definitions

For the purposes of this document, the following terms and definitions apply. The *IEEE Standards Dictionary Online* should be consulted for terms not defined in this clause.¹¹

analog boundary module (ABM): A circuit module connected between the core circuit and an analog function pin to provide facilities for test in a mixed-signal integrated circuit. *See:* **core circuit; function pin; mixed-signal circuit.**

NOTE—An ABM can be attached to a digital function pin in order to provide analog measurement capability to the pin.¹²

analog pin: A pin on an integrated circuit or other component that is intended to pass information represented as a current or voltage that can have any value between the limits defined by the driver or receiver to which it is connected. *Contrast with:* **digital pin.**

NOTE 1—Analog pins can have several forms. In addition to input, output, and bidirectional pins, which are analogous to corresponding digital forms, it is possible to have pins that do not readily fit into any of these categories (e.g., those supporting compensation elements for operational amplifiers). Any such pin that has no identifiable drive capability can be regarded for the purposes of this standard as an input pin.

NOTE 2—An analog pin can be put into a state in which no signals can pass in either direction between the pin and the core circuit. *See:* **high-Z; core circuit; core disconnect.**

NOTE 3—An analog pin can pass digital data using discrete levels that lie within its analog range.

analog test access port (ATAP): A set of two mandatory and two optional pins on a mixed-signal integrated circuit. The pins are connected to a bus allowing automatic test equipment to gain access to the components' on-chip analog test facilities. The mandatory pins are labeled AT1 and AT2; the optional pins (labeled AT1N and AT2N) are normally used for differential testing.

CD state: The state of an analog pin when it is isolated from the core circuit and all test circuits. *See also:* **core disconnect (CD); residual element.**

NOTE—When a pin is in the CD state, there could be residual elements to which it remains connected.

compliance-enable pins: A set of one or more pins on a component such that full compliance with the rules of this standard is achieved only when a defined pattern of enable signals (a compliance-enable pattern) is applied to the compliance-enable pins.

NOTE—There could be more than one compliance-enable pattern.

conceptual switch: A circuit feature, acting under the control of a digital control signal, that allows two circuit nodes to be electrically connected or isolated as though there were a switch between them. *See:* **switch.**

NOTE 1—Depending on physical constraints, such as size, power consumption, and electrical characteristics, it could be possible in any particular application to implement all, some, or none of the conceptual switches by conventional complementary metal oxide silicon (CMOS) transmission gates.

NOTE 2—The symbols shown in Figure 5 are used to represent conceptual switches in this standard. For a switch with active high control (Figure 5[a]), the switch is closed (Data line 1 = Data line 2) when Control = logic 1; for a switch with active low control [Figure 5[b)], the switch is closed when Control = logic 0. *See:* **logic 0, logic 1.**

¹¹ *IEEE Standards Dictionary Online* is available at: <http://dictionary.ieee.org>. An IEEE Account is required for access to the dictionary, and one can be created at no charge on the dictionary sign-in page.

¹² Notes in text, tables, and figures of a standard are given for information only and do not contain requirements needed to implement this standard.

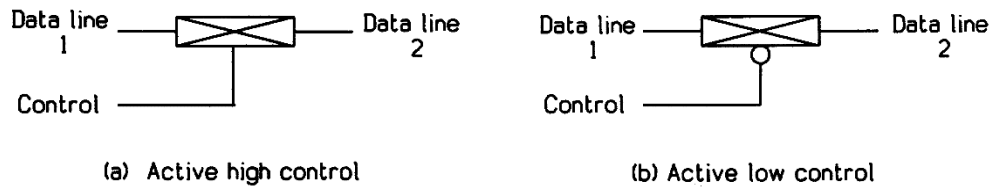


Figure 5—Conceptual switch symbols

core circuit: The part of the circuitry in an integrated circuit that provides the intended data manipulation function (as distinct from dedicated test circuitry). *See also:* **residual element**.

NOTE 1—The core circuit is analogous to the *system logic* in IEEE Std 1149.1.

NOTE 2—Residual elements, which are permanently connected to the pin (i.e., in test mode as well as in normal function mode), are not regarded as being part of the core circuit.

core disconnect (CD): A facility provided within an analog boundary module (ABM) (usually mediated by a conceptual switch) that allows a pin to be disconnected from the core circuit so that the signal at the pin can be driven to any value within the pin's normal functional range without affecting the core circuit, and no value generated in the core circuit affects the pin. *See:* **conceptual switch; core circuit**. *See also:* **high-Z; residual element; CD state**.

NOTE 1—The core disconnect facility could be provided as part of the functional driver or receiver attached to the pin, e.g., by implementing a driver with high-Z capability.

NOTE 2—It is necessary to document all residual elements that remain connected to the pin when the pin enters the CD state.

differential interconnect: A pair of connections carrying signals from a transmitter on one component to a receiver on another component, where the transmitted information (which can be either analog or digital) is represented by the difference between two signals rather than by either signal individually. *See also:* **simple interconnect; extended interconnect**.

digital boundary module (DBM): A circuit module connected between the digital core circuit and a digital function pin to provide facilities for test in a digital or mixed-signal component.

NOTE 1—A DBM serves the same function as, and conforms to the same rules as, the boundary-scan register cells defined in IEEE Std 1149.1.

NOTE 2—A DBM can contain one or more boundary-scan register cells as explained in IEEE Std 1149.1.

NOTE 3—A DBM can also be interposed at the boundary between the digital and analog portions of the core circuit.

NOTE 4—A control-and-observe DBM includes a switching function in the serial data path between pin and core. An observe-only DBM captures data from the data path without interrupting the path.

digital pin: A pin on an integrated circuit or other component that is intended to pass data represented as a voltage or current that can have one of two discrete values. *Contrast with:* **analog pin**.

NOTE 1—In this standard, the two discrete values are referred to as logic 0 and logic 1. *See:* **logic 0, logic 1**.

NOTE 2—In addition to the set of discrete data values, a digital pin might be put into a state in which its driver is disabled so that it cannot actively sink or source current and, therefore, cannot influence the state of the attached net. *See:* **high-Z; net**.

NOTE 3—If analog data are applied externally to a digital input pin, the internal circuitry typically interprets the data as digital. Use of the pin in this way can lead to possible adverse effects on the internal circuitry (e.g., power consumption).

NOTE 4—A digital function pin could have additional circuitry to allow analog signals to be applied or monitored for test purposes. This additional circuitry would not affect its status as a digital pin.

discrete component: An electrical element that is mounted on a printed circuit board or other substrate and connected to the interconnect wiring system but is not integrated to any significant extent with other elements and does not contain boundary module test circuitry adjacent to its pins. *See:* **interconnect**.

extended interconnect: A connection pathway consisting of two or more nets that includes one or more discrete components, where the test requirement is to verify both the integrity of the connections and the values of the components. *See:* **net**. *Contrast with:* **simple interconnect**. *See also:* **discrete component**.

function pin: An analog or digital pin on an integrated component that takes data into and/or out of the core circuit when operating in normal function mode. *Synonym:* **mission pin; system pin**.

NOTE—All pins carrying signals that affect the behavior of the component, including reference supply pins but excluding power supply pins and compliance-enable pins, are regarded as function pins.

high-Z: A condition in which the driver on a pin is inactive. The state of a net attached to a pin that is at high-Z is determined by values applied to other parts of the net. *See:* **net**. *Contrast with:* **CD state**. *See also:* **core disconnect**.

NOTE—For this standard, the impedance looking into a pin that is at high-Z is expected to be greater than 1 M Ω for any signal between V_{DD} and V_{SS} at any frequency up to 10 kHz.

in-circuit testing: A method of testing a printed circuit assembly by making direct physical contact between automatic test equipment and nets that are connected to the pins of individual components. *See:* **net**.

interconnect: The system of wiring that carries data and control signals between the different components mounted on a printed circuit assembly. *See also:* **simple interconnect; extended interconnect; differential interconnect**.

internal test bus: The system of wiring that carries analog test signals around the interior of an integrated circuit. *See:* **test bus interface circuit**.

logic 0, logic 1: The two logic voltage levels for digital signals. In positive logic systems, the more positive of the two logic voltage levels is taken to be logic 1.

NOTE 1—For convenience, positive logic is assumed throughout this standard.

NOTE 2—The voltage levels representing logic 0 and logic 1 are not necessarily the same at every function pin.

NOTE 3—Logic 0 and logic 1 are often represented as LO and HI, respectively.

mixed-signal circuit: A circuit in which some variables are represented by analog (continuously variable) quantities, and some variables are represented by digital (discrete) quantities.

net: An interconnection path between component pins where the resistance of the path is not significantly different from zero.

reference quality voltage: A dc source capable of sourcing and sinking current over a defined range without appreciable change of voltage and that is stable over a given time interval.

NOTE—Whether or not a given voltage source is of reference quality has a major impact on the accuracy of the measurement capabilities of the structures described in this standard.

residual element: A circuit element connected to a function pin that, for operational reasons, cannot be isolated from the pin in test mode. A residual element can be connected to a power supply pin—or another function pin or residual element—provided it can be modeled over a defined working range by a network of ideal resistors, capacitors, and inductors together with independent dc sources.

simple interconnect: A connection between two or more component pins consisting only of a net. *Contrast with:* **extended interconnect**.

switch: In the context of this standard, an electronic device connected between two data lines. A switch can exist in one of two states, referred to as “open” and “closed.” The state at any time depends on a digital control variable. When the switch is open, the pathway between the two data lines has a very high impedance (ideally infinite) so that signals appearing on the data lines could be considered completely independent. When the switch is closed, the pathway between the two data lines has a very low impedance (ideally zero) so that signals on the two data lines are considered identical.

NOTE 1—Practical electronic switches implemented in silicon depart from the ideal in at least three ways:

- a) In the “on” state, the pathway between the two data lines could have significant impedance, or the relationship between voltage and current could be non-linear (e.g., a voltage-dependent “impedance”).
- b) In the “off” state, there could be significant interaction between the signals on the two data lines due to, for example, stray capacitance.
- c) In either state, there could be significant leakage pathways through which current can pass from the data lines to the surrounding circuitry or vice versa.

The effects of all these characteristics are major considerations for the detailed implementation, especially in a system containing multiple-switch networks.

NOTE 2—A switching action effectively in series with the function signal pathway can sometimes be obtained without a physically separate device by incorporating a high-Z or enable facility into the functional circuitry. *See: **conceptual switch; high-Z**.*

NOTE 3—Data transmission through a switch is normally assumed to be bidirectional (as with electromechanical devices such as relays or semiconductor switches such as transmission gates). Some forms of switch can implement only unidirectional voltage or current dependence.

test access port (TAP): The test access port specified by IEEE Std 1149.1. *Contrast with: **analog test access port**.*

test bus interface circuit (TBIC): A circuit module that allows an internal analog test bus in an integrated circuit to be isolated from or connected to the pins in the analog test access port (ATAP). *See: **analog test access port**.*

test data: Data that are entered into an electronic system of any kind (component, printed circuit assembly, subsystem, system) to verify the integrity of part or all of the system. Test data can be entered through function pins, test pins, or both.

test pin: A pin on a component or a printed circuit assembly that is provided solely or primarily for use during test or maintenance operations.

3.2 Acronyms and abbreviations

ABM	analog boundary module
ADC	analog-to-digital converter
ATAP	analog test access port
ATE	automatic test equipment
BSDL	Boundary-Scan Description Language
CD	core disconnect
CMOS	complementary metal oxide silicon
CUT	circuit under test
DAC	digital-to-analog converter
DBM	digital boundary module
ESD	electrostatic discharge
FET	field effect transistor

GND	ground
I/O	input/output
PCA	printed circuit assembly
TAP	test access port
TBIC	test bus interface circuit
TCK	test clock
TDI	test data input
TDO	test data output
TMS	test mode select
TRST*	test reset (active low)

3.3 Voltage source symbols

Several voltage sources are required as part of the internal test structure described in this standard. The symbols used to denote these voltage sources are defined below. All of these sources are, in general, pin-specific.

V_{clamp} : A fixed voltage that can be applied to internal test buses when not in use to reduce the possibility of noise, crosstalk, or feedback.

V_G : A pin-specific reference quality voltage supplied to a component at a pin. Any function pin can be connected to V_G through its analog boundary module. *See:* **reference quality voltage**.

NOTE— V_G would normally be one of the power supply rail voltages.

V_H , V_L : Two dc voltages used as test signals on analog pins during interconnect testing and component measurement.

NOTE 1— V_H and V_L are pin-specific, and typically $V_H > V_L$.

NOTE 2— At output pins, V_H and V_L are supplied from the functional driver and will correspond to logic 1 and logic 0, respectively.

V_{TH} : A pin-specific voltage to which the voltage at a function pin is compared. The result of the comparison is a binary value that can be captured in the boundary-scan register.

4. Testability architecture

4.1 Overview

4.1.1 Specification rules

Specification rules for testability architecture include the following:

- a) The component shall conform to all provisions of IEEE Std 1149.1 except where specifically noted in this standard.

NOTE 1—This rule implies that a component conforming to this standard has a test access port (TAP) to provide access to the circuit for digital test signals. This TAP will contain three input lines (test data input [TDI], test clock [TCK], test mode select [TMS]) and one output line (test data output [TDO]); it can contain an optional fourth input line (test reset [TRST*]).

NOTE 2—In accordance with the rules of IEEE Std 1149.1, a component could require the application of a particular pattern of signals (a compliance-enable pattern) to a set of one or more compliance-enable pins before the component is brought into full compliance with this standard. There could be more than one compliance-enable pattern for a particular component.

NOTE 3—IEEE Std 1149.1 makes little provision for testing the analog portions of a mixed-signal component and contains a few rules relating to analog pins that are not compatible with the provisions of this standard.

NOTE 4—This rule implies that, when implementing this standard, the structure and performance of elements described in IEEE Std 1149.1 are in accordance with the specifications set out in IEEE Std 1149.1 except where the provisions of this standard are in conflict.

4.1.2 Description

This standard is an extension of IEEE Std 1149.1 and consists of additional structures to be added to an IEEE Std 1149.1-conformant component. Components that are conformant with this standard, when mounted on a common substrate with IEEE Std 1149.1-conformant components, allow common test operations (in particular, simple interconnect testing) to be performed in a consistent and coordinated manner.

The overall structure of a basic IEEE Std 1149.4-conformant component is illustrated in Figure 6, which shows the main mandatory elements of the standard. In IEEE Std 1149.1, the main testability features are a dedicated test access port (TAP), allowing test data to be passed to and from the circuit, and boundary modules associated with every digital function pin of the component, providing access to the core circuitry for the application of digital test stimuli and for the collection of digital test results. The IEEE Std 1149.4 extensions consist of analog boundary modules (ABMs) on every analog function pin, allowing access for analog test signals by way of an analog test access port (ATAP) consisting of two pins (AT1 and AT2), a test bus interface circuit (TBIC), and an internal analog test bus consisting of two lines (AB1 and AB2).

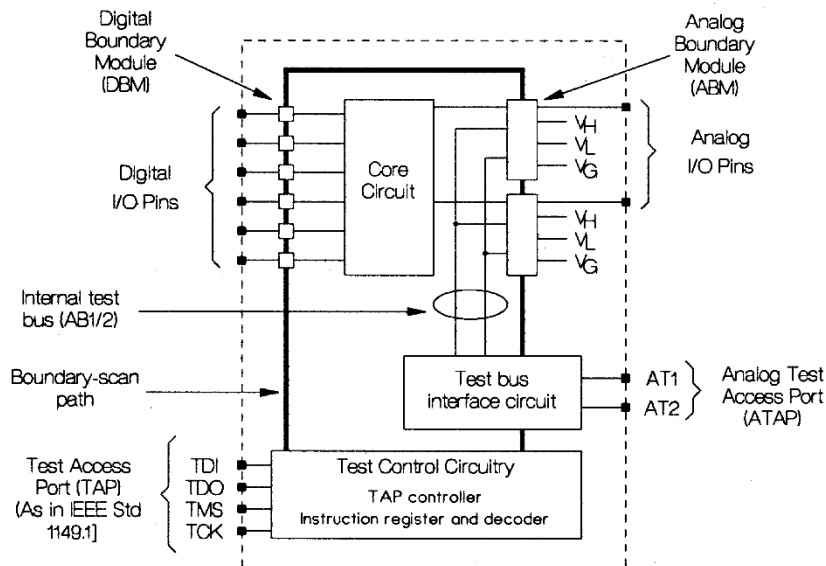


Figure 6—Structure of a basic (minimally configured) IEEE Std 1149.4-conformant component

The boundary modules associated with the digital pins are identical to the boundary cells, or groups of boundary cells, as specified in IEEE Std 1149.1. Boundary modules on analog pins, which are forbidden in IEEE Std 1149.1, form the main subject of this standard, in which they are mandatory. Each ABM has associated with it a set of voltages (V_H , V_L , and V_G). These voltages are defined on a pin-specific basis and, therefore, are not necessarily the same for each module.

Overall control of the testability structure rests with the test control circuitry, which consists of a TAP controller, an instruction register, and an instruction decoder.

4.2 TAP controller

4.2.1 State sequence

The TAP controller, which is identical to that mandated in IEEE Std 1149.1, is a synchronous finite state machine whose state transition diagram is shown in Figure 7. The state transitions are determined by the value present on TMS at the time of a rising edge on TCK.

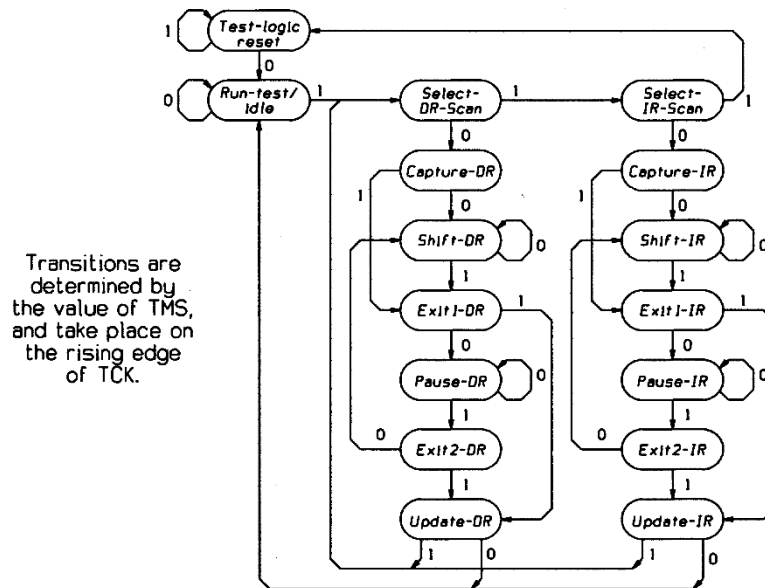


Figure 7—TAP controller state transition diagram

4.2.2 Initialization

The TAP controller is required to enter the *Test-Logic-Reset* state at power-up either by use of an optional additional pin in the TAP (TRST*) or as a result of circuitry built into the test logic. Further description of the initialization requirements can be found in IEEE Std 1149.1.

4.2.3 Controller outputs

4.2.3.1 Specification rules

Specification rules for controller outputs include the following:

- a) The TAP controller shall generate signals to control the operation of the TBIC as defined in 6.3.
- b) The TAP controller shall generate signals to control the operation of the ABMs and associated circuitry as defined in 7.3.5.
- c) When the TAP controller is in the *Test-Logic-Reset* state, all function pins shall be isolated from the analog test buses and from V_H , V_L , and V_G , irrespective of the state of the ABM control register bits.
- d) When the TAP controller is in the *Test-Logic-Reset* state, all ATAP pins shall be isolated from the analog test buses and from V_H , V_L , and V_{clamp} , irrespective of the state of the TBIC control register bits.

4.2.3.2 Description

Control signals for routing data, reconfiguring the test circuitry, and exerting control over the TAP, the ATAP, and the TBIC are derived partly from output logic of the TAP controller and partly from the instruction register. In addition, the TBIC and each ABM contain an individual control register so that their mode of operation can be individually controlled (see Clause 6 and 7.3). The instruction register, the ABM control registers, and the TBIC control register are all loaded through the TAP.

The precise set of signals required to control the test structure and boundary modules associated with digital function pins is not specified in IEEE Std 1149.1 except in terms of sample implementations. Boundary modules are not required by that standard to support all instructions; the control signals needed will vary depending on the particular set of instructions supported by the individual component. These signals occur on either the rising or the falling edge of TCK in each controller state as specified in IEEE Std 1149.1.

All the sample implementations of boundary-scan register cells described in IEEE Std 1149.1 use control signals ShiftDR and ClockDR and all those that incorporate the update register also use UpdateDR. Other control signals needed for the correct operation of the analog test structure can be generated by adding appropriate output logic to the TAP controller.

NOTE—Some output signals named in the sample implementations of IEEE Std 1149.1 and referred to in this standard have the same names as some controller states. Throughout this standard, where this ambiguity applies, control signals are shown in normal case (e.g., Shift-DR), and controller states are shown in italics (e.g., *Shift-DR*).

4.3 ATAP

4.3.1 Specification

4.3.1.1 Rules

Specification rules for ATAP include the following:

- a) Each component shall contain an ATAP.
- b) The ATAP shall include two analog test pins, AT1 and AT2 (defined in Clause 6).
- c) AT1 and AT2 shall be dedicated pins (i.e., they shall not be used for any other purpose).

4.3.1.2 Permission

Specification permission for ATAP includes the following:

- a) The ATAP may contain two further analog test pins, AT1N and AT2N, to allow for the testing of differential input and/or output. In this case, AT1 and AT1N shall form one differential pair, and AT2 and AT2N shall form the other differential pair.

4.3.2 Description

The ATAP is an analog port that provides access for analog test signals. Dedicated connections are required to allow access to the full range of mandatory features of this standard. The ATAP is composed of a minimum of one analog input connection and one analog output connection. Optional additional analog lines can provide additional capability (e.g., differential stimulus and/or measurement: see 8.1.3). The definition and properties of the TBIC are specified in Clause 6.

4.4 Register architecture

The test register architecture, shown in Figure 8, is essentially identical to that defined in IEEE Std 1149.1. It is entirely digital, consisting essentially of a number of shift-register paths, connected in parallel with a common serial data input connected to TDI and a common serial data output connected to TDO. Control signals are required both for the transfer of data and for the choice of which alternative parallel path is active. These signals are supplied, as shown in Figure 8, partly by the TAP controller and partly by the instruction decoder, which interprets the particular instruction loaded into the instruction register.

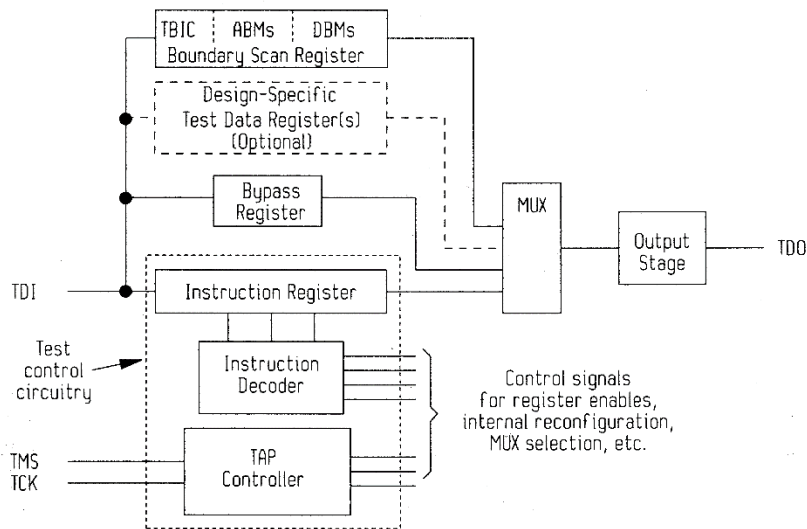


Figure 8—Test register architecture

The mandatory part of the test control architecture (as defined in IEEE Std 1149.1) consists of an instruction register and at least two test data registers:

- A bypass register
- A boundary-scan register (as defined in Clause 7)

The test register structure of a component conformant with this standard differs from that of an IEEE Std 1149.1-conformant component only in that additional shift-register stages are contained in the boundary-scan register. These additional stages consist of:

- The control stages in the ABMs (as defined in 7.3)
- The control stages in the TBIC (as defined in 6.3)

The order of the individual cells in the boundary-scan register can be chosen by the component manufacturer to suit layout convenience. It is not even necessary to keep the control stages belonging to a single ABM or to the TBIC together in a single block since the individual stages are identified by name.

An additional register (the device identification register) for part identification can be included as well as any number of design-specific test data registers to give access to design-specific testability features. An example of a design-specific test register that could be included in a mixed-signal design is an internal scan register used to give access to internal nodes of the core.

Depending on the style of implementation of the test logic defined by this standard, circuitry might be required to retime the signal passing through the output stage shown in Figure 8 to occur on the falling edge of TCK.

5. Instructions

5.1 General

5.1.1 Specification

5.1.1.1 Rule

Specification rules for instructions include the following:

- a) Each component shall provide a *PROBE* instruction (see 5.3.4).

5.1.1.2 Permissions

Specification permissions for instructions include the following:

- a) Additional instructions may be provided within the rules set out in this standard and in IEEE Std 1149.1.
- b) Any instruction code apart from all 1s may be used to represent any instruction.
NOTE—The instruction code consisting of all 1s is reserved for the *BYPASS* instruction.
- c) Any instruction (including *BYPASS* and *EXTEST*) may be represented by more than one instruction code.

5.1.2 Description

An instruction is a bit-pattern that is loaded into the instruction register and is then decoded by the instruction decoder. It has two major functions: It defines the set of test data registers that can operate while the instruction is selected, and it defines the serial test data register path that is used to shift data between TDI and TDO. The instruction set shall include one instruction (*PROBE*) designed to support analog testing and the mandatory instructions from IEEE Std 1149.1 (*BYPASS*, *SAMPLE*, *PRELOAD*, and *EXTEST*—some with extended facilities). It can also include user-defined instructions as well as optional instructions defined in IEEE Std 1149.1.

The remainder of this clause lists all defined instructions. Instructions that derive from IEEE Std 1149.1 shall satisfy the rules of that standard; the rules, recommendations, and permissions listed in this standard are additional to the specifications contained in IEEE Std 1149.1. The instruction that is unique to this standard is fully specified and described; others are described in general terms for convenience.

5.2 Response of test logic to instructions

5.2.1 Specification rules

Specification rules for the response of test logic to instructions include the following:

- a) Each component shall respond to the mandatory instructions of IEEE Std 1149.1 in accordance with the rules contained in IEEE Std 1149.1 and any additional rules listed in this standard.
- b) Each component shall respond to the *PROBE* instruction in accordance with the rules in this standard.
- c) If a component provides any optional instructions defined in IEEE Std 1149.1, its response to those instructions shall be in accordance with the rules contained in IEEE Std 1149.1 and any additional rules listed in this standard.

5.2.2 Description

The operation performed at any time by any particular digital boundary module (DBM) is determined in accordance with the rules of IEEE Std 1149.1. The operation performed at any time by any particular ABM is determined not only by the control signals supplied from the instruction decoder (which depend on the instruction currently loaded into the instruction register), but also by the control signals supplied by the TAP controller (which depend on the current state of the controller) and, depending on which instruction is selected, the values contained in the individual ABM control register.

The particular module design used in the test data registers (and the ABMs) determines what control signals are required from the TAP controller and the instruction decoder. For the ABM design shown in Figure 23, for example, ShiftDR, ClockDR, and UpdateDR would be supplied by the TAP controller; Mode1 and Mode2 would be supplied from the instruction decoder.

Each instruction is represented by one or more instruction codes and defines a particular test data register to be selected for serial connection between TDI and TDO. All instructions are defined in such a way that unselected test data registers have no effect on the operation of either the core circuitry or the selected test data register unless specifically mandated in the instruction definition.

When implementing the instruction decoder, it is important to consider the possible effects of decoding spikes when changing from one instruction to another (e.g., from *BYPASS* to *SAMPLE*) so that transitory instruction selections are reduced.

5.3 Mandatory instructions

5.3.1 The *BYPASS* instruction

5.3.1.1 Specification rules

Specification rules for the *BYPASS* instruction include the following:

- a) When the *BYPASS* instruction is selected, all ATAP pins shall be isolated from the internal analog test buses and from all test voltage sources, irrespective of the state of the boundary register bits.
- b) When the *BYPASS* instruction is selected, all analog function pins shall be connected to the core circuit.

- c) When the *BYPASS* instruction is selected, all analog function pins shall be isolated from the internal and external analog test buses and from all test voltage sources, irrespective of the state of the boundary register bits.

5.3.1.2 Description

The *BYPASS* instruction selects the bypass register to be connected for serial access between TDI and TDO in the *Shift-DR* controller state. The *BYPASS* instruction can be selected by loading logic 1 into every stage of the instruction register. (This coding is mandatory; optionally, other codes can also be designed to select *BYPASS*.)

When the *BYPASS* instruction is selected, test data registers that can operate in either system or test mode perform their system function, and the operation of the test logic has no effect on the action of either the analog or the digital core circuitry.

5.3.2 The *SAMPLE* and *PRELOAD* instructions

5.3.2.1 Specification rules

Specification rules for *SAMPLE* and *PRELOAD* instructions include the following:

- a) When the *SAMPLE* or *PRELOAD* instruction is selected, all ATAP pins shall be isolated from the internal analog test buses and from all test voltage sources, irrespective of the state of the boundary register bits.
- b) When the *SAMPLE* or *PRELOAD* instruction is selected, all analog function pins shall be connected to the core circuit.
- c) When the *SAMPLE* or *PRELOAD* instruction is selected, all analog function pins shall be isolated from the internal and external analog test buses and from all test voltage sources.

5.3.2.2 Description

SAMPLE uses the boundary-scan register to allow a snapshot to be taken of the data at the digital pins during normal operation. The snapshot is taken on the rising edge of TCK in the *Capture-DR* controller state and can be examined serially by shifting through TDO.

A digitized snapshot of the (analog) signal on an analog pin is captured in *SAMPLE* by way of the one-bit digitizer in the ABM (see 7.3). The ability to monitor the analog signal itself is provided by the *PROBE* instruction (see 5.3.4).

PRELOAD allows an initial digital data pattern to be loaded into the latched parallel outputs of the boundary-scan register prior to the selection of another boundary-scan test operation. The loading is performed on the falling edge of TCK in the *Update-DR* controller state. During the *PRELOAD* phase, the operation of the core circuit and the flow of signals between the function pins and the core circuit are unaffected by the test logic.

In the same way, a digital data pattern can be specified for each ABM by loading the appropriate values into its control register, which is part of the boundary-scan register.

5.3.3 The *EXTEST* instruction

5.3.3.1 Specification rule

The specification rule for the *EXTEST* instruction includes the following:

- a) When the *EXTEST* instruction is selected, each ABM shall be set so that the pin is disconnected from the core (i.e., the core disconnect switch shall be open).

5.3.3.2 Description

The *EXTEST* instruction is used to test simple interconnects as in IEEE Std 1149.1 by applying logic levels to all pins. It is also used to test extended interconnects by allowing automatic test equipment (ATE) to make measurements of discrete components connected to the pins. The facilities incorporated into the boundary-scan test structure allow the ATE to apply analog test signals and monitor analog responses and hence to obtain one of the major benefits of in-circuit testing without using physical probing. This instruction is the central feature of this standard. The principles underlying its use for analog measurements are outlined in Clause 8.

The *EXTEST* instruction selects the boundary-scan register to be connected for serial access between TDI and TDO in the *Shift-DR* controller state. While the *EXTEST* instruction is selected, all function output pins (analog and digital) are isolated from the core. This core disconnect (CD) state allows the signals driven from system output pins to be completely defined by the data shifted into the corresponding boundary modules. Function input pins (analog and digital) are monitored by their boundary modules and can be isolated from the core. If the facility to isolate input pins from the core during testing is not incorporated, designer verification ensures that signals appearing at an input pin during *EXTEST* execution do not cause damage to the core, affect measurements on other pins, or be affected by core signals.

It is suggested that the *EXTEST* instruction not be represented by the all 0s code, but represented by other code(s).

NOTE—If the all 0s code is chosen to represent *EXTEST*, a stuck-at-zero fault on TDI could then result in an unwanted selection of *EXTEST*.

5.3.4 The PROBE instruction

5.3.4.1 Specification rules

Specification rules for the *PROBE* instruction include the following:

- a) The *PROBE* instruction shall select the boundary-scan register to be connected for serial access between TDI and TDO in the *Shift-DR* controller state.
- b) When the *PROBE* instruction is selected, each DBM shall be set to allow core functions to propagate to and from the pins.

NOTE—This behavior is similar to the requirements in *SAMPLE*, *PRELOAD*, and *BYPASS*.

- c) When the *PROBE* instruction is selected, each ABM shall be set so that its pin is connected to the core (i.e., the core disconnect switch shall be closed).
- d) When the *PROBE* instruction is selected, one or both of the ATAP pins shall be connected to the corresponding internal analog test bus lines.
- e) When the *PROBE* instruction is selected, the internal analog test bus lines shall be connected to individual function pins as determined by the contents of the corresponding ABM control registers.

NOTE—The *PRELOAD* instruction may be used to set up the contents of the ABM and TBIC control registers before the *PROBE* instruction is selected.

5.3.4.2 Description

The *PROBE* instruction allows analog pins to be monitored on AB2, and/or stimulated from AB1, while the component is operating in its normal mission configuration with all function pins connected to the core.

5.4 Optional instructions

5.4.1 The *INTEST* instruction

5.4.1.1 Specification rules

Specification rules for the *INTEST* instruction include the following:

- a) While the *INTEST* instruction is selected, all inputs to the digital part of the core shall be supplied by data stored in the boundary-scan register, except clocks, which may be allowed to free-run provided that the component can be single-stepped through the test sequence.

NOTE—The *PRELOAD* instruction can be used to set up the contents of the boundary-scan register (including the ABM control registers) before the *INTEST* instruction is selected.

- b) While the *INTEST* instruction is selected, all analog pins shall be connected to the analog core.

NOTE—Because, in this mode of operation, much of the core is not isolated from the external circuitry, it can be necessary to control this external circuitry to help avoid unwanted interference. Care needs to be taken to verify that the core itself does not generate unwanted interference.

- c) While the *INTEST* instruction is selected, any analog pin shall be capable of being connected to AB1.

NOTE—Because normally only one analog test bus input line is available, only one analog stimulus can be supplied, although, if desired, the signal at AB1 could be applied to more than one input pin.

- d) While the *INTEST* instruction is selected, inputs to the analog core that are normally supplied from the digital core shall receive data determined by the contents of the corresponding DBMs.

NOTE—The *PRELOAD* instruction can be used to set up the contents of the DBMs before the *INTEST* instruction is selected.

- e) While the *INTEST* instruction is selected, any analog pin shall be capable of being monitored by AB2.

NOTE—The signal monitored by AB2 can be affected by more than one input. It might be necessary to apply external control to those inputs that are not being driven by AB1.

5.4.1.2 Description

The optional *INTEST* instruction is intended to allow testing of the core circuitry of a component while it is mounted on a printed circuit board. It selects the boundary-scan register to be connected for serial access between TDI and TDO in the *Shift-DR* controller state. If *INTEST* is provided, IEEE Std 1149.1 requires a DBM to be connected at each digital interface with the on-chip analog circuitry (see 7.2), as illustrated in Figure 9.

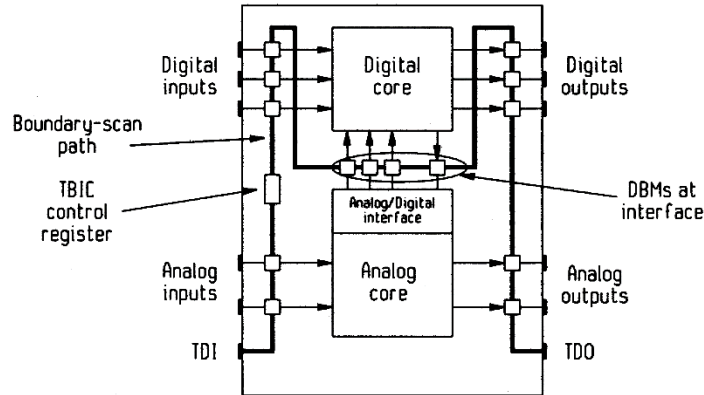


Figure 9—A component supporting INTEST (or RUNBIST) showing internal boundary modules

If the *INTEST* instruction is provided, it permits the same test of the digital core as would be the case with a component conforming to IEEE Std 1149.1. In addition, the presence of the analog test structure permits some testing of the analog core.

In accordance with the rules of IEEE Std 1149.1, while the *INTEST* instruction is selected, all outputs from the digital part of the core are captured in the boundary-scan register on the rising edge of TCK in the *Capture-DR* controller state.

The behavior noted above, together with Rule 5.4.1.1 a), provides that, as far as the digital part of the core is concerned, the operation of the instruction is exactly as described in IEEE Std 1149.1. Every input to the digital core, whether normally supplied from a function pin or from the analog core, should have test data supplied by the boundary-scan register. Every output from the digital core, whether normally connected to a function pin or to the analog core, should be captured in the boundary-scan register.

Figure 10 illustrates this part of the operation as applied to the component shown in Figure 9. The DBMs mandatorily fitted between the digital and analog cores enable complete isolation of the analog core while the digital core is being tested.

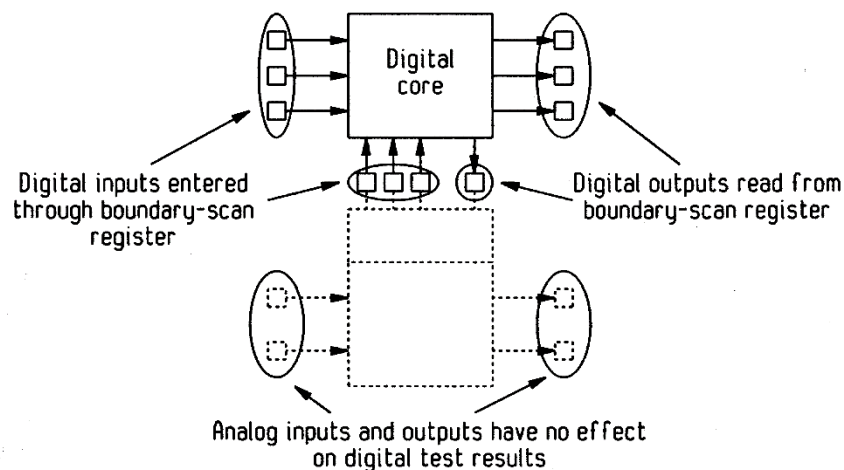


Figure 10—Testing the digital core in INTEST

Rule 5.4.1.1 b) through Rule 5.4.1.1 e) are provided to support the testing of the analog core. If only one pair of analog test bus lines exists, only one analog input signal can be supplied, and only one analog output can be fully monitored. However, it might be possible to supplement this limited access by additional direct probing. Furthermore, a one-bit digital representation of the voltage appearing at each analog pin shall be captured in the ABM control register on the rising edge of TCK in the *Capture-DR* controller state (see Rule 7.3.1.1 f)).

A typical analog core test, as it might be applied to the circuit of Figure 9, is illustrated in Figure 11. In this test, one of the analog outputs is being monitored through AT2 while one of the inputs is being supplied with an analog stimulus through AT1. Other inputs to the analog core include the signals normally supplied by the digital core and those coming from other analog function pins. During *INTEST*, the digital signals will be supplied from the boundary-scan register (into which appropriate data are scanned). Rule c) of 5.4.1.1 draws attention to the fact that all the analog pins (including the one being stimulated by way of AB1) are connected to the external circuitry on the board. This circuitry may have to be controlled to provide appropriate operating conditions or to verify that the input is rendered quiescent.

In addition to the analog output chosen for observation at AT2, digital test result data are captured in the DBMs in the analog/digital interface, and digitized results are captured in the control registers of all ABMs. These data are captured on the rising edge of TCK in the *Capture-DR* controller state. Further test results for the same stimulus conditions could be obtained by repeating the test while monitoring each analog output in turn.

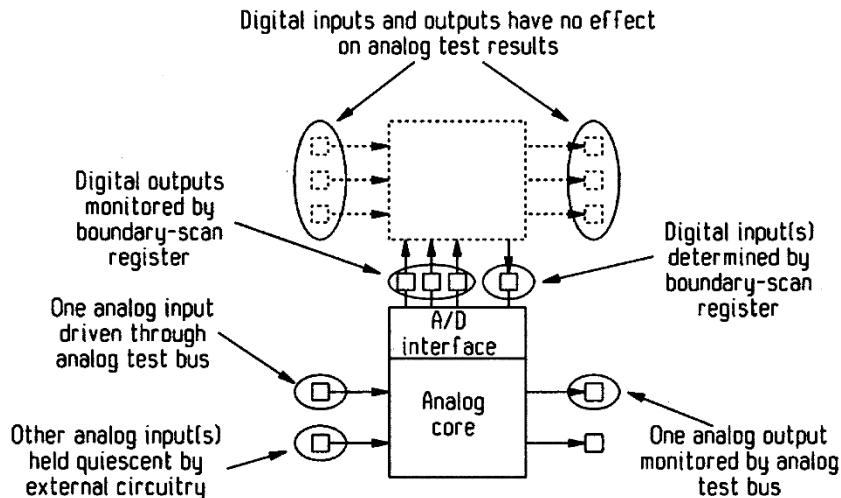


Figure 11—Testing the analog core in *INTEST*

5.4.2 Device identification register instructions

These instructions make use of the optional identification register to allow internally stored codes to be read serially from TDO to identify the manufacturer, part number, and version of the part. As far as the digital part is concerned, the behavior in response to these instructions of a component claiming conformance to this standard is substantially identical to the behavior of an IEEE Std 1149.1–conformant component.

5.4.2.1 The IDCODE instruction

5.4.2.1.1 Specification rules

Specification rules for the IDCODE instruction include the following:

- a) When the *IDCODE* instruction is selected, all ATAP pins shall be isolated from the analog test buses, irrespective of the state of the boundary register bits.
- b) When the *IDCODE* instruction is selected, all analog function pins shall be connected to the core.
- c) When the *IDCODE* instruction is selected, all analog function pins shall be isolated from the internal and external analog test buses and from all test voltage sources.

5.4.2.1.2 Description

If the device identification register is included in the design, then the *IDCODE* instruction shall be supported. This instruction is loaded into the instruction register on the falling edge of TCK following entry into the *Test-Logic-Reset* controller state. The instruction can also be loaded serially through TDI while in the *Shift-IR* controller state.

When the *IDCODE* instruction is selected, the manufacturer's identification code is loaded into the identification register on the rising edge of TCK following entry into the *Capture-DR* controller state and can then be read serially through TDO.

5.4.2.2 The USERCODE instruction

5.4.2.2.1 Specification rules

Specification rules for the USERCODE instruction include the following:

- a) When the *USERCODE* instruction is selected, all ATAP pins shall be isolated from the analog test buses, irrespective of the state of the boundary register bits.
- b) When the *USERCODE* instruction is selected, all analog function pins shall be connected to the core.
- c) When the *USERCODE* instruction is selected, all analog function pins shall be isolated from the internal and external analog test buses and from all test voltage sources.

5.4.2.2.2 Description

If the device identification register is included in the design and if the component is user-programmable so that the programming cannot otherwise be determined by the test logic, then the *USERCODE* instruction could be provided and a user-programmed identification code could be included in the component. When the *USERCODE* instruction is selected, this code is loaded into the identification register on the rising edge of TCK following entry into the *Capture-DR* controller state and can then be read serially through TDO.

5.4.3 The RUNBIST instruction

5.4.3.1 Specification

5.4.3.1.1 Rules

Specification rules for the RUNBIST instruction include the following:

- a) The *RUNBIST* instruction shall be self-contained and shall leave a single test result signature in the test data register selected by the *RUNBIST* instruction.

NOTE 1—The signature could be derived from a self-test conducted on the digital part of the core while maintaining the analog part in a quiescent state, or the circuit could be designed to incorporate structures necessary to support analog stimulus generation and result collection (and digitization) to produce a composite signature.

NOTE 2—The test data register is selected by the designer. It could be the boundary-scan register.

- b) While *RUNBIST* is selected, analog function outputs shall behave in one of two ways:
 - 1) All output signals shall be defined by the data held in the boundary-scan register; or
 - 2) Every output signal shall be placed in the inactive CD state, which may be high-Z.

NOTE—These options are the same as those offered in IEEE Std 1149.1 for digital output pins.

- c) The choice of output behavior (see 5.4.3.1.1 b)) shall be the same for analog and digital pins.

5.4.3.1.2 Recommendation

The recommendation for *RUNBIST* instruction includes the following:

- a) The test result should be a multi-bit signature.

NOTE—The purpose of a multi-bit signature is to allow a failed self-test to record diagnostic information rather than a simple GO/NOGO decision.

5.4.3.2 Description

The *RUNBIST* instruction is optional, but in IEEE Std 1149.1 it is recommended that either *INTEST* or *RUNBIST* be supported. If *RUNBIST* is supported, it is self-contained, executing while in the *Run-Test/Idle* controller state. It leaves, in the test data register connected between TDI and TDO (which could be the boundary-scan register), a test result signature that is independent of any external signals present at any of the pins. A mixed-signal circuit claiming conformance with this standard is required to provide exactly the same facilities.

5.4.4 The CLAMP instruction

5.4.4.1 Specification rules

Specification rules for the *CLAMP* instruction include the following:

- a) When the *CLAMP* instruction is selected, the state of all signals driven from analog function output pins shall be defined by the data held in the corresponding ABMs.
- b) While the *CLAMP* instruction is selected, the data held in the ABMs shall not change.
- c) When the *CLAMP* instruction is selected, the state of the AT1 and AT2 pins shall be defined by the data held in the TBIC control register (see 6.3).

5.4.4.2 Description

The optional *CLAMP* instruction selects the bypass register for connection between TDI and TDO in the *Shift-DR* controller state. While the *CLAMP* instruction is selected, the states of all signals driven from system output pins (analog and digital) are determined by the contents of the boundary modules. (These data can be previously inserted, e.g., by using the *PRELOAD* instruction.)