

1149.6™

IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks

IEEE Computer Society

Sponsored by the
Test Technology Standards Committee



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IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks

Sponsor

**Test Technology Standards Committee
of the
IEEE Computer Society**

Approved 20 March 2003

IEEE-SA Standards Board

Abstract: This standard augments IEEE Std 1149.1 to improve the ability for testing differential and/or ac-coupled interconnections between integrated circuits on circuit boards and systems.

Keywords: AC-coupled signaling, Boundary-Scan, circuit boards, differential signaling, integrated circuits, interconnect test, printed circuit boards, test

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Introduction

(This introduction is not part of IEEE Std 1149.6-2003, IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks.)

The development of this standard was begun 21 May 2001, by an ad hoc industry Working Group called by Agilent Technologies and Cisco Systems. This group formulated this standard, with the intention of handing it over to the IEEE for formal standardization when the underlying technology became understood.

The group adopted as its mission:

To define, document, and promote a means for designing ICs that support robust Boundary-Scan testing of boards where signal pathways make use of differential signaling and/or AC-coupled technologies. This technology utilizes and is compatible with the existing IEEE Std 1149.1. The goal is to upgrade the capabilities of IEEE Std 1149.1 to maintain the rapid and accurate detection and diagnosis of interconnection defects in boards and systems despite the fault-masking effects of differential signaling and the DC blocking effects of AC-coupled signaling.

The group first referred to itself as the “AC EXTEST” Working Group, but since expanded its charter to consider topics now called “Advanced I/O.”

The following is a list of participants in the Advanced I/O Working Group. Voting members at the time of publication are marked with an asterisk (*).

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IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks

1. Overview

1.1 Scope

This standard defines extensions to IEEE Std 1149.1TM to standardize the Boundary-Scan structures and methods required to ensure simple, robust, and minimally intrusive Boundary-Scan testing of advanced digital networks.¹ Such networks are not adequately addressed by existing standards, especially for those networks that are AC-coupled, differential, or both. Testing enabled by this standard will operate in parallel with IEEE Std 1149.1 testing of conventional digital networks and in conjunction with IEEE Std 1149.4TM testing of conventional analog networks. This standard also specifies software and Boundary-Scan Description Language (BSDL) extensions to IEEE Std 1149.1, which are required to support new I/O test structures.

1.2 Organization of the standard

Clause 1, Overview, provides an overview and context for this standard.

Clause 2, References, provides references necessary to understand this standard.

Clause 3, Definitions and acronyms, defines terminology and acronyms used in this standard.

Clause 4, Technology, is a tutorial that outlines the technologies addressed and utilized by this standard. This clause does not contain rules.

Clause 5, Instructions, provides rules for instructions used for testing.

Clause 6, Pin implementation specifications, provides rules for I/O pin implementation.

Clause 7, Conformance and documentation requirements, provides rules for conformance and documentation of devices designed to this standard.

Annex A, Applications and tools, shows how this standard is used in typical testing applications and how devices conforming to this standard can be verified before manufacture and tested in production.

¹Information of references can be found in Clause 2.

Annex B, Noise rejection in edge-detecting mode, gives guidance for designing test receivers with noise rejection capabilities.

Annex C, Advanced I/O Boundary-Scan Register cells, documents new Boundary-Scan Register cells used by this standard.

Annex D, Test receiver design examples, shows how the input pins of some common logic families can be designed to conform with this standard.

Annex E, A proposed “INITIALIZE” instruction, provides the outline of a proposed instruction that forcibly initializes complex devices into a state where testing operations can then proceed. This instruction is not yet fully developed nor is this portion of this standard normative. It is included here to alert the test standards community about the need for such an instruction and to invite comment.

Annex F, Bibliography

1.3 Context

Figure 1 shows a printed circuit board containing many types of devices. Of these, some could be compliant with IEEE Std 1149.1 for the support of testing activities. These devices contain Boundary-Scan testability circuitry which allows them to participate in manufacturing tests that detect and diagnose faults such as open solder joints, shorts and missing devices.

The additional testability elements added by this standard to these same integrated circuits (ICs) allow this interconnect testing, with enhanced coverage, to be conducted on differential signal pathways and/or where AC-coupling (which blocks normal DC Test Signals) has been used on signal paths between ICs.

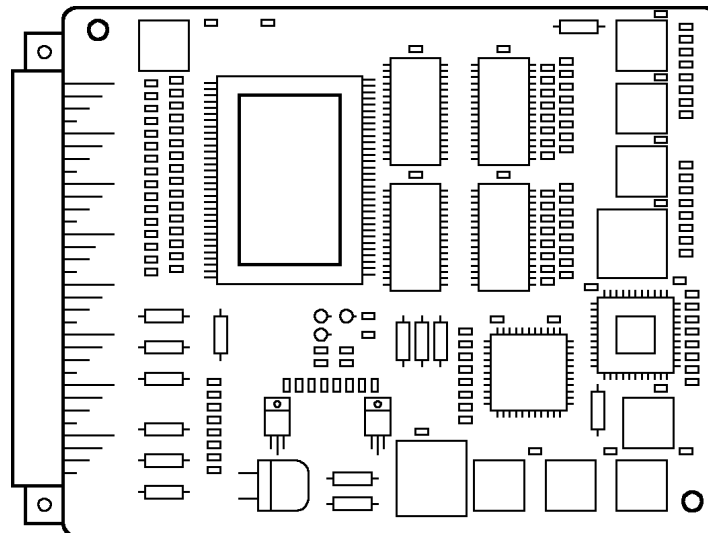


Figure 1—A printed circuit board containing a variety of components interconnected by printed wiring. Some ICs contain IEEE Std 1149.1 features that support Boundary-Scan interconnect testing.

This standard is built on top of IEEE Std 1149.1 using the same Test Access Port structure (with 4, optionally 5 pins) and Boundary-Scan architecture. It adds the concept of a “test receiver” to input pins that are expected to handle differential and/or AC-coupling. It adds two new instructions that cause drivers to emit AC waveforms that are processed by test receivers.

1.4 Objectives

The objective of this standard is to provide design guidance for testability circuitry added to an IC in addition to testability provisions specified by IEEE Std 1149.1, such that when such an IC contains differential signaling and/or is AC-coupled with other ICs compliant to this standard, board and system level tests can be readily and accurately conducted, with enhanced defect coverage.

Devices that adhere to this standard that are used in differential and/or AC-coupled signaling environments will realize significant savings in testing costs for boards and systems. Tools that are cognizant of the capabilities provided by this standard will be able to prepare, run, and interpret these tests in a highly automated fashion, with high diagnostic resolution.

This standard allows devices created by multiple vendors to operate together during testing despite the differing characteristics and parameters of the IC processes used to fabricate the devices. This standard also provides design guidance to board and system designers that will enhance the performance of the testability features of their products. This in turn will reduce system and production costs.

2. References

This standard shall be used in conjunction with the following standards. When the following standards are superseded by an approved revision, the revision shall apply.

IEEE Std 1149.1-2001, IEEE Standard Test Access Port and Boundary-Scan Architecture.^{2,3}

IEEE Std 1149.4-2000, IEEE Standard for a Mixed-Signal Test Bus.

3. Definitions and acronyms

For purposes of this standard, the following terms and definitions apply. IEEE 100, *The Authoritative Dictionary of IEEE Standards Terms*, Seventh Edition [B1],⁴ should be referenced for terms and definitions not defined in this clause.

3.1 Definitions

Defined terms appear in **bold type**.

3.1.1 AC-coupling: The use of series capacitance in a **signal path**. This coupling will block DC voltages on the drive side of the path from appearing on the receive side. Only the AC component of the driven signal will pass through the coupling, with the effect of high-pass filtering imposed on the original signal. *Contrast:* **DC-coupling**.

NOTE—AC-coupling may also be accomplished with transformers which, as with capacitive coupling, form a high-pass filtered transmission structure. While the principles used and rules defined in this standard apply to transformer coupling, this coupling technology is less often used and is thus omitted to simplify discussion.

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⁴The numbers in brackets correspond to those of the bibliography in Annex F.

3.1.2 AC pins: **Advanced I/O** pins that require a time-varying (AC) signal to permit testing of their interconnections. This includes all **differential signal** pins and differential or **single-ended signal** pins that are expected by design to support **AC-coupling**. *Contrast:* **DC pins**.

3.1.3 AC test mode: A **test mode** that enables Boundary-Scan testing between **AC pins** that are **AC-coupled** or **DC-coupled**. AC testing of DC-coupled pins may enable testing that cannot be supported in **DC test mode** due to voltage level incompatibilities. *Contrast:* **DC test mode**.

3.1.4 AC Test Signal: A signal generated by the **AC test mode** that is used to modulate static test data into a time-varying signal that can pass through **AC-coupling**. A test receiver and detector is used to recover the static test data value from within the time-varying signal.

3.1.5 Advanced I/O: Input/output (I/O) circuits and protocols that are designed to convey digital information, the interconnections of which cannot, either by design or by common usage, be adequately tested with static digital signals such as those provided for in IEEE Std 1149.1. For example, such an I/O pin may be self-referenced (i.e., to its own average voltage), or referenced to another I/O pin, rather than to a fixed voltage.

3.1.6 bias: A high-impedance (relative to line and termination impedance, typically >1000 ohms) voltage source often used on the input of a mission receiver to cause it to output a deterministic state in the absence of an input signal, and/or to select the **common-mode voltage** seen by a **differential receiver** in **AC-coupled** signal paths.

3.1.7 bias network: A network of impedances, usually higher valued than **termination** impedances and usually located in or near the receiver, used to establish a **common-mode** or **reference voltage**.

3.1.8 Boundary-Scan testing: Testing of interconnections between IC pins as supported by IEEE Std 1149.1 and this standard. This testing technology looks for manufacturing defects along **signal paths**, which include open solder joints, broken bond wires, shorted signal traces, damaged drivers and receivers, etc. Tests are performed on many paths in parallel.

3.1.9 channel: A **signal path** or set of signal paths that transmits a single data stream from a source to a destination. *See:* **differential signaling**; **single-ended signaling**.

3.1.10 characteristic impedance: The ratio of the complex voltage and complex current of a signal traveling forward on a conductive path. A **signal path** is often **terminated** with an impedance that matches the characteristic impedance of the path. This makes the path appear to be infinitely long and prevents signal degradation due to reflections that occur at unterminated ends of the path. *See:* **termination**.

3.1.11 common-mode noise: A noise signal added equally to both **signal paths** in a differential signal **channel**. Common-mode noise will affect or completely disrupt a single-ended measurement of a signal on one leg of a differential receiver, yet this **differential receiver** will accurately recover the signal within the noise.

3.1.12 common-mode range: The range of common-mode voltage that a differential receiver is capable of receiving while maintaining reliable signal recovery. A differential signal with common-mode voltage within this range will be received correctly. Outside this range the receiver may fail to recover the data signal.

3.1.13 common-mode voltage: The offset from ground of the mean of the maximum and minimum voltages that appear on a pair of differential signals. A **differential driver** will, by its operational characteristics, define a common-mode voltage. A **differential receiver** will properly receive data over a range of common-mode voltages, but will likely have an optimal common-mode voltage where its performance is best. When

the optimal common-mode voltage of a receiver is significantly different than that of its associated driver, **AC-coupling** with appropriate **bias** can be used to match the two components of a differential **channel**.

3.1.14 comparator: An amplifier with two inputs labeled positive and negative, typically with very high input impedance. The amplifier usually has very high gain and produces an output signal that is the amplified difference of the positive and negative input signals. For all but the smallest differences, the output will be $V_{\max}$ or $V_{\min}$, which are the most positive and most negative voltages the amplifier can produce on its output. A comparator can be used as a **differential receiver**. A comparator can be used to determine if an input signal is logically above or below a **reference voltage**.

3.1.15 current signaling: A signal encoded by the amplitude and direction of current flow. In a differential pair, a current signal is positive when current flows from positive to negative legs, and negative in the reverse direction. The voltage that may appear on these same legs does not carry information. *Contrast:* **voltage signaling**.

3.1.16 DC-coupling: The use of simple wires or small series resistances in a signal path. *Contrast:* **AC-coupling**.

3.1.17 DC pins: DC pins are single-ended pins that are DC-coupled. DC pins only need be equipped with test resources defined by IEEE Std 1149.1. DC pins that are AC-coupled are not normally testable as a **signal path**, but may be testable as logically independent pins if there are enough test resources on each pin. *Contrast:* **AC pins**.

3.1.18 DC test mode: A **test mode** that enables traditional **Boundary-Scan testing** between **DC pins** that are **DC-coupled**. *Contrast:* **AC test mode**.

3.1.19 defect: A defect is an unacceptable deviation from a norm; for example, an open solder joint. Because it is unacceptable, some remedial action is needed. *See:* **fault; manufacturing process defect**.

3.1.20 deprecated: Used in this standard for possible configurations or modes of operation that may not operate reliably and should be either avoided or treated with special care. (Synonyms: disapproved, belittled, discouraged, disparaged.)

3.1.21 derived voltage reference: A voltage reference derived from: 1) other references, such as a resistive divider between power and ground, or 2) a resistive divider between two differential signals that recovers the **common-mode voltage** of the signals.

3.1.22 differential driver: A driver that accepts a single data stream and drives it onto two independent signal paths where one signal is the inverse of the other. The two signals are centered at the **common-mode voltage**.

3.1.23 differential receiver: A receiver that recovers a single data stream encoded differentially on two signal paths. It effectively subtracts the signal on its negative leg from that on its positive leg. This eliminates **common-mode noise** appearing on both legs.

3.1.24 differential signaling: The use of two independent signal paths in a channel to carry a single data stream, where one path carries an inverted copy of the signal that appears on the other path. The original data signal can be reconstructed by taking the difference of the two signals and there is no reliance on a reference voltage for determining this signal. This has the property of eliminating **common-mode noise** in the transmitted signal. *Contrast:* **single-ended signaling**.

3.1.25 encoding protocol: A stream of data bits may be encoded into a new (typically longer) data stream that has characteristics favorable for its transmission on a **channel**. The encoded stream may have added redundancy to support error correction. The encoded stream may have extra bits added to deliberately

increase the number of transitions that appear in the stream, effectively raising its apparent **frequency** and facilitating data transmission that encodes clocking information into the stream.

3.1.26 fault: A fault is a physical manifestation of a **defect**. For example, an open solder joint (a defect) on the input to an IC may cause one or more of its outputs to produce incorrect data (a physical manifestation). In many cases, a fault and its causal defect are not co-located.

3.1.27 frequency: The number (f) of transition pairs that occur on a signal path in a period of time, expressed in Hertz (cycles per second). With respect to **AC-coupling**, a frequency is *high* when the period ($1/f$) is small compared to the **time constant** of the coupling. A frequency is *low* when the period is large compared to the time constant of the coupling. The frequency appearing on a signal path may vary greatly over time as a function of the data being transmitted and the data **encoding protocol**.

3.1.28 float: The input to a receiver that is connected to an undriven signal, or a high-impedance connection to a receiver input, is said to *float*.

3.1.29 high-pass filter: An electrical network that passes higher frequencies and attenuates lower frequencies. DC current is blocked.

3.1.30 HPLP_Ratio: High-Pass-Low-Pass Ratio, a multiplier used to derive the minimum ratio of high-pass coupling time constant (**HP_Mult**) to low-pass filter time constant (**LP_Mult**).

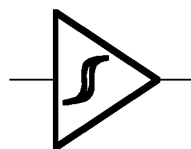
NOTE—See 6.2.3.1 and 6.2.3.3.

3.1.31 HP_Mult: High-Pass Multiplier, a multiplier used to derive the minimum high-pass coupling time constant.

NOTE—See 6.2.3.1 and 6.2.3.2.

3.1.32 hysteresis: From magnetics: lagging in the values of resulting magnetization in a magnetic material (such as iron) subjected to a changing magnetizing force. In this standard, hysteresis refers to the memory of an input state to an amplifier or buffer after that state is removed but before a different input state is applied. Typically, there is a hysteresis threshold that defines the difference between “no input” and “input.” As applied to electronics, a digital output circuit such as a comparator where the output switches to one output state when the input is above one level and switches to the opposite output state when the input is below a lower level, and the output does not switch at any intermediate level. Example: a buffer produces a high output when a voltage above 0.5 volts is applied, produces a low output when a voltage below 0.3 volts is applied, and does not change its output for voltages between 0.3 and 0.5 volts.

Hysteresis symbol in a buffer symbol:



3.1.33 hysteretic: Adjective form of **hysteresis**, as in “hysteretic amplifier.”

3.1.34 interconnect test: An IEEE Std 1149.1 Boundary-Scan test designed to detect and diagnose defects in the interconnection wiring between ICs. This standard extends the concept to include the testing of channels, where single-ended and differential signaling, and DC- or AC-coupling may exist.

3.1.35 load termination: A **termination** placed at the far end (away from the driver) of a **signal path** used to match the **characteristic impedance** of the path. *Contrast:* **source termination**.

3.1.36 low-pass filter: An electrical network that passes lower frequencies, including DC levels, and attenuates higher frequencies.

3.1.37 LP_Mult: Low-Pass Multiplier, a multiplier used to derive the minimum low-pass filter time constant.

NOTE—See 6.2.3.1 and 6.2.3.3.

3.1.38 manufacturing process defect: A **defect** that is an unacceptable by-product of the manufacturing process. For board manufacture these include missing devices (ICs, resistors, capacitors, etc.), improperly mounted devices (e.g., rotated 180 degrees), open solder joints, shorted solder joints, misaligned devices, and incorrect and dead devices.

3.1.39 mission logic: The circuitry inside an IC that performs its primary design function. *Contrast:* **test logic**.

3.1.40 mission mode: An **operational mode** in which a device performs its primary design function. *Contrast:* **test mode**.

3.1.41 negative leg: The signal path of a differential signal pair that has the opposite polarity as the original data signal.

3.1.42 null: The input state where the two inputs to a differential receiver that are supposed to be different (complementary) are instead receiving essentially the same value.

3.1.43 offset voltage: A constant DC voltage added to an AC signal.

3.1.44 operational modes: A device may function in several modes. For the purposes of this specification, two primary modes are considered. *See:* **mission mode; test mode**.

3.1.45 positive leg: The signal path of a differential signal pair that has the same polarity as the original data signal.

3.1.46 referenced termination: A **termination** for a differential channel where the two legs are both terminated to a **reference voltage**. This reference has an impedance that is low relative to the termination impedance, such that the two legs are independent. *Contrast:* **bias network**.

3.1.47 reference voltage: A low-impedance voltage source typically used to define a threshold for comparing signals. The low-impedance characteristic means it is resistant to conducting noise signals. *Contrast:* **bias**.

3.1.48 self-referenced comparison: The comparison of a signal with a delayed, averaged version of the same signal, used to detect signal transitions. This process does not need a static reference voltage to find a transition in a signal.

3.1.49 signal path: An electrical pathway formed by a simple conductor, or a terminated pathway containing a series resistance, or an AC-coupled pathway containing a series capacitance that transmits a signal from a driver to a receiver.

3.1.50 signal reflection: A signal wavefront traveling across a discontinuity in the **characteristic impedance** of the **signal path** may have a fraction of its energy reflected in the opposite direction on the path. The reflection may be of the same or opposite polarity and will add into the waveforms appearing on the path, impacting their shape. *See also:* **transmission line**.

3.1.51 single-ended signaling: The use of a single signal path in a channel to carry a data signal. The signal is referenced to a static **reference voltage**. *Contrast:* **differential signaling**.

3.1.52 slew rate: Rate of change in either direction of voltage, measured in units of volts per second.

3.1.53 source termination: A **termination** placed near the source driver of a signal to satisfy DC current requirements of a driver and/or to match the **characteristic impedance** of a **transmission line** structure to reduce **signal reflections**. *Contrast:* **load termination**.

3.1.54 termination: An impedance usually near the end of a signal path used to satisfy the electrical matching requirements of the **characteristic impedance** of the **signal path** and reduce **signal reflections**. The impedance is typically low, often 100 ohms or less. *See also:* **characteristic impedance; load termination; referenced termination; source termination; unreferenced termination**.

3.1.55 test logic: Testability logic defined by this standard and IEEE Stds 1149.1 and 1149.4. *Contrast:* **mission logic**.

3.1.56 test mode: An operational mode of the device in response to the EXTEST or an AC testing instruction whereupon the pins are driving or receiving test data as controlled by the test logic of the device. The device pins have been disconnected from the internal mission logic. *Contrast:* **mission mode**.

3.1.57 test receiver: A circuit, which can operate in **AC test mode** and **DC test mode**, that examines an incoming signal. Its purpose is to extract test data from a signal that may have been altered by DC level shifting or AC-coupling decay.

3.1.58 time constant: Typically, the product of resistance and capacitance of an RC network (e.g., a high-pass filter) measured in seconds. One time constant is the time for a capacitor to discharge 63% of its voltage through a resistor. In AC-coupled systems, the termination resistance combined with the coupling capacitor forms a **high-pass filter**.

NOTE—In discussions comparing time periods to time constants, a period is significantly longer (shorter) than a time constant if it is five (one-fifth) times the time constant value. For example, as shown in Figure 2 using the five-time-constant rule, a signal will decay to 0.7% of its original value. The one-fifth-time-constant rule means that 81.9% of a signal still remains.

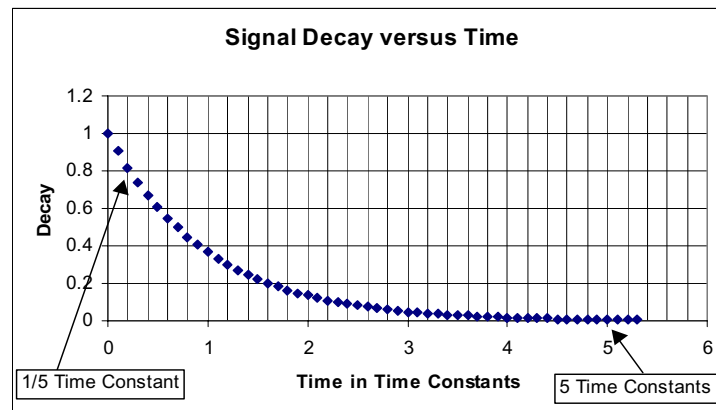


Figure 2—Signal decay versus time in units of time constants

3.1.59 transition: A voltage transition occurs when a signal traverses a specified voltage range in a specified time in either direction. *See:* **slew rate**.

3.1.60 transmission line: A **signal path** with a specific construction that produces a uniform, known **characteristic impedance** along its length. This minimizes degradation of a signal passing along this path that can result from impedance variations.

3.1.61 unreferenced termination: A **termination** for a differential channel where a termination impedance is connected between the two legs with no connection to a reference voltage.

3.1.62 voltage signaling: Signals are encoded by the voltage appearing on a wire compared to a reference voltage (single-ended) or the voltage appearing on a pair of wires (differential). *Contrast:* **current signaling**.

3.2 Acronyms

AC	alternating current (used here for any time-varying voltage)
BSDL	Boundary-Scan Description Language
CML	current mode logic
CMOS	complementary metal oxide semiconductor
DC	direct current (used here for static voltage levels)
HPLP_Ratio	High-Pass-Low-Pass Ratio
HP_Mult	High-Pass Multiplier
IC	integrated circuit
ICT	in-circuit test
LP_Mult	Low-Pass Multiplier
LVDS	low-voltage differential signaling
LVPECL	low-voltage PECL (pseudo emitter-coupled logic)
PECL	pseudo emitter-coupled logic
PLL	phase-locked loop
SERDES	serialize/deserialize
TAP	Test Access Port (from IEEE Std 1149.1)
TCK	test clock
TDI	test data in
TDO	test data out
TMS	test mode select
TRST	test reset

VHDL	VHSIC High-Level Design Language
VHSIC	very high-speed integrated circuit

4. Technology

The presence of coupling capacitors on-chip interconnects, whether they are discrete devices mounted on a PC board or integrated inside an IC, prevents DC values from being driven between a driver and receiver. An AC Boundary-Scan methodology must therefore use a time-varying signal to pass through the AC-coupling when in AC test mode.

Differential signaling is often used to increase signaling speeds and noise immunity, compared to single-ended signaling. Differential signaling, combined with termination schemes, can have significant defect masking properties that reduce test effectiveness. (See 4.3.)

This clause contains tutorial discussions of AC-coupling, differential signaling, and the effects of defects in such circuits needed to understand Advanced I/O testing technology. Rules based on these technologies are found in subsequent clauses.

4.1 Signal pin types

It is expected that a chip possessing pins requiring AC-coupling may also possess “normal” pins (i.e., intended to be DC-coupled) as well. These DC pins would supply data and/or control to/from portions of the chip that do not require AC-coupling. For test purposes, it is necessary that all these pins be tested simultaneously with an EXTEST-like capability because that is how shorts (unwanted connectivity) between these pins are reliably detected and diagnosed. It is desirable for higher test throughput to test all pins simultaneously with an EXTEST-like capability as well.

NOTE—There are some issues related to simultaneously switching all outputs during the EXTEST instruction. These issues will be discussed in later clauses. The implementation of EXTEST on AC and DC pins will provide the needed shorts detection and minimize the noise due to simultaneous switching.

This standard will refer to DC and AC pins henceforth. DC pins are those for which IEEE Std 1149.1 provides adequate testing. AC pins are those Advanced I/O that require additional test resources in order to be adequately tested, including those pins intended for AC-coupling or differential signaling.

AC pins are a principle target of this standard. IC designers implementing this standard are expected to identify such pins and add new test capabilities for them.

4.2 Signal coupling and coupling combinations

This subclause reviews a range of coupling options.

4.2.1 Single-ended DC

A basic, single-ended connection scheme is shown in Figure 3, along with the Boundary-Scan control and observation capability specified by IEEE Std 1149.1. This type of coupling has been quite common and is very testable using Boundary-Scan.

It is important to note that in a typical Boundary-Scan test, the time between launching a signal from a driver (at the falling edge of test clock (TCK) in the *Update-DR* or *Update-IR* TAP Controller state) and capturing that signal (at the rising edge of TCK in the *Capture-DR* TAP Controller state) is no less than 2.5 TCK

cycles. Further, the time between successive launches on a driver is governed not only by the TCK rate, but by the amount of serial data shifting needed to load the next pattern data in the concatenated Boundary-Scan Registers of the Boundary-Scan chain. Thus the effective test data rate of a driver could be thousands of times lower than the TCK rate. For DC-coupled interconnect, this time is of no concern. For AC-coupled interconnect, the signal may easily decay partially or completely before it can be captured. If only partial decay occurs before capture, that decay will very likely be completed before the driver produces the next edge.

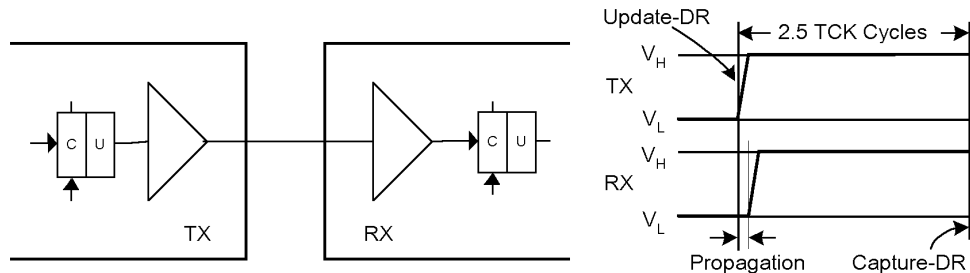


Figure 3—Basic single-ended signaling with Boundary-Scan control and observation

4.2.2 Single-ended AC

Figure 4 shows an AC-coupled single-ended connection. (The termination resistor and voltage source shown may actually reside within the IC.) The size of the capacitors used is determined by the mission requirements of the coupling and may vary widely across applications. While the devices may have been designed for DC-coupling and actually contain Boundary-Scan resources, the AC-coupling will block their operation. This interconnection configuration could only be tested at very high TCK frequencies or lower frequencies with very large coupling capacitors, and even then the results may be unreliable. TCK frequencies are likely to be significantly lower than the normal operating frequency of the channel being tested. Thus the data seen by the receiver may decay before it can be captured.

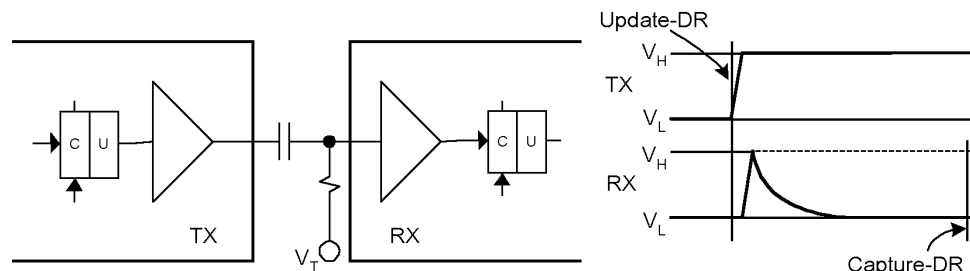


Figure 4—Basic single-ended signaling with AC-coupling

In general, AC-coupling can distort a signal transmitted across a channel depending on its frequency. For example, Figure 5 shows a channel transmitting a high and low frequency waveform across an AC channel and observed at the input of the receiver. The high frequency signal is relatively unaffected by the coupling. The low frequency signal is severely impacted. First, it decays to V_T after a few time constants. Second, its amplitude is double the input amplitude. A key item to note is that the transitions in the original signal are preserved, although their start and end points are offset compared to where they were in the high frequency case.

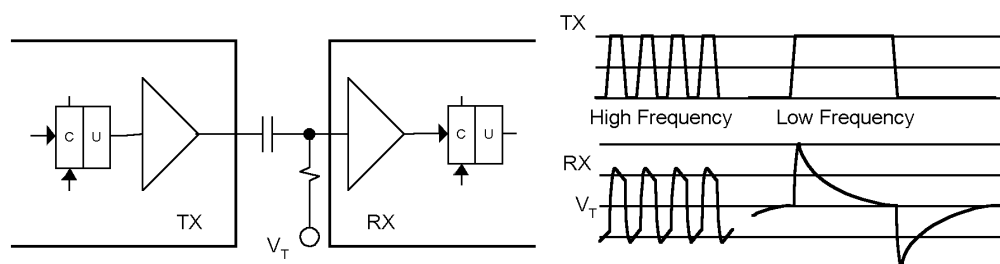


Figure 5—High and low frequency response of an AC-coupled channel

4.2.3 Differential DC

Figure 6 shows a basic differential DC-coupled signal path. The termination resistor may exist for impedance matching and/or source termination of the driver. The placement of Boundary-Scan resources is optional per IEEE Std 1149.1 in that they can be omitted altogether. The IEEE Std 1149.1 standard allows a designer to designate the differential signal path as “analog.” Then the digital-to-analog and analog-to-digital interfaces (optionally) can be provided with Boundary-Scan resources as shown in Figure 6. When this option is taken, it is then possible to test the analog signal path with Boundary-Scan algorithms. In this case, the signal path is viewed by the test logic as if it were single-ended, leading to diagnostic ambiguity and possible loss of test coverage (see 4.3).

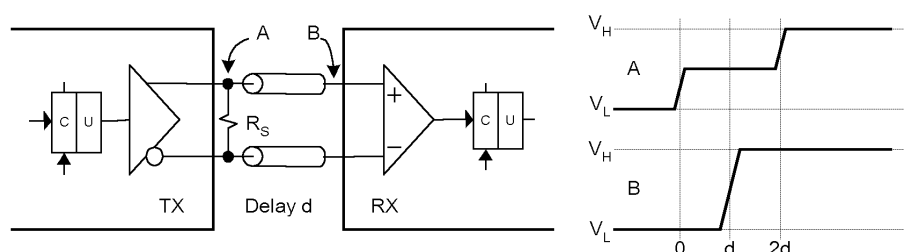


Figure 6—Basic differential signaling with DC-coupling and source loading

The driver in Figure 6 could be producing a voltage signal, and the resistor is used to match the signal line impedance. Alternatively, the driver could be producing a current signal, where the direction of flow represents data, and the resistor is needed not only to match signal line impedance, but also to provide a DC current path to satisfy the driver's requirements. This is called a source termination.

The driver in Figure 6 is looking into a termination R_S and transmission lines with characteristic impedance R_S as well. This forms a voltage divider which sends $1/2$ the signal into the transmission lines. When the signal wavefront reaches the receiver (after delay d) its high impedance does not match the characteristic impedance which reflects the signal back down the lines toward the driver. This signal ($1/2$ the driver voltage) adds to the signal received so that the receiver perceives a full voltage swing. After the second transmission line delay d , the reflected signal reaches the driver and brings the voltage seen there to the full level. Thus a clean transition is seen at the receiver, but the signal seen at the driver is a two-step staircase. Since there is an impedance match at the driver, no new reflections occur.

In the case where the impedance R_S is moved to the receiver (to the right of the transmission lines), this is called load termination (and the resistor is renamed R_L) as shown in Figure 7. Now the driver is looking into the transmission lines with characteristic impedance R_L . The full waveform is transmitted (no divider is now

present) and this edge propagates to the receiver. At the receiver, the termination resistor matches the line impedance, and thus there is no reflection. The waveforms at both the driver and receiver are full transitions.

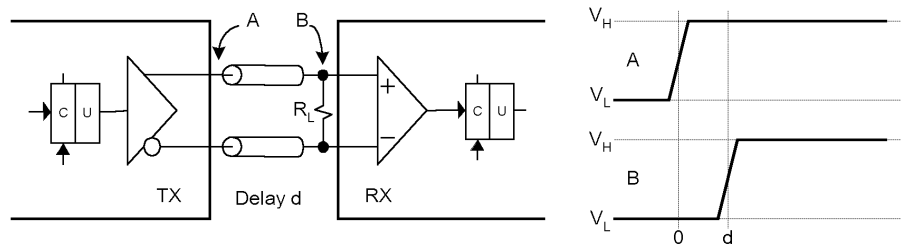


Figure 7—DC-coupled driver and receiver with load termination

Figure 8 shows a driver/receiver pair that has been both source and load terminated. In this case, the voltage swing seen on both sides of the transmission line has been divided by two (note R_S equals R_L). This type of termination assures that in the case of an imperfect impedance match, the resulting reflections can be attenuated at both ends of the line.

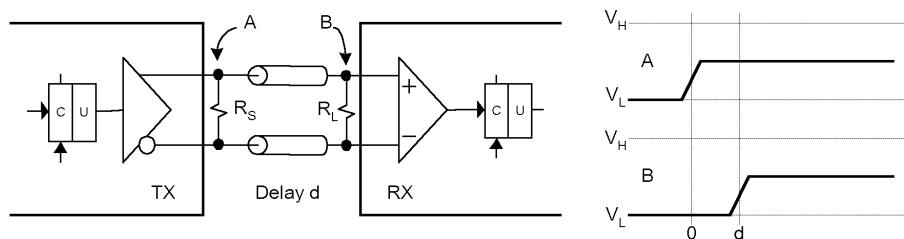


Figure 8—DC-coupled driver and receiver with both source and load termination

4.2.4 Differential AC

Figure 9 shows AC-coupling of a voltage driver and receiver whose voltage levels are assumed to be incompatible for DC-coupling (the voltage levels used by the driver are too far removed from the acceptable common-mode range of the receiver). The bias network referenced to the common-mode voltage source V_{Bias} (the optimal common-mode point of the receiver) along with the DC blocking effect of the coupling capacitors forms a level shifter that allows this configuration to work properly. This enforced compatibility is a common reason why board designers may use AC-coupling. The size of the capacitors used is determined by the mission requirements of the coupling and may vary widely across applications.

NOTES

1—The receiver waveforms in Figure 9 will decay to V_{Bias} if the driver frequency is low compared to the time constant of the coupling network. Since Boundary-Scan test data application rates can be low, the receiver may indeed see float (undriven) levels due to signal decay.

2—It is assumed in Figure 9 that the distance between R_L and the receiver inputs is small, such that there are no significant transmission line effects beyond R_L .

Figure 10 shows a basic differential AC signal path with an unreferenced termination. The termination is used for impedance matching. The driver is a voltage driver and thus does not need a source termination to provide a current path.

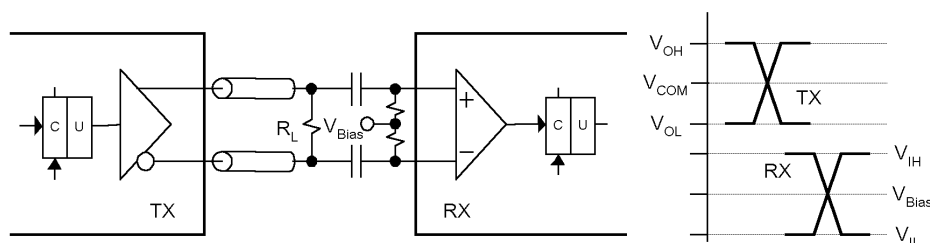


Figure 9—A basic differential AC signal path with load termination and receiver common-mode generation using a bias network

Figure 11 shows a basic differential AC signal path with a current driver and source termination and also a referenced bias generator to select the common-mode voltage appropriate for the receiver. The source termination may also serve as an impedance match for the line. The bias network may use significantly higher value resistors as long as the line distance from the capacitors to the receiver is small. This will significantly increase the time constant of the coupling network.

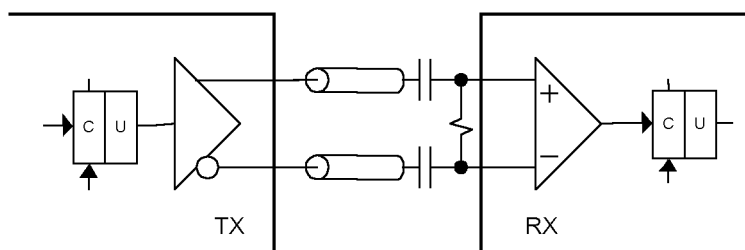


Figure 10—A basic differential AC signal path with un referenced termination

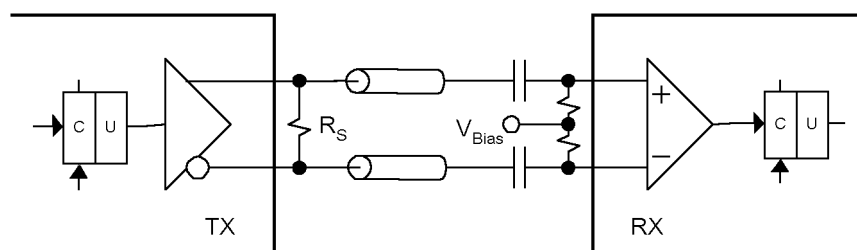


Figure 11—Basic differential AC signal path with source termination and bias provision

Finally, all the terminations, bias networks, and even the coupling capacitors may ultimately be integrated into the receiver IC. Externally, the signal path appears to be DC-coupled but internally it is still AC-coupled, as shown in Figure 12. On-chip component defects will not need to be tested during board test. Thus only the interconnect defects (typically solder) will be relevant.

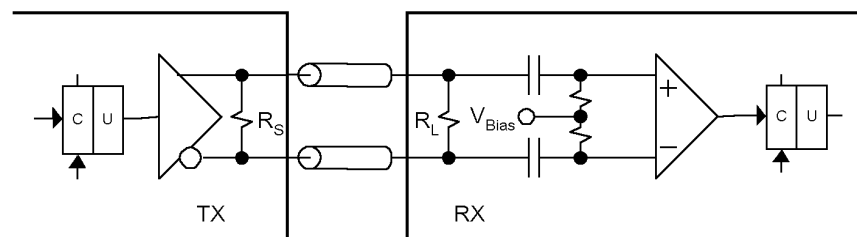


Figure 12—AC-coupling, termination, and bias generation internal to the ICs

4.2.5 Intention: When AC capability is DC-coupled

The standard for AC testing proposed herein is intended to be implemented on AC pins of an IC. However, there is the possibility that a board designer may still choose to use DC-coupling between devices that are DC compatible. Thus a test developer could find a situation where AC testing is needed to test a DC-coupled signal path. This could occur when more than one AC-capable interface exists on an IC and one is AC-coupled while another is DC-coupled. The test developer would need to load an AC testing instruction into the device to test the AC-coupled interface. It is the intention of this standard that if DC-coupling of AC-capable interface is possible and gives acceptable mission performance, then the AC test performance will also be acceptable.

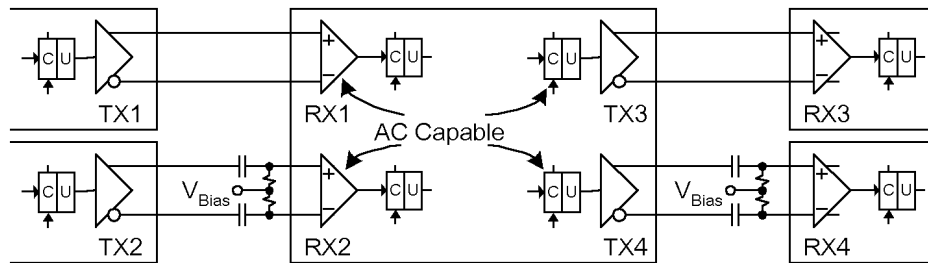


Figure 13—Combinations of AC-capable drivers and receivers connected to conventional drivers and receivers

For example, in Figure 13 a conventional IC (TX1, containing only EXTEST support) is DC-coupled to receiver RX1. An AC-capable driver TX2 is also connected to the RX2 receiver. To test all the signal paths simultaneously, the conventional device TX1 must be in EXTEST, while the other two use an AC testing instruction. If TX1, TX2, RX3, and RX4 are all AC-capable, then it is the intent of this standard that all of these configurations should be testable. If TX1, TX2, RX3, and RX4 are not AC-capable (only support EXTEST), then the configurations may or may not be testable. See a summary of capture behaviors for various coupling and testing scenarios given in 4.10.

4.3 The effects of defects

Defects are abnormalities in the structure of a circuit board (or similar assembly) that occur during manufacturing that must be found and corrected. This “manufacturing defect” model includes things like open solder joints, shorts, missing components, and dead devices. Not included in this model are performance-related issues, for example, the failure of a device to operate at its highest specified frequency at -40 degrees centigrade. This recognizes the traditional role of IEEE Std 1149.1 as a test standard for board level manufacturing defects.

The advent of AC-coupling, especially in the differential signaling domain, threatens this role. Boundary-Scan testing is inherently a “DC” technology. Further, there is inherent redundancy in differential structures that can mask the presence of seemingly obvious defects. An example is shown in Figure 14.

In this case, the positive leg of the circuit is eliminated by a defect, for example, an open solder joint on the capacitor. Yet the receiver still receives the negative leg signal and compares it to the V_{ref} voltage (assuming that V_{ref} is a true voltage source with negligible impedance). The receiver will still produce the correct output, although its common-mode noise rejection capability is completely compromised. This might not be noticed until subsequent functional or performance testing is encountered. There it may show up as an elevated bit error rate that would not provide very much diagnostic information. This simple example illustrates why it is important to monitor *both* legs of a differential pair independently, as covered in 4.6.4. In this case, the positive leg exhibits the “float” syndrome, or is simply said to float. In this case, the terminations (which may be internal in some devices) hold the leg at the reference voltage.

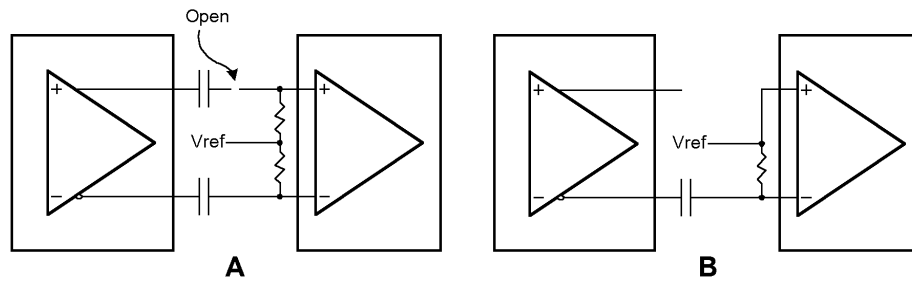


Figure 14—An AC-coupled differential path containing a defect (A) and an equivalent circuit (B)

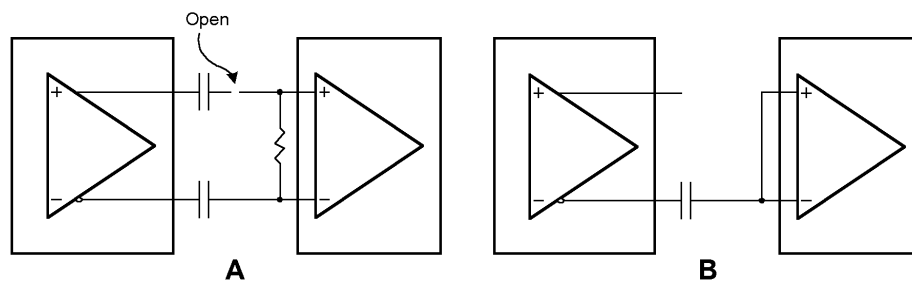


Figure 15—A null signal defect condition (A), where both legs see near-identical rather than complementary signals in the equivalent circuit (B)

The same defect, but with different termination, creates what is called the *null* syndrome, shown in Figure 15. As a result of unreferenced termination, the open defect allows the signal on the negative leg to appear on both legs of the receiver, in phase rather than 180 degrees out of phase. Note the termination resistance and parasitic capacitances, etc., may make the signal on the two input pins slightly different, and the mission-mode receiver may respond unpredictably to these small differences.

One defect in particular may be troublesome to detect in AC-coupled structures: the shorted capacitor. This defect restores DC-coupling. This defect may go unnoticed particularly in differential signal paths, especially when the DC characteristics of the driver and receiver are reasonably similar. For this reason, it is important to support the standard EXTEST instruction, because it can be used to test for shorted capacitor defects. This can be done by supplying a stream of 0s and 1s to the driver side of the capacitor and showing that this stream does not show up on the receive side, i.e., it has been blocked by the capacitor. This assumes that the EXTEST instruction is changing the data at a slow enough rate to allow the signals to decay.

When a net is AC-coupled and may be used with unreferenced termination, as shown in Figure 15, it is important that the receiver provide some sort of bias voltage (usually high impedance) to center the input signals at the optimal voltage offset for the mission receiver. Several defects produce the float syndrome described above, where the input just sits at this bias level. It is important to detect this condition for proper defect detection and diagnosis, meaning that for test we need to detect and capture any of three input states: a valid '1,' a valid '0,' and an invalid, or floating, input.

Finally, it is important to realize that for the defects that occur in high-speed circuits (where slew rates are often faster than signal path transmission delay), the transmission lines may alter the circuit's faulty behavior as shown in Figure 16. Simulation of the circuit's behavior may be necessary to understand the effects of defects. It is important to consider transmission lines as components of the simulated model when slew rates are elevated.

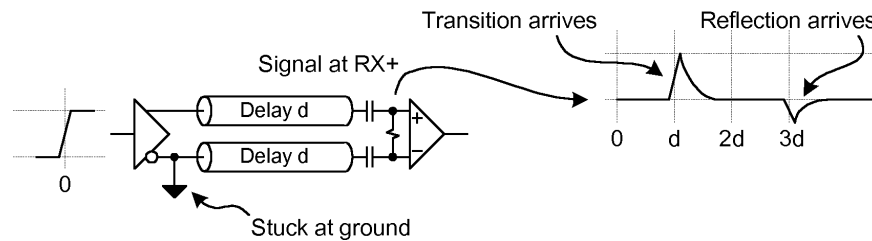


Figure 16—A defect may interact with transmission lines to produce unusual effects

4.4 Defects targeted by the standard

This standard (as well as IEEE Std 1149.1) provides test support for detecting “manufacturing process defects” that are found on printed circuit boards coming out of the manufacturing process. These defects include missing devices (ICs, resistors, capacitors, etc.), improperly mounted devices (e.g., rotated 180 degrees), open solder joints, shorted solder joints, and misaligned and dead devices. This standard focuses on those defects concentrated in AC-coupled and/or differential channels. As seen in 4.3, these defects may be difficult to detect or may be effectively masked from detection. Figure 17 and Table 1 show a representative set of defects considered by this standard. Note the model shows a single un referenced termination, but the table gives results for other termination schemes.

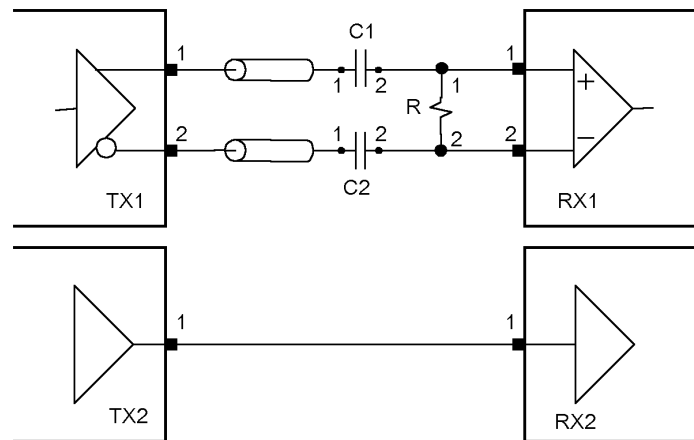


Figure 17—General AC-coupled channel and nearby DC channel used to illustrate defects

The least predictable defect syndromes occur when two signals driven by drivers of different technologies or protocols [for example, a differential LVDS driver and a “standard” single-ended complementary metal oxide semiconductor (CMOS) driver] are shorted together. The two shorted signals tend to “average” as the drivers fight to control the combined net, attenuating the transition amplitude on the differential leg, though often not enough to prevent detection of the transitions. When the “other” net is shorted to one driver leg of a true differential driver (defect 12), both outputs of the driver will tend to track each other. As the short forces one output to a voltage different from its normal common-mode voltage, the other tends to follow. When the “other” signal transitions, this will appear to put large, same direction (common-mode) transitions on both legs of the driver. When the “other” net is shorted to one receiver leg of an AC-coupled channel (defect 13), it will control the center voltage of the received signal, possibly forcing it outside the common-mode range of the test receiver. The information that would allow detection and isolation of many defects is not only in the differential transitions, but also in the levels created by some defects. As a result, some defects may actually be easier to detect and diagnose using the IEEE Std 1149.1 EXTEST than using AC test instructions. For these and other reasons, it is necessary to perform a full interconnection shorts test of the

board using EXTEST in all chips in addition to any AC test instructions, and base defect detection and diagnosis on the combined results.

The syndrome information presented in Table 1 is the result of hundreds of analog simulations on specific technologies and circuit designs. Different results can be expected for other technologies or implementations. Therefore, it is highly recommended that test receiver designs under consideration be simulated for both defect-free behavior and how they react to channel defects.

Table 1—Potential defects for the circuit in Figure 17

Defect ID	Defect site (Note 1)	Possible defect cause(s)	Typical receiver AC test syndromes (Note 2)
1	TX1 pin 1 open	Open solder joint, broken bond wire	Pin-1-follows-pin-2 null, possibly with detectable reflections on both pins (unreferenced), or pin 1 float (referenced)
2	C1 pin 2 open	Open solder joint, missing capacitor	Pin-1-follows-pin-2 null (unreferenced), or pin 1 float (referenced)
3	RX1 pin 1 open	Open solder joint, broken bond wire	Pin 1 float
4	TX1 pin 1 short to VDD	Pin-to-pin short, solder splash	Pin 1 float, possibly with detectable reflections if unreferenced
5	TX1 pin 1 short to ground	Pin-to-pin short, solder splash	Pin 1 float, possibly with detectable reflections if unreferenced
6	TX1 pins 1, 2 shorted together	Pin-to-pin short, solder splash	Both pins float, transients at switching times suppressed by voltage and time hysteresis
7	C1 pins 1, 2 shorted together	Solder splash, internal short in C1	Pin 1 passes EXTEST, which would normally “fail” due to DC blocking of capacitor
8	C1 pin 1 short to C2 pin 2	Pin-to-pin short, solder splash	Pin-2-follows-pin-1 null, or both pins float (high frequency shorted legs, low frequency driven by driver pin 1)
9	RX1 pin 1 short to VDD	Pin-to-pin short, solder splash	Pin 1 float, stuck-at-1 detected by EXTEST. Pin 2 common-mode shifted and may also appear to be stuck-at-1 in EXTEST (unreferenced).
10	RX1 pin 1 short to ground	Pin-to-pin short, solder splash	Pin 1 float, stuck-at-0 detected by EXTEST. Pin 2 common-mode shifted and may also appear to be stuck-at-0 in EXTEST (unreferenced).
11	RX1 pins 1, 2 shorted	Pin-to-pin short, solder splash	Both pins float (transients at switching times suppressed by voltage and time hysteresis)
12	TX1 pin 1 short to TX2 pin 1	Pin-to-pin short, solder splash	There are a large number of effects of device-to-device shorts. See text.
13	RX1 pin 1 short to RX2 pin 1	Pin-to-pin short, solder splash	There are a large number of effects of device-to-device shorts. See text.
14	R pin 1 open	Open solder joint, missing resistor	Much longer time constant on both pins (unreferenced) or just pin 1 (referenced), which may “pass” EXTEST.
NOTES 1—Defects that are equivalent by symmetry are omitted. 2—Referenced termination (to low-impedance voltage sources) will isolate legs, while unreferenced termination will allow interactions between legs. This produces differences in faulty behavior.			

4.5 Differential termination and testability

Extensive study of differential channels and the effects of defects within those channels has shown that the effects of defects are heavily influenced by the termination schemes used. There are three functions of terminations:

- to provide for proper DC current paths needed for proper driver functioning (usually source termination),
- to provide impedance matching of transmission lines, and
- in some AC-coupled cases, to set common-mode operating points for the receiver.

A given termination may provide one or more of these functions. The following subclauses discuss termination options.

4.5.1 Unreferenced termination

Source termination is often needed for current signaling technologies where the direction of current flow is used to encode binary data. A typical example is a low-voltage differential signaling (LVDS) driver/receiver pair. Since all differential receivers operate by comparing voltages, a current signal is translated into a voltage signal for that comparison. Figure 18 shows an LVDS driver DC-coupled to a voltage receiver, where R_S provides both source termination and impedance matching. The direction of current flow represents data.

NOTE—It is assumed that R_S is placed very close to the receiver so that any transmission line effects are only present between the driver and the resistor.

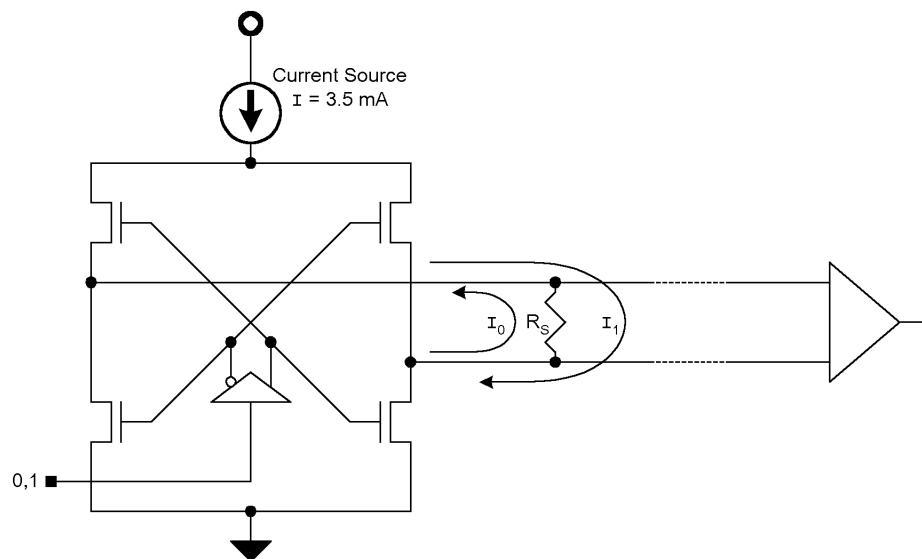


Figure 18—LVDS driver and receiver, DC-coupled

This form of termination is called unreferenced because there is a single resistor R_S rather than two resistors center tapped to a reference voltage (seen later in Figure 20). In effect, the receiver is referenced to the common-mode voltage of the driver/resistor combination. This means the receiver's common-mode range must be compatible with the driver's output

Figure 19 shows an unreferenced AC termination. Resistor R_S still provides source and line termination. Resistor R_L provides termination and a current path on the receive side, since the comparator input impedance is effectively infinity. Note R_L and C determine the time constant of this coupling.

NOTE—The receiver in Figure 19 will have its own biasing circuitry built-in to establish its common-mode operating point.

If the time between signal transitions is long, the voltage across R_L will decay to zero volts or a null input condition with results that may be undefined. Note that some defects can also cause this to occur, such as a missing capacitor, C . In this case, both inputs get essentially the same signal, resulting in a very small differential signal, if any.

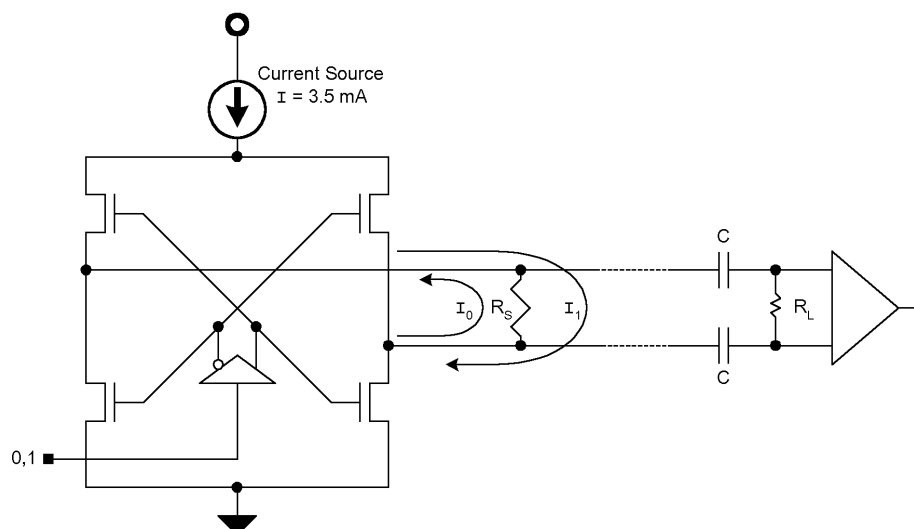


Figure 19—LVDS driver and receiver, AC-coupled with un referenced termination on the receive side

4.5.2 Referenced termination

Figure 20 shows an AC-coupled, referenced termination. This type of termination is used to set the common-mode voltage of the receiver at its optimal value (here, V_{Bias}). Resistors R_B along with capacitance C determine the time constant of the coupling. The value of R_B may be larger, simply providing bias and a larger time constant, or may be smaller to provide bias, load impedance matching, and a smaller time constant. In the referenced termination case, if a defect such as a missing capacitor is present (this defect is shown in Figure 14) the leg with the missing capacitor will see V_{Bias} while the other leg will see a valid signal. (The un referenced case presented both legs with essentially the same signal, a null input state.) Since test structures are to be added to both legs (see 4.6.4) they will respond in a deterministic way.

NOTE—It is assumed here that the V_{Bias} reference has low enough impedance to isolate the two legs. If this is not true, then the receiver may see signals more like the null condition.

4.6 Test signal implementation

In order to test the various combinations of single-ended and differential signal paths with variations on coupling, modifications have to be made to the drive and receive sides of the path.

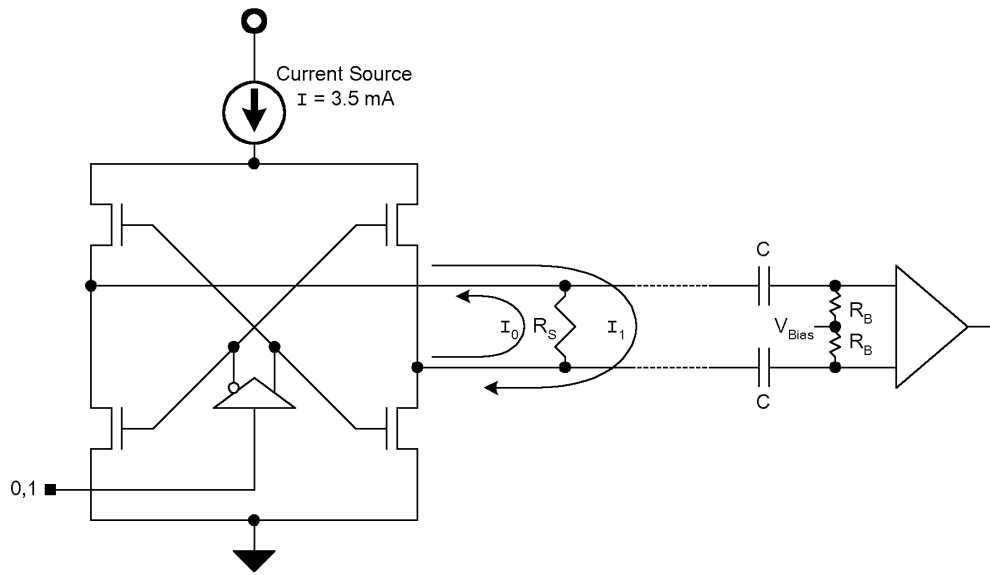


Figure 20—LVDS driver and receiver, AC-coupled with referenced termination on the receive side

4.6.1 Single-ended drive

Figure 21 shows a single-ended output stage modified in the familiar way given by IEEE Std 1149.1 for test purposes. One of two signals, the normal mission signal or test data is selected for transmission by a mode signal. (This figure does not show the full detail of the Boundary-Scan Register cells that supply test data.) The test data is either the content of the Boundary-Scan Register Update latch (U) when executing the (DC) EXTEST instruction, or an “AC Signal” when an AC testing instruction is loaded into the device. The AC signal is a test waveform suited for transmission through AC-coupling. The concept here is that the single-ended driver itself is not modified and no additional logic is inserted into the mission signal path except the multiplexer already required by IEEE Std 1149.1, which is to select the path between mission and test data. The multiplexer selection for AC mode is not inserted in the mission data path, but in the test data path.

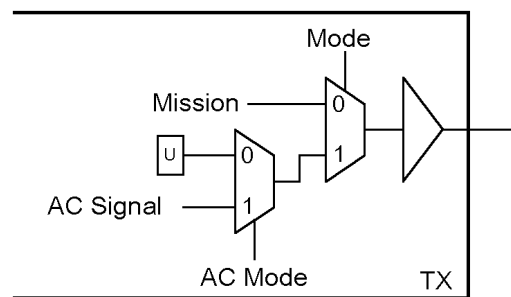


Figure 21—A single-ended driver path

4.6.2 Differential drive

There are two options for implementing a differential driver when incorporating test. The first is shown in Figure 22 where the selection between test and mission data is performed before the conversion to differential signaling. This means there will be only one data stream presented to the two differential pins and that the data will be transmitted in true differential form, using either current or voltage modes of the

driver in question. Due to aggressive performance requirements in some higher-speed driver designs, it is expected that this option will often be chosen.

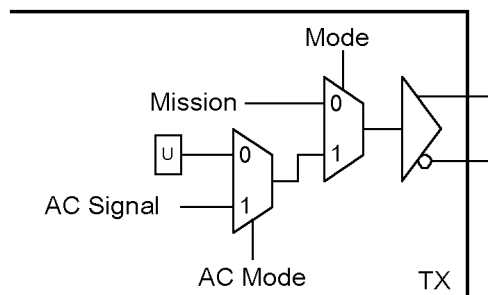


**Figure 22—Full differential driver for both mission and test modes.
(More common choice.)**

A second option for implementing testability in a differential driver is shown in Figure 23. In this case, the mission mode signal path is differential, while in test mode the mission driver is disabled and two single-ended drivers with independent test data sources are enabled. Each controls a single side of the differential signal path. During test, the path is now a pair of independent single-ended signals. The two new single-ended test drivers must have similar drive characteristics as the mission driver to assure they are compatible with the loading and coupling that the mission driver would encounter.

NOTES

1—In describing this case in BSDL (see 7.2 and 7.3), the test mode of the driver signals are described, which is single ended. Thus the signal pair is not described as differential. (See the Grouped port identification, B.8.8 in IEEE Std 1149.1-2001.)

2—If such a device supports IEEE Std 1149.4, then the structure in Figure 23 may be implemented, but with drivers of insufficient drive capacity to drive the load impedance. (This is because IEEE Std 1149.4 may implement the digital “driver” with relatively high-impedance switches.) In this case, a hybrid of Figure 22 and Figure 23 may be implemented where AC testing operates using the model in Figure 22.

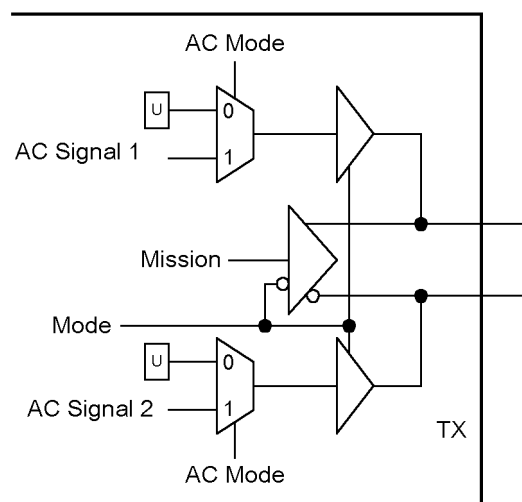


Figure 23—Differential mission/single-ended test mode driver. (Less common choice.)

This option has desirable testability and diagnosability features in that it removes some of the redundancy inherent in differential signaling, but it also reduces some of the noise immunity that differential signaling affords and may generate more noise during testing since the test signals on the two legs are no longer balanced and offsetting. There is additional cost in that the drive specifications (slew rate and amplitude) for the two added drivers must be substantially similar to those of the mission driver, into the mission load.

There may be unacceptable mission performance degradation with this approach that makes it the less commonly chosen option.

4.6.3 Single-ended test signal reception

Figure 24 shows two options for single-ended test signal reception, again familiar from IEEE Std 1149.1, but with a provision for detecting an AC Test Signal when an AC testing instruction is loaded in the device. When an AC testing instruction is loaded, a specialized test receiver (see 4.7) detects transitions of the AC signal seen at the input and determines if this represents a logic '0' or '1.' When EXTEST is loaded, the input signal level is detected and sent to the output of the test receiver to the Boundary-Scan Register cell. One option shown in Figure 24 supports INTEST (control and observe capability), and the other uses a simpler observe-only structure that will not support INTEST.

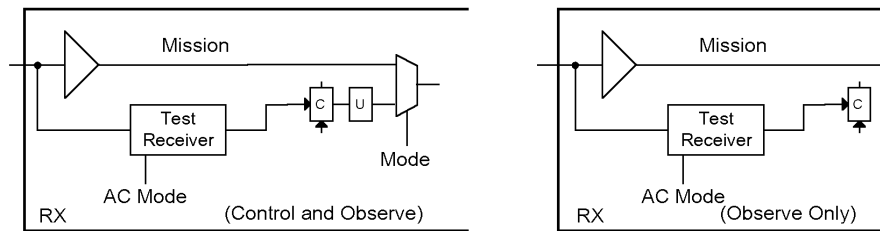


Figure 24—Single-ended signal reception, with and without support for the INTEST instruction

NOTE—The test receiver may be connected to the output of the mission input amplifier if it is a true amplifier (e.g., unity gain) rather than a threshold comparator. The test receiver is intended to process the actual waveform seen at the input pin, not an interpretation of the waveform.

A single-ended receiver has some form of reference used to distinguish a '0' from a '1' and this feature is used during (DC) EXTEST as well. However, during AC testing, the signal may decay to some intermediate value that cannot be reliably received by the mission receiver. The test receiver is therefore used to sense the AC Test Signal transitions.

4.6.4 Differential test signal reception

A differential receiver is modified for testability as shown in Figure 25. Optionally (via IEEE Std 1149.1), the mission differential receiver path is modified to capture test data seen by the mission receiver in differential mode. The mission receiver itself is unmodified.

Each leg of the differential signal path has its own added test receiver. The purpose of each receiver is to monitor a leg of the signal path independently. A test receiver is required on each pin to provide adequate defect coverage and diagnosis capability.

NOTE—No variations in the test receiver are needed for INTEST support since this is an observe-only monitor.

Again, when an AC testing instruction is loaded, the specialized test receivers (see 4.7) detect transitions of the AC signals seen at the inputs and determine if these transitions represent a logic '0' or '1.' When EXTEST is loaded, the input signal level is compared to a fixed reference designed into the test receiver.

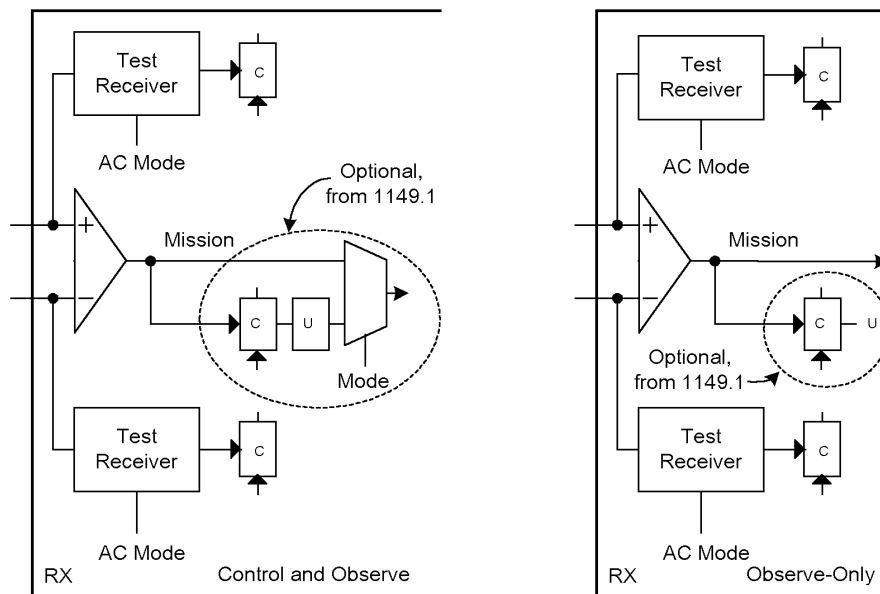


Figure 25—Differential signal reception, with and without support for the INTEST instruction

4.6.5 Coupling compatibility and EXTEST

When a test receiver is DC-coupled to a driver, either by design or due to a shorted capacitor, and the EXTEST instruction is executed, then one of two effects will be seen:

- if the driver voltage levels bracket the threshold value(s) of the test receiver (i.e., one is above and the other below), the driven data will be captured, or
- if the driver levels do not bracket the threshold value(s) of the test receiver, then a static (stuck-at) value or only one polarity of the data will be observed by the test receiver.

Thus, interconnects between DC-coupled differential ICs may or may not pass data when performing EXTEST. (This is a reason to use an AC testing instruction even when AC pins are DC-coupled.) It is probable (at least for single-ended signals) that the fact they are DC-coupled in the mission design indicates they will pass EXTEST data. Test generation tools should examine the logic family information of the two ICs to determine if this will happen.

NOTE—Logic family information is not included in the definition of BSDL and must come from other data sheet sources.

Since the signals on a DC-coupled differential pair may contain a significant common-mode offset as well as the test signal, the design of the AC test receiver must account for the fact that there is no fixed reference available to discriminate a logic '0' from a '1.' A general discussion of the test receiver is given in 4.7, 4.8, and 4.9, and rules for its implementation are given in 6.2.

4.7 Test receiver support for AC testing instructions

The principle purpose of the test receiver seen in Figure 24 and Figure 25 is to extract a test signal even when the received signal contains an unknown offset. Because of the offset, a simple comparison of the test signal to a static reference may not reliably extract the test signal. Using the opposite leg of the pair as a reference (as is done by the mission receiver) will often mask important defects. A solution is to look for

information contained in the *transitions* of the signal. These will be independent of the offset seen in Figure 26. Valid transitions have a defined voltage swing ΔV and transition time Δt .

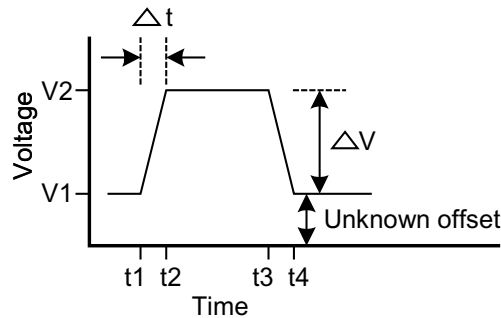


Figure 26—A signal with unknown voltage offset and the signal transitions it contains

One way to find the transitions in a signal with an unknown offset is to compare the signal with a delayed version of itself, that is, to use its recent history as a reference. This is illustrated in Figure 27. The original signal, a delayed version, and the output of the hysteretic comparator are shown. The output is a faithful reconstruction of the original waveform, delayed by the time it takes for the input waveform to pass the hysteresis threshold. The output waveform has been converted to standard logic levels, that is, the unknown offset is removed.

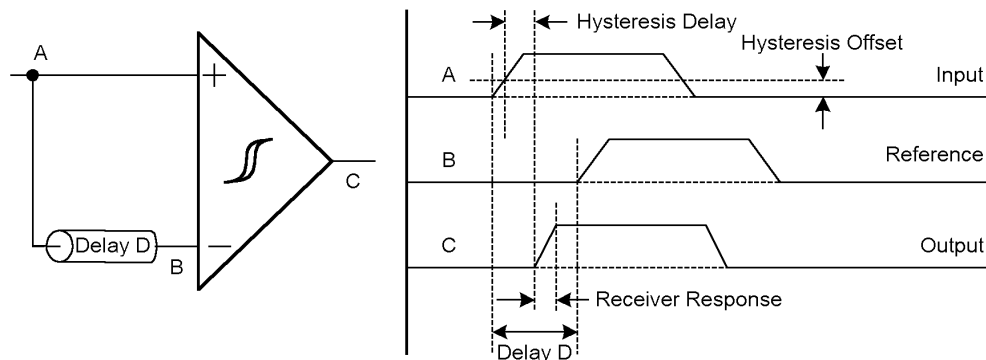


Figure 27—Delayed self-referenced reconstruction of a DC-coupled input waveform with unknown voltage offset

It will be important to assure that the delay D is longer than the transition times to be sensed. The use of hysteresis (the hysteresis voltage) can eliminate unwanted response to small signal noise (runt pulses). Additional filtering in the design of the comparator (the hysteresis delay) can eliminate response to larger signal noise of insufficient duration (noise spikes).

The waveforms that are applied to the test receiver may or may not be AC-coupled to the driver. When AC-coupled they may or may not decay significantly depending on the coupling time constant. For the signals shown in Figure 27, the test receiver is either DC-coupled or AC-coupled with a very long time constant. If AC-coupled signals with periods that are long with respect to the coupling time constant are applied to this simple circuit, the decaying signals will cause the comparator to reset itself early (after delay D) in response to the delayed reference edges, and the reconstructed waveform will differ from the original, as in Figure 28, where the reconstructed waveform has been shortened.

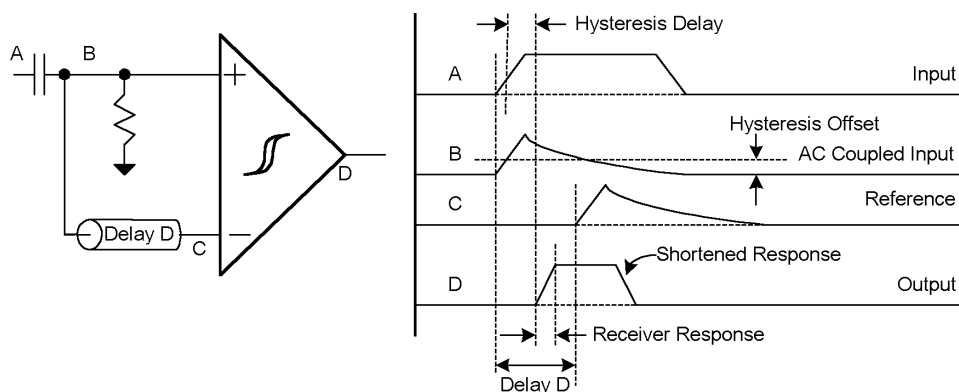


Figure 28—AC-coupled waveform with short coupling time constant

A low-pass filtered delay solves this problem as shown in Figure 29, a concept called “self-referencing.” The simple low-pass filter with a filtering time constant of $R_F \times C_F$ is used to hold the reference input to the test receiver at a constant value that is largely unaffected by short term events such as the high-pass filtered edges seen when AC-coupling (low time constant) is used. If high time constant AC-coupling or DC-coupling is used, then the low-pass filter adjusts the reference point again to represent near term history of the input signal. The hysteresis voltage and hysteresis delay are used to control response to noise.

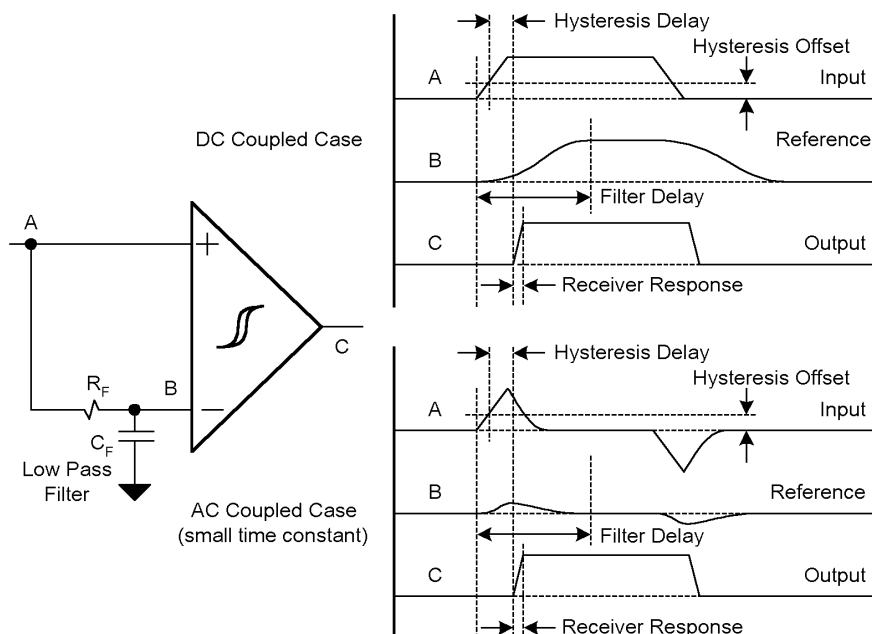


Figure 29—Delayed and filtered self-referenced waveform reconstruction of both DC- and AC-coupled waveforms by a test receiver

To summarize the concepts shown in Figure 29, the test receiver reconstructs an original waveform driven from either a single-ended driver or one leg of a differential driver, that is either AC or DC-coupled, and is insensitive to DC offsets that may exist in the driven waveform. It does this by responding to the edges of the original waveform that are still present despite DC- or AC-coupling.

Figure 30 shows a theoretical model of the concept shown in Figure 29. The hysteretic comparator of Figure 30 is expanded into: two simple comparators, one to sense rising edges and the other to sense falling edges; two V_{Hyst} voltage sources, to set the hysteresis voltage for the comparators; and a D-type flip-flop memory element, to hold the reconstructed signal. The internal bandwidth or slew rate limits of the simple comparators determine the hysteresis delay. The comparator outputs set or clear the flip-flop upon receipt of rising and falling edges, respectively. The values of R_F and C_F are chosen to provide a delay longer than the expected transition times being sensed. Typical values of R_F and C_F might be 5 Kohms and 5 picofarads (pf), which could be integrated into an IC. The input waveform at point A may be high-pass filtered by AC-coupling, or it could be a normal DC-coupled digital waveform (with an unknown offset). In either case, the edges are used to reconstruct the original digital waveform. This model will be used throughout this standard when discussing the test receiver, with the understanding that the actual implementation will typically be a single analog hysteretic comparator circuit.

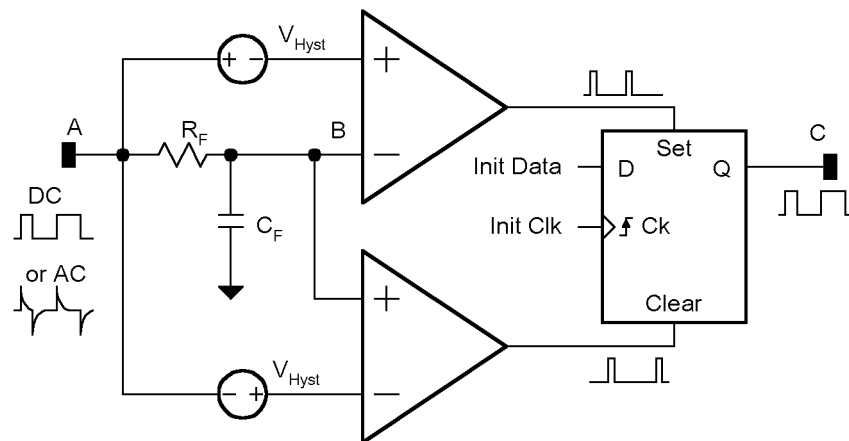


Figure 30—A simple self-referenced test receiver model of the concept in Figure 29

NOTE—The memory inherent in a hysteretic comparator would normally be modeled here as a simple Set/Clear asynchronous flip-flop. However, as will be discussed below, and detailed in Clause 6, it is necessary to initialize this memory at certain times during the test, so this hysteretic memory will be modeled throughout this standard as a D-type flip-flop. It could also be modeled in other ways, including as a level-sensitive (transparent) latch with appropriate changes to the clock signal timings.

Figure 31 shows an AC-coupled, differential signal channel from the drive side, with test receivers on each receiver pin. The output of the test receiver for each pin is represented by the “Q” output of each D flip-flop. (The mission receiver has been omitted for clarity.) This model supports the AC testing instructions.

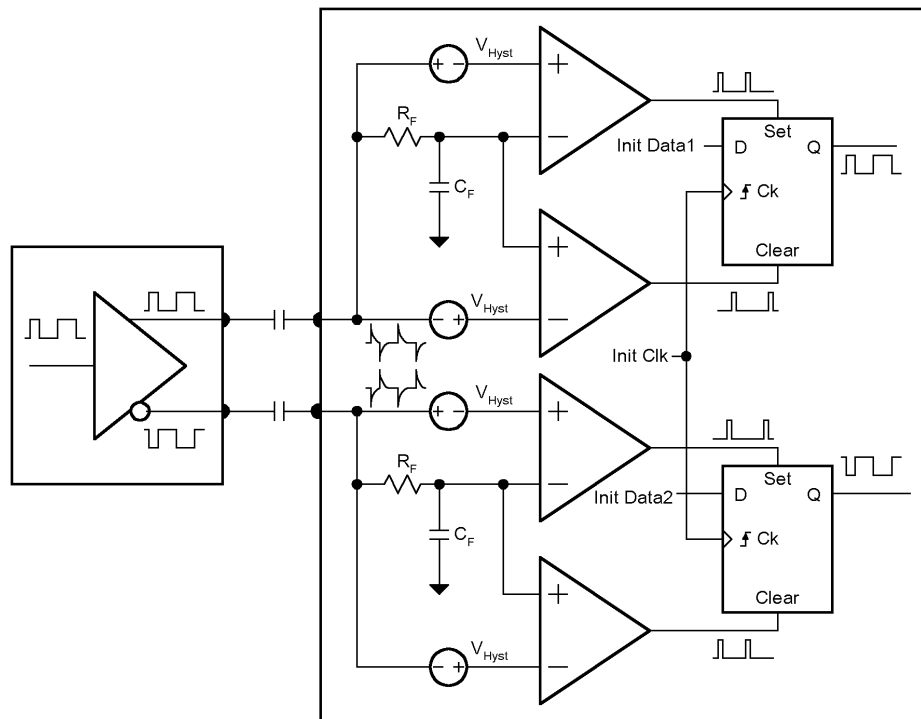


Figure 31—Differential driver, AC-coupling, and test receiver model

NOTE—In Figure 31 the mission receiver has not been shown. It would include load termination and/or biasing that would determine the time constant of the AC-coupling.

4.8 Test receiver support for the (DC) EXTEST instruction

The test receiver behavior for AC testing has been described. However it also is important to support the standard (DC) EXTEST instruction. This amounts to “turning off” the edge-detecting capability of the test receiver and having it respond only to levels. This is further complicated by the problem that there may be common-mode offsets added to the signals. This necessitates choosing a reference voltage that can be used for single-ended comparison.

One choice is to use the internal bias voltage V_{Bias} used to set the V_{Com} point of the mission receiver (the “sweet spot”) as shown in Figure 32. This bias voltage will work well as a static reference for the test receivers when AC-coupling is used.

If the receiver IC is DC-coupled to the driver, then the test receiver may or may not receive data depending on whether the high and low values driven by the driver are above the bias voltage plus the hysteresis voltage and below the bias voltage minus the hysteresis voltage, respectively. If data is not received, the test receiver may perceive a constant logic value, either 1 or 0.

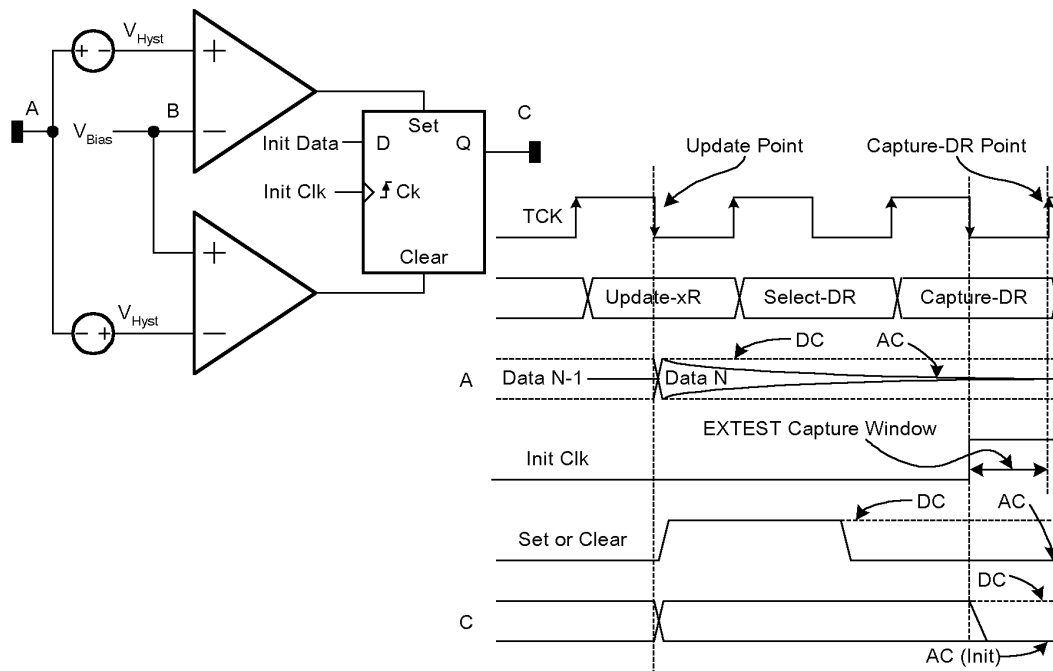


Figure 32—Static reference used to support (DC) EXTEST. Comparators may set or reset the hysteresis flip-flop after the falling edge and before the rising edge of TCK in the *Capture-DR* state.

If the receiver IC is AC-coupled to the driver, then Figure 32 shows the transition signal decaying away to less than the bias voltage plus or minus the hysteresis voltage prior to the *Capture-DR* TAP Controller state. The initial value loaded into the hysteresis at the falling edge of TCK in the *Capture-DR* TAP Controller state will then be captured. When testing for a shorted capacitor, this is the desired effect: a shorted capacitor will pass data from the driver in EXTEST, but a good capacitor will not. This effect depends on the time constant of the AC-coupling relative to the time between *Update-DR* and *Capture-DR* TAP Controller states. When testing for a shorted capacitor, the test software must ensure that enough time has passed for the signal to decay before entering *Capture-DR*, either by stopping TCK or by spending additional TCK cycles in the *Run-Test/Idle* TAP Controller state.

On the other hand, if testing the (deprecated) case where the driver pins are DC-only pins, yet are AC-coupled to AC pins (see 4.10), then the test for opens on the net will need to keep the time between the *Update-DR* and *Capture-DR* TAP Controller states short enough that the signal will not have decayed below the hysteresis thresholds. This may also require a large coupling time constant.

4.9 A general test receiver for DC and AC testing instructions

A test receiver that supports both the AC and (DC) EXTEST instructions is required. This could be accomplished simply by taking the two structures already shown and selecting between them with multiplexers. However it is possible to merge their behaviors into a more efficient structure as shown in Figure 33. In this structure an analog multiplexer selects between (DC) EXTEST support and AC testing support.

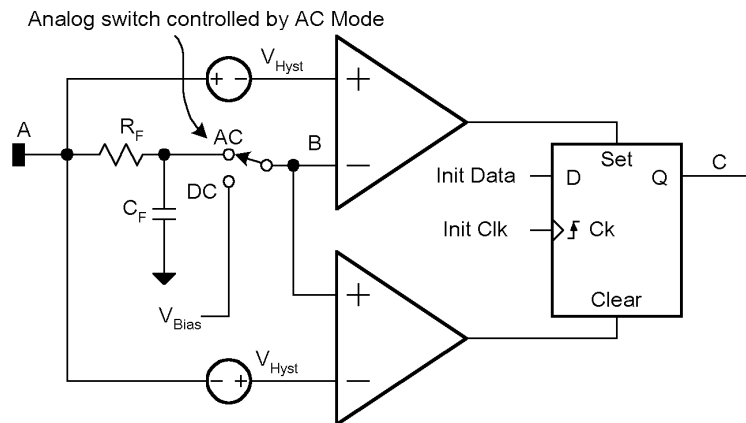


Figure 33—A test receiver model that supports both AC and (DC) EXTEST

Implicit in the above discussions is the fact that the test receiver, whether in AC or DC test mode, actually detects three mutually exclusive input states: a valid logic '1,' a valid logic '0,' and an invalid float state where the input stays within the range of the threshold voltage plus and minus the hysteretic voltage. As the Boundary-Scan Register cell can only capture a binary value, we initialize the hysteretic memory to a known, or default, value (see Figure 32) that will not change if the input is floating. This initialization defines the start of the sampling window, and also allows the test software to differentiate between driven data and the stuck-at-1, stuck-at-0, and float syndromes through appropriate choices of the data being driven and the initialization data for the test receiver. (A rising edge of TCK in the *Capture-DR* TAP Controller state always defines the end of the sampling window.) An alternate means of initializing the hysteretic memory and preserving the Boundary-Scan Register cell value is modeled in 6.2.4, Figure 49, in the discussion of integration of the test receiver with the Boundary-Scan Register cell.

4.10 Boundary-Scan capture data versus configuration

The content of Table 2 shows what Boundary-Scan data will be captured by a test receiver for various combinations of coupling, DC compatibility, and whether a given IC is executing EXTEST or an AC testing instruction.

Note in Table 2 that both rows with the driving IC performing a DC test coupled to a receiving IC performing an AC test are discouraged. In the case where the two are DC-coupled, then the channel should be tested with IEEE Std 1149.1 EXTEST (DC tests) in both ICs, with the expected loss of coverage and diagnosability. The case where the two are AC-coupled, testing for continuity through the coupling becomes problematic, and this case is deprecated. Board designers should avoid the situation. See the discussion following Figure 44 (in 6.2.3.3) and A.3.4.4.1 for further discussion and guidance.

Any time a receiver with only IEEE Std 1149.1 capabilities is AC-coupled to its driver, the ability to test that net becomes dependent on the coupling time constant, TAP navigation, and requires a minimum TCK during the period of the test (*Update-DR* through *Capture-DR* TAP Controller states). As this is highly dependent on tester capabilities, and including these nets in the test of the board as a whole may create conflicting requirements with other net configurations, board designers should avoid this situation. See A.3.4.4.2 for further discussion and guidance.

Table 2—Boundary-Scan capture results for various combinations of driver-to-receiver coupling, test instruction, and driver-to-receiver DC compatibility

Driver to receiver coupling	Channel test performed by pin of:		Capture result when DC levels (drive/receive) are:		Comments
	Driving IC	Receiving IC	Compatible	Incompatible	
DC	DC test (Note 1)		Date (Note 3)	Stuck-at 0/1 (Note 4)	Typical test for DC-coupling per IEEE Std 1149.1
	AC test (Note 2)		Data		Preferred test of differential channels
	DC test	AC test	Data when driver toggles at <i>Update-DR</i> , or Default when driver does not toggle (Note 5)		Static drive with AC receive deprecated: 1. Test data may not transition for multiple test cycles, preventing receiver from detecting data, 2. Driver only transitions at <i>Update-DR</i> (noisiest point in test).
	AC test	DC test	Data	Stuck-at 0/1	AC action compatible with DC receiver.
AC	DC test (for typical TCK frequencies)		Default		Used to test shorted capacitors if receiver is AC-capable and deprecated otherwise. Will transmit data (a failure) or will retain a default value (pass).
	AC test		Data		Preferred test for all AC-coupled channels.
	DC test	AC test	Data or default, depending on the relationship between <i>Update-DR</i> to <i>Capture-DR</i> time vs. net time constant(s), when driver toggles at <i>Update-DR</i> , or Default when driver does not toggle.		Static drive with AC receive deprecated: 1. Test data may not transition for multiple test cycles, preventing receiver from detecting data, 2. Driver only transitions at <i>Update-DR</i> (noisiest point in test).
	AC test	DC test	Default		May be used to test shorted capacitors if receiver is AC-test capable, but DC-to-DC test preferred. Deprecated otherwise.

NOTES

1—In Table 2, “DC test” implies that the IC has the EXTEST instruction loaded, or the channel pins are DC Pins, or the TAP Controller state sequence does not transit the *Run-Test/Idle* TAP Controller state.

2—“AC test” implies that the IC has either the EXTEST_PULSE or EXTEST_TRAIN instruction (see 5.2) loaded, that the channel pins are AC pins, and that the state sequence transits the *Run-Test/Idle* TAP Controller state.

3—“Data” indicates Boundary-Scan data is successfully transmitted.

4—“Stuck-at 0 or 1” indicates the incompatible levels will be seen as either a 1 or 0 depending on where the test receiver threshold is set. (An attached differential mission receiver, by contrast, does not see stuck-at behavior due to its common-mode range.)

5—“Default” indicates the response is the same that a floating test receiver would produce.

4.11 Noise sources and sensitivities

It has been pointed out that one advantage of differential signaling is better noise immunity for some types of noise, primarily common-mode noise. Because this standard looks at signals from a single-ended perspective, some of this noise immunity may be diminished or lost completely. Therefore it is important to be aware of the various sources of noise, their extent, magnitude, and duration. This standard addresses the effects of noise through the use of hysteresis (voltage and time) in the input test receiver, and by causing drivers to change states (differentially) at times other than the known-to-be-noisy *Update-IR* and *Update-DR* TAP Controller states. Designers should carefully evaluate all noise sources and their effects before determining hysteresis parameters. This standard assumes that “Best Design Practices” have been used to reduce noise effects wherever possible, especially on that noise which is not common-mode. This standard does not address noise issues that will impact mission operation. The standard will only address those sources of noise where noise immunity may have been diminished by single-ended testing of the receiver.

There are several sources of noise in the board test environment. The most prevalent sources of noise are ground bounce and coupling effects. Ground bounce consideration will be focused on on-chip switching of internal signals and on on-chip simultaneous switching of input/output signals, but will not consider ground bounce issues that are caused by inadequate grounding and bypassing of the board. Signal integrity issues are not covered since they would be considered a part of Best Design Practices.

NOTE—The term “ground bounce” is intended to include distortions that occur in any power supply rail including ground. Ground bounce attacks the assumption that there are stable voltage sources when in reality, the power and ground rails used by devices and boards are subject to transient inductive and resistive voltage offsets that can disrupt circuit behavior.

4.11.1 Noise effects generated by on-chip switching of internal signals

The best way to reduce noise would be to disable all mission mode circuitry on-chip. If devices have on-chip oscillators or phase-locked loops (PLL) along with functional (mission) circuitry which is not disabled during testing or a clock input which has not been disabled during testing, there may be some “ground bounce” internal to the device which could affect both driver and receiver operation. This noise, synchronous with the on-chip oscillator, would be minimized by good power distribution layout and good on-chip decoupling, and this would be considered a Best Design Practice. For example, the magnitude of this noise effect in a recent complementary metal oxide semiconductor (CMOS) technology can be modeled as a triangular current pulse on the power supply rails with duration of 0.5 nsec. (See Figure 34.) The amplitude of the pulse will increase or decrease depending upon on-chip decoupling. The voltage domain response will be determined by the specific design implementation (RLC) of the on-chip power distribution system, but it will typically be a damped sine wave with peak amplitude of about 5% of the supply voltage for best practices, though up to 15% has been observed. Proper care in separating I/O power distribution from internal circuitry power distribution is also important so that on-chip generated noise does not severely impact test receiver performance.

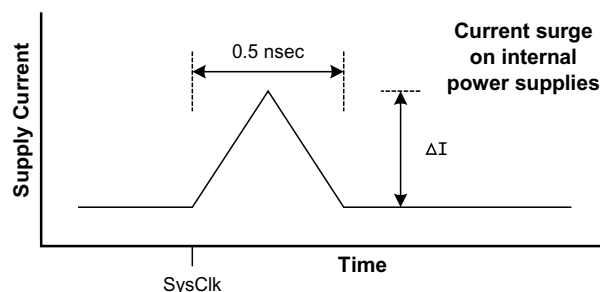


Figure 34—Internal supply current surge in CMOS, synchronized to an internal clock edge, a source of noise in the power distribution system

The noise pulse can be filtered by appropriate hysteresis settings in test receivers. In general, device designers should assure that on-chip logic, which is not part of the test logic, be forced to a quiescent state during Boundary-Scan testing. Internal oscillators and PLLs should be disabled when possible, or their output distribution disabled.

4.11.2 Noise effects that are generated by switching of I/O signals

Noise effects that are caused by simultaneous switching of component outputs are well understood by the design community. In general, simultaneous switching of single-ended outputs can create significant current surges in either or both I/O voltage rails. This results in significant voltage excursions that can affect operation of circuits on-chip as well as signal integrity across the board. Differential drivers contribute very little to the current surge since they are balanced, but can be affected by resulting voltage excursions, as can differential or single-ended receivers. Simultaneous switching may be significantly worse during Boundary-Scan testing, since all drivers are updated with a single clock. The chip and board designers must address these issues for both mission and test operation of the chip. Therefore, much of the noise generated by simultaneous switching of outputs should be addressed as Best Design Practices.

Noise effects that are generated by simultaneous output switching may be greater in amplitude and duration than noise due to on-chip switching that was discussed in 4.11.1. Noise due to simultaneous switching of outputs can be simulated as shown in Figure 35. The current surge induced may last several nanoseconds (ns) and the resulting voltage sag (reduction in I/O voltage, $V_{dd}-V_{ss}$) may range from 500 mV–1000 mV, depending on the application and I/O voltage levels.

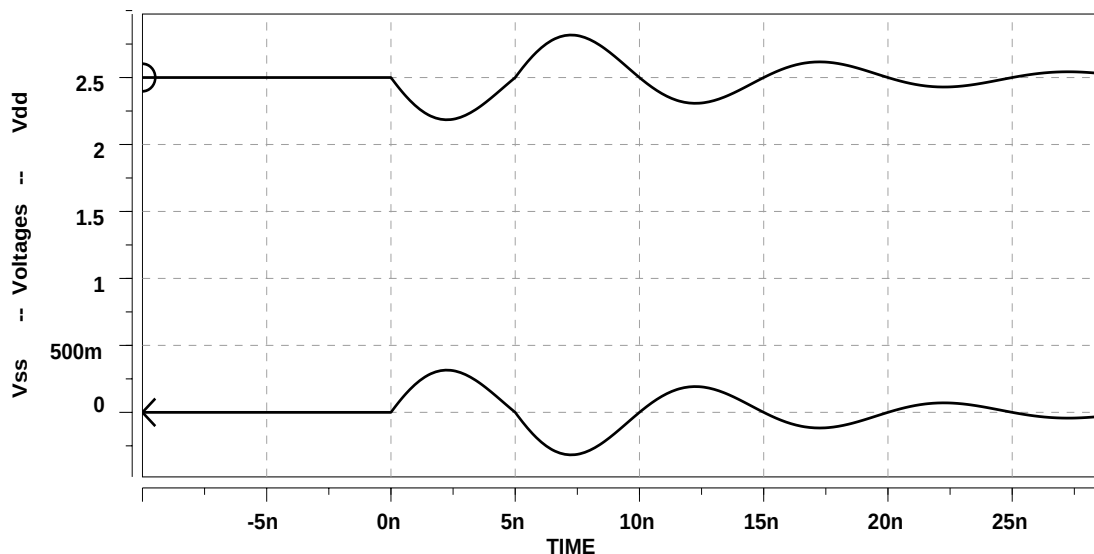


Figure 35—Example of a signal model used for simulation of supply voltage (V_{ss} , V_{dd}) bounce within an IC due to simultaneous I/O switching

The traces in Figure 35 show typical voltage fluctuations due to the almost simultaneous switching of many single-ended outputs for a .18 micron CMOS chip, assuming an equal number of outputs switch from '0' to '1' and from '1' to '0.' The current surge peaks about 5 ns after the falling edge of TCK in the *Update-DR* TAP Controller state and returns to quiescent after about another 5 ns. These traces show sag of about 750 mV total and extended ringing that will depend on the RLC characteristics of the supply distribution network.

The testability circuitry provided by this standard minimizes the effects of simultaneous switching of outputs based on the way that signals are driven from the output boundary cells and captured at the receiver. Outputs under control of AC testing instructions (AC output pins) will switch additional times while the DC

pins are not switching in order to avoid the noise generated by the DC pins. In addition, AC input pins, for both AC and DC testing instructions, will be sampled in a way that will minimize the window in which the noise effect can impact the test results. It is also assumed that switching of differential signals will not have

a significant noise effect due to the current balancing that is inherent to differential signaling. Noise effects can still be minimized by judicious selection of hysteresis parameter values and well-designed board-level power distribution and bypassing. See 6.2.3 for discussion of selection of hysteresis parameters.

4.11.3 Noise effects generated by signal coupling

Inductive coupling from a signal (S) to a differential pair (D1 and D2) is shown Figure 36. This coupling effect may or may not be considered common-mode based on the layout of the printed wiring. If the distance of S from the differential pair is significantly greater than the distance d of the two traces of the differential pair, the effect will be nearly equal (i.e., common-mode) on both traces.

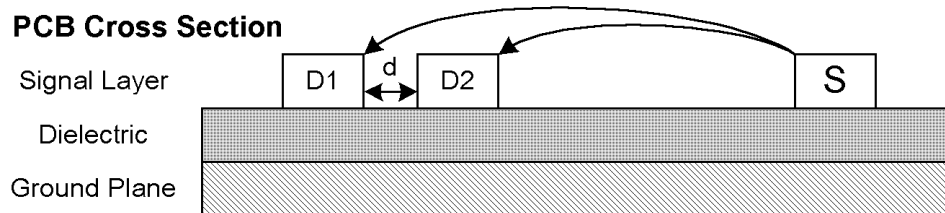


Figure 36—Crosstalk from a single aggressor signal (S) to two differential victim signals (D1 and D2)

This type of behavior could be considered as Best Design Practice, since the benefit of differential signaling will be lost if the coupling effect is greater on one of the two traces. As before, this standard will not address layout issues that cause coupling effects that also impact mission performance.

The magnitude of the coupling effect is related to the transition time of the signal, the distance from neighboring traces, and the trace “coupling length” for which this “coupling distance” is maintained. Coupling effects could be several hundred mV and could last for several ns based on the distance that the traces stay adjacent (coupling length).

Again, because AC-coupled and DC-coupled signals are switched and sampled at different times during the test, the coupling effect can be minimized to some extent. Since software exists that can model the effect of coupling, the test engineer should proactively work with the board designer to ensure that coupling effects can be minimized (both magnitude and duration) on differential pairs that use test receivers. All coupling effects should fall within the hysteresis windows (meaning the test receiver will filter them out). The test engineer should be able to provide the design engineer with information pertaining to when signals switch and how they are sampled to determine possible problem areas that may need to be changed in the board layout.

4.11.4 General notes to design and test engineers

It is important that the chip designer, board designer, and test engineer work proactively to minimize the effect of noise on the Boundary-Scan test. Chip designers should work with both board designers and test engineers to determine the optimal hysteresis settings based on the environment that the chip is expected to operate in for both mission and test modes. The test engineer must now work with the board designer to minimize noise effects in areas where these effects will impact test results and should work with the chip designers to guarantee optimal noise immunity for any components built to the specification herein. How to determine the appropriate hysteresis values to obtain acceptable noise immunity will be covered later in this

standard (see 6.2.3). It is important that the board designer, chip designer, and test engineer all understand how to determine these values and their effect in order to minimize any potential impacts to testing.

Finally, as is the case with most “structural” test techniques [in-circuit test (ICT) and Boundary-Scan], the board should be “disabled” as much as possible during test. This would include controlling and/or disabling any functional clocks and any non-Boundary-Scan logic that could be actively transitioning during Boundary-Scan testing of the board.

5. Instructions

5.1 IEEE Std 1149.1 instructions

All instructions provided by IEEE Std 1149.1 perform as specified in that standard for all DC pins. For AC pins, all IEEE Std 1149.1 instructions perform as specified with the exception of an inversion between the boundary register cell and the negative leg of a differential driver (see 6.2.2).

5.1.1 Rules

- a) All instructions specified by IEEE Std 1149.1 shall perform as specified in that standard, and for any such instruction that controls or observes pins, all AC and DC pins shall also perform as specified by that standard, with one exception: for any output or bidirectional pair of AC pins controlled by a differential driver, there shall be a logical inversion between the Boundary-Scan Register data cell and one of the AC pins.

NOTE—In addition, the AC pins shall perform per rules specified herein.

5.1.2 Description

IEEE Std 1149.1 allows a single data register cell to control a differential driver, but treats this situation as a digital-to-analog boundary, where no rules are given to govern the behavior of the analog portion. IEEE Std 1149.1 does maintain that there be no signal inversion between data register cells and digital pins. Rule a) in 5.1.1 clarifies that a single data register cell providing data to a differential driver that controls a pair of AC pins will have no inversion with one pin and signal inversion with the other. Thus a differential receiver connected to these two pins (and provisioned with independent test receivers on both legs, per 6.2) will see data and inverted data from the driver’s Boundary-Scan Register data cell.

IEEE Std 1149.1 is the foundation for this standard. The (DC) EXTEST instruction enables level-detecting behavior (see 6.2.2) on signal paths containing AC pins. This instruction is useful for detecting shorted capacitors on AC-coupled paths, and certain other possible defects (defects 7, 9, 10, 12, 13 and 14 listed in Table 1 in 4.4).

5.2 AC testing instructions

This standard mandates the addition of two new instructions. The first is EXTEST_PULSE (see 5.3), and the second is EXTEST_TRAIN (see 5.4). These instructions are similar in that they cause the outputs of drivers connected to AC pins to change state at least two times after entering the *Run-Test/Idle* TAP Controller state, and differ in the details of how those transitions are generated.

Throughout this subclause, and in several others, these instructions are described as generating and processing an “AC Test Signal.” This signal never appears at an I/O pin where it can be directly observed. It is a tool for visualizing the requirements of this standard and does not need to be implemented as documented herein. However, its actions upon other signals that are observable at I/O pins are required. The