

IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks

IEEE Computer Society

Sponsored by the
Test Technology Standards Committee



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USA

IEEE Std 1149.6™-2015
(Revision of
IEEE Std 1149.6-2003)

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IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks

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Test Technology Standards Committee
of the
IEEE Computer Society

Approved 5 December 2015

IEEE-SA Standards Board

Abstract: IEEE Std 1149.1™ is augmented by this standard to improve the ability for testing differential and/or ac-coupled interconnections between integrated circuits on circuit boards and systems.

Keywords: ac-coupled signaling, boundary scan, circuit boards, differential signaling, IEEE 1149.6™, integrated circuits, interconnect test, printed circuit boards, test

*This standard is dedicated to the memory
of our friend and colleague, Carl Barnhart.
This was Carl's standard from start to
finish. Carl was our leader and mentor.
We will dearly miss his passion, humor
and vast knowledge.*

The Institute of Electrical and Electronics Engineers, Inc.
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Introduction

This introduction is not part of IEEE Std 1149.6-2015, IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks.

History of the development of this standard

The development of this standard was started on 21 May 2001 by an ad hoc industry Working Group called by Agilent Technologies¹ and Cisco Systems. This group formulated this standard with the intention of handing it over to the IEEE for formal standardization when the underlying technology became understood.

The group adopted as its mission: To define, document, and promote a means for designing integrated circuits (ICs) that support robust boundary-scan testing of boards where signal pathways make use of differential signaling and/or ac-coupled technologies. This technology utilizes and is compatible with the existing IEEE Std 1149.1². The goal is to upgrade the capabilities of IEEE Std 1149.1 to maintain the rapid and accurate detection and diagnosis of interconnection defects in boards and systems despite the fault-masking effects of differential signaling and the dc blocking effects of ac-coupled signaling.

The group first referred to itself as the “AC EXTEST” Working Group, but has since expanded its charter to consider topics now called “Advanced I/O.”

Changes introduced by this revision

A summary of the changes includes the following:

- Deletion of Annex E content
- Changes driven by the 2013 update to IEEE Std 1149.1
- Added new level-detection behavior to the test receiver for ac-coupled channels
- Documentation of driver and test receiver analog parameters, including documenting programmability of those parameters
- Programmability of coupling capacitor shunts
- Documentation of non-compliance of certain pins to EXTEST_PULSE performance
- Addition of Procedure Description Language (PDL) routines for documenting the procedures to access programmable analog parameters
- IP Package support in Boundary-Scan Description Language (BSDL)
- New “AC” boundary register cell designs

This revision affirms what has been required from the previous version, and products that conform to the previous version are still compliant with this revision. There is one deletion: Annex E (informative) proposed an “Initialize” instruction. This topic has since been subsumed into IEEE Std 1149.1-2013.

Many of the changes found in this revision are in response to the major revision of the underlying IEEE 1149.1 standard that was released in 2013. This standard introduced new concepts, such as segmented data registers, the initialization data register, and register descriptions. These concepts, once adopted in new ICs,

¹ Now called Keysight Technologies.

² Information on references can be found in Clause 2.

will materially affect the design, and subsequent description in BSDL, for those devices that are to conform to this standard.

There are also changes that come from industry commentary and usage practices developed over the past decade. A known problem exists in the 2003 version of this standard for level-sensitive behavior when using the EXTEST instruction defined in IEEE Std 1149.1. Simply, in some cases it is impossible to ensure compatible drive and receive voltage levels. When a channel is guaranteed to be ac-coupled, and the only use for the EXTEST instruction is to detect a shorted capacitor, there is a new behavior defined that essentially performs a simple but robust continuity check. See option 2) of rule a) in 6.2.2.1.

A significant addition provided by this revision is the ability to provide for (and describe) variable, programmable parameters such as threshold and common mode voltages. This will assist the users of test generation and diagnosis tools in creating and debugging tests, where analog parameter mismatches could occur.

On-chip ac coupling capacitors can now have provisions to shunt them out of the input signal pathway under control of the test circuitry. Improvements are offered to the ability to test external (board level) capacitors for shorts and to compensate for mismatches in voltages between devices.

It is recognized in this revision that for some pins, it may not be possible for the EXTEST_PULSE instruction to transmit or receive data due to dynamic conditioning of the associated circuitry that is not fully completed by a single data pulse; that is, a longer set of transitions, such as that provided by EXTEST_TRAIN, may be required. Such pins that need this exception can now be identified in BSDL so that tools can make appropriate tradeoffs for them.

The 2013 revision of IEEE Std. 1149.1 also added a new PDL, which is used to describe how devices and their registers are used for various testing purposes. This revision requires the documentation of certain programmable features, when implemented in a device, in PDL.

The 2013 revision of IEEE Std. 1149.1 made significant additions to BSDL, which affect the BSDL representation of 1149.6 technology as described in Clause 7. Part of these changes are driven by the electronics industry's movement towards the usage of intellectual property packages, where portions of circuitry are bought and sold for inclusion in other IC designs. This means that, along with the circuitry description, any relevant test-oriented information about IEEE 1149.1 or IEEE 1149.6 implementations contained within such IP must also be provided in BSDL packages. Thus, significant changes for such support are found in Clause 7 — see 7.4 and 7.5, taking note of “Port Behavior” descriptions. New and updated examples for both BSDL and PDL appear in Clause 7.

Annex C contains information on ac boundary register cell designs. Two new cells [AC_40 and AC_41 (see C.9)] are documented there.

Updating BSDL to the new standard

Components compliant with the 2003 version of this standard will typically be compliant with this new version. However, the BSDL documentation must be updated. First, the BSDL will need to be updated to comply with the changes introduced in IEEE Std 1149.1-2013, including as a minimum:

- Changing all “Linkage” pin types to the new linkage and power pin types in the port declaration.
- Updating “Use” and component conformance statements to STD_1149_1_2013.
- Adding an <input spec> for all pins of type "input" in the Boundary-Scan Register description.
- Taking advantage of the optimal register structural descriptions (REGISTER_MNEMONICS, REGISTER_FIELDS, REGISTER_ASSEMBLY, etc.) and of the PDL language to document

programmable characteristics of the component that could not be documented in a standard form before. This would be particularly valuable when documenting any initialization built into the component and required for proper operation of the I/O and boundary tests.

Second, the BSDL will need to be updated to comply with the changes introduced by this standard:

- Updating AIO component conformance statement to STD_1149_6_2015.
- Adding to the AIO_Pin_Behavior attribute the new parameters for driver common-mode and peak-to-peak voltages, test receiver threshold and hysteresis voltages, bypass control of on-chip capacitors, and any ports that require the EXTEST_TRAIN instruction.
- Adding PDL procedures to document initialization of any programmable I/O parameters. This ties into the new initialization documentation introduced in IEEE Std 1149.1-2013.

A component compliant with IEEE Std 1149.1-2001 and IEEE Std 1149.6-2003 may have included proprietary capabilities for initializing I/O, including advanced I/O. If the capabilities are conformant to the new requirements of these standards, then they must be documented in order to be compliant. However, even if those proprietary capabilities are not conformant, if they can be made public by writing procedures in PDL using the reserved PDL procedure names where appropriate, doing so will improve the automation of test generation and execution.

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Also, the PDF version of this document contains bookmarks of major headings and page thumbnails, also helpful in navigating the document.

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IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks

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1. Overview

1.1 Scope

This standard defines extensions to IEEE Std 1149.1™ to standardize the boundary-scan structures and methods required to [help](#) ensure simple, robust, and minimally intrusive boundary-scan testing of advanced digital networks.¹ Such networks are not adequately addressed by existing standards, especially for those networks that are ac-coupled, differential, or both. Testing enabled by this standard will operate in parallel with IEEE Std 1149.1 testing of conventional digital networks and in conjunction with IEEE Std 1149.4™ testing of conventional analog networks. This standard also specifies software and Boundary-Scan Description Language (BSDL) extensions to IEEE Std 1149.1, which are required to support new I/O test structures.

¹ Information of references can be found in Clause 2.

1.2 Purpose

Existing boundary-scan test standards (IEEE Std 1149.1, IEEE Std 1149.4) do not fully address some of the increasingly common, newer digital network topologies, such as ac-coupled, differential interconnections on very high speed (1+ Gb/s) digital data paths. IEEE Std 1149.1 structures and methods are intended to test static (dc-coupled), single-ended networks. They are unable to test dynamic (ac-coupled) digital networks, since ac coupling blocks static signals. Differential networks are also inadequately tested by IEEE Std 1149.1, which requires either the insertion of boundary cells between the differential driver or receiver and the chip pads (this often creates an unacceptable performance degradation), or insertion of single boundary cells before the differential driver and after the differential receiver (this reduces controllability and observability to the point that many board assembly defects cannot be detected). IEEE Std 1149.4 structures and methods are intended for testing analog networks, and in most cases are not able to test these newer digital networks as well. Specifically, IEEE Std 1149.4 provides the opportunity to inject dynamic (time-varying) or analog signals for test, but these structures intended for analog testing are often too intrusive (too high an impact on performance and pin count) for high speed chip designs, and require additional resources and test application time not otherwise required for testing digital circuits. Finally, very high-speed logic imposes new restrictions on test structures that were not considered in IEEE Std 1149.1.

1.3 Organization of the standard

Clause 1, Overview, provides an overview and context for this standard.

Clause 2, Normative references, provides references necessary to understand this standard.

Clause 3, Definitions and acronyms, defines terminology and acronyms used in this standard.

Clause 4, Technology, is a tutorial that outlines the technologies addressed and utilized by this standard. This clause does not contain rules.

Clause 5, Instructions, provides rules for instructions used for testing.

Clause 6, Pin implementation specifications, provides rules for I/O pin implementation.

Clause 7, Conformance and documentation requirements, provides rules for conformance and documentation of devices designed to this standard.

Annex A,

(informative)

Applications and tools, shows how this standard is used in typical testing applications and how devices conforming to this standard can be verified before manufacture and tested in production.

Annex B,

(informative)

Noise rejection in edge-detecting mode, gives guidance for designing test receivers with noise rejection capabilities.

Annex C,

(informative)

Advanced I/O boundary-scan register cells, documents new boundary-scan register cells used by this standard.

Annex D,

(informative)

Test receiver design examples, shows how the input pins of some common logic families can be designed to conform to this standard.

Annex E,

(informative)

A proposed “INITIALIZE” instruction. This annex is omitted from this revision of this standard. The topic of test data initialization has been included in the revised IEEE Std 1149.1-2013.

~~A proposed “INITIALIZE” instruction, provides the outline of a proposed instruction that forcibly initializes complex devices into a state where testing operations can then proceed. This instruction is not yet fully developed nor is this portion of this standard normative. It is included here to alert the test standards community about the need for such an instruction and to invite comment.~~

Annex F,

(informative)

Bibliography

1.4 Context

Figure 1 shows a printed circuit board containing many types of devices. Of these, some could be compliant with IEEE Std 1149.1 for the support of testing activities. These devices contain boundary-scan testability circuitry, which allows them to participate in manufacturing tests that detect and diagnose faults such as open solder joints, shorts, and missing devices.

The additional testability elements added by this standard to these same integrated circuits (ICs) allow this interconnect testing, with enhanced coverage, to be conducted on differential signal pathways and/or where ac coupling (which blocks normal dc test signals) has been used on signal paths between ICs.

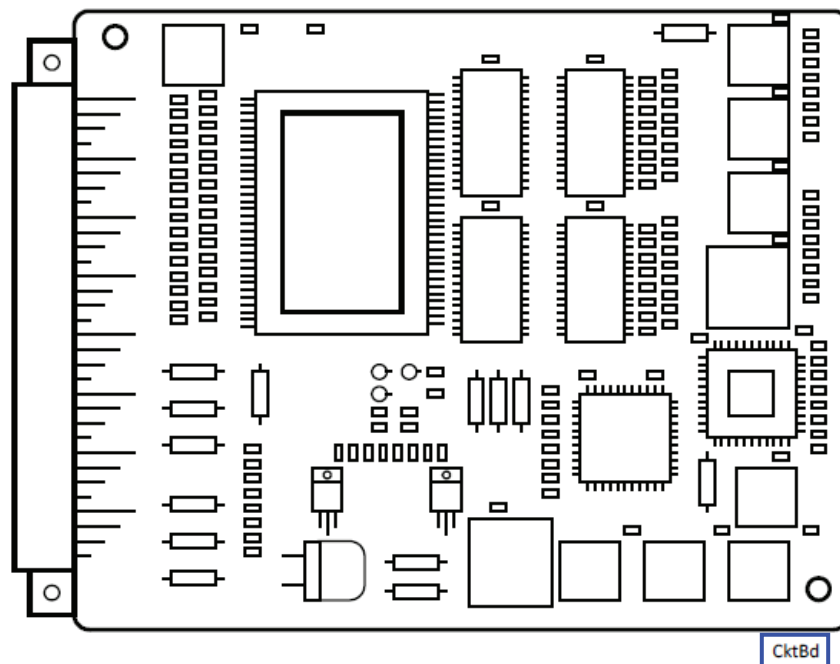


Figure 1 — A printed circuit board containing a variety of components interconnected by printed wiring. Some ICs contain IEEE Std 1149.1 features that support boundary-scan interconnect testing

~~This standard is built on top of IEEE Std 1149.1 using the same Test Access Port structure (with 4, optionally 5 pins) and Boundary Scan architecture. It adds the concept of a “test receiver” to input pins that are expected to handle differential and/or AC coupling. It adds two new instructions that cause drivers to emit AC waveforms that are processed by test receivers.~~

1.5 Objectives

The objective of this standard is to provide design guidance for testability circuitry added to an IC in addition to testability provisions specified by IEEE Std 1149.1, such that when ~~such~~ an IC contains differential signaling and/or is ac-coupled with other ICs compliant to this standard, board and system level tests can be readily and accurately conducted with enhanced defect coverage.

Devices that adhere to this standard that are used in differential and/or ac-coupled signaling environments will realize significant savings in testing costs for boards and systems. Tools that are cognizant of the capabilities provided by this standard will be able to prepare, run, and interpret these tests in a highly automated fashion, with high diagnostic resolution.

This standard allows devices created by multiple vendors to operate together during testing despite the differing characteristics and parameters of the IC processes used to fabricate the devices. This standard also provides design guidance to board and system designers that will enhance the performance of the testability features of their products. This in turn will reduce system and production costs.

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

~~This standard shall be used in conjunction with the following standards. When the following standards are superseded by an approved revision, the revision shall apply.~~

IEEE Std 1149.1TM ~~2001~~, IEEE Standard Test Access Port and Boundary-Scan Architecture.^{2,3}

IEEE Std 1149.4TM ~~2000~~, IEEE Standard for a Mixed-Signal Test Bus.

3. Definitions and acronyms

For the purposes of this document ~~standard~~, the following terms and definitions apply. ~~IEEE 100,~~ The ~~Authoritative~~ IEEE Standards Dictionary Online ~~Terms, Seventh Edition [B1]~~,⁴ should be consulted ~~referenced~~ for terms ~~and definitions~~ not defined in this clause.⁴

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⁴ IEEE Standards Dictionary Online subscription is available at: <http://ieeexplore.ieee.org/xpls/dictionary.jsp>

⁴ ~~The numbers in brackets correspond to those of the bibliography in Annex F.~~

3.1 Definitions

~~Defined terms appear in bold type.~~

ac coupling: The use of series capacitance in a signal path. This coupling will block dc voltages on the drive side of the path from appearing on the receive side. Only the ac component of the driven signal will pass through the coupling, with the effect of high-pass filtering imposed on the original signal. *Contrast:* **dc coupling**.

ac pins: Advanced I/O pins that require a time-varying (ac) signal to permit testing of their interconnections. This includes all differential signal pins and differential or single-ended signal pins that are expected by design to [support ac coupling](#). *Contrast:* **dc pins**.

NOTE—AC coupling [could](#) ~~may~~ also be accomplished with transformers, which, as with capacitive coupling, form a high-pass filtered transmission structure. While the principles used and rules defined in this standard apply to transformer coupling, this coupling technology is less often used and is thus omitted to simplify discussion.⁵

ac test mode: A test mode that enables boundary-scan testing between ac pins that are ac-coupled or dc-coupled. Testing dc-coupled ac pins [in ac test mode could](#) ~~may~~ enable testing that cannot be supported in dc test mode due to voltage level incompatibilities. *Contrast:* **dc test mode**.

ac test signal: A signal generated by the ac test mode that is used to modulate static test data into a time-varying signal that can pass through ac coupling. A test receiver and detector are used to recover the static test data value from within the time-varying signal.

⁵ [Notes in text, tables, and figures of a standard are given for information only and do not contain requirements needed to implement this standard.](#)

ac testing: Testing ac pins using an ac test mode.

advanced I/O: Input/output (I/O) circuits ~~and protocols~~ that are designed to convey digital information, the interconnections of which cannot, either by design or by common usage, be adequately tested with static digital signals such as those provided for in IEEE Std 1149.1. For example, such an I/O pin could be self-referenced (i.e., to its own average voltage), or referenced to another I/O pin, rather than to a fixed voltage.

bias: A high-impedance (relative to line and termination impedance, typically $>1000\ \Omega$) voltage source often used on the input of a mission receiver to cause it to output a deterministic state in the absence of an input signal, and/or to select the common-mode voltage seen by a differential receiver in ac-coupled signal paths.

bias network: A network of impedances, usually higher valued than termination impedances and usually located in or near the receiver, used to establish a common-mode or reference voltage.

boundary-scan testing: Testing of interconnections between IC pins as supported by IEEE Std 1149.1 and this standard. This testing technology looks for manufacturing defects along signal paths, which include open solder joints, broken bond wires, shorted signal traces, damaged drivers and receivers, etc. Tests are performed on many paths in parallel.

channel: A signal path or set of signal paths that transmits a single data stream from a source to a destination. *See:* **differential signaling; single-ended signaling.**

characteristic impedance: The ratio of the complex voltage and complex current of a signal traveling forward on a conductive path. A signal path is often terminated with an impedance that matches the characteristic impedance of the path. This makes the path appear to be infinitely long and prevents signal degradation due to reflections that occur at unterminated ends of the path. *See: **termination**.*

common-mode noise: A noise signal added equally to both signal paths in a differential signal channel. Common-mode noise will affect or completely disrupt a single-ended measurement of a signal on one leg of a differential receiver, yet this differential receiver will accurately recover the signal within the noise.

common-mode range: The range of common-mode voltage that a differential receiver is capable of receiving while maintaining reliable signal recovery. A differential signal with common-mode voltage within this range will be received correctly. Outside this range the receiver could ~~may~~ fail to recover the data signal.

common-mode voltage: The offset from ground of the mean of the maximum and minimum voltages that appear on a pair of differential signals. A differential driver will, by its operational characteristics, define a common-mode voltage. A differential receiver will properly receive data over a range of common-mode voltages, but will likely have an optimal common-mode voltage where its performance is best. When the optimal common-mode voltage of a receiver is significantly different than that of its associated driver, ac coupling with appropriate bias can be used to match the two components of a differential channel.

[NOTE—Common-mode voltage is discussed extensively in Clause 4 and 6.2.](#)

comparator: An amplifier with two inputs labeled positive and negative, typically with very high input impedance. The amplifier usually has very high gain and produces an output signal that is the amplified difference of the positive and negative input signals. For all but the smallest differences, the output will be $V_{\max}$ or $V_{\min}$, which are the most positive and most negative voltages the amplifier can produce on its output. A comparator can be used as a differential receiver. A comparator can be used to determine if an input signal is logically above or below a reference voltage.

current signaling: A signal encoded by the amplitude and direction of current flow. In a differential pair, a current signal is positive when current flows from positive to negative legs, and negative in the reverse direction. The voltage that ~~may~~ appears on these same legs does not carry information. *Contrast: voltage signaling.*

dc coupling: The use of simple wires or small series resistances in a signal path. *Contrast: ac coupling.*

dc pins: ~~DC pins are~~ Single-ended pins that are dc-coupled. DC pins only need be equipped with test resources defined by IEEE Std 1149.1. [Single-ended](#) ~~DC~~ pins that are ac-coupled are not normally testable as a signal path, but might be testable as logically independent pins if there are enough test resources on each pin. *Contrast: ac pins.*

dc test mode: A test mode that enables traditional boundary-scan testing ([as defined by IEEE Std 1149.1](#)) between dc pins ~~that are DC-coupled~~. *Contrast: ac test mode.*

defect: A defect is an unacceptable deviation from a norm. For example, an open solder joint. Because it is unacceptable, some remedial action is needed. *See: fault; manufacturing process defect.*

deprecated: Used in this standard for possible configurations or modes of operation that might not operate reliably and should be either avoided or treated with special care. *Synonyms:* **disapproved, belittled, discouraged, disparaged.**)

derived voltage reference: A voltage reference derived from: a) other references, such as a resistive divider between power and ground, or b) a resistive divider between two differential signals that recovers the common-mode voltage of the signals.

differential driver: A driver that accepts a single data stream and drives it onto two independent signal paths where one signal is the inverse of the other. The two signals are centered at the common-mode voltage.

differential receiver: A receiver that recovers a single data stream encoded differentially on two signal paths. It effectively subtracts the signal on its negative leg from that on its positive leg. This eliminates common-mode noise appearing on both legs.

differential signaling: The use of two independent signal paths in a channel to carry a single data stream where one path carries an inverted copy of the signal that appears on the other path. The original data signal can be reconstructed by taking the difference of the two signals. There is no reliance on a reference voltage for determining this signal. This has the property of eliminating common-mode noise in the transmitted signal. *Contrast:* **single-ended signaling.**

encoding protocol: A stream of data bits **may be** encoded into a new (typically longer) data stream that has characteristics favorable for its transmission on a channel. The encoded stream might have added redundancy to support error correction. The encoded stream **could may** have extra bits added to deliberately increase the number of transitions that appear in the stream, effectively raising its apparent frequency and facilitating data transmission that encodes clocking information into the stream.

fault: A fault is a physical manifestation of a defect. For example, an open solder joint (a defect) on the input to an IC could ~~may~~ cause one or more of its outputs to produce incorrect data (a physical manifestation). In many cases, a fault and its causal defect are not co-located.

float: The input to a receiver that is connected to an undriven signal, or a high-impedance connection to a receiver input, is said to float.

frequency: The number (f) of transition pairs that occur on a signal path in a period of time, expressed in Hertz (cycles per second). With respect to ac coupling, a frequency is high when the period ($1/f$) is small compared to the time constant of the coupling. A frequency is low when the period is large compared to the time constant of the coupling. The frequency appearing on a signal path could ~~may~~ vary greatly over time as a function of the data being transmitted and the data encoding protocol.

high-pass filter: An electrical network that passes higher frequencies and attenuates lower frequencies (dc current is blocked).

HP_Mult: High-Pass Multiplier, a multiplier used to derive the minimum high-pass coupling time constant.

NOTE—See 6.2.3.1 and 6.2.3.3.

HPLP_Ratio: High-Pass-Low-Pass Ratio, a multiplier equal to the ratio of the HP time constant to the LP time constant, and used to derive the minimum ratio of high-pass coupling time constant (T_{HP}) ~~(HP_Mult)~~ to edge-detection ~~low-pass~~ filter time constant (T_{LP}) ~~(LP_Mult)~~.

NOTE—See 6.2.3.1 and 6.2.3.2.

hysteresis: From magnetics: lagging in the values of resulting magnetization in a magnetic material (such as iron) subjected to a changing magnetizing force. In this standard, hysteresis refers to the memory of an input state to an amplifier or buffer after that state is removed but before a different input state is applied. Typically, there is a hysteresis threshold that defines the difference between “no input” and “input.” As applied to electronics, a digital output circuit such as a comparator where the output switches to one output state when the input is above one level and switches to the opposite output state when the input is below a lower level, and the output does not switch at any intermediate level. [For](#) example, a buffer produces a high output when a voltage above 0.5 V is applied, produces a low output when a voltage below 0.3 V is applied, and does not change its output for voltages between 0.3 V and 0.5 V.

[A](#) hysteresis symbol in a buffer symbol [is shown in Figure 2](#).



Figure 2 — A hysteresis symbol in a buffer symbol

hysteretic: Adjective form of hysteresis, as in “hysteretic amplifier.”

hysteretic voltage: Given a specified threshold voltage where a logical interpretation of signal would change from 0 to 1 (or vice versa), a hysteretic voltage is a band of values on either side of the threshold where the logical interpretation will not change from its current interpretation. A signal that exceeds (in either direction) the threshold voltage by more than the hysteretic voltage determines the current logical interpretation of the signal.

NOTE—Hysteretic voltage appears as V_{Hyst} in 4.7 and as V_{Hyst_Edge} and V_{Hyst_Level} in 6.2.1.

interconnect test: An IEEE Std 1149.1 boundary-scan test designed to detect and diagnose defects in the interconnection wiring between ICs. This standard extends the concept to include the testing of channels, where single-ended and differential signaling, and dc- or ac coupling could exist.

load termination: A termination placed at the far end (away from the driver) of a signal path used to match the characteristic impedance of the path. *Contrast:* **source termination**.

low-pass filter: An electrical network that passes lower frequencies, including dc levels, and attenuates higher frequencies.

LP_Mult: Low-Pass Multiplier, a multiplier used to derive the minimum edge-detection (usually a low-pass) filter time constant.

NOTE—See 6.2.3.1 and 6.2.3.3.

manufacturing process defect: A defect that is an unacceptable by-product of the manufacturing process. For board manufacture these include missing devices (ICs, resistors, capacitors, etc.), improperly mounted devices (e.g., rotated 180°), open solder joints, shorted solder joints, misaligned devices, and incorrect and dead devices.

mission logic: The circuitry inside an IC that performs its primary design function. *Contrast:* **test logic**.

mission mode: An operational mode in which a device performs its primary design function. *Contrast:* **test mode**.

negative leg: The signal path of a differential signal pair that has the opposite polarity as the original data signal.

null: The input state where the two inputs to a differential receiver that are supposed to be different (complementary) are instead receiving essentially the same value.

offset voltage: A constant dc voltage added to an ac signal.

operational modes: A device could function in several modes. For the purposes of this specification, two primary modes are considered. *See:* **mission mode**, **test mode**.

peak-to-peak voltage: The maximum voltage minus the minimum voltage appearing on a waveform. This is always a non-negative voltage.

NOTE—Peak-to-peak voltage appears as ΔV_{Min} in 6.2.1.

positive leg: The signal path of a differential signal pair that has the same polarity as the original data signal.

reference voltage: A low-impedance voltage source typically used to define a threshold for comparing signals. The low-impedance characteristic means it is resistant to conducting noise signals. *Contrast:* **bias**.

referenced termination: A termination for a differential channel where the two legs are both terminated to a reference voltage. This reference has an impedance that is low relative to the termination impedance, such that the two legs are independent. *Contrast:* **bias network**.

self-referenced comparison: The comparison of a signal with a delayed, averaged version of the same signal, used to detect signal transitions. This process does not need a static reference voltage to find a transition in a signal.

signal path: An electrical pathway formed by a simple conductor, ~~or~~ a terminated pathway containing a series resistance, or an ac-coupled pathway containing a series capacitance that transmits a signal from a driver to a receiver.

signal reflection: A signal wave front traveling across a discontinuity in the characteristic impedance of the signal path will have a fraction of its energy reflected in the opposite direction on the path. The reflection will be of either the same or opposite polarity and will add into the waveforms appearing on the path, impacting their shape. *See also:* **transmission line**.

single-ended signaling: The use of a single signal path in a channel to carry a data signal. The signal is referenced to a static reference voltage. *Contrast:* **differential signaling**.

slew rate: Rate of change in either direction of voltage, measured in units of volts per second.

source termination: A termination placed near the source driver of a signal to satisfy dc current requirements of a driver and/or to match the characteristic impedance of a transmission line structure to reduce signal reflections. *Contrast:* **load termination**.

termination: An impedance usually near the end of a signal path used to satisfy the electrical matching requirements of the characteristic impedance of the signal path and reduce signal reflections. The impedance is typically low, often 100 Ω or less. *See also:* **characteristic impedance, load termination, referenced termination, source termination, unreferenced termination**.

test logic: Testability logic defined by this standard and IEEE Std 1149.1 ~~and 1149.4~~. *Contrast:* **mission logic**.

test mode: An operational mode of the device in response to the EXTEST or an ac testing instruction whereupon the pins are driving or receiving test data as controlled by the test logic of the device. The device pins have been disconnected from the internal mission logic. *Contrast:* **mission mode**.

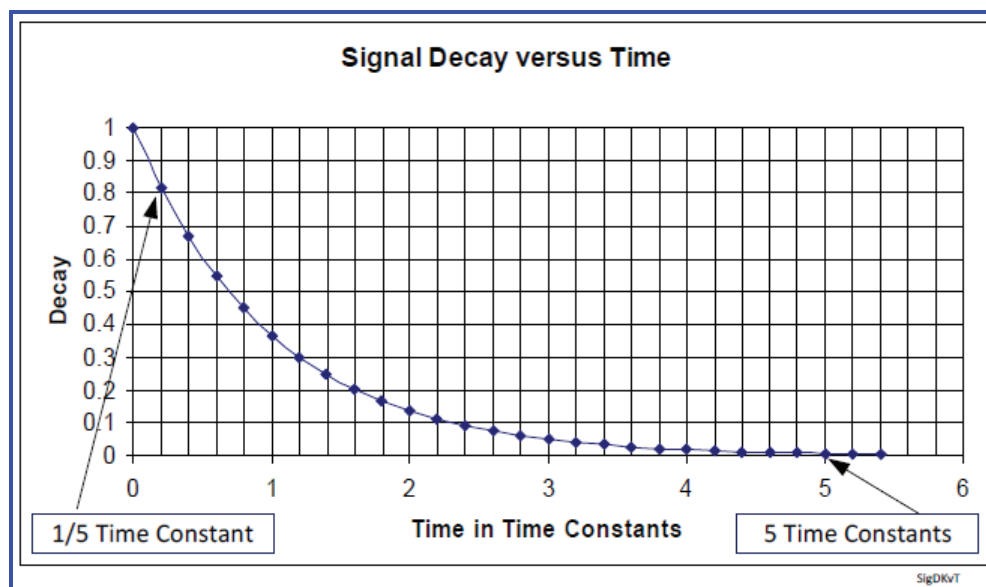
test receiver: A circuit, which can operate in ac test mode and dc test mode, and ~~that~~ examines an incoming signal. Its purpose is to extract test data from a signal that might have been altered by dc level shifting or ac coupling decay.

threshold voltage: A voltage level used to determine if a signal has a logical interpretation of 0 or 1; if the signal is below the threshold, it is interpreted as 0, and it is interpreted as 1 if the signal is above the threshold. For systems with hysteresis, the final interpreted state of the current voltage also depends on how the signal evolved in time and the value of the hysteretic voltage.

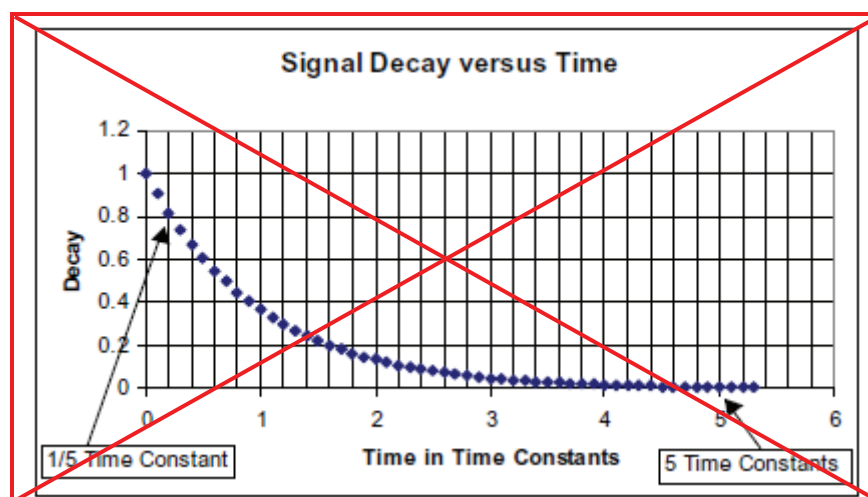
NOTE—Threshold voltage appears as $V_{Threshold}$, discussed in 4.8 and 6.2.2.

time constant: Typically, the product of resistance and capacitance of an RC network (e.g., a high-pass filter) measured in seconds. One time constant is the time for a capacitor to discharge 63% of its voltage through a resistor. In ac-coupled systems, the termination resistance combined with the coupling capacitor forms a high-pass filter.

NOTE—In discussions comparing time periods to time constants, a period is significantly longer (shorter) than a time constant if it is five (one-fifth) times the time constant value. For example, as shown in Figure 3 using the five-time-constant rule, a signal will decay to 0.7% of its original value. The one-fifth-time-constant rule means that 81.9% of a signal still remains.



(New)



(Deleted)

Figure 3 —Signal decay versus time in units of time constants

transition: A voltage transition occurs when a signal traverses a specified voltage range in a specified time in either direction. *See:* **slew rate**.

transmission line: A signal path with a specific construction that produces a uniform, known characteristic impedance along its length. This minimizes degradation of a signal passing along this path that can result from impedance variations.

unreferenced termination: A termination for a differential channel where a termination impedance is connected between the two legs with no connection to a reference voltage.

voltage signaling: Signals are encoded by the voltage appearing on a wire compared to a reference voltage (single-ended) or the voltage [difference](#) appearing on a pair of wires (differential). *Contrast:* **current signaling**.

[wrapper:](#) In the context of this standard, a wrapper is composed of dedicated or shared test logic for a plurality of logic core terminals, providing each terminal with a control/observe capability via serially connected logic elements in test mode, and functional operation while in mission mode. Generally, a wrapper is a thin shell of circuitry around a core circuit that provides controllability and/or observability at the core inputs and outputs.

3.2 Acronyms

[ASCI](#)

[application-specific integrated circuit](#)

~~AC~~ ~~alternating current (used here for any time-varying voltage)~~

BSDL Boundary-Scan Description Language

CML current mode logic

CMOS complementary metal-oxide semiconductor

~~DC~~ ~~direct current (used here for static voltage levels)~~

HPLP_Ratio High-Pass-Low-Pass Ratio

~~HP_Mult~~ ~~High-Pass Multiplier~~

IC integrated circuit

ICT in-circuit test

IP Intellectual Property

LP_Mult Low-Pass Multiplier

LVDS low-voltage differential signaling

LVPECL	low-voltage PECL (~~positive~~ ~~pseudo~~ emitter-coupled logic)
<u>PDL</u>	<u>Procedure Description Language (see IEEE Std 1149.1-2013, Annex C)</u>
~~PECL~~	~~pseudo-emitter-coupled logic~~
PLL	phase-locked loop
<u>RC</u>	<u>resistor/capacitor</u>
SERDES	serialize/deserialize
TAP	Test Access Port (from IEEE Std 1149.1)
TCK	test clock
<u>Tcl</u>	<u>Tool Command Language (see IEEE Std 1149.1-2013, Annex C)</u>
TDI	test data in
TDO	test data out
<u>TDR</u>	<u>test data register</u>

TMS	test mode select
TRST	test reset
VHDL	VHSIC High-Level Design Language
VHSIC	very high-speed integrated circuit

4. Technology

The presence of coupling capacitors [in signal](#) ~~on-chip~~ interconnections [among chips](#), whether they are discrete devices mounted on a PC board or integrated inside an IC, prevents dc values from being driven between a driver and receiver. An ac boundary-scan methodology must therefore use a time-varying signal to pass through the ac coupling when in ac test mode.

Differential signaling is often used to increase signaling speeds and noise immunity, compared to single-ended signaling. Differential signaling, combined with termination schemes, can have significant defect-masking properties that reduce test effectiveness (see 4.3).

This clause contains tutorial discussions of ac coupling, differential signaling, and the effects of defects in such circuits needed to understand Advanced I/O testing technology. Rules based on these technologies are found in subsequent clauses.

4.1 Signal pin types

It is expected that a chip possessing pins requiring ac coupling ~~will often~~ ~~may~~ also possess “normal” pins (i.e., intended to be dc-coupled) ~~as well~~. These dc pins would supply data and/or control to/from portions of the chip that do not require ac coupling. For test purposes, it is necessary that all ~~these~~ pins be tested simultaneously with an EXTEST-like capability because that is how shorts (unwanted connectivity) between these pins are reliably detected and diagnosed. It is desirable for higher test throughput to test all pins simultaneously with an EXTEST-like capability as well.

NOTE—There are some issues related to simultaneously switching all outputs during the EXTEST instruction. These issues will be discussed in later clauses. The implementation of EXTEST on ac and dc pins will provide the needed shorts detection and minimize the noise due to simultaneous switching.

This standard will refer to dc and ac pins henceforth. DC pins are those for which IEEE Std 1149.1 provides adequate testing. AC pins are those Advanced I/O that require additional test resources in order to be adequately tested, including those pins intended for ac coupling or differential signaling.

AC pins are a principle target of this standard. IC designers implementing this standard are expected to identify such pins and add new test capabilities for them.

4.2 Signal coupling and coupling combinations

This subclause reviews a range of coupling options.

4.2.1 Single-ended dc

A basic, single-ended connection scheme is shown in Figure 4, along with the boundary-scan control and observation capability specified by IEEE Std 1149.1. This type of coupling has been quite common and is very testable using boundary-scan.

It is important to note that in a typical boundary-scan test, the time between launching a signal from a driver (at the falling edge of test clock (TCK) in the Update-DR or Update-IR TAP Controller state) and capturing that signal (at the rising edge of TCK in the Capture-DR TAP Controller state) is no less than 2.5 TCK cycles. Further, the time between successive launches on a driver is governed not only by the TCK rate, but by the amount of serial data shifting needed to load the next pattern data in the concatenated boundary-scan registers of the boundary-scan chain. Thus, the effective test data rate of a driver could be thousands of times lower than the TCK rate. For dc-coupled interconnect, this time is of no concern. For ac-coupled interconnect, the signal could easily decay partially or completely before it can be captured. If only partial decay occurs before capture, that decay will very likely be completed before the driver produces the next edge.

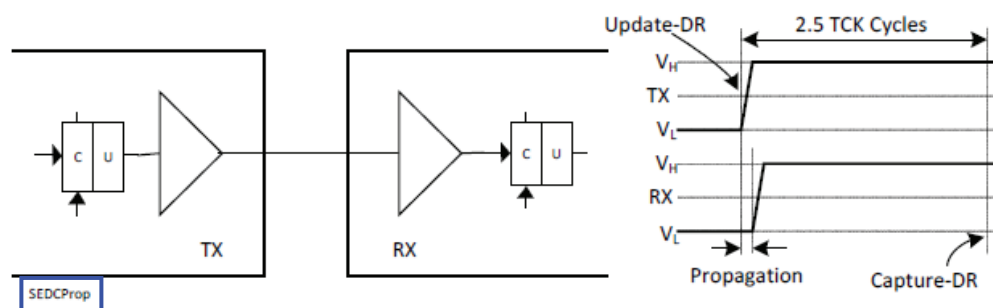


Figure 4 — Basic single-ended signaling with boundary-scan control and observation

4.2.2 Single-ended ac

Figure 5 shows an ac-coupled single-ended connection (The termination resistor and voltage source shown could actually reside within the IC). The size of the capacitors used is determined by the mission requirements of the coupling and could vary widely across applications. While the devices may have been designed for dc coupling and actually contain boundary-scan resources, the ac coupling will block their operation. This interconnection configuration could only be tested at very high TCK frequencies or lower frequencies with very large coupling capacitors, and even then the results might be unreliable. TCK frequencies are likely to be significantly lower than the normal operating frequency of the channel being tested. Thus the data seen by the receiver could decay before it can be captured.

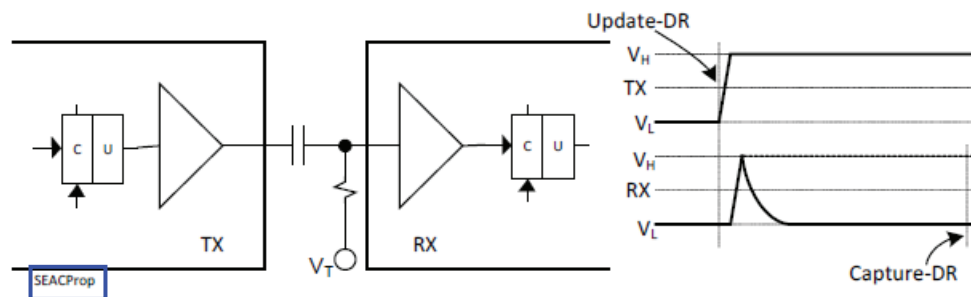


Figure 5 — Basic single-ended signaling with ac coupling

In general, ac coupling can distort a signal transmitted across a channel depending on its frequency. For example, Figure 6 shows a channel transmitting a high and low frequency waveform across an ac channel and observed at the input of the receiver. The high frequency signal is relatively unaffected by the coupling. The low frequency signal is severely impacted. First, it decays to V_T after a few time constants. Second, its [peak-to-peak](#) amplitude is double the input amplitude. A key item to note is that the transitions in the original signal are preserved, although their start and end points are offset compared to where they were in the high frequency case.

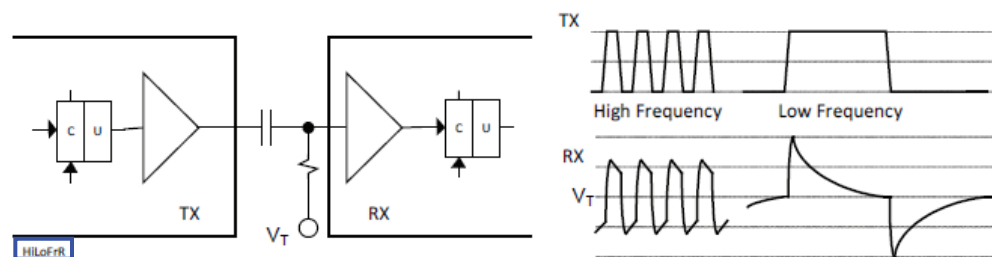


Figure 6 — High- and low-frequency response of an ac-coupled channel

NOTE—The high- and low-frequencies in Figure 6 are relative to the ac coupling time constant. "High frequency" has a cycle time significantly less than the coupling time constant ($< 1/6$), and "Low frequency" has a cycle time significantly greater than the coupling time constant (> 6 times). For the remainder of this document, "High frequency" may be thought of as functional or mission mode behavior, while "Low frequency" may be thought of as test mode behavior clocked by TCK.

4.2.3 Differential dc

Figure 7 shows a basic differential dc-coupled signal path. The termination resistor might exist for impedance matching and/or source termination of the driver. The placement of boundary-scan resources is optional per IEEE Std 1149.1 in that they can be omitted altogether. The IEEE Std 1149.1 standard allows a designer to designate the differential signal path as "analog." Then the digital-to-analog and analog-to-digital interfaces (optionally) can be provided with boundary-scan resources as shown in Figure 7. When this option is taken, it is then possible to test the analog signal path with boundary-scan algorithms. In this case, the signal path is viewed by the test logic as if it were single-ended, leading to diagnostic ambiguity and possible loss of test coverage (see 4.3).

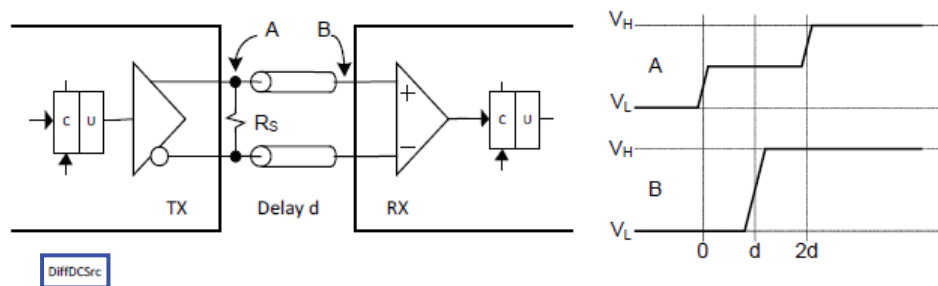


**Figure 7 — Basic differential signaling
with dc coupling and source loading**

The driver in Figure 7 could be producing a voltage signal, and the resistor is used to match the signal line impedance. Alternatively, the driver could be producing a current signal, where the direction of flow represents data, and the resistor is needed not only to match signal line impedance, but also to provide a dc current path to satisfy the driver's requirements. This is called a source termination.

The driver in Figure 7 is looking into a termination R_s and transmission lines with characteristic impedance R_s as well. This forms a voltage divider which sends $1/2$ the signal into the transmission lines. When the signal wave front reaches the receiver (after Delay d) its high-impedance does not match the characteristic impedance, which reflects the signal back down the lines toward the driver. This signal ($1/2$ the driver voltage) adds to the signal received so that the receiver perceives a full voltage swing. After the second transmission line Delay d , the reflected signal reaches the driver and brings the voltage seen there to the full level. Thus a clean transition is seen at the receiver, but the signal seen at the driver is a two-step staircase. Since there is an impedance match at the driver, no new reflections occur.

In the case where the impedance R_s is moved to the receiver (to the right of the transmission lines), this is called load termination (and the resistor is renamed R_L) as shown in Figure 8. Now the driver is looking into the transmission lines with characteristic impedance R_L . The full waveform is transmitted (no divider is now present) and this edge propagates to the receiver. At the receiver, the termination resistor matches the line impedance, and thus, there is no reflection. The waveforms at both the driver and receiver are full transitions.

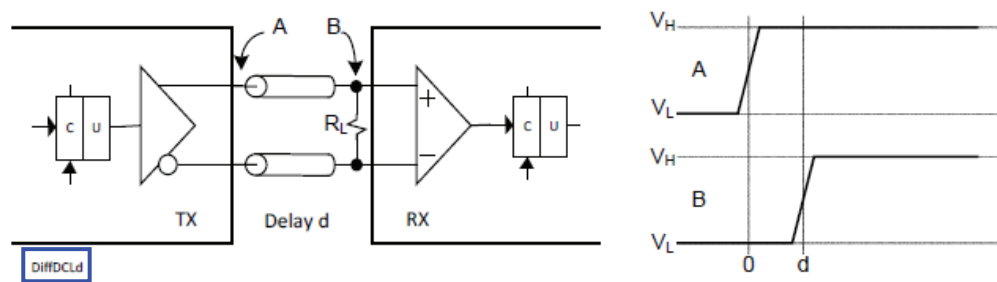


Figure 8 — A dc-coupled driver and receiver with load termination

Figure 9 shows a driver/receiver pair that has been both source and load terminated. In this case, the voltage swing seen on both sides of the transmission line has been divided by two (note R_s equals R_L). This type of termination assures that in the case of an imperfect impedance match, the resulting reflections can be attenuated at both ends of the line.

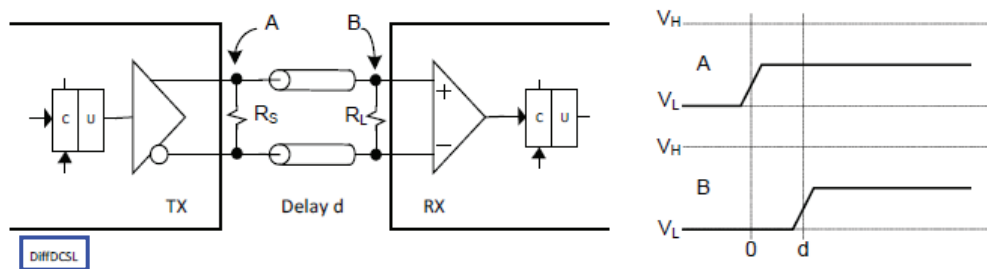


**Figure 9 — A dc-coupled driver and receiver
with both source and load termination**

4.2.4 Differential ac

Figure 10 shows ac coupling of a voltage driver and receiver whose voltage levels are assumed to be incompatible for dc coupling (the voltage levels used by the driver are too far removed from the acceptable common-mode range of the receiver). The bias network referenced to the common-mode voltage source V_{Bias} (the optimal common-mode point of the receiver) along with the dc blocking effect of the coupling capacitors forms a level shifter that allows this configuration to work properly. This enforced compatibility is a common reason why board designers ~~may~~ use ac coupling. The size of the capacitors used is determined by the mission requirements of the coupling and could vary widely across applications.

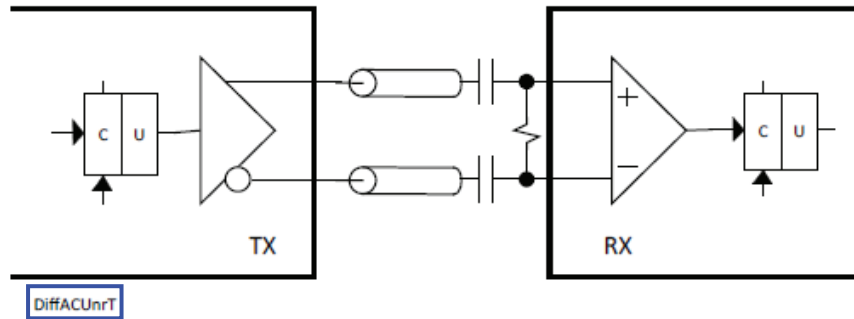


Figure 11 — A basic differential ac signal path with unreferenced termination

Figure 12 shows a basic differential ac signal path with a current driver and source termination and also a referenced bias generator to select the common-mode voltage appropriate for the receiver. The source termination could also serve as an impedance match for the line. The bias network might use significantly higher value resistors as long as the line distance from the capacitors to the receiver is small. This will significantly increase the time constant of the coupling network.

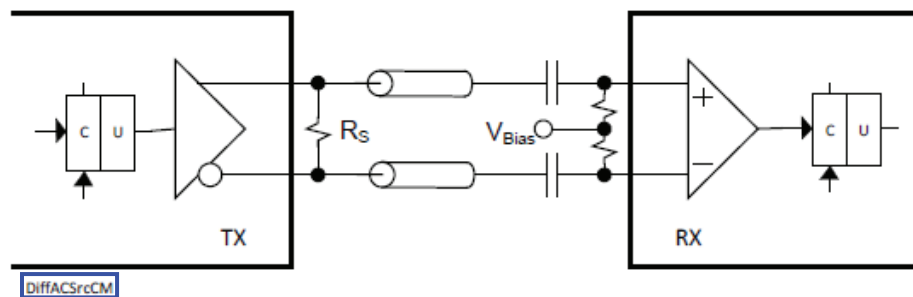


**Figure 12 — Basic differential ac signal path
with source termination and bias provision**

Finally, all the terminations, [high-impedance](#) bias networks, and even the coupling capacitors could ultimately be integrated into the receiver IC. Externally, the signal path appears to be dc-coupled but internally it is still ac-coupled, as shown in Figure 13. On-chip component defects will not need to be tested during board test. Thus only the interconnect defects (typically solder) will be relevant.

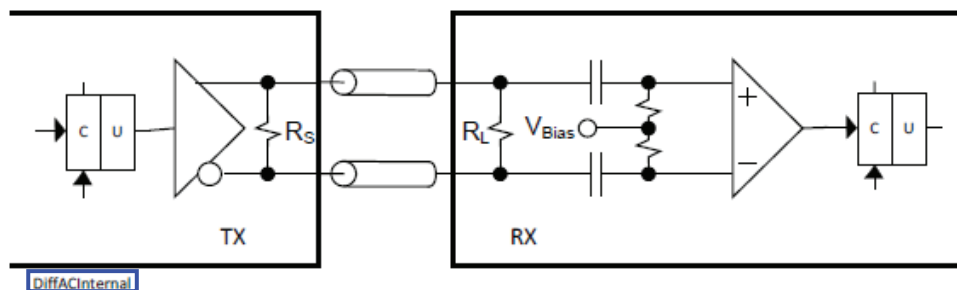


**Figure 13 — AC coupling, termination,
and bias generation internal to the ICs**