IEEE SA
STANDARDS ASSOCIATION

IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture

STANDARDS

IEEE Computer Society

Developed by the
Test Technology Standards Committee



IEEE Std 1149.7™-2022
(Revision of IEEE Std 1149.7™-2009)

IEEE

AVA Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

IEEE Std 1149.7™-2022
(Revision of IEEE Std 1149.7-2009)

IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture

Developed by the

Test Technology Standards Committee
of the
IEEE Computer Society

Approved 16 June 2022

IEEE SA Standards Board

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

This is a Redline document produced by Accuris.

Redlines are designed to save time and improve productivity by using the latest software technology to find and highlight document changes from one edition to the next. It includes a full-text version of the new document, plus an indication of changes from the previous version.

Because it may not be technically possible to capture all changes accurately, it is recommended that users consult previous editions as appropriate. In all cases, only the current base version of this publication is to be considered the official document. This Redline is produced solely by Accuris. The publisher has not prepared this Redline and is not responsible for its accuracy.

Contact:
https://store.accuristech.com/pages/contact.html

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Redline Processing Notes:

1. ~~**Red Text**~~ - Red strikethrough text denotes deletions.

2. **Blue Text** - Blue underlined text denotes modifications and additions.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Abstract: Circuitry that may be added to an integrated circuit to provide access to on-chip Test Access Ports (TAPs) specified by IEEE Std 1149.1™ is described in this standard. The circuitry uses IEEE Std 1149.1 as its foundation, providing complete backward compatibility, while aggressively adding features to support test and applications debug. It defines six classes of IEEE 1149.7 Test Access Ports (TAP.7s), T0 to T5, with each class providing incremental capability, building on that of the lower level classes. Class T0 provides the behavior specified by 1149.1 from startup when there are multiple on-chip TAPs. Class T1 adds common debug functions and features to minimize power consumption. Class T2 adds operating modes that maximize scan performance. It also provides an optional hot-connection capability to prevent system corruption when a connection is made to a powered system. Class T3 supports operation in either a four-wire Series or Star Scan Topology. Class T4 provides for communication with either a two-pin or four-pin interface. The two-pin operation serializes IEEE 1149.1 transactions and provides for higher Test Clock rates. Class T5 adds the ability to perform data transfers concurrently with scan, supports utilization of functions other than scan, and provides control of TAP.7 pins to custom debug technologies in a manner that ensures current and future interoperability.

Keywords: 2-pin, 2-wire, 4-pin, 4-wire, Advanced Protocol, Advanced Protocol Unit, APU, Background Data Transfer, background data transport, BDX, boundary scan, BSDL, BSDL.1, BSDL.7, BYPASS, Capture-IR, CDX, Chip-Level TAP Controller, CID, Class T0, Class T1, Class T2, Class T3, Class T4, Class T5, CLTAPC, compact JTAG, compliant behavior, compliant operation, control level, controller address, Controller ID, Controller Identification Number, CP, Custom Data Transfer, custom data transport, Data Register, debug interface, debug logic, debug and test interface, DOT1, DOT7, DTI, DTS, DTT, Debug Test System, debug test target, Escape, EOT, EPU, extended operation, Extended Protocol, EXTEST, four-pin, four-wire, HSDL, HSDL.7, IDCODE, IEEE 1149.1™, IEEE 1149.7™, Instruction Register, JScan, JScan0, JScan1, JScan2, JScan3, JTAG, MScan, MTCP, Multi-TAP Control Path, narrow Star Scan Topology, nTRST, nTRST_PD, optimized scan, OScan, OScan0, OScan1, OScan2, OScan3, OScan4, OScan5, OScan6, OScan7, Pause-DR, Pause-IR, PC0, PC1, RSU, Reset and selection unit, RTI, Run-Test/Idle, scan, scan DR, scan format, scan IR, Scan Packet, scan path, scan performance, scan protocol, scan topology, series, Series Branch, Series Scan, Series Scan Topology, Series-Equivalent Scan, Series Topology, Shift-DR, Shift-IR, SiP, Star Scan, Star Scan Topology, Star Topology, Star-2, Star-2 Branch, Star-2 Scan, Star-2, Scan Topology, Star-4, Star-4 Branch, Star-4 Scan, Star-4 Scan Topology, SP, SScan, SScan0, SScan1, SScan2, SScan3, stall, SSD, Scan Selection Directive, Standard Protocol, star scan, STL, System Test Logic, TAP, TAP controller, TAP controller address, TAP selection, TAP.1, TAP.7, TAPC, TCA, TCK, TCKC, TDI, TDIC, TDOC, TDOE, Test Access Port, test and debug, Test-Logic-Reset, TLR, TMSC, Transport Packet, T0, T0 TAP.7, T1, T1 TAP.7, T2, T2 TAP.7, T3, T3 TAP.7, T4, T4 TAP.7, T4(N), T4(N) TAP.7, T4(W), T4(W) TAP.7, T5, T5 TAP.7, T5(N), T5(N) TAP.7, T5(W), T5(W) TAP.7, TP, two-pin, two-wire, Update-DR, Update-IR, ZBS, zero bit scan

---

The Institute of Electrical and Electronics Engineers, Inc.
3 Park Avenue, New York, NY 10016-5997, USA

Copyright © 2022 by The Institute of Electrical and Electronics Engineers, Inc.
All rights reserved. Published 14 October 2022. Printed in the United States of America.

IEEE is a registered trademark in the U.S. Patent & Trademark Office, owned by The Institute of Electrical and Electronics Engineers, Incorporated.

PDF: ISBN 978-1-5044-8875-4 STD25536
Print: ISBN 978-1-5044-8876-1 STDPD25536

IEEE prohibits discrimination, harassment, and bullying.
For more information, visit https://www.ieee.org/about/corporate/governance/p9-26.html.
No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Important Notices and Disclaimers Concerning IEEE Standards Documents

IEEE Standards documents are made available for use subject to important notices and legal disclaimers. These notices and disclaimers, or a reference to this page (https://standards.ieee.org/ipr/disclaimers.html), appear in all standards and may be found under the heading "Important Notices and Disclaimers Concerning IEEE Standards Documents."

Notice and Disclaimer of Liability Concerning the Use of IEEE Standards Documents

IEEE Standards documents are developed within IEEE Societies and subcommittees of IEEE Standards Association (IEEE SA) Board of Governors. IEEE develops its standards through an accredited consensus development process, which brings together volunteers representing varied viewpoints and interests to achieve the final product. IEEE Standards are documents developed by volunteers with scientific, academic, and industry-based expertise in technical working groups. Volunteers are not necessarily members of IEEE or IEEE SA and participate without compensation from IEEE. While IEEE administers the process and establishes rules to promote fairness in the consensus development process, IEEE does not independently evaluate, test, or verify the accuracy of any of the information or the soundness of any judgments contained in its standards.

IEEE makes no warranties or representations concerning its standards, and expressly disclaims all warranties, express or implied, concerning this standard, including but not limited to the warranties of merchantability, fitness for a particular purpose and non-infringement. In addition, IEEE does not warrant or represent that the use of the material contained in its standards is free from patent infringement. IEEE standards documents are supplied "AS IS" and "WITH ALL FAULTS."
Use of an IEEE standard is wholly voluntary. The existence of an IEEE Standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEEE standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard.

In publishing and making its standards available, IEEE is not suggesting or rendering professional or other services for, or on behalf of, any person or entity, nor is IEEE undertaking to perform any duty owed by any other person or entity to another. Any person utilizing any IEEE Standards document, should rely upon his or her own independent judgment in the exercise of reasonable care in any given circumstances or, as appropriate, seek the advice of a competent professional in determining the appropriateness of a given IEEE standard.

IN NO EVENT SHALL IEEE BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO: THE NEED TO PROCURE SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE PUBLICATION, USE OF, OR RELIANCE UPON ANY STANDARD, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE AND REGARDLESS OF WHETHER SUCH DAMAGE WAS FORESEEABLE.

Translations

The IEEE consensus development process involves the review of documents in English only. In the event that an IEEE standard is translated, only the English version published by IEEE is the approved IEEE standard.

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Official statements

A statement, written or oral, that is not processed in accordance with the IEEE SA Standards Board Operations Manual shall not be considered or inferred to be the official position of IEEE or any of its committees and shall not be considered to be, nor be relied upon as, a formal position of IEEE. At lectures, symposia, seminars, or educational courses, an individual presenting information on IEEE standards shall make it clear that the presenter's views should be considered the personal views of that individual rather than the formal position of IEEE, IEEE SA, the Standards Committee, or the Working Group. Statements made by volunteers may not represent the formal position of their employer(s) or affiliation(s).

Comments on standards

Comments for revision of IEEE Standards documents are welcome from any interested party, regardless of membership affiliation with IEEE or IEEE SA. However, **IEEE does not provide interpretations, consulting information, or advice pertaining to IEEE Standards documents**.
Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments. Since IEEE standards represent a consensus of concerned interests, it is important that any responses to comments and questions also receive the concurrence of a balance of interests. For this reason, IEEE and the members of its Societies and subcommittees of the IEEE SA Board of Governors are not able to provide an instant response to comments, or questions except in those cases where the matter has previously been addressed. For the same reason, IEEE does not respond to interpretation requests. Any person who would like to participate in evaluating comments or in revisions to an IEEE standard is welcome to join the relevant IEEE working group. You can indicate interest in a working group using the Interests tab in the Manage Profile & Interests area of the IEEE SA myProject system.[a] An IEEE Account is needed to access the application.

Comments on standards should be submitted using the Contact Us form.[b]

Laws and regulations

Users of IEEE Standards documents should consult all applicable laws and regulations. Compliance with the provisions of any IEEE Standards document does not constitute compliance to any applicable regulatory requirements. Implementers of the standard are responsible for observing or referring to the applicable regulatory requirements. IEEE does not, by the publication of its standards, intend to urge action that is not in compliance with applicable laws, and these documents may not be construed as doing so.

Data privacy

Users of IEEE Standards documents should evaluate the standards for considerations of data privacy and data ownership in the context of assessing and using the standards in compliance with applicable laws and regulations.

Copyrights

IEEE draft and approved standards are copyrighted by IEEE under US and international copyright laws. They are made available by IEEE and are adopted for a wide variety of both public and private uses. These include both use, by reference, in laws and regulations, and use in private self-regulation, standardization, and the promotion of engineering practices and methods. By making these documents available for use and

[a] Available at: https://development.standards.ieee.org/myproject-web/public/view.html#landing.
[b] Available at: https://standards.ieee.org/content/ieee-standards/en/about/contact/index.html.

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

adoption by public authorities and private users, neither IEEE nor its licensors waive any rights in copyright to the documents.

Photocopies

Subject to payment of the appropriate licensing fees, IEEE will grant users a limited, non-exclusive license to photocopy portions of any individual standard for company or organizational internal use or individual, non-commercial use only. To arrange for payment of licensing fees, please contact Copyright Clearance Center, Customer Service, 222 Rosewood Drive, Danvers, MA 01923 USA; +1 978 750 8400; https://www.copyright.com/. Permission to photocopy portions of any individual standard for educational classroom use can also be obtained through the Copyright Clearance Center.

Updating of IEEE Standards documents

Users of IEEE Standards documents should be aware that these documents may be superseded at any time by the issuance of new editions or may be amended from time to time through the issuance of amendments, corrigenda, or errata. An official IEEE document at any point in time consists of the current edition of the document together with any amendments, corrigenda, or errata then in effect.

Every IEEE standard is subjected to review at least every 10 years. When a document is more than 10 years old and has not undergone a revision process, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE standard.

In order to determine whether a given document is the current edition and whether it has been amended through the issuance of amendments, corrigenda, or errata, visit IEEE Xplore or contact IEEE.[c] For more information about the IEEE SA or IEEE's standards development process, visit the IEEE SA Website.

Errata

Errata, if any, for all IEEE standards can be accessed on the IEEE SA Website.[d] Search for standard number and year of approval to access the web page of the published standard. Errata links are located under the Additional Resources Details section. Errata are also available in IEEE Xplore. Users are encouraged to periodically check for errata.

Patents

IEEE Standards are developed in compliance with the IEEE SA Patent Policy.[e]

Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken by the IEEE with respect to the existence or validity of any patent rights in connection therewith. If a patent holder or patent applicant has filed a statement of assurance via an Accepted Letter of Assurance, then the statement is listed on the IEEE SA Website at https://standards.ieee.org/about/sasb/patcom/patents.html. Letters of Assurance may indicate whether the Submitter is willing or unwilling to grant licenses under patent rights without compensation or under reasonable rates, with reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to obtain such licenses.

[c] Available at: https://ieeexplore.ieee.org/browse/standards/collection/ieee.
[d] Available at: https://standards.ieee.org/standard/index.html.
[e] Available at: https://standards.ieee.org/about/sasb/patcom/materials.html.

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Essential Patent Claims may exist for which a Letter of Assurance has not been received. The IEEE is not responsible for identifying Essential Patent Claims for which a license may be required, for conducting inquiries into the legal validity or scope of Patents Claims, or determining whether any licensing terms or conditions provided in connection with submission of a Letter of Assurance, if any, or in any licensing agreements are reasonable or non-discriminatory. Users of this standard are expressly advised that determination of the validity of any patent rights, and the risk of infringement of such rights, is entirely their own responsibility. Further information may be obtained from the IEEE Standards Association.

IMPORTANT NOTICE

IEEE Standards do not guarantee or ensure safety, security, health, or environmental protection, or ensure against interference with or from other devices or networks. IEEE Standards development activities consider research and information presented to the standards development group in developing any safety recommendations. Other information about safety practices, changes in technology or technology implementation, or impact by peripheral systems also may be pertinent to safety considerations during implementation of the standard. Implementers and users of IEEE Standards documents are responsible for determining and complying with all appropriate safety, security, environmental, health, and interference protection practices and all applicable laws and regulations.

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Participants

At the time this IEEE standard was completed, the P1149.7 Working Group had the following membership:

Jason L. Peck, *Chair*
Rolf Kühnis, *Vice Chair*
Gary A. Cooper *, *Editor*
Ashwini Athalye, *Secretary*

John Horley Adam W. Ley Bradford G. Van Treuren

*Member Emeritus

The P1149.7 Working Group would like to acknowledge the work of the original Working Group responsible for IEEE Std 1149.7™-2009:

Robert Oshana, *Chair*
Bart Vermeulen, *Vice Chair*
Gary Swoboda, *Technical Architect and Principal Author*

ARM Ltd.
ASSET InterTech, Inc.
Freescale Semiconductor
Intel Corporation
Lauterbach Datentechnik GmbH
Nokia Corporation
NXP Semiconductors
Texas Instruments

The following members of the individual balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

Ashwini Athalye
Adam Cron
Heiko Ehrenberg
Peter Harrod
Werner Hoelzl
Rolf Kühnis
Adam W. Ley
Ian Mcintosh
Nick S. A. Nikjoo
Jim O'Reilly
Jason L. Peck
Saghir Shaikh
Walter Struppler
David Thompson
Lisa Ward
Oren Yuen

When the IEEE SA Standards Board approved this standard on 16 June 2022, it had the following membership:

David J. Law, *Chair*
Ted Burse, *Vice Chair*
Gary Hoffman, *Past Chair*
Konstantinos Karachalios, *Secretary*

Edward A. Addy
Ramy Ahmed Fathy
J. Travis Griffith
Guido R. Hiertz
Yousef Kimiagar
Joseph L. Koepfinger*
Thomas Koshy
John D. Kulick
Johnny Daozhuang Lin
Kevin Lu
Daleep C. Mohla
Andrew Myles
Damir Novosel
Annette D. Reilly
Robby Robson
Jon Walter Rosdahl
Mark Siira
Dorothy V. Stanley
Lei Wang
F. Keith Waters
Karl Weber
Sha Wei
Philip B. Winston
Daidi Zhong

*Member Emeritus

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Introduction

This introduction is not part of IEEE Std 1149.7-2022, IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture.

This standard defines a debug and Test Access Port that provides both compatibility with IEEE Std 1149.1 and operation with as few as two pins. It complements IEEE Std 1149.1 and is not intended to replace it. The facilities defined by the standard seek to provide a cost-effective debug and test interface solution supporting the debug and test of applications. The standard supports the needs for application debug of products with complex digital circuitry, applications software, and one or more central processing units (CPUs). The interface also provides a means to instrument these applications concurrently with scan transactions associated with the underlying IEEE 1149.1 foundation.

History of the development of this standard

The process of developing this standard began in 2004 when the Mobile Industry Processor Interface (MIPI) Alliance Test and Debug Working Group was formed. During 2004, a standard that addressed the needs of both test and debug was described and requirements were gathered. The emphasis was on creating an interface that allowed standardization of access to debug and test capabilities on-chip while addressing the needs of applications developers sharing an integrated circuit's Test Access Port with test uses. This interface also targeted making chips exhibit the behavior that is specified by IEEE Std 1149.1 when multiple Test Access Ports are deployed on a single chip. It was thought that applications development tools vendors would be a big beneficiary of this interface as common connectors providing access to the debug and test interface would be recommended. It was felt that all of this would best be accomplished with an interface that was compatible with chip intellectual property already utilizing IEEE Std 1149.1.

Once the requirements gathering process was completed in 2004, the Test and Debug Working Group turned its attention to proposals for addressing the above requirements. Both competing and complementary proposals were submitted. The proposals were debated, and one was selected as a basis to move forward in April 2005. A preliminary specification replaced the proposal and was reviewed inside the MIPI Test and Debug Working Group and by the NEXUS standards body in late 2005. Since both bodies felt the applicability of the specification was well beyond their own objectives, they both recommended using the on-chip portions of those specifications as the basis for an IEEE standard in a joint meeting in December 2005.

Multiple drafts of the specification were completed and reviewed from 2005 until the standard's approval, with the capability provided by the standard expanded along the way. Revisions in the presentation and number of capabilities took place along the way to the standard's unanimous approval in 2009.

As the standard was scheduled to become inactive in 2019, some of the original Working Group members were queried and there was a general consensus that the effort should be made for revision per maintenance policy for IEEE standards. A new PAR was created, and a new Working Group was formed.

No major additions or changes to the standard were targeted as part of the renewal effort. As such, this is not a major update and the revised version is fully backward compatible with the original. However, the Working Group did agree to evaluate feedback from customers of the original version in an effort to clarify certain issues and fix potential errors.

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Changes introduced by this revision

After reviewing the feedback against the original version, the Working Group agreed to make the following two changes to help clarify the technical content of the standard:

— Subclause 23.7 was updated to include an explicit Specification section (23.7.2). The normative material contained here existed in the original standard but was not called out using the formalized method outlined in 1.12.2.

— Subclause F.6 was added to Annex F in an effort to clarify the design issues associated with how the K-bias requirements on TMS(C) can impact system performance. Several system design considerations are outlined that can help minimize the impact of this problem.

In addition, several updates were made to address editorial and presentation issues. The major ones include the following:

— Added 1.3.

— Updated several figures to address issues related to appearance, rendering, and avoiding the use of color to convey meaning.

— Eliminated the use of dated references to IEEE standards.

— Updated BSDL usage within document to IEEE Std 1149.1-2013.

— Introduced initiator/responder as a culturally neutral alternative to describe entity relationships previously presented in disfavored terms.

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Contents

1. Overview 56
1.1 Scope 56
1.2 Purpose 56
1.3 Word usage 56
1.4 Contrasting IEEE Std 1149.1 and this standard 57
1.5 Challenges 58
1.6 Important considerations 59
1.7 Nomenclature 59
1.7.1 References to technology and standards 59
1.7.2 Describing Test Access Port behaviors 59
1.7.3 Describing TAPs and TAP controllers 60
1.7.4 Describing scan exchanges 61
1.7.5 Describing TAP signals 61
1.8 Ensuring transparency to IEEE 1149.1 intellectual property 62
1.8.1 IEEE 1149.1 constraints 62
1.8.2 IEEE 1149.1 constraints/requirements balancing 62
1.8.3 IEEE 1149.1 upgrade path 62
1.9 Maximizing compatibility with 1149.1 IP 63
1.9.1 IEEE 1149.1 infrastructure 63
1.9.1.1 IEEE 1149.1 instructions 63
1.9.1.2 IEEE 1149.1 Scan Paths 63
1.9.1.3 IEEE 1149.1 boundary-scan capability 63
1.9.2 Test Clock treatment 63
1.9.2.1 Test Clock source 63
1.9.2.2 Test Clock shared or dedicated use 64
1.9.2.3 Unorthodox use of Test Clock 64
1.10 Scalability 65
1.10.1 Types of operation/capability classes 65
1.10.2 Signaling 67
1.11 Flexibility 67
1.11.1 Supporting various scan topologies 67
1.11.2 Operation with more than one scan topology/other technologies 69
1.12 Document content 69
1.12.1 Descriptive material 70
1.12.2 Specification material 70
1.13 Document organization 70
1.13.1 Partitioning 70
1.13.1.1 Foundation 71
1.13.1.2 TAP.7 Classes 72
1.13.1.3 Test description languages 72
1.13.1.4 Annexes 72
1.13.2 Pictorial view 73
1.14 Using the standard 74
1.14.1 User background knowledge 74
1.14.2 Types of users 74
1.14.2.1 Chip designer 74
1.14.2.2 Programmer 74
1.14.3 Use summary 74
1.15 Conventions 75
2. Normative references 81
3. Definitions, acronyms, and abbreviations 82

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

3.1 Definitions 82
3.2 Acronyms and abbreviations 86
4. TAP.7 concepts and architecture 91
4.1 Introduction 91
4.2 Concepts supporting system architecture 91
4.2.1 Maximizing compatibility with IEEE Std 1149.1 91
4.2.1.1 Hardware components 92
4.2.1.2 Software components 92
4.2.2 TAPC hierarchy 92
4.2.2.1 Overview 92
4.2.2.2 Hierarchy levels 93
4.2.3 Parking the TAPC state 94
4.2.3.1 Overview 94
4.2.3.2 Parking-state relationships 95
4.2.3.3 Parking-state terminology 96
4.2.3.3.1 ADTAPC selection states 96
4.2.3.3.2 CLTAPC selection states 96
4.2.3.3.3 EMTAPC selection states 97
4.2.3.3.4 Selection state summary 98
4.2.4 Choice of parking states 98
4.2.5 Parking methods 98
4.2.6 Operation of the TAP.7 Controller 98
4.2.6.1 TAP.7 Controller management 98
4.2.6.2 System and Control Paths 99
4.2.6.3 Power management 100
4.2.7 Scan topologies 101
4.2.7.1 Series and Star Scan Topologies 101
4.2.7.2 Scan Topology Training 102
4.2.7.3 Sharing of signaling with other technologies 102
4.2.7.4 Direct addressability for Star Scan Topologies 102
4.2.7.5 Series-Equivalent Scans for Star Scan Topologies 103
4.2.7.6 Output-drive characteristics 104
4.2.7.7 Scan formats 105
4.2.7.8 Interoperability 106
4.3 Concepts supporting pin efficiency 106
4.3.1 Signaling methods 106
4.3.2 Protocols 107
4.3.2.1 Protocol types 107
4.3.2.2 Standard Protocol 108
4.3.2.3 Advanced Protocol 108
4.3.2.3.1 Interleaving of scan and non-scan information 109
4.3.2.3.2 Serialization of scan information 110
4.3.2.4 Control Protocol 111
4.3.3 Advanced and Control Protocol characteristics 111
4.3.3.1 Packets, bit-frames, and bits 111
4.3.3.2 Data and control information 112
4.3.4 Performance 113
4.3.4.1 TAP operation 113
4.3.4.1.1 Signal timing 113
4.3.4.1.2 Registering of signals 114
4.3.4.2 Scan transfer efficiency 114
4.4 Concepts supporting capability 114
4.4.1 Concepts already described 114
4.4.2 Resets 115
4.4.3 Private commands and registers 115
4.5 IEEE 1149.7 architecture 115

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

4.5.1 Components 115
4.5.2 Reset types 118
4.5.3 Start-up options 119
4.6 Operating models 120
4.6.1 Model types 120
4.6.2 Standard models 120
4.6.3 Advanced models 122
5. T0–T3 TAP.7 operational overview 123
5.1 Introduction 123
5.2 T0 TAP.7 123
5.2.1 Overview 123
5.2.2 Operating modes and capabilities 124
5.2.3 Operation 125
5.2.3.1 Multi-TAPC architecture 125
5.2.3.2 Selection and deselection of EMTAPCs 125
5.2.4 T0 TAP.7 high-level block diagram 126
5.3 T1 TAP.7 127
5.3.1 Overview 127
5.3.2 Operating modes and capabilities 128
5.3.3 Operation 128
5.3.3.1 Adding TAP.7 functionality to the *BYPASS* and *IDCODE* instructions 128
5.3.3.2 Zero-bit DR scans 128
5.3.3.3 Utilizing ZBSs for TAP.7 Controller functionality 129
5.3.3.3.1 Locking the ZBS count 129
5.3.3.3.2 Control levels 129
5.3.3.3.3 Exiting a control level 130
5.3.3.3.4 Zeroing the ZBS count 130
5.3.3.4 EPU Operating States 130
5.3.3.5 Commands 130
5.3.3.6 Registers 133
5.3.3.7 Using the System and Control Paths 135
5.3.3.7.1 System Path 136
5.3.3.7.2 Control Path 136
5.3.3.7.3 TDO Drive Policy 137
5.3.3.8 EPU groups 137
5.3.4 T1 TAP.7 high-level block diagram 137
5.4 T2 TAP.7 137
5.4.1 Overview 137
5.4.2 Operating modes and capabilities 139
5.4.3 Operation 140
5.4.3.1 Overview 140
5.4.3.2 Using the System and Control Paths 141
5.4.3.3 TDO Drive Policy 142
5.4.3.4 STL groups 142
5.4.3.4.1 STL group types 142
5.4.3.4.2 STL Group Membership changes 143
5.4.4 T2 TAP.7 high-level block diagram 143
5.5 T3 TAP.7 144
5.5.1 Overview 144
5.5.2 Operating modes and capabilities 145
5.5.3 Operation 147
5.5.3.1 Within series and star scan topologies 147
5.5.3.2 T3 TAP.7 Controller addressability in a Star-4 Scan Topology 147
5.5.3.3 Pause-IR and Pause-DR STL groups 147
5.5.3.4 Series/star scan equivalency 148
5.5.3.4.1 Defining scan equivalency 148

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

5.5.3.4.2 Creating a Series-Equivalent Scan within a Star Scan Topology 148
5.5.3.5 Scan Selection Directives 149
5.5.3.5.1 Enabling the use of SSDs 149
5.5.3.5.2 Types of SSDs 149
5.5.3.5.3 SSD execution 150
5.5.3.5.4 SSD State Machine 150
5.5.3.6 Series-Equivalent Scan creation 151
5.5.3.6.1 Exclusivity of SSD and TAP.7 Controller commands 152
5.5.3.7 Using the System and Control Paths 153
5.5.3.8 TDO Drive Policy 154
5.5.4 T3 TAP.7 high-level block diagram 154
6. T4–T5 TAP.7 operational overview 156
6.1 Introduction 156
6.2 T4 TAP.7 157
6.2.1 Operating modes and capabilities 157
6.2.2 Operation 158
6.2.2.1 Signal behaviors 158
6.2.2.2 Rising and falling TMSC input sampling 158
6.2.2.3 Controller addressability in a Star-2 Scan Topology 159
6.2.2.4 RSU and APU functions 159
6.2.2.4.1 Bypass (*BPA*) 161
6.2.2.4.2 Check Process Active (*CPA*) 161
6.2.2.4.3 Scan Packet Active (*SPA*) 164
6.2.3 T4 TAP.7 high-level block diagram 165
6.3 T5 TAP.7 166
6.3.1 Overview 166
6.3.2 Operating modes and capabilities 168
6.3.2.1 Transport source/destinations 168
6.3.2.1.1 Single-client operation 168
6.3.2.1.2 Multi-client operation 169
6.3.2.1.3 Client-to-client operation 170
6.3.2.2 Transfer characteristics 171
6.3.3 Operation 172
6.3.3.1 Transport Control Function 172
6.3.3.2 *TPA* 173
6.3.4 T5 TAP.7 high-level block diagram 174
6.4 TAP.7 feature summary 175
7. System concepts 177
7.1 Introduction 177
7.2 Key system attributes 177
7.3 DTS/TS connectivity with a mix of technologies 177
7.3.1 Technology mixes 177
7.3.2 Technology branches 178
7.4 TAP.7 deployment scenarios 179
7.4.1 TAP.1 Series Branches 179
7.4.2 TAP.7 Series, Star-4, and Star-2 Branches 179
7.5 Chip TAPC hierarchy 180
7.6 Combined view of TAP connectivity and TAPC hierarchy 181
7.7 Chips, components, and boards 182
8. TAPC hierarchy 184
8.1 Introduction 184
8.2 Selection/deselection with the TAPC hierarchy 184
8.2.1 Selection choices 184
8.2.2 Selection/deselection/class relationships 185
8.2.3 TAPC parent/child relationships 185
8.3 TAPC selection/deselection characteristics 185

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

8.3.1 TAPC and scan path behavior 185
8.3.2 Selection/deselection mechanisms 186
8.3.3 Parking states and resynchronization 186
8.4 ADTAPC selection/deselection 187
8.4.1 Parking use cases 187
8.4.2 DTS/ADTAPC relationship 187
8.4.3 ADTAPC operation 188
8.5 CLTAPC selection/deselection 189
8.5.1 Parking use cases 189
8.5.2 ADTAPC/CLTAPC relationship 189
8.5.3 CLTAPC operation 189
8.6 EMTAPC selection/deselection 191
8.6.1 Parking use cases 191
8.6.2 CLTAPC/EMTAPC relationship 191
8.6.3 EMTAPC operation 191
8.7 Using a common selection/deselection protocol across technologies 192
8.8 RSU deployment 192
8.8.1 Use with new or existing IP 192
8.8.2 Using TAP pins for multiple functions 193
8.9 Using the TAPC hierarchy 193
8.9.1 Selection considerations 193
8.9.2 Start-up considerations 194
8.10 Test/debug applications and the TAPC hierarchy 194
8.10.1 Debug use of the TAPC hierarchy 194
8.10.2 Test use of the TAPC hierarchy 195
9. Registers, commands, and scan paths 197
9.1 Introduction 197
9.2 Command basics 197
9.3 Register portfolio 199
9.3.1 Description 199
9.3.1.1 Global and Local Registers 199
9.3.1.2 Register loads 199
9.3.1.3 Register reset values 200
9.3.2 Specifications 200
9.4 Command portfolio 202
9.4.1 Description 202
9.4.1.1 Command types 202
9.4.1.2 Store commands 202
9.4.1.3 Select commands 203
9.4.1.4 Scan commands 203
9.4.1.5 Enumerate commands 203
9.4.1.6 Private commands 203
9.4.1.7 Effects a TAP.7 Controller reset 203
9.4.2 Specifications 204
9.5 Representation of commands in examples 209
9.6 Global and Local Register programming with commands 209
9.7 Scan paths 210
9.7.1 Conceptual and physical views 210
9.7.1.1 Description 210
9.7.1.1.1 Path characteristics 210
9.7.1.1.2 Conceptual path selection 210
9.7.1.1.3 Physical path selection 211
9.7.1.2 Specifications 212
9.7.2 EPU Scan Paths and their selection 214
9.7.2.1 Description 214
9.7.2.2 Specifications 214

Copyright © 2022 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

9.7.3 EPU Scan Path characteristics 215
9.7.3.1 Description 215
9.7.3.1.1 Scan-path continuity 215
9.7.3.1.2 EPU Bypass-Path characteristics 216
9.7.3.1.3 EPU Bit-Path characteristics 216
9.7.3.1.4 EPU String-Path characteristics 216
9.7.3.1.5 Enumerate-Path characteristics 219
9.7.3.1.6 Auxiliary Path 219
9.7.3.2 Specifications 219
9.8 Two-part commands 221
9.9 Three-part commands 221
9.9.1 SCNB Command characteristics 221
9.9.2 SCNS Command characteristics 222
9.9.3 CIDA Command characteristics 223
9.10 RDBACKx and CNFGx Registers 225
9.10.1 RDBACKx Registers 226
9.10.1.1 Description 226
9.10.1.2 Specifications 226
9.10.2 CNFGx Registers 227
9.10.2.1 Description 227
9.10.2.1.1 Overview 227
9.10.2.1.2 CNFG0 mandatory configuration information 228
9.10.2.1.3 CNFG0 optional configuration information 228
9.10.2.1.4 CNFG1 optional configuration information 229
9.10.2.1.5 CNFG2 and CNFG3 Registers 229
9.10.2.1.6 Determining the TAP type and class using configuration information 229
9.10.2.2 Specifications 229
9.11 An approach to implementing command processing and scan paths 231
10. RSU ancillary services 235
10.1 Introduction 235
10.2 Resets 235
10.2.1 Description 235
10.2.1.1 Overview 235
10.2.1.2 Reset considerations 236
10.2.1.3 Reset effects 236
10.2.1.3.1 Type-5 Reset 237
10.2.1.3.2 Type-4 Reset 237
10.2.1.3.3 Type-3 Reset 237
10.2.1.3.4 Type-2 Reset 238
10.2.1.3.5 Type-1 Reset 238
10.2.1.3.6 Type-0 Reset 238
10.2.1.3.7 Type-0 versus a Type-2 Reset 238
10.2.1.4 TAP.7 Controller operation is ensured after power-up 238
10.2.1.5 Other effects of a TAP.7 Controller reset 238
10.2.1.6 An approach to implementing TAP.7 Controller resets 239
10.2.2 Specifications 240
10.3 Start-up options 242
10.3.1 Description 242
10.3.1.1 Overview 242
10.3.1.2 1149.1-compliant behavior start-up option 243
10.3.1.3 1149.1-Compatible Start-up option 243
10.3.1.4 IEEE 1149.1-Protocol Compatible 244
10.3.1.5 Offline-at-Start-up option 244
10.3.1.6 Start-up behavior 245
10.3.2 Specifications 246
10.4 Escape Detection 250

Copyright © 2022 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

10.4.1 Description 250
10.4.1.1 Overview 250
10.4.1.2 Detection 251
10.4.1.2.1 Custom Escape 252
10.4.1.2.2 Selection and Deselection Escapes 252
10.4.1.3 Reset Escape 253
10.4.1.4 Timing considerations 253
10.4.1.5 An approach to implementing Escape Detection 253
10.4.2 Specifications 255
10.5 Selection Alert 256
10.5.1 Description 256
10.5.1.1 Overview 256
10.5.1.2 Selection Alert Bit Sequence 257
10.5.1.3 Selection Alert detection 258
10.5.1.4 An approach to implementing Selection Alerts 258
10.5.2 Specifications 260
10.6 Deselection Alert 262
10.6.1 Description 262
10.6.2 Specifications 262
10.7 Programming considerations 263
10.7.1 Resets 263
10.7.2 Escapes 263
10.7.3 Selection Alerts 263
10.7.4 Test and debug 263
10.7.5 Concurrent use of a Selection Escape and Selection Alert 263
10.8 ADTAPC State Machine 264
10.8.1 Need 264
10.8.2 An approach to implementing the ADTAPC 264
11. RSU Online/Offline capability 266
11.1 Introduction 266
11.2 Managing Online/Offline operation 266
11.3 Online/Offline operating principles 267
11.3.1 Conceptual view of Online/Offline operation 267
11.3.2 Events affecting Online/Offline operation 268
11.3.3 Summary of responses to selection/deselection events 269
11.3.4 Interoperability with other technologies 269
11.4 Initiating Offline operation 271
11.4.1 Description 271
11.4.1.1 Events initiating Offline operation 271
11.4.1.2 Escapes 271
11.4.1.3 Alerts 272
11.4.1.4 Use of an unsupported feature 272
11.4.1.5 Offline-at-Start-up 272
11.4.2 Specifications 272
11.5 Initiating Online operation 272
11.5.1 Description 272
11.5.2 Specifications 273
11.6 Context-sensitive response to Selection and Deselection Escapes 273
11.6.1 Description 273
11.6.1.1 Escape qualification criteria during Online operation 274
11.6.1.2 Escape qualification criteria during Offline-at-Start-up operation 274
11.6.1.3 Selection Alert during Offline-at-Start-up operation 275
11.6.2 Specifications 275
11.7 Selection Sequence 276
11.7.1 Initiation 276
11.7.2 Format 276

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

11.7.3 Technology-independent portion 276
11.7.4 Technology-dependent portion 277
11.7.5 Forms of Selection Sequence 277
11.7.6 Online Activation Code 278
11.7.6.1 Description 278
11.7.6.2 Specifications 279
11.7.7 TAP.7 Extension Code 281
11.7.7.1 Description 281
11.7.7.2 Specifications 282
11.7.8 Global Register load 283
11.7.8.1 Description 283
11.7.8.2 Specifications 284
11.7.9 Check Packet 284
11.7.9.1 Description 284
11.7.9.1.1 Format 284
11.7.9.1.2 Function 285
11.7.9.1.3 Directives 286
11.7.9.2 Specifications 286
11.8 Parking-state considerations 287
11.8.1 Description 287
11.8.2 Specifications 287
11.9 Control State Machine 290
11.9.1 Mandatory and optional behaviors 290
11.9.1.1 Description 290
11.9.1.2 Specifications 291
11.9.2 Standard state (*STD*) 292
11.9.2.1 Description 292
11.9.2.2 Specifications 292
11.9.3 Advanced state (*ADV*) 293
11.9.3.1 Description 293
11.9.3.2 Specifications 293
11.9.4 Offline waiting state (*OLW*) 294
11.9.4.1 Description 294
11.9.4.2 Specifications 294
11.9.5 Test state (*TEST*) 295
11.9.5.1 Description 295
11.9.5.1.1 Selection test 295
11.9.5.1.2 Factors requiring a Global Register load for placement Online 296
11.9.5.1.3 ADTAPC resynchronization 296
11.9.5.1.4 Priority of conditions causing state changes 297
11.9.5.1.5 Test state function 297
11.9.5.1.6 Selection Sequences requiring a state load 298
11.9.5.2 Specifications 299
11.9.6 Check Packet state (*CHK*) 302
11.9.6.1 Description 302
11.9.6.1.1 *CHK* substates 302
11.9.6.1.2 CP examples 303
11.9.6.2 Specifications 305
11.9.7 Offline-at-Start-up state (*OLS*) 308
11.9.7.1 Description 308
11.9.7.1.1 Placement Online 308
11.9.7.1.2 CLTAPC state initialization 308
11.9.7.1.3 Selection Escape qualification in the *OLS* state 309
11.9.7.1.4 Example of exiting the *OLS* state 309
11.9.7.2 Specifications 310
11.9.7.3 An approach to implementing the CSM 311

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

11.10 Programming considerations 313
11.10.1 Escapes....313
11.10.1.1 Selection Escape....313
11.10.1.2 Deselection Escape....313
11.10.1.3 Reset Escape....314
11.10.2 Alerts....314
11.10.2.1 Deselection Alert....314
11.10.2.2 Selection Alert....314
11.10.2.3 Offline-at-Start-up....314
11.10.3 Selection Sequences....315
11.10.3.1 DTS/TAP.7 Controller synchronization....315
11.10.3.2 Short Form....315
11.10.3.3 Long Form....315
11.10.4 Hang caused by a programming error....316
12. TAP signals....317
12.1 Introduction....317
12.2 TAP.7 Class/signal relationships....317
12.2.1 Description....317
12.2.2 Specifications....318
12.3 Signal function and bias....319
12.3.1 Description....319
12.3.2 Specifications....320
12.4 Test Reset (nTRST and nTRST_PD) signals....321
12.4.1 Description....321
12.4.2 Specifications....322
12.5 TAP.7 signal functions with corresponding IEEE 1149.1 names....322
12.5.1 Description....322
12.5.2 Specifications....322
12.6 Test Clock (TCK)....322
12.6.1 Description....322
12.6.2 Specifications....322
12.7 Test Mode Select (TMS/TMSC)....323
12.7.1 Description....323
12.7.1.1 Online start-up....323
12.7.1.2 Offline start-up....324
12.7.1.3 Combined view of Online and Offline-at-Start-up TMS(C) signal behaviors....326
12.7.2 Specifications....329
12.8 Test Data Input (TDI/TDIC)....330
12.8.1 Description....330
12.8.2 Specifications....331
12.9 Test Data Output (TDO/TDOC)....333
12.9.1 Description....333
12.9.2 Specifications....334
12.10 Offline-at-Start-up behavior....335
12.10.1 Description....335
12.10.2 Specifications....336
12.11 TAP connections....336
12.11.1 Description....336
12.11.2 Specifications....336
12.12 Applicability of this standard....337
12.12.1 Description....337
12.12.2 Specifications....337
12.13 Recommendations for interoperability....338
12.13.1 Overview....338
12.13.2 Power-up behavior....338
12.13.3 IEEE 1149.7-Non-disruptive behavior....338

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

12.13.3.1 Description 338
12.13.3.2 Specifications 339
12.13.4 IEEE 1149.7-Other Behavior 339
12.13.4.1 Description 339
12.13.4.2 Specifications 339
13. TDO(C) Signal Drive Policy 341
13.1 Introduction 341
13.2 TDO(C) Signal Drive Types 341
13.2.1 TDO(C) Signal Drive Types 341
13.2.1.1 Single Drive 342
13.2.1.2 Joint Drive 342
13.2.1.3 Voting Drive 342
13.2.1.4 Inhibited Drive 342
13.2.2 Wire-ANDed TDOC data created with a combination of drives 342
13.3 Factors affecting the TDO(C) Drive Policy 343
13.4 TDO(C) Drive Policy template 344
13.4.1 General characteristics 344
13.4.2 TDOC drive enables 344
13.4.3 TDO(C) Drive Policy components 344
13.4.4 TAP.7 Class/TDO(C) Drive Policy component applicability 345
13.4.5 Dormant TDO(C) Drive Policy 345
13.4.6 Transition TDO(C) Drive Policy 345
13.4.7 Series TDO(C) Drive Policy components 345
13.4.7.1 Series System 345
13.4.7.2 Series Command 346
13.4.7.3 Series Control Level 346
13.4.8 Star-4 TDO(C) Drive Policies 346
13.4.8.1 Star-4 System 346
13.4.8.2 Star-4 Command 346
13.4.8.3 Star-4 control level 347
13.4.9 Hierarchical and flat views of the TDO(C) Drive Policy 347
13.4.10 Conceptual diagram of the TDO(C) Drive Policy 350
13.5 T0 TAP.7 TDOC Drive Policy 351
13.5.1 Description 351
13.5.2 Specifications 351
13.6 T1 and T2 TAP.7 TDOC Drive Policy 352
13.6.1 Description 352
13.6.2 Specifications 353
13.7 T3 and above TAP.7 TDOC Drive Policy 354
13.7.1 Description 354
13.7.2 Specifications 355
13.8 STL Group Membership 357
13.8.1 Tracking the Group Membership of STLs 357
13.8.2 STL Group Membership changes 357
13.8.2.1 Group membership changes with the *Test-Logic-Reset* state 357
13.8.2.2 Group membership changes with the *Run-Test/Idle* state 357
13.8.2.3 Group membership changes with the *Pause-IR* state 358
13.8.2.4 Group membership changes with the *Pause-DR* state 358
13.8.3 Commands/SSDs affecting group Scan Group Candidacy and Membership 358
13.8.3.1 Commands affecting Scan Group Candidacy 358
13.8.3.2 SSDs affecting Scan Group Candidacy and Membership 359
13.8.3.2.1 SSDs associated with the *Run-Test/Idle* state 359
13.8.3.2.2 SSDs associated with the *Pause-IR* state 359
13.8.3.2.3 SSDs associated with the *Pause-DR* state 359
13.8.4 Only Scan Group Member determination 360
13.8.4.1 Criteria 360

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

13.8.4.2 Method and information used to make determination 360
13.8.4.2.1 Idle Group Membership and membership counts 360
13.8.4.2.2 Pause-xR Group Membership and membership counts 361
13.8.4.2.3 Scan Group Membership and membership counts 361
13.8.4.2.4 Information recorded 362
13.8.5 STL group candidate and membership counts 362
13.8.5.1 Description 362
13.8.5.1.1 Scan Group Candidate Count (SGCC) 362
13.8.5.1.2 Potential Scan Group Membership Count Last 364
13.8.5.1.3 Factors creating SGCC and PSGMCL ambiguity 365
13.8.5.2 Specifications 365
13.8.6 Scan Group Membership Count Last determination 368
13.8.6.1 Description 368
13.8.6.2 Specification 368
13.8.7 Only Scan Group Member Last determination 369
13.8.7.1 Description 369
13.8.7.2 Specification 369
13.9 EPU Group Membership 371
13.9.1 Description 371
13.9.1.1 Tracking the EPU's Group Membership 371
13.9.1.2 Conditional Group Member Count 371
13.9.1.3 Only Conditional Group Member determination 372
13.9.2 Specifications 373
13.10 Drive Policy summary 375
13.11 An approach to implementing TDOC Drive Policy 376
13.11.1 Policy generation 376
13.11.2 Potential Scan Group Member Last 377
13.11.3 The SGCC and PSGMCL functions 377
13.11.4 Determining Scan Group Only Member Last/Membership Count Last 378
13.11.5 The CGMC function 379
13.12 Programming considerations 379
14. TMS(C) Signal Drive Policy 380
14.1 Introduction 380
14.2 TMS(C) output bit types 380
14.2.1 Scan Packet content 380
14.2.2 Transport Packet content 381
14.2.3 Drive relationship with TCKC 382
14.3 Drive policy by output bit type 383
14.4 TMSC Signal Drive Types 384
14.4.1 TMSC Signal Drive Types 384
14.4.1.1 Single Drive 385
14.4.1.2 Joint Drive 385
14.4.1.3 Voting Drive 385
14.4.1.4 Inhibited Drive 385
14.4.2 Wire-ANDed TMSC signal values 385
14.5 Dormant Bit Drive Policy 386
14.5.1 Description 386
14.5.2 Specifications 386
14.6 Precharge Bit Drive Policy 386
14.6.1 Description 386
14.6.2 Specifications 386
14.7 RDY Bit Drive Policy 387
14.7.1 Description 387
14.7.1.1 Characteristics 387
14.7.1.2 Policy details 387
14.7.1.3 Relationship to CLTAPC selection state changes 388

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

14.7.2 Specifications 388
14.8 TDO Bit Drive Policy 390
14.8.1 Description 390
14.8.1.1 Characteristics 390
14.8.1.1.1 Policy details for System Path 390
14.8.1.1.2 Policy details for Control Path 391
14.8.1.2 Correlation to TDO(C) Drive Policy 391
14.8.1.3 Combined TDO bit drive summary 392
14.8.2 Specifications 393
14.9 Transport Bit Drive Policy 394
14.9.1 Description 394
14.9.2 Specifications 395
14.10 An approach to implementing TMSC Drive Policy 395
14.11 Programming considerations 399
15. IEEE 1149.1-compliance concepts 401
15.1 Introduction 401
15.2 Background 401
15.3 Test and debug views of a system of interest 402
15.4 An approach to implementing EMTAPC selection/deselection 403
16. T0 TAP.7 404
16.1 Introduction 404
16.2 Deployment 404
16.3 Capabilities 405
16.4 Configurations 405
16.4.1 Description 405
16.4.2 Specifications 405
16.5 Start-up behavior 406
16.5.1 Description 406
16.5.2 Specifications 406
16.6 Supporting multiple on-chip TAPCs 406
16.7 Controlling the selection state of EMTAPCs 407
16.7.1 Description 407
16.7.2 Specifications 408
16.8 Control via the CLTAPC Instruction Register 410
16.8.1 Description 410
16.8.1.1 Exclusion of TAPCs 410
16.8.1.2 Isolation of TAPCs 412
16.8.1.3 CLTAPC output registering of MTCP and MTDP control 413
16.8.2 Specifications 414
16.9 Control via one or more CLTAPC Data Registers 414
16.9.1 Description 414
16.9.2 Specifications 415
16.10 Control via internal or external *tapc_select* signals 416
16.10.1 Description 416
16.10.2 Specifications 417
16.11 Example use cases 418
16.11.1 IR control method with exclusions of TAPCs 419
16.11.2 IR control method with isolation of TAPCs 419
16.11.3 DR control method with exclusion of TAPCs 420
16.11.4 DR control method with isolation of TAPCs 420
16.12 Identification of on-chip TAP controller(s) 421
16.12.1 Description 421
16.12.2 Specifications 422
16.13 Multiple dies in one package 422
16.13.1 Description 422
16.13.1.1 Exposing an IEEE 1149.1 DR for the *BYPASS* and *IDCODE* instructions 423

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

16.13.1.2 Exposing the complete boundary-scan chain for IEEE 1149.1 instructions....423
16.13.1.3 BSDL documentation....423
16.13.1.4 Packaging dies....424
16.13.1.5 SiP-TAP POR* functionality....425
16.13.1.6 DR-wire bypass....425
16.13.2 Specifications....426
16.14 Managing STL Group Membership....427
16.15 RSU operation....427
16.15.1 Description....427
16.15.2 Specifications....427
16.16 Programming considerations....428
17. Extended concepts....429
17.1 Introduction....429
17.2 Suitability of *BYPASS* and *IDCODE* instructions for extended control....429
17.3 ZBS detection....429
17.3.1 Description....429
17.3.2 Specifications....430
17.4 Incrementing, locking, and clearing the ZBS count....430
17.4.1 Description....430
17.4.2 Specifications....431
17.5 Shared use of ZBSs by the EPU and STL....433
17.5.1 Description....433
17.5.1.1 EPU Operating States....433
17.5.1.2 EPU Operating State characteristics....434
17.5.1.3 ZBS use that is compatible with EPU Operating States....435
17.5.1.4 An approach to implementing EPU Operating States....436
17.5.2 Specifications....438
17.6 EPU functionality associated with the ZBS count....439
17.6.1 Description....439
17.6.2 Specifications....439
17.7 Programming considerations....440
18. T1 TAP.7....441
18.1 Introduction....441
18.2 Deployment....442
18.3 Capabilities....442
18.3.1 Inherited....442
18.3.2 New....443
18.4 Register and command portfolio....443
18.4.1 Description....443
18.4.1.1 General information....443
18.4.1.2 Register acronyms....444
18.4.1.3 Global Registers....445
18.4.1.4 Registers already described....445
18.4.1.5 New register descriptions....445
18.4.2 Specifications....445
18.5 Configurations....447
18.5.1 Description....447
18.5.2 Specifications....447
18.6 Start-up behavior....448
18.6.1 Description....448
18.6.2 Specifications....448
18.7 Conditional Group Membership....448
18.8 Test Reset....449
18.8.1 Description....449
18.8.2 Specifications....450
18.9 Functional reset....451

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

18.9.1 Description 451
18.9.2 Specifications 453
18.10 Power control 455
18.10.1 Description 455
18.10.1.1 Overview 455
18.10.1.1.1 Use cases 456
18.10.1.1.2 Power-control options 456
18.10.1.1.3 Power management within a typical system 457
18.10.1.1.4 Power-control topics 458
18.10.1.2 Power-Control Model 458
18.10.1.2.1 TAP.7 Controller power-management states 458
18.10.1.2.2 Key model attributes 459
18.10.1.3 The chip-level power manager's role in power control 460
18.10.1.3.1 Responsibilities 460
18.10.1.3.2 Interaction with TAP.7 Controller 460
18.10.1.3.3 Periods when a Type-0 Reset is asserted 461
18.10.1.3.4 Handling of power-up and power-down requests 461
18.10.1.3.5 Chip-Level power-up and power-down enables 462
18.10.1.3.6 The default Power-Control Mode 462
18.10.1.4 The DTS' role in power control 463
18.10.1.4.1 Responsibilities 463
18.10.1.4.2 Directed power-up 463
18.10.1.4.3 Detected power-up 464
18.10.1.5 The TAP.7 Controller's role in power control 465
18.10.1.5.1 Responsibilities 465
18.10.1.5.2 Operation 465
18.10.1.5.3 Test periods 466
18.10.1.5.4 Power-up confirmation test 467
18.10.1.5.5 Power-down initiation test 467
18.10.1.5.6 Power-down request summary 468
18.10.1.5.7 Awaiting power-down with the TAP.7 Controller operation shutdown 468
18.10.1.6 Example power-down sequences 469
18.10.1.7 An approach to implementing power control 471
18.10.2 Specifications 471
18.11 RSU operation 476
18.11.1 Description 476
18.11.2 Specifications 477
18.12 Programming considerations 477
19. T2 TAP.7 478
19.1 Introduction 478
19.2 Deployment 480
19.3 Capabilities 480
19.3.1 Inherited 480
19.3.2 New 480
19.4 Register and command portfolio 481
19.4.1 Description 481
19.4.1.1 General information 481
19.4.1.2 Register acronyms 481
19.4.1.3 Effects of a Long-Form Selection Sequence 481
19.4.1.4 New register descriptions 481
19.4.2 Specifications 482
19.5 Configurations 483
19.5.1 Description 483
19.5.2 Specifications 483
19.6 Start-up behavior 483
19.6.1 Description 483

Copyright © 2022 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

19.6.2 Specifications 483
19.7 Scan formats 484
19.7.1 Description 484
19.7.2 Specifications 484
19.8 STL Group Membership 484
19.8.1 Description 484
19.8.1.1 Factors affecting group membership 484
19.8.1.2 Reset effects 485
19.8.1.3 TAPC state effects 485
19.8.1.4 Control Path effects 485
19.8.1.5 Parked state/selection relationships 487
19.8.1.6 Concurrent CLTAPC and EMTAPC selection changes 488
19.8.1.7 An approach to implementing CLTAPC selection with the T2 Class 489
19.8.2 Specifications 491
19.9 RSU operation 493
19.9.1 Description 493
19.9.2 Specifications 493
19.10 Programming considerations 494
20. T3 TAP.7 495
20.1 Introduction 495
20.2 Deployment 497
20.3 Capabilities 498
20.3.1 Inherited 498
20.3.2 New 498
20.4 Register and command portfolio 498
20.4.1 Description 498
20.4.1.1 General information 498
20.4.1.2 Register acronyms 499
20.4.1.3 Effect of a Long-Form Selection Sequence 499
20.4.2 Specifications 499
20.5 Configurations 500
20.5.1 Description 500
20.5.2 Specifications 501
20.6 Start-up behavior 501
20.6.1 Description 501
20.6.2 Specifications 501
20.7 Scan formats 501
20.7.1 Description 501
20.7.2 Specifications 502
20.8 TAP.7 Controller Address (TCA) 502
20.8.1 Description 502
20.8.2 Specifications 503
20.9 Aliasing the TCA to a Controller ID 504
20.9.1 Description 504
20.9.1.1 CID Allocate Command (CIDA) 504
20.9.1.1.1 CID-allocation criteria 505
20.9.1.1.2 CID-allocation candidates 505
20.9.1.1.3 CID-allocation process 505
20.9.1.1.4 Directed CID Allocation 506
20.9.1.1.5 Undirected CID Allocation 506
20.9.1.2 External AT generation with the JScan3 Scan Format 506
20.9.1.3 CID-allocation examples 507
20.9.1.4 An approach to implementing CID allocation 508
20.9.2 Specifications 509
20.10 Scan Selection Directives 512
20.10.1 Description 512

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

20.10.1.1 Overview 512
20.10.1.2 SSD format 513
20.10.1.3 SSD effects on STL Group Membership 513
20.10.1.4 Enabling SSD processing 514
20.10.1.5 SSD processing 514
20.10.1.6 Conditional SSD execution 517
20.10.1.7 SSD interaction with other controller functions 517
20.10.1.8 SSD State Machine 517
20.10.1.9 SSD states allowing Scan Group Membership 519
20.10.1.9.1 Using SSDs to create Series and Star-Equivalent Scans 520
20.10.1.9.2 Examples of SSD use 520
20.10.1.10 An approach to implementing the SSD function 525
20.10.2 Specifications 527
20.11 Scan Topology Training Sequence 531
20.11.1 Description 531
20.11.1.1 Overview 531
20.11.1.2 Topology Register Function 531
20.11.1.3 Use cases 532
20.11.1.3.1 Operation with a single TAP.7 Branch 532
20.11.1.3.2 Operation with more than one TAP.7 Branch 533
20.11.1.4 Scan-path characteristics used to determine the scan topology 533
20.11.1.5 Scan Topology Training Command Sequence 534
20.11.1.5.1 Connectivity test 535
20.11.1.5.2 Continuity test 535
20.11.2 Specifications 536
20.12 Managing STL Group Membership 536
20.12.1 Description 536
20.12.1.1 Factors affecting group membership 536
20.12.1.2 An approach to implementing CLTAPC selection with T3 and above classes 536
20.12.2 Specifications 538
20.13 RSU operation 540
20.13.1 Description 540
20.13.2 Specifications 541
20.14 Programming considerations 541
21. Advanced concepts 542
21.1 Architecture 542
21.2 Advanced capabilities 543
21.2.1 Mandatory and optional capabilities 543
21.2.2 Online and Offline operation 544
21.2.3 Interoperability with T0–T3 TAP.7s 544
21.2.4 Interoperability with T4 and above TAP.7s 544
21.3 Comparing the Standard and Advanced Protocols 545
21.4 APU functions 545
21.4.1 Conceptual view 545
21.4.2 Bypass Function 546
21.4.3 Scan Function 547
21.4.4 Transport Function 548
21.4.5 Bypass/Scan/Control Function interactions 550
21.5 APU interfaces 550
21.5.1 TAP 550
21.5.2 EPU 551
21.5.3 DCC 551
21.6 APU function/Operating State relationships 553
21.6.1 Operating State/function relationships 553
21.6.2 APU Operating State changes 554
21.6.3 Example operating state sequences 555

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

21.7 TAPC state/packet relationships 557
21.7.1 TAPC state and packet sequence relationships 557
21.7.2 Constructing packet sequences 559
21.7.3 Packet combinations/TAPC state relationships 560
21.7.4 Scheduling of packets 560
21.8 User's and implementer's views of the Advanced Protocol 562
21.8.1 User's view 562
21.8.2 Implementer's view 563
21.9 An approach to implementing APU Operating State scheduling 563
21.10 Structure of the clauses describing T4 and above TAP.7s 565
22. APU Scan Packets 567
22.1 CPs 567
22.2 SPs 567
22.2.1 Conceptual view of an SP 567
22.2.2 SP format 568
22.2.3 SP content 569
22.2.3.1 Header Element content 569
22.2.3.2 Payload Element content 569
22.2.3.3 Delay Element content 570
22.2.4 Types of output bit-frame transactions 571
22.3 SPs that advance the TAPC state 572
22.4 TPs 573
22.4.1 Conceptual view of a TP 573
22.4.2 TP format 573
22.4.3 Content 575
22.5 APU state diagram 575
22.6 An approach to implementing packet scheduling 577
22.6.1 Pipelining and its effects 577
22.6.2 SP Element scheduling 577
22.6.3 TP Element scheduling 578
23. T4 TAP.7 579
23.1 Introduction 579
23.2 Deployment 579
23.3 Capabilities 580
23.3.1 Inherited 580
23.3.2 New 580
23.4 Register and command portfolio 581
23.4.1 Description 581
23.4.1.1 General information 581
23.4.1.2 Register acronyms 581
23.4.1.3 Effect of a Long-Form Selection Sequence 581
23.4.1.4 New register descriptions 582
23.4.1.4.1 Auxiliary Pin Function Control (APFC) Register 582
23.4.1.4.2 Delay Control (DLYC) Register 582
23.4.1.4.3 Ready Control (RDYC) Register 582
23.4.1.4.4 Sample Using Rising Edge (SREDGE) Register 582
23.4.1.4.5 Scan Format (SCNFMT) Register 582
23.4.1.4.6 System Test Clock Duty Cycle (STCKDC) Register 582
23.4.2 Specifications 583
23.5 Configurations 585
23.5.1 Description 585
23.5.2 Specifications 585
23.6 Start-up behavior 586
23.6.1 Description 586
23.6.2 Specifications 586
23.7 Scan formats 587

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

23.7.1 Description 587
23.7.1.1 Overview 587
23.7.1.2 Addition of optional scan formats 589
23.7.1.3 Influences on scan format definition 589
23.7.1.4 Performance and flexibility tradeoffs 589
23.7.1.5 Comparing the scan formats 590
23.7.1.5.1 MScan 590
23.7.1.5.2 OScan 590
23.7.1.5.3 SScan 591
23.7.2 Specification 592
23.8 Configuration Faults 592
23.8.1 Description 592
23.8.2 Specifications 592
23.9 Increasing STL performance 593
23.9.1 Description 593
23.9.2 Specifications 594
23.10 Auxiliary Pin Function Control 595
23.10.1 Description 595
23.10.2 Specifications 596
23.11 Sample Using Rising Edge 596
23.11.1 Description 596
23.11.2 Specifications 597
23.12 System and EPU TMS signal values 597
23.12.1 Description 597
23.12.2 Specifications 598
23.13 System and EPU TDI signal values 599
23.13.1 Description 599
23.13.2 Specifications 600
23.14 RDY bit values 601
23.14.1 Description 601
23.14.2 Specifications 602
23.15 TDO bit values 603
23.15.1 Description 603
23.15.2 Specifications 604
23.16 Advanced Protocol effects on the EPU/CLTAPC relationship 604
23.16.1 Description 604
23.16.2 Specifications 604
23.17 SSD detection 604
23.17.1 Description 604
23.17.2 Specifications 604
23.18 Programming considerations 605
23.19 An approach to implementing a TAP.7 Controller with maximum performance 605
24. MScan Scan Format 607
24.1 Capabilities 607
24.1.1 Primary purpose 607
24.1.2 Application types supported 607
24.1.3 Important characteristics 608
24.2 High-level operation 608
24.3 Scan Packet content 609
24.3.1 Description 609
24.3.2 Specifications 609
24.4 Payload Element 609
24.4.1 Description 609
24.4.1.1 Format 609
24.4.1.2 Relationship to EPU signals 610
24.4.1.3 RDY bits 611

Copyright © 2022 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

24.4.2 Specification 613
24.5 Delay Element 613
24.5.1 Description 613
24.5.1.1 Format 613
24.5.1.2 Delay Element Directives 614
24.5.1.3 Uses 614
24.5.2 Specifications 615
24.6 Advancing the TAPC state 616
24.6.1 Description 616
24.6.2 Specifications 617
24.7 CID allocation 617
24.7.1 Description 617
24.7.2 Specifications 619
24.8 Increasing STL performance with the MScan Scan Format 619
24.9 An approach to implementing the MScan Scan Format 619
24.9.1 Payload State Machine 619
24.9.2 Ready State Machine 621
24.9.3 Delay State Machine 622
24.10 Where to find examples 623
25. OScan Scan Formats 624
25.1 Capabilities 624
25.1.1 Primary purpose 624
25.1.2 Application types supported 624
25.1.3 Important characteristics 625
25.2 High-level operation 625
25.3 Scan Packet content 626
25.3.1 Description 626
25.3.2 Specifications 626
25.4 Payload Element 627
25.4.1 Description 627
25.4.1.1 Format 627
25.4.1.2 Optimizations 628
25.4.1.3 Relationship to EPU signals 629
25.4.1.4 Input bit-frame 633
25.4.1.5 Drive types 633
25.4.1.6 RDY bits 634
25.4.2 Specifications 635
25.5 Delay Element 636
25.6 Advancing the TAPC state 637
25.6.1 Description 637
25.6.2 Specifications 639
25.7 CID allocation 640
25.7.1 Description 640
25.7.2 Specifications 640
25.8 Increasing STL performance with OScan Scan Formats 640
25.9 An approach to implementing OScan Scan Formats 641
25.9.1 Payload State Machine 641
25.9.2 Shift Progress flag 643
25.9.3 CSM and SSM activation 644
25.9.4 RDY State Machine 644
25.9.5 TAP advance 645
25.10 Where to find examples 645
26. SScan Scan Formats 646
26.1 Capabilities 646
26.1.1 Primary purpose 646
26.1.2 Application types supported 647

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

26.1.3 Control Segments 648
26.1.4 Data Segments 649
26.1.5 Stall profiles 649
26.1.6 Important characteristics 650
26.2 High-level operation 650
26.2.1 Overview 650
26.2.2 Segments and their use 651
26.2.2.1 Description 651
26.2.2.1.1 Use with a TAP.1-like component 651
26.2.2.1.2 Use with a DMA or FIFO component 652
26.2.2.1.3 Use with a direct-access data-rate-dependent component 653
26.2.2.1.4 Use with a buffered TDI/TMS component 653
26.2.2.1.5 Utilizing the same scan format for two applications types 654
26.2.2.2 Specifications 655
26.3 Scan Packet content 655
26.3.1 Description 655
26.3.2 Specifications 656
26.4 Header Element 657
26.4.1 Description 657
26.4.2 Specifications 657
26.5 Payload Element 658
26.5.1 Description 658
26.5.1.1 Factors determining payload content 658
26.5.1.2 Optimizations 660
26.5.1.3 Input bit-frame 663
26.5.1.4 Output bit-frame 666
26.5.1.4.1 Content 666
26.5.1.4.2 SScan0/1 output-only segments 666
26.5.1.4.3 SScan2/3 output-only segments 667
26.5.2 Specifications 671
26.6 Delay Element 673
26.7 Packet sequences and factors influencing them 674
26.7.1 Description 674
26.7.2 Specifications 676
26.8 Advancing the TAPC state 677
26.8.1 Description 677
26.8.1.1 SP followed by a CP 677
26.8.1.2 Control Segments 677
26.8.1.3 Data Segments 677
26.8.2 Specifications 681
26.9 CID allocation 681
26.9.1 Description 681
26.9.2 Specifications 681
26.10 Increasing STL performance with SScan Scan Formats 682
26.11 An approach to implementing SScan Scan Formats 682
26.11.1 Payload State Machine 682
26.11.2 Escape Detection State Machine 683
26.11.3 Shift Progress flag 684
26.11.4 TAP advance 685
26.11.5 Additional entry point loads for output-only segments 685
26.11.6 Header Register 686
26.11.7 Timing diagrams 687
26.12 Where to find examples 689
27. T5 TAP.7 690
27.1 Introduction 690
27.2 Deployment 691

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

27.3 Capabilities 692
27.3.1 Inherited 692
27.3.2 New 692
27.4 Register and command portfolio 692
27.4.1 Description 692
27.4.1.1 General information 692
27.4.1.2 Register acronyms 693
27.4.1.3 Effect of a Long-Form Selection Sequence 693
27.4.1.4 Transport protocol revision (TPPREV) register 693
27.4.1.5 Transport states (TPST) 694
27.4.1.6 Data Element length (TP_DELN) 694
27.4.1.7 Physical Data Channel to Logical Data Channel association (PDCx_LCA) 694
27.4.1.8 Physical Data Channel selected (PDCx_SEL) 694
27.4.1.9 Physical Data Channel DCC selection (PDCx_DCC) 694
27.4.1.10 Physical Data Channel DCC Control Registers (PDCx_DCCy_CRz) 694
27.4.2 Specifications 695
27.5 Configurations 699
27.5.1 Description 699
27.5.2 Specifications 700
27.6 Start-up behavior 701
27.6.1 Description 701
27.6.2 Specifications 701
27.7 Configuration Faults 701
27.7.1 Description 701
27.7.2 Specifications 701
27.8 Enabling transport 702
27.8.1 Description 702
27.8.2 Specifications 702
27.9 Transport Packet composition 703
27.9.1 Operations 703
27.9.2 Directive, Register, and Data Elements 704
27.10 Directive Elements 704
27.10.1 Description 704
27.10.1.1 Overview 704
27.10.1.2 Directive Element acronyms 705
27.10.1.3 Surrounding context of directives 705
27.10.1.4 Directive/transport building block relationships 706
27.10.1.5 Directive encoding 707
27.10.1.6 Directive types 708
27.10.1.6.1 Unconditional Directives 709
27.10.1.6.2 Reset Directives 709
27.10.1.6.3 Selection Directives 709
27.10.1.6.4 Conditional Directives 710
27.10.1.6.5 Transfer Directives 711
27.10.2 Specifications 711
27.11 Register Elements 715
27.11.1 Description 715
27.11.1.1 Overview 715
27.11.1.2 Register Element length 715
27.11.1.3 Transfer direction 715
27.11.1.4 Summary of Register Element characteristics 715
27.11.2 Specifications 716
27.12 Data Elements 716
27.12.1 Description 716
27.12.1.1 Overview 716
27.12.1.2 Data Element length 716

Copyright © 2022 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

27.12.1.3 Transfer direction 716
27.12.1.4 Utilization and generation of data 717
27.12.1.5 Operation with single and multiple clients 717
27.12.1.6 Summary of Data Element characteristics 718
27.12.2 Specifications 718
27.13 Selection of control and data targets 719
27.14 Data Channel Client functions 720
27.14.1 Description 720
27.14.1.1 Initializing a Data Channel Client 720
27.14.1.2 Orderly shutdown of a transfer 720
27.14.1.3 Effects of Online/Offline operation on the Transport Function 721
27.14.2 Specifications 722
27.15 Partitioning of the Transport Control Function 722
27.15.1 Building blocks 722
27.15.2 Directive/register/operational relationships 724
27.16 Programming considerations 725
27.16.1 Managing transport with the DTS 725
27.16.2 Single and multi-client data exchanges 725
27.16.3 Bandwidth allocation 725
27.16.4 Common and uncommon operations performed with directives 725
27.16.5 Dynamic source/destination changes 726
27.16.6 Transfer alignment characteristics 727
27.17 Aspects of transport not covered by this specification 727
28. Transport operation and interfaces 728
28.1 Introduction 728
28.2 TAP interface 728
28.2.1 *TPA* state flow 728
28.2.2 Directive Element characteristics 729
28.2.2.1 Description 729
28.2.2.2 Specifications 729
28.2.3 Register Element characteristics 731
28.2.3.1 Description 731
28.2.3.1.1 Format, timing, and TMSC signal drive characteristics 731
28.2.3.1.2 Register Element length 731
28.2.3.1.3 Register Element content 732
28.2.3.2 Specifications 733
28.2.4 Data Element characteristics 734
28.2.4.1 Description 734
28.2.4.1.1 Format, timing, and TMSC signal drive characteristics 734
28.2.4.1.2 Data Element length 735
28.2.4.1.3 Data Element content 736
28.2.4.1.4 Drive characteristics 737
28.2.4.1.5 Multi-client data transfers 737
28.2.4.1.6 Data Element alignment with the data that is transported 738
28.2.4.2 Specifications 738
28.3 Transport State Machine 739
28.3.1 Description 739
28.3.1.1 Conceptual view 739
28.3.1.2 TSM operation 741
28.3.1.3 Scheduling a TP 742
28.3.1.4 Starting/restarting directive processing 744
28.3.1.5 Completing a TP 744
28.3.2 Specifications 745
28.4 PDCx/DCC interface 746
28.4.1 Description 746
28.4.1.1 Signal functions 747

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

28.4.1.2 Signal descriptions 747
28.4.1.3 Signal use 749
28.4.2 Specifications 753
28.5 Five-bit directives 753
28.5.1 Description 753
28.5.2 Specifications 753
28.6 Eight-bit directives 755
28.6.1 Description 755
28.6.2 Specifications 756
28.7 12-bit directives 757
28.7.1 Description 757
28.7.2 Specifications 757
28.8 DCC interface operation 760
28.8.1 Basic capability 760
28.8.2 Pipelining register *dcc_rdo* signaling 761
28.8.3 Pipelining *dcc_ddo* and *dcc_cor* signaling 761
28.9 An approach to implementing the Transport Function 762
28.9.1 Overview 762
28.9.2 The Transport State Machine 763
28.9.3 Multi-use register bits 764
28.9.3.1 Input configurations 764
28.9.3.2 Transport Packet processing 765
28.9.3.2.1 Directive processing 765
28.9.3.2.2 Data Element processing 765
28.9.3.2.3 12-bit directive processing (other than TP_CRR and TP_CRW) 766
28.9.3.2.4 TP_CRR and TP_CRW Directive processing 766
28.9.3.3 TSM state/register value relationships 767
28.9.3.4 Transport output and DCR input selection 770
28.9.3.5 TP activity examples 772
29. Test concepts 777
29.1 Introduction 777
29.2 Interoperability 777
29.3 Construction of the unit under test 778
29.4 Background (IEEE 1149.1 paradigm) 778
29.4.1 Topology 779
29.4.2 Scan-state sequencing 779
29.5 Implications for test applications arising from this standard 780
29.5.1 Divergences versus IEEE Std 1149.1 780
29.5.2 Accommodation/resolution of divergences versus IEEE Std 1149.1 781
29.6 Test example—a narrative 781
29.7 Describing the unit under test 782
29.8 Documentation model 783
29.9 Considerations for large-system applications 784
30. Documenting IEEE 1149.7 test endpoints (BSDL.7) 786
30.1 Introduction 786
30.2 Conventions 787
30.3 Purpose of BSDL.7 787
30.4 Scope of BSDL.7 787
30.5 Expectations of a BSDL.7 parser 788
30.6 Relationship of BSDL.7 to BSDL.1 788
30.6.1 Description 788
30.6.2 Specifications 789
30.7 Lexical elements of BSDL.7 789
30.7.1 Description 789
30.7.2 Specifications 789
30.8 BSDL.7 reserved words 789

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

30.8.1 Description 789
30.8.2 Specifications 789
30.9 Components of a BSDL.7 description 790
30.9.1 Description 790
30.9.2 Specifications 790
30.10 The entity description (BSDL.7) 790
30.10.1 Overall structure of the entity description (BSDL.7) 790
30.10.1.1 Syntax and content 790
30.10.1.1.1 Description 790
30.10.1.1.2 Specifications 791
30.10.1.2 Semantic checks 792
30.10.1.2.1 Description 792
30.10.1.2.2 Specifications 792
30.10.2 Standard use statement (BSDL.7) 792
30.10.2.1 Syntax and content 792
30.10.2.1.1 Description 792
30.10.2.1.2 Specifications 793
30.10.2.2 Examples 793
30.10.3 Version control 794
30.10.3.1 Syntax and content 794
30.10.3.1.1 Description 794
30.10.3.1.2 Specifications 794
30.10.4 Component conformance statement (BSDL.7) 794
30.10.4.1 Syntax and content 794
30.10.4.1.1 Description 794
30.10.4.1.2 Specifications 795
30.10.4.2 Examples 795
30.10.4.3 Semantic checks 795
30.10.5 Scan port identification (BSDL.7) 795
30.10.5.1 Syntax and content 795
30.10.5.1.1 Description 795
30.10.5.1.2 Specifications 796
30.10.5.2 Examples 796
30.10.5.3 Semantic checks 798
30.10.5.3.1 Description 798
30.10.5.3.2 Specifications 798
30.10.6 Compliance enable description (BSDL.7) 799
30.10.6.1 Syntax and content 799
30.10.6.1.1 Description 799
30.10.6.1.2 Specifications 799
30.10.6.2 Examples 799
30.10.6.3 Semantic checks 800
30.10.6.3.1 Description 800
30.10.6.3.2 Specifications 800
30.10.7 Device identification register description (BSDL.7) 800
30.10.7.1 Syntax and content 800
30.10.7.1.1 Description 800
30.10.7.1.2 Specifications 800
30.10.7.2 Examples 800
30.10.7.3 Semantic checks 801
30.10.7.3.1 Description 801
30.10.7.3.2 Specifications 801
30.10.8 Configuration register description (BSDL.7) 801
30.10.8.1 Syntax and content 801
30.10.8.1.1 Description 801
30.10.8.1.2 Specifications 801

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

30.10.8.2 Examples 801
30.10.8.3 Semantic checks 802
30.10.8.3.1 Description 802
30.10.8.3.2 Specifications 802
30.11 The Standard BSDL.7 Package STD_1149_7_2009 803
30.11.1 Description 803
30.11.2 Specifications 803
30.12 A typical application of BSDL.7 803
31. Documenting IEEE 1149.7 test modules (HSDL.7) 806
31.1 Introduction 806
31.2 Conventions 806
31.3 Purpose of HSDL.7 807
31.4 Scope of HSDL.7 807
31.5 Expectations of an HSDL.7 parser 808
31.6 Relationship of HSDL.7 to BSDL.7 (and BSDL.1) 808
31.6.1 Description 808
31.6.2 Specifications 809
31.7 Lexical elements of HSDL.7 809
31.7.1 Description 809
31.7.2 Specifications 809
31.8 HSDL.7 reserved words 809
31.8.1 Description 809
31.8.2 Specifications 809
31.9 Components of an HSDL.7 description 809
31.9.1 Description 809
31.9.2 Specifications 810
31.10 The entity description (HSDL.7) 810
31.10.1 Overall structure of the entity description (HSDL.7) 810
31.10.1.1 Syntax and content 810
31.10.1.1.1 Description 810
31.10.1.1.2 Specifications 810
31.10.1.2 Semantic checks 811
31.10.1.2.1 Description 811
31.10.1.2.2 Specifications 811
31.10.2 Module standard use statement (HSDL.7) 811
31.10.2.1 Syntax and content 811
31.10.2.1.1 Description 811
31.10.2.1.2 Specifications 812
31.10.2.2 Examples 813
31.10.3 Version control 813
31.10.3.1 Syntax and content 813
31.10.3.1.1 Description 813
31.10.3.1.2 Specifications 813
31.10.4 Module component conformance statement (HSDL.7) 814
31.10.4.1 Syntax and content 814
31.10.4.1.1 Description 814
31.10.4.1.2 Specifications 814
31.10.4.2 Examples 814
31.10.4.3 Semantic checks 814
31.10.5 Module package pin mappings (HSDL.7) 815
31.10.5.1 Syntax and content 815
31.10.5.1.1 Description 815
31.10.5.1.2 Specifications 815
31.10.5.2 Examples 815
31.10.5.3 Semantic checks 815
31.10.5.3.1 Description 815

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

31.10.5.3.2 Specifications 815
31.10.6 Module scan port identification (HSDL.7) 815
31.10.6.1 Syntax and content 815
31.10.6.1.1 Description 815
31.10.6.1.2 Specifications 816
31.10.6.2 Examples 816
31.10.6.3 Semantic checks 817
31.10.6.3.1 Description 817
31.10.6.3.2 Specifications 817
31.10.7 Module members declaration (HSDL.7) 818
31.10.7.1 Syntax and content 818
31.10.7.1.1 Description 818
31.10.7.1.2 Specifications 819
31.10.7.2 Examples 820
31.10.7.3 Semantic checks 821
31.10.7.3.1 Description 821
31.10.7.3.2 Specifications 821
31.11 The Standard HSDL.7 Package STD_1149_7_2009_module 822
31.11.1 Description 822
31.11.2 Specifications 822
31.12 Applications of HSDL.7 822
31.12.1 HSDL.7 for IEEE 1149.1 serial connection using one TMS signal 822
31.12.2 HSDL.7 for IEEE 1149.1 connection in two paralleled serial chains 824
31.12.3 HSDL.7 for a basic Star Scan Topology 825
31.12.4 HSDL.7 for a basic hierarchical topology 826
31.12.5 A typical application of HSDL.7 828
Annex A (informative) IEEE 1149.1 reference material 830
Annex B (informative) Scan examples in timing diagram form 834
B.1 MScan and OScan SP types 834
B.2 MScan and OScan transactions 835
B.2.1 MScan transaction 835
B.2.2 OScan0 transaction 837
B.2.3 OScan1 transaction 838
B.2.4 OScan2 transaction 839
B.2.5 OScan3 transaction 840
B.2.6 OScan4 transaction 841
B.2.7 OScan5 transaction 842
B.2.8 OScan6 transaction 843
B.2.9 OScan7 transaction 845
B.3 SScan transactions 846
B.3.1 SScan0 transaction 847
B.3.2 SScan1 transaction 850
B.3.3 SScan2 transaction 853
B.3.4 SScan3 transaction 856
B.4 BDX and CDX Transport Packet examples 859
Annex C (informative) Scan examples in tabular form 861
C.1 Overview 861
C.2 MScan and OScan SP types 861
C.3 SScan SP types 876
Annex D (informative) Programming considerations 903
D.1 Overview 903
D.2 DTS' view of TAPs 903
D.2.1 Technology branches 903
D.2.2 Power-management RSU combinations 904
D.2.3 TAP.7 Controller deselection and selection 906
D.2.4 Start-up versus steady-state operation 907

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

D.2.5 Start-up 908
D.2.6 Initialization requirements 909
D.2.6.1 Initial state....909
D.2.6.2 Factors influencing initialization 909
D.2.6.3 Initialization function....909
D.2.6.4 Reset Escape 910
D.2.6.5 Reset TAP.7 Controllers without an RSU....911
D.2.6.6 Power-up TAP.7 Controllers that are un-powered....911
D.2.6.7 Placing a TAP.7 Controller Online that is Offline-at-Start-up....911
D.2.7 Scan Topology Training 915
D.3 Scan topology interrogation....916
D.3.1 Series Branch interrogation....917
D.3.1.1 Series characteristics used for interrogation 917
D.3.1.2 Interrogation process....918
D.3.1.3 Configuration Register reads 920
D.3.1.4 Determining whether a Series Branch is selectable 921
D.3.1.5 Quick determination of TAP types in a Series Branch 921
D.3.2 Star-4 Branch interrogation....922
D.3.2.1 Information provided 922
D.3.2.2 Interrogation process....922
D.3.3 Star-2 Branch interrogation....926
D.3.3.1 Information provided 926
D.3.3.2 Interrogation process....926
D.4 Establishing TAP.7 operating conditions....929
D.5 CID management 929
D.6 Managing simultaneous debug actions 930
D.7 Operations to avoid with a Star-4 Scan Topology 930
D.7.1 The use of the JScan0–JScan2 Scan Formats 930
D.7.2 The selection of CLTAPCs of TAP.7 Controllers allocated the same CID 930
D.8 Using a T5 TAP.7 931
D.8.1 Setup and use of the Transport Function....931
D.8.2 Sharing the use of a Logical Data Channel....931
D.8.3 Transferring data with Transport Packet Data Payloads....931
Annex E (informative) Recommended electrical characteristics....932
Annex F (informative) Connectivity/electrical recommendations....933
F.1 Overview 933
F.1.1 General information....933
F.1.2 Factors affecting reliable operation 933
F.1.3 Factors affecting link performance....934
F.2 Physical connection topologies considered 935
F.3 Termination schemes considered....936
F.4 Chip considerations 938
F.4.1 SOC input conditioning....938
F.4.2 Signal driver rise and fall times 939
F.4.3 Clock-to-output delays 941
F.4.4 Supply and buffer impedances....941
F.4.5 Additional chip considerations related to multi-TAPC topologies....941
F.5 Board considerations 941
F.5.1 Signaling requiring a termination scheme 941
F.5.1.1 Lumped load....942
F.5.1.2 Distributed load 942
F.5.1.3 Classifying a load 942
F.5.1.4 Transmission-line impedance 943
F.5.2 Impedance discontinuities/symmetry 944
F.5.3 Transmission-line construction....947
F.5.3.1 Uniformity of transmission-line impedance 947

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

F.5.3.2 Proper construction....947
F.5.3.3 Improper construction....949
F.5.3.4 Connector treatment....949
F.5.4 Choosing a connection configuration....949
F.5.5 Termination schemes with simple configurations....950
F.5.5.1 Series termination....950
F.5.5.1.1 Overview....950
F.5.5.1.2 Challenges in series termination....951
F.5.5.1.3 Benefits of using series termination....951
F.5.5.2 Parallel termination....951
F.5.5.2.1 Overview....951
F.5.5.2.2 Challenges in using parallel termination....953
F.5.5.2.3 Benefits of using parallel termination....954
F.5.5.3 Parallel AC termination....954
F.5.5.3.1 Overview....954
F.5.5.3.2 Challenges in using parallel AC termination....956
F.5.5.3.3 Benefits of using parallel AC termination....957
F.5.6 Effects of transmission-line length on operating frequency....957
F.5.7 Capacitive load isolation and input pin low-pass filtering....958
F.5.8 DTS and chip models....958
F.5.9 Additional board considerations related to multi-TAPC topologies....959
F.6 System considerations for supporting Keeper bias (K bias) in multi-TAPC topologies....959
F.6.1 K bias considerations at the chip and board level....959
F.6.2 K bias considerations for embedded TAPC topologies....961
F.7 DTS considerations....963
F.7.1 Source impedance....963
F.7.2 Input capacitance isolation....964
F.7.2.1 DTS output levels with parallel terminated target topologies....964
F.7.2.2 DTS output edge rates....964
F.7.2.3 High-speed, high-current, low-voltage configurable edge-rate drivers....965
F.7.2.4 Low-voltage, high-current fixed slow edge-rate drive translator....965
F.7.2.5 In-system DTS considerations....967
F.7.2.5.1 Output buffer impedance....967
F.7.2.5.2 Power considerations....967
F.7.2.5.3 Signal edge rates....967
F.8 Point-to-Point configuration....967
F.8.1 Model....967
F.8.2 Unidirectional signaling....968
F.8.2.1 Series termination....968
F.8.2.2 Parallel AC termination....968
F.8.3 Bidirectional signaling....969
F.9 Line configuration of a transmission line....971
F.9.1 Model....971
F.9.2 Unidirectional signaling....973
F.9.2.1 Parallel AC termination....978
F.9.2.2 Parallel termination....980
F.9.2.3 Summary....980
F.9.3 Bidirectional signaling....980
F.9.3.1 Four loads....983
F.9.3.2 Eight loads....986
F.10 T configuration of a transmission line....989
F.10.1 Model....989
F.10.2 Unidirectional signaling....992
F.10.3 Bidirectional signaling....993
F.11 X configuration of a transmission line....997
F.11.1 Model....997

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

F.11.2 Unidirectional signaling 999
F.11.3 Bidirectional signaling....1002
F.12 XT configuration of a transmission line 1008
F.12.1 Model....1008
F.12.2 Unidirectional signaling 1009
F.12.3 Bidirectional signaling....1011
F.13 Recommendations 1017
F.13.1 Summary 1017
F.13.2 Connectivity/termination scheme 1018
F.13.3 Termination scheme/capacitive load isolation/signal relationships....1020
F.13.4 Utilizing board design tools and simulation 1022
Annex G (informative) Utilizing SScan Scan Formats....1023
Annex H (informative) The RTCK signal 1027
Annex I (informative) Bibliography....1035
Index....1036

Copyright © 2022 IEEE. All rights reserved.
Documents
Document Sharing Hub
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

Figures

Figure 1-1 — IEEE 1149.7 impact areas 57
Figure 1-2 — IEEE 1149.7/IEEE 1149.1 upgrade path 62
Figure 1-3 — Systems where the DTS and TS source the Test Clock 63
Figure 1-4 — Dedicated and Shared Test Clock signal 64
Figure 1-5 — Systems with a Return Test Clock 64
Figure 1-6 — Types of TAP.7 operation 65
Figure 1-7 — TAP.7 capability classes and their layered capability 66
Figure 1-8 — Utilization of TAP.7 Classes within scan topologies 68
Figure 1-9 — A system with TCK(C) and TMS(C) shared between TAP.7 and technologies 69
Figure 1-10 — IEEE 1149.7 standard organization 71
Figure 1-11 — Document organization 73
Figure 1-12 — Clause subject areas 75
Figure 1-13 — Annex subject areas 75
Figure 1-14 - Arc priority 78
Figure 1-15 - Flowchart symbol expansion 79
Figure 1-16 - MSB/LSB conventions 80
Figure 4-1 — Scan architectures utilizing IEEE Std 1149.1 93
Figure 4-2 — TAP.7 TAPC hierarchy 94
Figure 4-3 — Relationships of parking the TAPC state to its associated resources 95
Figure 4-4 — TAP.7 Controller management 99
Figure 4-5 — System and Control Path relationship 100
Figure 4-6 — Components involved in TAP.7 Controller power management 101
Figure 4-7 — TAP.7 Protocols and Escapes 108
Figure 4-8 — Control/Standard/Advanced Protocol relationships 110
Figure 4-9 — Expanded view of an SP sequence with the OScan1 Scan Format 110
Figure 4-10 — Control Protocol/Standard and Advanced Protocol relationships 111
Figure 4-11 — Packets, bit-frames, and bits 112
Figure 4-12 — TAP.7 architecture 116
Figure 4-13 — Conceptual view of the interface bridge 117
Figure 4-14 — Operating model types 120
Figure 4-15 — Conceptual view of basic T0–T2 TAP.7 operation without RSU 121
Figure 4-16 — Conceptual view of T0–T3 TAP.7 operation with an RSU 121
Figure 4-17 — TMSC pin utilization flow diagram for a T5 TAP.7 122
Figure 5-1 — T0 TAP.7 chip block diagram 123
Figure 5-2 — T0 TAP.7 test and debug views of the chip 124
Figure 5-3 — System-on-Chip (SoC) with IEEE 1149.7 multiple TAPC architecture 125
Figure 5-4 — High-level T0 TAP.7 functional block diagram 127
Figure 5-5 — T1 TAP.7 chip block diagram 127
Figure 5-6 — T1 TAP.7 features 128
Figure 5-7 — Command generation 131
Figure 5-8 — DR-Scan sequence used for command creation 132
Figure 5-9 — High-level view of TAP.7 Controller registers 133
Figure 5-10 — High-level view of TAP.7 Controller Global/Local Registers 134
Figure 5-11 — T1 TAP.7 physical and conceptual path relationships 135
Figure 5-12 — T1 TAP.7 Control and System Paths 136
Figure 5-13 — High-level T1 TAP.7 functional block diagram 138
Figure 5-14 — T2 TAP.7 chip block diagram 138
Figure 5-15 — T2 TAP.7 scan-path length reduction 140
Figure 5-16 — T2 TAP.7 physical and conceptual path relationships 141
Figure 5-17 — T2 TAP.7 Control and System Paths 142
Figure 5-18 — T2 TAP.7 group membership determination 143
Figure 5-19 — High-level T2 TAP.7 functional block diagram 144

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Figure 5-20 — T3 TAP.7 chip block diagram....145
Figure 5-21 — T3 TAP.7 scan-path length reduction....146
Figure 5-22 — T3 TAP.7 group membership related to the use of the System Path....148
Figure 5-23 — Series-Equivalent Scan using SSDs in a Star Scan Topology....152
Figure 5-24 — T2 TAP.7 physical and conceptual path relationships....153
Figure 5-25 — T2 TAP.7 Control and System Paths....154
Figure 5-26 — High-level T3 TAP.7 functional block diagram....155
Figure 6-1 — T4/T5 TAP.7 chip block diagram....156
Figure 6-2 — Conceptual block diagram of the functions of a T4 TAP.7....159
Figure 6-3 — TMSC pin utilization flow diagram for a T4 TAP.7....160
Figure 6-4 — *CPA* state entry from the *BPA* state with subsequent Online operation....161
Figure 6-5 — *CPA* state entry from the *SPA* state with subsequent Online operation....162
Figure 6-6 — *CPA* state entry from the *BPA* state with subsequent Offline operation....162
Figure 6-7 — *CPA* state entry from the *SPA* state with subsequent Offline operation....163
Figure 6-8 — Reset initiated *CPA* state entry/awaiting a Selection Sequence for an exit....163
Figure 6-9 — SP and TAPC state relationships....164
Figure 6-10 — Expanded view of an SP sequence....164
Figure 6-11 — Serialization and de-serialization of SP information....165
Figure 6-12 — High-level T4 TAP.7 functional block diagram....166
Figure 6-13 — T5 TAP.7 chip block diagram....167
Figure 6-14 — Logical channel configurations....168
Figure 6-15 — DTS data exchanges with one client....169
Figure 6-16 — DTS data exchanges with more than one client....170
Figure 6-17 — DTS data exchange between multiple clients....171
Figure 6-18 — Conceptual block diagram of the functions of T5 TAP.7....172
Figure 6-19 — TMSC pin utilization flow diagram for a T5 TAP.7....173
Figure 6-20 — TP placement and content....174
Figure 6-21 — High-level T5 TAP.7 functional block diagram....175
Figure 7-1 — System connectivity with mixed use of technologies and scan topologies....178
Figure 7-2 — TAP.1 Series Branches....179
Figure 7-3 — TAP.7 Series, Star-4, and Star-2 Scan Topologies....180
Figure 7-4 — TAP.7 TAPC hierarchy....181
Figure 7-5 — System connectivity supported by the TAP.7 architecture....182
Figure 7-6 — Contrasting IEEE 1149.1 and IEEE 1149.7 test views....183
Figure 8-1 — Parking the ADTAPC state....189
Figure 8-2 — Parking the Chip-Level TAPC state....190
Figure 8-3 — Parking the Chip-Level TAPC state....192
Figure 8-4 — Selection within a chip or system....193
Figure 8-5 — Example of debug use of the RSU....194
Figure 8-6 — Using Series/Star-4/and Star-2 Scan Topologies concurrently....195
Figure 9-1 — DR Scan sequence used for command creation....198
Figure 9-2 — Command completion timing....204
Figure 9-3 — Command construction and execution....205
Figure 9-4 — Conceptual to physical path mapping paths....211
Figure 9-5 — Conceptual view of the T1 and above TAP.7 Scan Paths....212
Figure 9-6 — Saved Scan Group Candidacy/ZBS-count and scan path selection relationships....213
Figure 9-7 — Conceptual view of a String Scan Path that supports reads and writes....217
Figure 9-8 — Example Series Scan Path with a String Path selected in a chip of interest....218
Figure 9-9 — Example of DTS-generated string-write data for three trailing bits....218
Figure 9-10 — String Scan Path characteristics in a Series Scan Topology....219
Figure 9-11 — Conceptual view of the Enumerate Scan Path....219
Figure 9-12 — Enumerate Scan Path characteristics in a Star-4 Scan Topology....225
Figure 9-13 — Conceptual view of command processing....232
Figure 9-14 — Conceptual view of command processor....233
Figure 9-15 — Conceptual view of EPU Scan Paths....234
Figure 10-1 — Conceptual view of the EPU reset logic and state machines....235

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Figure 10-2 — Reset State Machine....239
Figure 10-3 — Conceptual view of reset function....240
Figure 10-4 — Test Reset setup time....242
Figure 10-5 — A Type-0 through Type-2 Reset invoking the use of the Standard Protocol....247
Figure 10-6 — A Type-3 Reset invoking the use of the Standard Protocol....248
Figure 10-7 — A Type-4 Reset invoking the use of the Standard Protocol....249
Figure 10-8 — Type-0 through Type-2 Resets invoking Offline-at-Start-up operation....249
Figure 10-9 — A Type-3 Reset invoking Offline-at-Start-up operation....250
Figure 10-10 — Escape Detection....252
Figure 10-11 — Selection Escape followed by a Selection Sequence....253
Figure 10-12 — Conceptual view of the Escape Detection function....254
Figure 10-13 — Selection-Alert Bit Sequence....258
Figure 10-14 — Selection Alert LFSR for bit sequence generation....258
Figure 10-15 — TMSC delay options....259
Figure 10-16 — Selection Alert support logic....260
Figure 10-17 — Deselection Alert operation....262
Figure 10-18 — Selection Alert with embedded Selection Escape....264
Figure 10-19 — Falling-edge ADTAPC State Machine....265
Figure 11-1 — Conceptual view of technology selection mechanism....267
Figure 11-2 — Online/Offline operation with a TAP.7 Controller....268
Figure 11-3 — Online/Offline operation with another technology/RSU with Escapes....270
Figure 11-4 — Online/Offline operation with another technology/RSU with Alerts....270
Figure 11-5 — Offline initiation events....271
Figure 11-6 — Online initiation events....273
Figure 11-7 — TAP.7 Selection Sequence....276
Figure 11-8 — Conceptual view of TAP.7 Controller Selection Sequence....277
Figure 11-9 — Selection Escape/subsequent data timing relationship....280
Figure 11-10 — Selection Alert/subsequent data timing relationship....281
Figure 11-11 — Serial load and initialization of Global Registers....283
Figure 11-12 — CP format....285
Figure 11-13 — TAPC parking-state creation with a deselection Escape/Standard Protocol....288
Figure 11-14 — TAPC parking-state creation with a Selection Escape/Standard Protocol....288
Figure 11-15 — TAPC parking state/Selection Escape/the Advanced Protocol/relationship....289
Figure 11-16 — TAPC parking state/Deselection Escape/the Advanced Protocol/relationship....289
Figure 11-17 — Conceptual view of the Control State Machine....291
Figure 11-18 — CSM *TEST* state function....298
Figure 11-19 — Substates of the CSM *CHK* state....303
Figure 11-20 — A CP_NOP Directive initiated extension of the CP Body Element....303
Figure 11-21 — A CP_END Directive followed by Offline operation....304
Figure 11-22 — A CP_END Directive followed by the use of the Standard Protocol....304
Figure 11-23 — A CP_END Directive followed by the use of the Advanced Protocol....305
Figure 11-24 — A CP_RSO Directive initiating a Type 3 TAP.7 Controller reset....305
Figure 11-25 — CP template....306
Figure 11-26 — *OLS* Selection Escape qualification sequence....309
Figure 11-27 — Simultaneous Selection Escape qualification and TAPC state initialization....310
Figure 11-28 — Conceptual view of the CSM with all sub-states exposed....312
Figure 11-29 — Counter supporting function of the *OLS* state....313
Figure 12-1 — Conceptual view of TAP.7 signal functions....319
Figure 12-2 — Conceptual view of bias for TAP.7 input and input/output signal functions....320
Figure 12-3 — Online-at-Start-up Test Mode Select/signal bias relationships....324
Figure 12-4 — Offline-at-Start-up Test Mode Select/signal bias relationships....325
Figure 12-5 — A Type-0–Type-2 Reset initiating Offline-at-Start-up operation....326
Figure 12-6 — Test Mode Select signal bias changes....329
Figure 12-7 — Test Data Input/signal bias relationships for legacy operation....331
Figure 12-8 — Test Data Output/signal bias relationships....334
Figure 13-1 — TDO(C) Drive Policy/factor relationships....343

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Figure 13-2 — Hierarchical view of the TDO(C) Drive Policy 348
Figure 13-3 — Flattened view of the TDO(C) Drive Policy 349
Figure 13-4 — Conceptual view of TDOC Drive Policy 350
Figure 13-5 — T0 TAP.7 TDO Drive Policy 351
Figure 13-6 — T1–T2 TAP.7 TDO Drive Policy 353
Figure 13-7 — T3, T4(W), and T5(W) TAP.7 TDOC Drive Policies 355
Figure 13-8 — Conceptual view of the Scan Group Candidate Count operation 364
Figure 13-9 — *SGCC* and *PSGMCL* timing relationships 367
Figure 13-10 — SSD State/Delayed SSD State/timing relationships 369
Figure 13-11 — Conceptual view of the Conditional Group Membership Count operation 372
Figure 13-12 — Only Conditional Group Member determination 373
Figure 13-13 — Example of TDOC Drive Policy for a T3 and above TAP.7 376
Figure 13-14 — Conceptual view of SGCC and PSGMCL State Machines 378
Figure 13-15 — Determining Scan Group Only Member Last/Membership Count Last 378
Figure 13-16 — Conceptual view of CGMC state development 379
Figure 14-1 — SP content preview 380
Figure 14-2 — SP payload template 381
Figure 14-3 — Transport Packet content preview 382
Figure 14-4 — TMSC Advanced Protocol drive characteristics 383
Figure 14-5 — The TMSC Signal's Distributed Drive Policy 384
Figure 14-6 — Precharge Bit Drive Policy 386
Figure 14-7 — RDY Bit Drive Policy 388
Figure 14-8 — CLTAPC selection state/STL sourced output value relationships 390
Figure 14-9 — Correlation of TDO(C) and TDO Bit Drive Policies 392
Figure 14-10 — TDO Bit Drive Policy 393
Figure 14-11 — Transport Bit Drive Policy 395
Figure 14-12 — Conceptual view of TMSC signal output and miscellaneous support logic 397
Figure 14-13 — Conceptual view of TMSC data and drive enables 398
Figure 15-1 — Inclusion and exclusion of the STL from the scan path 402
Figure 15-2 — Conceptual view of the operation of an EMTAPC 403
Figure 16-1 — Deployment of the T0 TAP.7 405
Figure 16-2 — SoC with IEEE 1149.7 multiple TAPC architecture 406
Figure 16-3 — Operating mode changes/*Run-Test/Idle* state relationships 409
Figure 16-4 — Example IEEE 1149.7 multi-TAP architecture with IR-controlled TAPC exclusion 410
Figure 16-5 — IR Scan Path after the CLTAPC has exited the *Test-Logic-Reset* state and entered the *Run-Test/Idle* state 411
Figure 16-6 — DR Scan Path with the *IDCODE* instruction loaded in the CLTAPC IR 411
Figure 16-7 — DR selection with the TAPC_SELECT_NNN instruction loaded in the CLTAPC IR 412
Figure 16-8 — Example IEEE 1149.7 multi-TAP architecture to allow isolating of individual TAPCs under CLTAPC IR control 413
Figure 16-9 — Example IEEE 1149.7 multi-TAP architecture with DR-controlled TAPC exclusion or isolation 415
Figure 16-10 — Example IEEE 1149.7 multi-TAP architecture to allow control over the operating mode of individual TAPCs by using *tapc_select* chip signals 416
Figure 16-11 — Conceptual view of the TAP_QUERY instruction 417
Figure 16-12 — Example system 418
Figure 16-13 — Example of the active *BYPASS* instruction 423
Figure 16-14 — Package-level connectivity of the POR* and nTRST signals 425
Figure 16-15 — The DR-wire solution in the SiP-TAP approach 426
Figure 17-1 — Conceptual view of zero bit DR Scan detection 430
Figure 17-2 — Conceptual view of ZBS count locking 431
Figure 17-3 — TAPC-state/control-state and ZBS-count relationships 433
Figure 17-4 — EPU Operating States 433
Figure 17-5 — ZBS use state and ZBS-count control flow 436
Figure 17-6 — Conceptual view of the ZBS use states with both TAP.7 and other ZBS use 438
Figure 18-1 — Conceptual view of a T1 TAP.7 441

Copyright © 2022 IEEE. All rights reserved.
Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.
Full document details: IEEE 1149.7-2022

Figure 18-2 — Deployment of the T1 TAP.7....442
Figure 18-3 — Conceptual view of *nsys_trst* and *sys_tms* generation....449
Figure 18-4 — Conceptual view of functional reset request generation....452
Figure 18-5 — Conceptual view of function reset request timing/system-initiated clear....452
Figure 18-6 — Conceptual view of function reset request timing with DTS-initiated clear....453
Figure 18-7 — Components involved in TAP.7 Controller power management....457
Figure 18-8 — TAP.7 Controller power-management state progression....459
Figure 18-9 — TAP.7 power-manager operation....461
Figure 18-10 — Conceptual view of the TAP.7 power manager....462
Figure 18-11 — Typical power-mode interface....463
Figure 18-12 — Directed power-up of a TAP.7 Controller....464
Figure 18-13 — Detected power-up of a TAP.7 Controller....465
Figure 18-14 — Conceptual operation of TAP.7 Controller power control....466
Figure 18-15 — TAP.7 Controller power-management responsibilities....466
Figure 18-16 — Power-down criteria selection....467
Figure 18-17 — Mode 2 – TAP.7 Controller and STL shutdown....469
Figure 18-18 — Mode 0 – with a TCK TIMEOUT initiating power-down....470
Figure 18-19 — Mode 1 – with the *Test-Logic-Reset* state and TCK TIMEOUT initiating power-down....470
Figure 18-20 — Mode 2—with the *Test-Logic-Reset* state initiating power-down....470
Figure 18-21 — Power-down logic example....471
Figure 18-22 — Power-down request generation flowchart....473
Figure 18-23 — Power-down criteria selection....474
Figure 18-24 — Default Power-Control Mode....474
Figure 18-25 — A PD_STOP initiating a Type-3 TAP.7 Controller reset....476
Figure 19-1 — Typical T2 TAP.7....479
Figure 19-2 — Deployment of the T2 TAP.7....480
Figure 19-3 — *Run-Test/Idle*/Control Path/Scan Group Candidacy relationships....486
Figure 19-4 — Skewed *Run-Test/Idle*/Control Path/Scan Group Candidacy relationships....487
Figure 19-5 — TAP.7 Controller reset creating *Test-Logic-Reset* parking state....488
Figure 19-6 — Re-synchronization of ADTAPC and CLTAPC states following assertion of *nsys_trst*....489
Figure 19-7 — Conceptual view of T2 TAP.7 Scan Group Membership management....490
Figure 19-8 — Conceptual view of T2 TAP.7 current Scan Group Candidacy development....490
Figure 19-9 — CLTAPC selection state change/*Run-Test-Idle_f*/register relationships....492
Figure 19-10 — CLTAPC selection state change/*Test-Logic-Reset_f*....492
Figure 20-1 — T3 TAP.7....496
Figure 20-2 — Deployment of the T3 TAP.7....497
Figure 20-3 — TDOC output with the JScan3 Scan Format within the CR Scan....507
Figure 20-4 — CID allocation with a DTS-sourced AT....508
Figure 20-5 — CID allocation with a TS-sourced AT....508
Figure 20-6 — Conceptual view of CID and CIDI Registers....509
Figure 20-7 — Conceptual view of an SSD....513
Figure 20-8 — SSDs detection and completion regions....515
Figure 20-9 — Conceptual view of SSD Processing State Machine....516
Figure 20-10 — SSD Interlocking State Machine....518
Figure 20-11 — SSD detection and completion window....521
Figure 20-12 — SSDs changing the Scan Group Membership in the *RTI* state....522
Figure 20-13 — SSD_SA ignored because of early exit from the *RTI* state....523
Figure 20-14 — SSDs changing the Pause Selection state....524
Figure 20-15 — SSD_SA ignored in the *Pause-xR* state....525
Figure 20-16 — Conceptual view of SSD processing....526
Figure 20-17 — Conceptual view of SSD state and SSD state delayed....526
Figure 20-18 — Conceptual view of TCA and CID comparison....527
Figure 20-19 — TMS and reset value required for SSD to perform its designated function....529
Figure 20-20 — SSD effects....531
Figure 20-21 — Scan topology characteristics used in Scan Topology Training....534

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Figure 20-22 — Conceptual view of current Scan Group Candidacy development—T3 and above TAP.7s 537
Figure 20-23 — Current Scan Group Candidacy development T3 and above TAP.7s 537
Figure 20-24 — Group membership operation....539
Figure 20-25 — Saved Scan Group Candidacy operation....540
Figure 20-26 — *sys_tck* gating/Scan Group Membership change relationships 540
Figure 21-1 — T4 and above TAP.7 chip block diagram....542
Figure 21-2 — Conceptual view of fully deployed APU functionality 543
Figure 21-3 — Conceptual block diagram of the APU and RSU functions 546
Figure 21-4 — APU/EPU interface....551
Figure 21-5 — APU/DCC(s) interface....552
Figure 21-6 — Conceptual view of TAP.7 use with a T5 TAP.7 Controller 553
Figure 21-7 — APU functions/APU Operating State relationships 554
Figure 21-8 — Operating state sequence examples....556
Figure 21-9 — Typical DTS-initiated packet sequences and APU state transitions 558
Figure 21-10 — Packet combinations used to advance the TAPC state....560
Figure 21-11 — Conceptual view of packet scheduling....563
Figure 21-12 — Example of scheduling and sequencing of state machine activity 565
Figure 21-13 — Advanced operation function/description relationships....566
Figure 22-1 — Conceptual view of a Scan Packet 568
Figure 22-2 — Scan exchange types 571
Figure 22-3 — Voting bit transaction....572
Figure 22-4 — Initiator/Responder bit transaction....572
Figure 22-5 — Scripted scan exchange 572
Figure 22-6 — Conceptual view of a TP....574
Figure 22-7 — TP placement and content 575
Figure 22-8 — APU state diagram 576
Figure 22-9 — Use of the virtual TAPC state 577
Figure 22-10 — Conceptual view of a Scan Packet Element scheduling....578
Figure 23-1 — Deployment of the T4 TAP.7....580
Figure 23-2 — Advanced Scan Format overview 588
Figure 23-3 — TAP.7 data path with positive- and negative-edge clocking....593
Figure 23-4 — The *sys_tck* signal 594
Figure 23-5 — Example of the MScan Scan Format with *sys_tck* signal duty-cycle options 594
Figure 23-6 — *sys_tck* signal logic 1 time 595
Figure 23-7 — Conceptual view of APFC operation 596
Figure 23-8 — SREDGE/tmsc_mux/tmsc_r relationships 597
Figure 23-9 — Conceptual view of *sys_tms* generation for a T4 and above TAP.7....597
Figure 23-10 — Conceptual view of TMS generation with the Advanced Protocol....598
Figure 23-11 — Conceptual view of *sys_tdi* signal generation for a T4 and above TAP.7....600
Figure 23-12 — Conceptual view of System Ready treatment in its simplest form....601
Figure 23-13 — Conceptual *sys_rdy* generation for more complex use cases 602
Figure 23-14 — Conceptual view of TDO data generation for output via the TMSC signal 603
Figure 23-15 — Using the TMSC value in next state equations 606
Figure 24-1 — Application types supported by the MScan Scan Format 608
Figure 24-2 — High-level operation of the MScan Scan Format....608
Figure 24-3 — Scan Packet Elements with the MScan Scan Format 609
Figure 24-4 — MScan payload template....610
Figure 24-5 — MScan payload/EPU input and output relationships....610
Figure 24-6 — MScan output bit-frame 611
Figure 24-7 — MScan output bit-frame with stalled completion....611
Figure 24-8 — Typical TCKC and TMSC signal system delays 612
Figure 24-9 — Use of [RDY] bit(s) to accommodate propagation delays 612
Figure 24-10 — Delay Element format 614
Figure 24-11 — MScan SPs with Delay Elements....615
Figure 24-12 — Type-3 Reset generated by a variable-length Delay Element 616

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Figure 24-13 — MScan SP payload/TAPC state advance relationship....617
Figure 24-14 — CID allocation with MScan SPs....618
Figure 24-15 — Conceptual view of MScan SP Payload Element behavior....620
Figure 24-16 — Conceptual view of the Payload State Machine for the MScan Scan Format....621
Figure 24-17 — Conceptual view of Ready State Machine MScan operation....622
Figure 24-18 — Conceptual Delay Element operation....622
Figure 24-19 — Conceptual view of the Delay State Machine....623
Figure 25-1 — Application types supported by OScan Scan Formats....625
Figure 25-2 — High-level operation of the OScan Scan Formats....626
Figure 25-3 — Scan Packet Elements with the OScan Scan Format....626
Figure 25-4 — OScan payload template....627
Figure 25-5 — Payloads for *Shift-xR* and non-*Shift-xR* TAPC states....628
Figure 25-6 — EPU input/output relationships with an nTDI, TMS, RDY, and TDO SP payload....630
Figure 25-7 — EPU input/output relationships with a TMS SP payload....630
Figure 25-8 — EPU input/output relationships with an nTDI, RDY, and TDO SP payload....631
Figure 25-9 — EPU input/output relationships with an nTDI SP payload....631
Figure 25-10 — EPU input/output relationships with an nTDI/TDO SP payload....632
Figure 25-11 — TMS generation with an EOT Escape....632
Figure 25-12 — OScan6 PAD bit and its function....633
Figure 25-13 — OScan output bit-frame....634
Figure 25-14 — OScan/SScan bit-frame with stalled completion....635
Figure 25-15 — Using delays with the OScan Scan Formats....637
Figure 25-16 — OScan6 SP payload/TAPC state advance relationship....638
Figure 25-17 — Virtual TAPC state with OScan6 Scan Format....639
Figure 25-18 — Example with the *sys_tck* signal duty-cycle options with OScan1....641
Figure 25-19 — Conceptual view of OScan SP Payload Element behavior....642
Figure 25-20 — Conceptual view of Payload State Machine entry point generation....643
Figure 25-21 — Shift Progress flag for OScan6 support....643
Figure 25-22 — CSM and SSM activation....644
Figure 25-23 — Conceptual view of Ready State Machine OScan/SScan operation....644
Figure 25-24 — Conceptual view of TAP advance with MScan/OScan Scan Formats....645
Figure 26-1 — Application types supported by SScan Scan Formats....647
Figure 26-2 — Stall profile/application relationships....650
Figure 26-3 — SScan segment use cases....651
Figure 26-4 — SScan transactions with a TAP.1-like component....652
Figure 26-5 — SScan transactions with a DMA or FIFO....652
Figure 26-6 — SScan transactions with an FIFO....653
Figure 26-7 — SScan transactions with rate-dependent components....653
Figure 26-8 — SScan transactions with a buffered rate-dependent component....654
Figure 26-9 — Stall profile combinations....654
Figure 26-10 — Scan Packet Elements with the SScan Scan Formats....656
Figure 26-11 — Header Element of an SP....657
Figure 26-12 — SP payloads for *Shift-xR* and non-*Shift-xR* TAPC states....659
Figure 26-13 — Segment composition....663
Figure 26-14 — SScan input-only and input/output Data Segment processing....664
Figure 26-15 — SScan0/SScan1 output-only Data Segment processing....667
Figure 26-16 — SScan2/3 output-only Data Segment processing....668
Figure 26-17 — TDO pipelining with the SScan2/SScan3 Scan Formats....669
Figure 26-18 — CLTAP TDO pipelining with SScan2/SScan3 Scan Formats/with stalls....670
Figure 26-19 — Using delays with the SScan Scan Formats....674
Figure 26-20 — Packets following an SP associated with the *Update-DR* and other states....675
Figure 26-21 — Packets following an SP associated with the *Capture-xR/Exit2-xR states*....676
Figure 26-22 — SScan0/1 TAPC state advance examples....678
Figure 26-23 — SScan2/3 TAPC state advance examples for I/O and input-only segments....679
Figure 26-24 — SScan2/3 TAPC state advance examples for output-only segments....680
Figure 26-25 — Conceptual view of the Payload State Machine with Header handling....682

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Figure 26-26 — Conceptual view of the Escape Detection State Machine 684
Figure 26-27 — SScan Shift Progress flag 685
Figure 26-28 — Conceptual view of TAP advance with MScan/OScan/SScan Scan Formats 685
Figure 26-29 — SScan entry point reload additions for output only 686
Figure 26-30 — Conceptual view of Header Register 686
Figure 26-31 — Conceptual view of Payload State Machine entry point with SScan support 687
Figure 26-32 — Joint operation of the state machines 688
Figure 26-33 — Joint operation of state machines with Command Part Two *Update-DR* 688
Figure 27-1 — Conceptual view of T5 TAP.7 Transport Function 690
Figure 27-2 — Deployment of a T5 TAP.7 Controller 691
Figure 27-3 — Conceptual view of T5 TAP.7 Controller configurations 699
Figure 27-4 — TP placement and content 703
Figure 27-5 — Transport Packet Elements 704
Figure 27-6 — TP Directive Elements and their surrounding context 706
Figure 27-7 — Directive/transport building block relationships 707
Figure 27-8 — Summary of Register Element characteristics 715
Figure 27-9 — Summary of Data Element characteristics 718
Figure 27-10 — Selection mechanisms for data and register transfers 720
Figure 27-11 — Operation of the DCCy_ENAR and DCCy_ENAA register bits 720
Figure 27-12 — Operation of the DCCy_DCNR and DCCy_DRNA register bits 721
Figure 27-13 — Conceptual view of T5 TAP.7 transport control 723
Figure 27-14 — Conceptual view of transport control facilitating a data exchange 724
Figure 28-1 — *TPA* state behaviors 728
Figure 28-2 — *TPA* state flow 729
Figure 28-3 — TP Directive Element format, timing, and TMSC signal drive characteristics 730
Figure 28-4 — A Type-3 Reset generated by the TP_RSZ and TP_RSO Directives 730
Figure 28-5 — TP Register Element format, timing, and TMSC signal drive characteristics 731
Figure 28-6 — Register Element with surrounding TP Directives 732
Figure 28-7 — TP Data Element format, timing, and TMSC signal drive characteristics 735
Figure 28-8 — Fixed-length Data Payload with surrounding TP Directives 735
Figure 28-9 — Variable-length Data Payload with surrounding headers 736
Figure 28-10 — DCCy_DIRA Register/Data Payload content relationships 737
Figure 28-11 — Data payload and data channel data alignment relationship 738
Figure 28-12 — Conceptual view of the Transport State Machine 740
Figure 28-13 — Queuing a TP to follow an SP 742
Figure 28-14 — Queuing a TP to follow an SP with the OScan2 Scan Format 743
Figure 28-15 — Queuing a TP to follow an SP with the OScan1 Scan Format 744
Figure 28-16 — Starting directive processing/ending TP processing 745
Figure 28-17 — PDCx/DCC interface signals with a single DCC connected to the DCC 746
Figure 28-18 — PDCx/DCC interface signals with multiple DCCs sharing the PDC 747
Figure 28-19 — Conceptual view of T5 TAP.7 Transport Control 750
Figure 28-20 — PDCx/DCC interface signaling/TP_NOP and TP_END Directives 754
Figure 28-21 — DCC interface signaling/TP_DCx Directives 755
Figure 28-22 — PDCx/DCC interface signaling/nonterminating eight-bit directives 756
Figure 28-23 — PDCx/DCC interface signaling/TP_RSO and TP_RSZ Directives 757
Figure 28-24 — PDCx/DCC interface signaling/12-bit directives other than TP_CRR/TP_CRW 758
Figure 28-25 — PDCx/DCC interface signaling with the TP_CRR Directive 759
Figure 28-26 — PDCx/DCC interface signaling with the TP_CRW Directive 760
Figure 28-27 — DCC interface signaling required for Custom Operation 761
Figure 28-28 — Pipelining data transfers 761
Figure 28-29 — Conceptual view of the Transport Function 762
Figure 28-30 — Example Transport State Machine 763
Figure 28-31 — Behavior of the *next_dir* signal 764
Figure 28-32 — Multi-use register bit input configurations 765
Figure 28-33 — Multi-use Register values/TSM relationships 767
Figure 28-34 — Transport drive and DCR input selection 771

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022

Figure 28-35 — TP with fixed-length data transfer with nonpipelined scan operations 773
Figure 28-36 — TP with fixed-length data transfer with pipelined scan operations 774
Figure 28-37 — TP with continuous data transfer 775
Figure 28-38 — TP with no data transferred 776
Figure 29-1 — Typical test application – testing component interconnections 779
Figure 29-2 — Unit-under-test description 784
Figure 31-1 — Serial connection using one TMS signal 822
Figure 31-2 — Connection in two paralleled serial chains 824
Figure 31-3 — Basic Star Scan Topology 825
Figure 31-4 — Basic hierarchical topology 826
Figure A-1 — IEEE 1149.1 TAPC State Machine 830
Figure A-2 — IEEE 1149.1 signaling 831
Figure A-3 — Zero-bit DR Scan state sequences, path A 832
Figure A-4 — Zero-bit DR Scan state sequences, path B 833
Figure B-1 — MScan and OScan SP content 834
Figure B-2 — MScan transaction 836
Figure B-3 — OScan0 transaction 837
Figure B-4 — OScan1 transaction 838
Figure B-5 — OScan2 transaction 839
Figure B-6 — OScan3 transaction 840
Figure B-7 — Oscan4 transaction 841
Figure B-8 — OScan5 transaction 842
Figure B-9 — OScan6 transaction 844
Figure B-10 — OScan7 transaction 845
Figure B-11 — SScan0 transaction/first SP stall profile 848
Figure B-12 — SScan0 transaction/all stall profile 849
Figure B-13 — SScan1 transaction/first SP stall profile 851
Figure B-14 — SScan1 transaction/no stall profile 852
Figure B-15 — SScan2 transaction/first SP stall profile 854
Figure B-16 — SScan2 transaction/all stall profile 855
Figure B-17 — SScan3 transaction/first stall profile 857
Figure B-18 — SScan3 transaction/no stall profile 858
Figure B-19 — OScan1 Scan Format/TPs with fixed-length Data Element following SPs 859
Figure B-20 — OScan7 Scan Format/TPs with fixed-length Data Element following SPs 859
Figure B-21 — OScan1 Scan Format/TPs with variable-length Data Element following SPs 860
Figure B-22 — OScan7 Scan Format/TPs with variable-length Data Element following SPs 860
Figure D-1 — Power-control states 905
Figure D-2 — Consolidated view of CSM states 906
Figure D-3 — TAP initialization and topology determination 908
Figure D-4 — TS initialization 910
Figure D-5 — Scan Topology Training 915
Figure D-6 — Branch interrogation 916
Figure D-7 — Series Branch interrogation 919
Figure D-8 — Reads of CNFG0–CNFG3 Registers in a Series Scan Topology 920
Figure D-9 — Determining the type/class of series TAPs 922
Figure D-10 — Star-4 Branch interrogation—part one 924
Figure D-11 — Star-4 Branch interrogation—part two 925
Figure D-12 — Star-2 Branch interrogation—part one 927
Figure D-13 — Star-2 Branch interrogation—part two 928
Figure E-1 — Electrical characteristics 932
Figure F-1 — Typical TCK(C) frequency versus number of TAPs 935
Figure F-2 — Connection topologies 936
Figure F-3 — Series termination scheme 937
Figure F-4 — Parallel termination schemes 937
Figure F-5 — The use of input buffers with hysteresis 938
Figure F-6 — Signal filtering using a one shot 938

Copyright © 2022 IEEE. All rights reserved.

Documents
Document Sharing Hub

Authorized licensed use limited to: Tsinghua University. Downloaded on February 24,2026 at 10:47:46 UTC from IEEE Xplore. Restrictions apply.

Full document details: IEEE 1149.7-2022