

IEEE Standard for Boundary-Scan-Based Stimulus of Interconnections to Passive and/or Active Components

IEEE Computer Society

Sponsored by the
Test Technology Committee

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IEEE Standard for Boundary-Scan-Based Stimulus of Interconnections to Passive and/or Active Components

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Test Technology Committee
of the
IEEE Computer Society

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Abstract: Extensions to IEEE Std 1149.1™ that define the boundary-scan structures and methods required to facilitate boundary-scan-based stimulus of interconnections to passive and/or active components are specified. Such networks are not adequately addressed by existing standards, including those networks that are ac-coupled or differential. The selective ac stimulus generation enabled by this standard, when combined with non-contact signal sensing, will allow testing of the connections between devices adhering to this standard and circuit elements such as series components, sockets, connectors, and integrated circuits (ICs) that do not implement IEEE Std 1149.1. This standard also specifies Boundary-Scan Description Language (BSDL) extensions to IEEE Std 1149.1 required to describe and support the new structures and methods.

Keywords: boundary scan, Boundary-Scan Description Language, BSDL, IC, IEEE 1149.8.1, integrated circuit, loaded board testing, manufacturing defects

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Introduction

This introduction is not part of IEEE Std 1149.8.1-2012, IEEE Standard for Boundary-Scan-Based Stimulus of Interconnections to Passive and/or Active Components.

This standard defines specific modifications and capabilities that can be added to integrated circuit devices that also conform to IEEE Std 1149.1.^a This allows them to support tests on other devices, which may be active or passive, to determine if there are manufacturing defects (shorts or opens) in the interconnections between them.

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^a Information on references can be found in Clause 2.

Contents

1. Overview	1
1.1 Scope	1
1.2 Purpose	1
1.3 Context	2
1.4 Organization of the standard.....	3
2. Normative references.....	3
3. Definitions	4
4. Technology	6
4.1 Evolution of printed circuit assembly technology	6
4.2 Shifts in board testing challenges	6
4.3 Signal pin types	7
4.4 Defects targeted by the standard.....	12
4.5 Selective toggle theory of operation	15
5. Instructions	21
5.1 IEEE Std 1149.1 instructions.....	21
5.2 Additional instructions added by this standard.....	22
5.3 TOGGLE_SETUP instruction	22
5.4 SELECTIVE_TOGGLE instruction.....	23
6. Pin implementation specifications.....	25
6.1 Pin classification.....	25
6.2 Implementation of normal pins.....	26
6.3 Implementation of ST-pins.....	28
6.4 Toggle behavior for ST-pins.....	47
7. Toggle_Control register.....	49
7.1 Rules	50
7.2 Permissions.....	50
7.3 Recommendations	50
7.4 Description	51
8. Conformance and documentation requirements	54
8.1 Conformance	54
8.2 Documentation.....	55
8.3 BSDL package for Selective Toggle description (STD_1149_8_1_2012).....	56
8.4 BSDL extension structure.....	58
8.5 BSDL attribute definitions.....	59
8.6 Example BSDL.....	63
Annex A (informative) Unpowered testing for open connections on printed circuit assemblies	73
Annex B (informative) Boundary register cells that support ST-pins and IEEE 1149.6 ac-pins.....	80
Annex C (informative) Bibliography.....	82

IEEE Standard for Boundary-Scan-Based Stimulus of Interconnections to Passive and/or Active Components

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1. Overview

1.1 Scope

This standard specifies extensions to IEEE Std 1149.1™ that define the boundary-scan structures and methods required to facilitate boundary-scan-based stimulus of interconnections to passive and/or active components.¹ Such networks are not adequately addressed by existing standards, including those networks that are ac-coupled or differential. The selective ac stimulus generation enabled by this standard, when combined with non-contact signal sensing, will allow testing of the connections between devices adhering to this standard and circuit elements such as series components, sockets, connectors, and integrated circuits (ICs) that do not implement IEEE Std 1149.1. This standard also specifies Boundary-Scan Description Language (BSDL) extensions to IEEE Std 1149.1 required to describe and support the new structures and methods.

1.2 Purpose

The purpose of this standard is to codify testability circuitry added to an IC incremental to the testability provisions specified by IEEE Std 1149.1. This will enable selective ac stimulus generation that, when

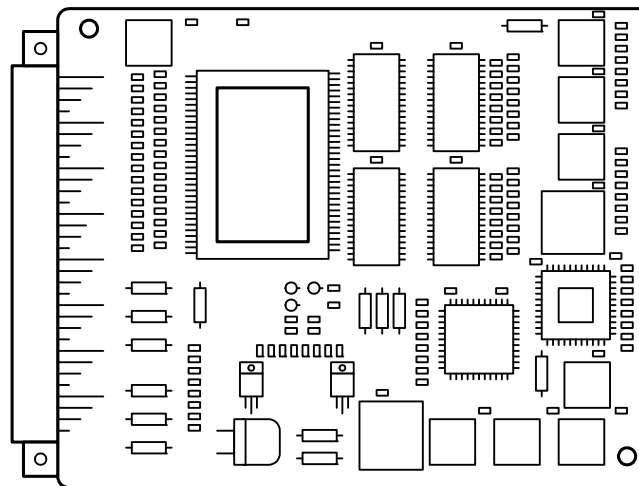
¹ Information on references can be found in Clause 2.

combined with non-contact signal sensing, allows testing signal paths between devices adhering to this standard and passive and/or active components.

1.3 Context

Figure 1 shows a printed circuit assembly (PCA) containing many types of devices. Of these, some could be compliant with IEEE Std 1149.1 for the support of testing activities. These devices contain boundary-scan testability circuitry that allows them to participate in manufacturing tests that detect and diagnose faults such as open solder joints, shorts, and missing devices.

The additional testability elements added by this standard to these same ICs allow this interconnect testing, to be extended, to include interconnections between these ICs and passive or active components that do not support IEEE Std 1149.1, when these testability elements are operated in conjunction with auxiliary sensing technologies.



Source: IEEE Std 1149.6-2003

Figure 1—A printed circuit assembly containing a variety of components interconnected by printed wiring—some ICs contain IEEE 1149.1 features that support boundary-scan interconnect testing

This standard is built on top of IEEE Std 1149.1 using the same test access port (TAP) and boundary-scan architecture. It adds new instructions that cause drivers to emit ac waveforms that are compatible with auxiliary sensing technologies.

There are two audiences addressed by this document. The first is made up of IC device designers (device designers) and the second is a more general class of IC device users (device users). Device designers will use this standard while creating new devices that adhere to the rules of this standard. Device users will make use of those features. Device users include board and system designers, design-for-test consultants, and test engineers. In many cases, it is expected that there will be communication and negotiation between the two groups, as the device users will lobby for investments in the silicon made by device designers who will balance these requests against various factors (schedule, cost) and trade those off for enhanced testability and defect coverage.

1.4 Organization of the standard

Clause 1 provides an overview and context for this standard.

Clause 2 provides references necessary to understand this standard.

Clause 3 defines terminology and acronyms used in this standard.

Clause 4 is a tutorial that outlines the technologies addressed and utilized by this standard. This clause does not contain rules.

Clause 5 provides rules for instructions used for testing.

Clause 6 provides rules for input/output (I/O) pin implementation.

Clause 7 provides rules for the design and behavior of a Toggle_Control register used to control the operation of the SELECTIVE_TOGGLE instruction.

Clause 8 provides rules for conformance and documentation of devices designed to this standard. An extension to the BSDL language for machine-readable description of implementations of this standard is provided.

Annex A describes a capacitively sensed test technology for testing for open connections between printed circuit assemblies and device pins.

Annex B describes boundary register cell designs that support both the requirements of ST-pins and ac-pins as defined by IEEE Std 1149.6.

Annex C gives background reading for testing with IEEE Std 1149.1 and for unpowered capacitive opens testing.

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1149.1TM, IEEE Standard Test Access Port and Boundary-Scan Architecture.^{2, 3}

IEEE Std 1149.6TM, IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks.

NOTE—IEEE Std 1149.6 is important for those devices that are intended to implement the rules of this standard alongside the rules of IEEE Std 1149.6. IEEE Std 1149.1 is the foundation for both IEEE Std 1149.6 and this standard.⁴

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⁴ Notes in text, tables, and figures of a standard are given for information only and do not contain requirements needed to implement this standard.

3. Definitions

For the purposes of this document, the following terms and definitions apply. The *IEEE Standards Dictionary Online* should be consulted for terms not defined in this clause.⁵

ac pins: Advanced input/output (I/O) pins that require a time-varying (ac or alternating current) signal to permit testing of their interconnections. This includes all differential signal pins and differential or single-ended signal pins that are expected by design to support ac-coupling. (From IEEE Std 1149.6.)

balanced differential pins: The outputs of a differential driver (negative and positive legs) that have complementary and symmetrical behavior, such that the sum of the voltages on the two pins at any time is constant. This is the normal behavior for differential pins. *Contrast:* **unbalanced differential pins.**

bed-of-nails: A test fixture that contains many spring-loaded probes positioned to contact conductive targets on the surface of a printed circuit assembly (PCA). Each probe is mapped via fixture wiring to one or more tester resources provided in a regular array below the fixture.

capacitive opens test: An (unpowered) test technology where printed circuit board (PCB) nets are grounded, with one stimulated with a small ac voltage. This net stimulates a pin under a device (such as an IC, vacant connector, or socket). A capacitive sense plate assembly, positioned over the device (but not inserted into a receiving device such as a connector or socket) picks up the signal and buffers it. The buffered signal is interpreted. If the connection between the board net and the device pin is sound, then a stronger signal is sensed than if the connection has an open *defect*, which gives an attenuated signal.

defect: An *unacceptable* deviation from a norm. A defect requires action that may include repairing the defect or discarding the assembly containing the defect. This justifies investment in tests and diagnostic procedures aimed at discovering and eliminating defects. Examples of manufacturing defects on *printed circuit assemblies* are: missing solder causing open connections, bridging solder causing shorts, missing components, incorrect components, dead or faulty components, components that are misaligned, etc.

device: An integrated circuit (IC) device, also referred to as a “component” that is the target of this standard. In the context of describing *printed circuit assemblies*, devices may also include other component types such as resistors, capacitors, connectors, etc.

device designer: The person(s) responsible for implementing circuitry within an integrated circuit (IC) device, and who make trade-off decisions for circuit features, performance levels, cost, and producibility. Device designers are charged with making additional trade-offs in their designs that affect the producibility of subsequent levels of product hierarchy, such as *printed circuit assemblies* and systems.

device user: Persons who utilize integrated circuits (ICs) provided by *device designers*. These include *printed circuit assembly* and system designers, as well as testability consultants and test engineers. Device users will provide information to inform trade-off decisions made by device designers.

differential pins: A pair of input or output pins that is complementarily dependent in function mode. For example, the (ideal, noise-free) voltage waveforms seen during data passage are mirror images of each other. *Contrast:* **single-ended pins.** *See also:* **balanced differential pins.**

loaded board test: A set of tests performed on *printed circuit assemblies* that determine if the printed circuit assembly (PCA) has been constructed properly and does not contain defects.

⁵IEEE Standards Dictionary Online subscription is available at
http://www.ieee.org/portal/innovate/products/standard/standards_dictionary.html.

normal pins: Device system pins defined as those that will not be provisioned with the *selective toggle* capability. *Contrast:* **ST-pins**.

NOTE—The concept of “system pin” is defined by IEEE Std 1149.1.

opens: A **defect** condition that breaks an intended electrical connection. Typically this may occur when an electrical device on a *printed circuit assembly* (PCA) has a missing or broken connection, for example, a missing ball joint in a ball grid array, a pin with missing solder, a pin that has been bent or broken off of its device, or a device defect such as a missing bond wire.

printed circuit assembly (PCA): A *printed circuit board* (PCB) that has had circuit components attached to it such that those components can receive and/or transmit signals among their connections.

printed circuit board (PCB): A substrate containing embedded wiring and metallic planar structures. A PCB serves as a mounting substrate for numerous electrical devices, with the embedded wiring forming interconnections between device pins. Without those devices, the PCB is a “bare board” and after they are installed, it is a “loaded board.”

process-voltage-temperature (PVT) variability: Variability in analog performance characteristics that are due to the physical implementation of an integrated circuit (IC) device and environmental factors. These are fabrication process variations, variations due to tolerance in the supply voltage(s), and variations due to the operating temperature of the device. Note that some devices may be expressly designed to operate from several different power supply voltages. This type of variability is outside of the PVT set of variations.

selective toggle: The name of the principal feature enabled by this standard; the ability to selectively cause some pins to toggle output drive states while others remain at pre-assigned static output drive levels.

single-ended pin: An input or output pin that is not part of a pin pair but is an independent path for information. *Contrast:* **differential pins**.

ST-pins: Device, system pins defined as those in need of the *selective toggle* capability defined by this standard and requiring an output drive capability. *Contrast:* **normal pins**.

NOTE—The concept of “system pin” is defined by IEEE Std 1149.1.

test pad: A conductive target on the surface of a *printed circuit assembly* (PCA) that can be contacted by a test probe in a *bed-of-nails* fixture. This provides electrical access to a circuit node that can be used for testing.

toggle: A single transition of a signal from one stable state (of two possible states) to a second stable state.

unbalance bit: A bit that determines “balanced/unbalanced” behavior of differential pin drivers. It is stored in an *unbalance cell* in the boundary register.

unbalance cell: A cell in the boundary register used to select the “balanced/unbalanced” behavior of one or more differential pin drivers. *Balanced* behavior means a differential driver has both legs operating in completely complementary fashion as would be their normal system function. *Unbalanced* behavior means they are no longer complementary. *See:* **balanced differential pins; unbalanced differential pins**.

unbalanced differential pins: The outputs of a differential driver (negative and positive legs) that, under the influence of features defined by this standard, IEEE Std 1149.8.1-2012, have a non-complementary and asymmetrical behavior, such that the sum of the voltages on the two pins is not constant, but rather meets a minimum voltage change requirement. *Contrast:* **balanced differential pins**.

unpowered opens test: A test for **open** pin connections between a *printed circuit assembly* (PCA) and device pins that does not require the assembly to have power applied to support the test.

4. Technology

4.1 Evolution of printed circuit assembly technology

It is the nature of the electronics industry to undergo large technological change on a regular basis. The driving force for these changes can be traced mainly to Moore's Law that observes that ICs double in density periodically, typically every 18 months. This has both increased the capabilities of products while driving down their costs. For printed circuit assemblies, change has manifested itself in several ways.

- IC packages have become physically smaller while pin counts have risen dramatically. This leads to concomitant increases in board layout density. Other devices (for example, termination resistors) have also decreased in size to match up better with the decreasing dimensions in board layouts. Increased layout density may lead to increased board layer counts in order to pack more interconnects into smaller areas.
- IC operating frequencies have risen dramatically. This leads to the need for controlled impedance board layout technology. Controlled impedance layout rules are much stricter and will sometimes lead to increases in board layer counts as intervening layers may need ground planes between them. As a result, board layouts may contain more interconnect on inner layers that are not visible at the surface layers, and layout rules may not permit the application of standard test pads to surface traces.
- While densities and operating frequencies have risen adding complexity to designing and manufacturing printed circuit assemblies, there has been contrary pressure to lower the cost of these assemblies, even though the scaling effects of Moore's Law have not been as accessible to board technology beyond the IC level.⁶ For testing printed circuit assemblies, this has translated into doing far more testing over time, but with pressure for an overall reduction in cost.

High level architecture has also played a role. For example, many product categories consist of multi-board implementations. These boards are connected directly to each other (or via backplanes) in the final product, but during individual board test, there may be vacant connectors that do not have mating boards attached. Global manufacturing, customs, and tax laws also create conditions where boards are manufactured and tested while certain components (typically large, costly components) are missing. Such components are thus socketed so that they can be added later. Thus, vacant sockets become a test problem—how can they be tested for proper assembly and attachment?

4.2 Shifts in board testing challenges

These evolutionary trends create board test issues and can be categorized as density-driven or architecture-driven. Density-driven problems come from growing difficulty in physically accessing specific points within a board for test purposes. Access limitations have been predicted for over 20 years and some design-for-testability technologies such as IEEE 1149.1 boundary scan have been developed and adopted to varying degrees across the electronics industry. However, adopting boundary scan has a lesser effect on solving architecturally driven problems; for example, large amounts of interconnect that cannot be tested in traditional ways even when boundary scan is available to counteract declining access. A major example of this problem is when boundary-scan devices are connected to non-boundary-scan devices such as passive devices like connectors or sockets. While boundary scan can test interconnections between compliant

⁶ Gains provided by Moore's Law, it is argued, should not be dissipated at the board and system levels.

devices, it was not specifically intended to test interconnections to devices that cannot cooperate via that standard.⁷

In the middle of the 1990s, a novel test technology was invented that quickly became widely adopted, known generically as unpowered capacitive opens testing. This technology is described in Annex A, where Clause A.1 and Clause A.2 describe a test coverage problem, and a solution presented by unpowered capacitive opens testing. Clause A.3 then discusses how this test technique, originally developed for boards where significant physical access is possible, can be updated by using boundary scan to provide test stimulus where physical access is no longer possible. Note that the “unpowered” property is eliminated when boundary scan is utilized. While boundary scan can indeed provide some relief, there are some significant defect coverage deficiencies, described in Clause A.4, that remain. In essence, IEEE Std 1149.1 does not provide enough capability to adequately solve this problem. New capabilities added to boundary scan that can provide a solution are the subject of this standard and are provided in following clauses.

4.3 Signal pin types

4.3.1 Classification of pins

When implementing this standard, a device designer should take note of the intended use of a device and then categorize the system signal pins as “normal” or in need of “selective toggle” functionality. This standard will refer to these categories as normal pins and as “ST-pins.” The normal pins will be implemented in full compliance with IEEE Std 1149.1. The ST-pins will also have full compliance with IEEE Std 1149.1, but will respond to a new testing instruction provided by this standard. ST-pins will have more capability in the following significant ways:

- All pins identified as ST-pins that would normally be implemented as input-only pins will be given drive capability as well. This effectively converts them to bidirectional pins, and they shall be provisioned with boundary-scan capabilities per IEEE Std 1149.1 rules for bidirectional pins. The system behavior of these drivers could be logically disabled, with the test mode behavior controlled by a boundary register control cell.
- Single-ended output pins identified as ST-pins may optionally be provided with self-monitoring observe capability, per option 2) of rule a) in 11.6.1 in IEEE Std 1149.1-2001. The threshold used to determine the logic level should not be close to the level that two adjacent drivers might reach when they are at opposite states and shorted together. The self-monitoring feature is intended for use with EXTEST to detect shorts to other driven pins.
- Differential output pins identified as ST-pins may optionally be provided with self-monitoring observe capability. The self-monitoring feature is intended for use with EXTEST to detect shorts to other driven pins and between the pins of the differential pair.
- All pins identified as ST-pins will be provided with new toggle drive functionality under the control of new testing instructions provided by this standard.
- Differential drivers will have an “unbalancing” feature added so that the two normally complementary legs can exhibit non-complementary waveforms while under the control of new instructions provided by this standard. Because of this, both pins of a differential pair (never just one) are classified either as normal or as ST-pins. The unbalancing feature is turned on or off by the content of an added cell (at least one) in the boundary register.

⁷ Note that conventional digital ICs may be tested with boundary-scan resources that exist in surrounding compliant devices, if enough of those resources exist to support such a test, and any timing requirements of the test can be honored by such an approach.

Normal pins will perform as if **EXTEST** has been loaded when the new testing instruction provided by this standard is in effect. More descriptive detail about normal and ST-pin behavior is found in 4.5.2 and normative rules are found in Clause 6.

The decision on pin classification is made with respect to the anticipated board architecture that a device is intended to reside within, and to the goals required for adequate test coverage for the board architecture. The principle example of board test technology is described in Annex A, but others exist or may be developed as a result of the capabilities offered by this standard. An example of a board architecture that would require pin classification is shown in Figure 2. In this example, device U1 will be given a boundary-scan capability, but is also being considered for compliance to this standard.

The signal pins of U1 are circled and labeled as normal (circled with dotted line) or ST-pins (circled with dashed lines). The decision is based on whether boundary scan can test the interconnections to other devices. The interconnections between U1 and both U2 and U3 are fully provisioned with IEEE Std 1149.1 in all these devices. Those pins of U1 that connect to U2 and U3 are classified as normal. However the interconnect between U1 and the socket S1 and the connectors C1, C2 and C3 are untestable for open connections, since all of the devices S1, C1–C3 will be vacant during test. The pins involved here are classified as ST-pins as devices S1, C1–C3 are incapable, by themselves, in participating in a boundary-scan test. The test strategy is to use a capacitive opens test to supply coverage for these device interconnects. Note that U1 will need additional drive capability (bidirectional) on those ST-pin signals that propagate to U1 from a socket or connector (circled with solid bold lines). This has the added benefit that the functional inputs, since they are to be provisioned with bidirectional capability, can be tested with boundary-scan tests for shorts.

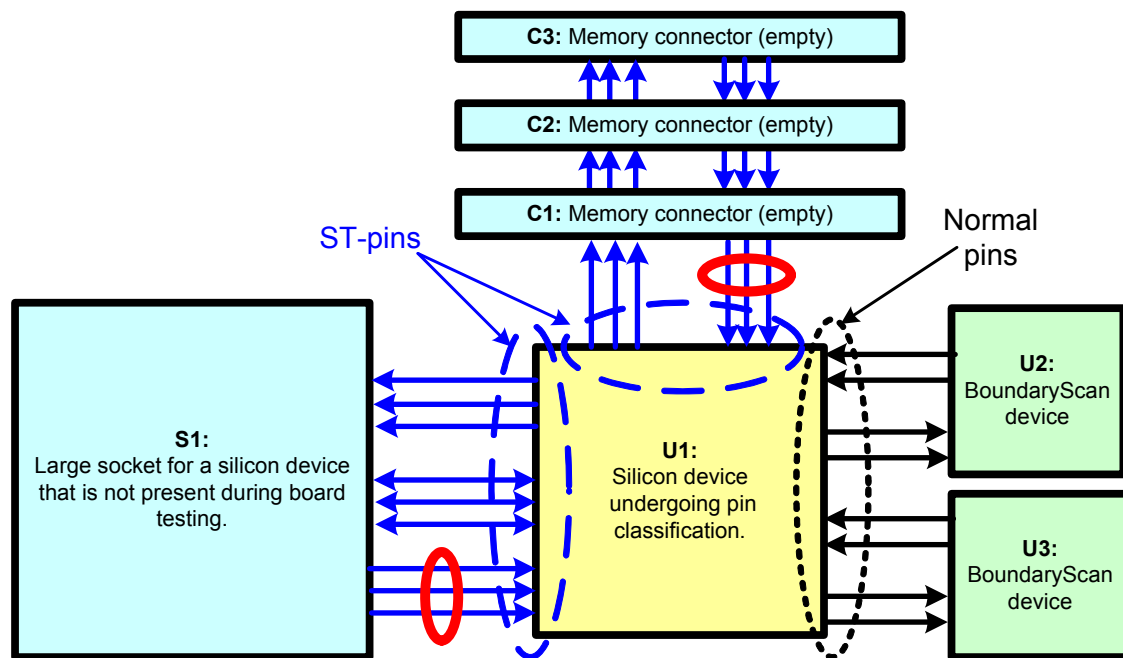


Figure 2—Board architecture determining pin classification.

So the device designer, utilizing information about board architecture and test coverage needs, will categorize device pins into “normal pin” and “ST-pin” types at the outset of implementing this standard. The device designer may also incorporate scheduling, technology, and economic factors into the decision, trading off defect coverage.

4.3.2 Differential pins

A specific requirement for this standard is that differential drivers of ST-pins have two modes of operation: *balanced* and *unbalanced*. It is instructive to look at a “typical” differential driver circuit and its normal (balanced) behavior. A simplified circuit is shown in Figure 3. This circuit is a steering network for a current source I_S and a termination R_S . When data “0” is applied, two of the four *field effect transistors* (FETs) turn on, steering the current I_0 in one direction through R_S . When a data “1” is applied the opposite FETs turn on (while the original FETs turn off), reversing the current I_1 in R_S . Since the magnitudes of $I_S = I_0 = I_1$, this means the voltage difference across R_S will switch so that the voltage difference changes sign, but otherwise has the identical value for either polarity of data. A downstream differential receiver will ignore voltage offsets and respond only to the voltage difference. The net effect is the two leg voltage waveforms will appear to be nearly perfectly symmetric to each other centered at some offset voltage.

The capacitive opens test technique (see Annex A) depends on a signal being capacitively coupled into a sense plate. If the signals Pos and Neg in Figure 3 are coupled to a sense plate with approximately equal capacitance, then, being symmetric they will cancel and the sense plate will see no net signal. To get an observable signal at the sense plate, the legs of the differential amplifier, under control of a specific condition set up by this standard, are made different, or unbalanced with respect to its complementary signal.

One way to do this is to “modulate” the current source I_S . The amount of current produced by the current source determines the voltages seen at the outputs Pos and Neg. The two waveform charts in Figure 3 show the voltages at Pos and Neg when I_S is set to 6 mA and 12 mA. The voltage swing at the pins changes by a factor of 2, and there is an offset change that is a function of the voltage drops across the FETs.

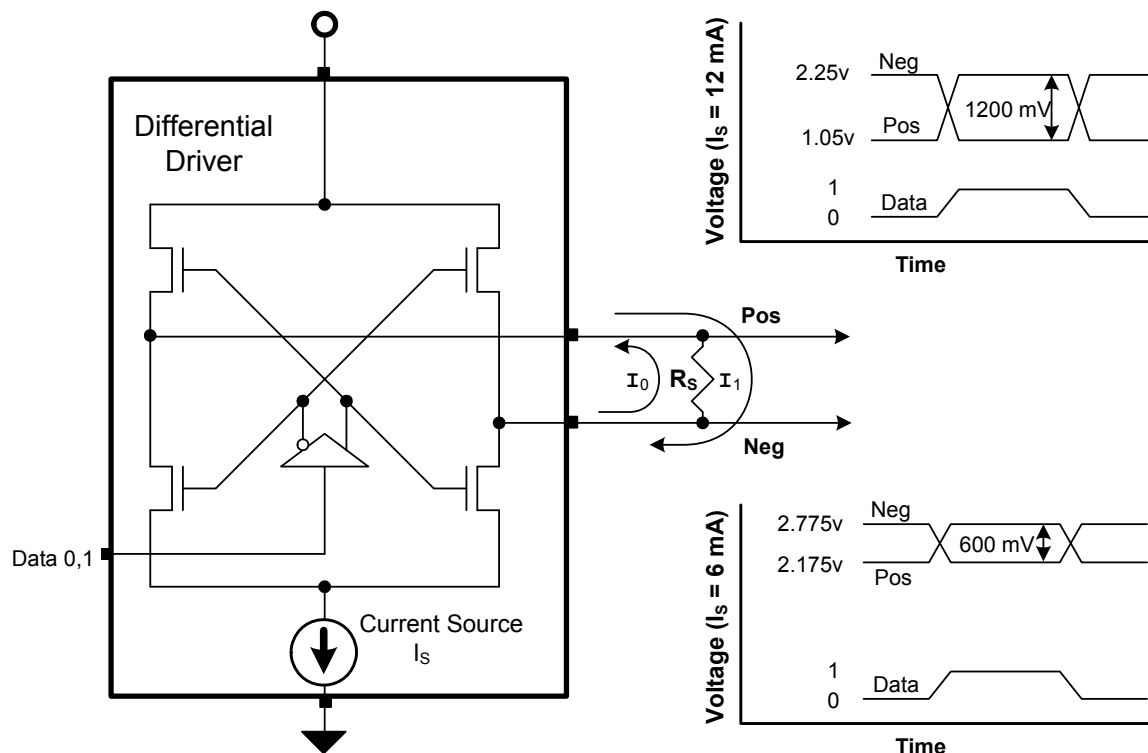


Figure 3—Simplified schematic for a differential driver

By adding a control signal to the current source, it can switch between two levels of current. This allows controlled unbalancing. During “unbalanced” testing the Data signal would be held constant while the current control signal would be toggled, producing waveforms on the two legs, as seen in Figure 4. There is action on both legs, but both legs are now in phase instead of being perfectly symmetrical. Thus a defect-free pair of legs will now generate a visible signal in a sense plate rather than the null signal seen before, due to cancellation by symmetry. However, setting Data to “0” or “1” causes one of the two pins to have somewhat more swing than the other, but, since the measurement of capacitance (at the sense plate) is largely independent of signal amplitude, two pins’ worth of capacitance would be measured in either case. This means this scheme could detect one pin being open, but not allow reliable indication which of the two was open. If both were open, then no signal would be detected, indicating both pins were open.

NOTE—The example in Figure 4 produces unbalanced behavior when the Data line is held constant at either level while toggling the Current_Select signal. This particular example shows no difference, but depending on implementation, the amount of toggling (in terms of the sum of the two voltages seen at the legs) may be more for one constant value on Data versus the other. Because these summed voltage swings are what are being sensed, a larger swing is generally desired. Thus, when there is a choice, the value that maximizes the summed voltage swing should be implemented.

Detecting open defects on the two pins thus requires the balanced and unbalanced modes of operation. The unbalanced mode is used to produce a signal at the sense plate when no defects are present. This is useful for calibrating the operation of the sense plate and the measurement technology used to determine capacitance. The unbalanced mode also will detect the case where both pins are open simultaneously. The balanced mode is then used to determine if either pin is open by itself. In this case, a strong signal will be sensed, and its phase will indicate the leg of the differential pair that is open. Defect detection of these modes is summarized in Table 1.

Table 1—Differential operational modes and defects detected

Defect	Unbalanced mode	Balanced mode	Comment
None	Signal sensed	No signal sensed	Use unbalanced mode for calibration of a known-good device-under-test (DUT)
Open in positive leg	Signal may be sensed	Negative signal sensed, defect detected	The balanced mode is best for detecting this open
Open in negative leg	Signal may be sensed	Positive signal sensed, defect detected	The balanced mode is best for detecting this open
Both legs open	No signal sensed, defect detected	No signal sensed	The unbalanced mode is best for detecting a pair of opens

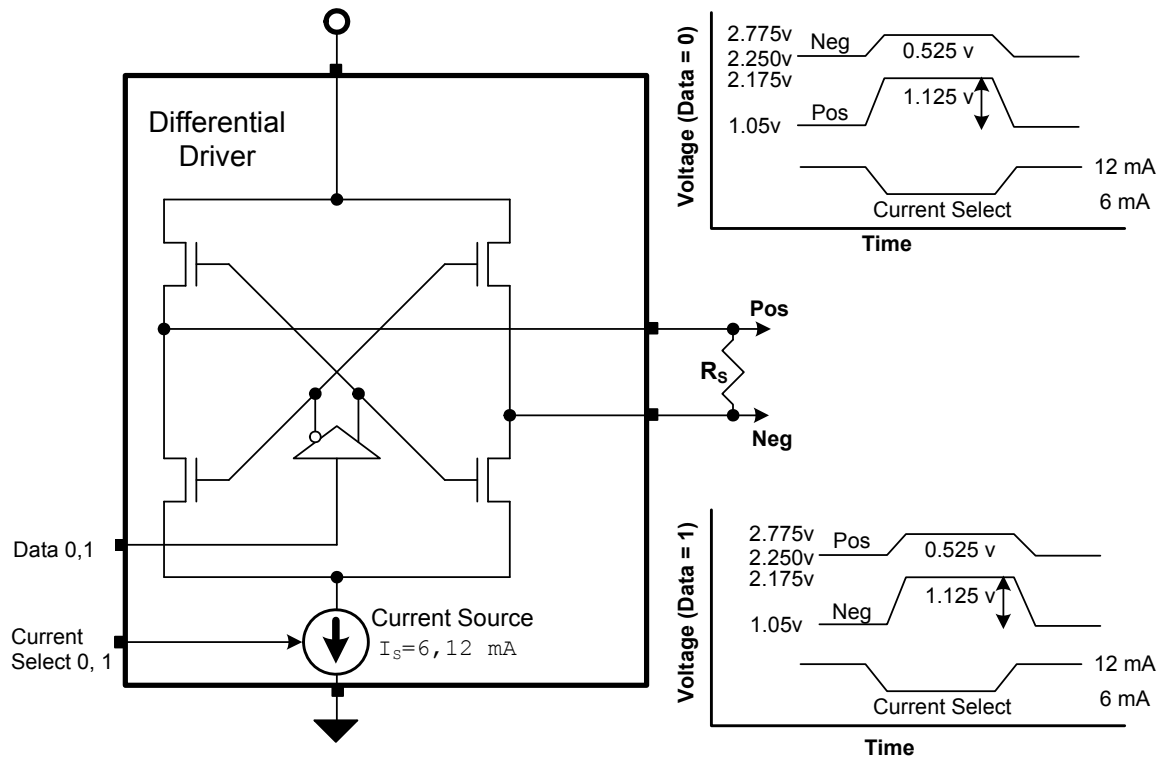


Figure 4—Driver with a controllable dual-current source

Both Figure 3 and Figure 4 show a source termination resistance R_S that provides a path for the current flow. R_S could be implemented within the IC or be provided as part of external circuitry. If R_S is part of the external circuitry, this path may not exist. For example, the path could be broken due to an open defect at a device pin, or, because the termination is located on a plug-in assembly that will not be present during testing. (The device itself is assumed to be defect-free, meaning the current path would not be interrupted on-chip.) In the first case a defect causes the open path where in the second, a defect-free path will not pass current.

The current sources in Figure 3 and Figure 4 could be implemented as shown in Figure 5. (Note the selectable current source implementation shown is one of several that are possible.)

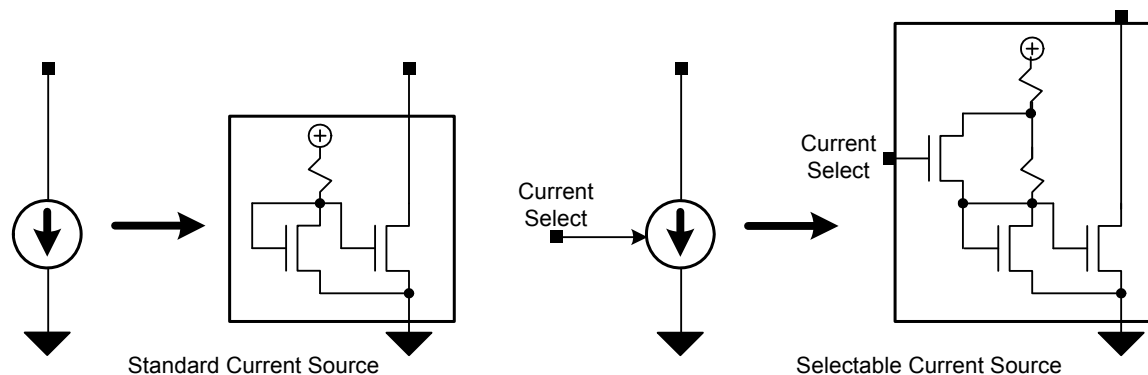


Figure 5—Current source implementations

The previous discussion of a modulated current source to provide unbalancing is one way the unbalanced effect could be implemented. There are others, including (but not limited to) the following possibilities:

- a) Both legs toggle in the same direction (as demonstrated by the modulated current source)
- b) One leg toggles in one direction while the other is held at a fixed dc level
- c) One leg toggles in one direction while the other is in a high impedance state
- d) One leg toggles in one direction while the other toggles in the opposite direction, but with a different magnitude of voltage swing

The key is that when unbalanced, the sum of the voltages on the two legs is not constant, but meets the requirements given in Clause 6.

The transition between the two modes could produce odd waveforms on the driver legs, as shown in Figure 6.

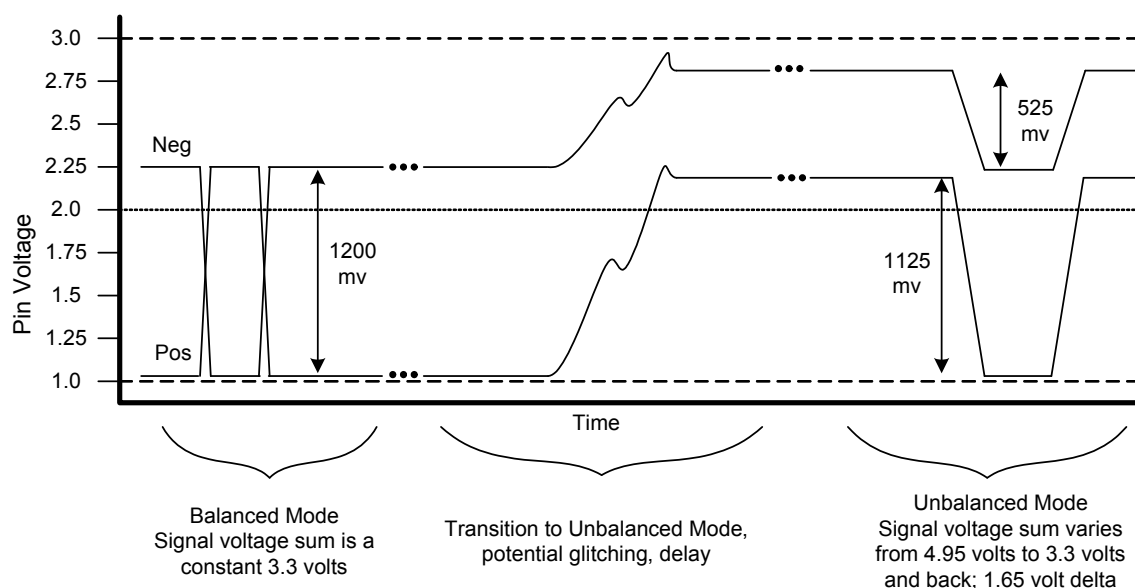


Figure 6—The transition between balanced and unbalanced modes may require delay

The transition will likely be very quick, compared to some small number of test clock (TCK) periods, but the behavior of the two legs is not specified during this transition time to allow maximum flexibility for the device designer. Thus, this transitional behavior cannot be used as part of test, but should instead be avoided and allowed to settle out. Creators of testing software should first be aware of how the capacitive sensing part of their test system may respond to transitional behavior and how long it takes for that response to dissipate. Second, they should take note of the time expected between the transition event and when the subsequent test stimulus they are preparing will occur. This time should exceed the settling time of the sensing system.

4.4 Defects targeted by the standard

This standard (together with IEEE Std 1149.1) provides test support for detecting “manufacturing process defects” that are found on printed circuit boards (PCBs) coming out of the manufacturing process. These

defects include missing devices (ICs, resistors, capacitors, etc.), improperly mounted devices (e.g., rotated 180 degrees), open solder joints, shorted solder joints, misaligned and dead devices. This standard focuses on those defects within the interconnections between devices that support this standard and devices being capacitively sensed. (See Annex A.)

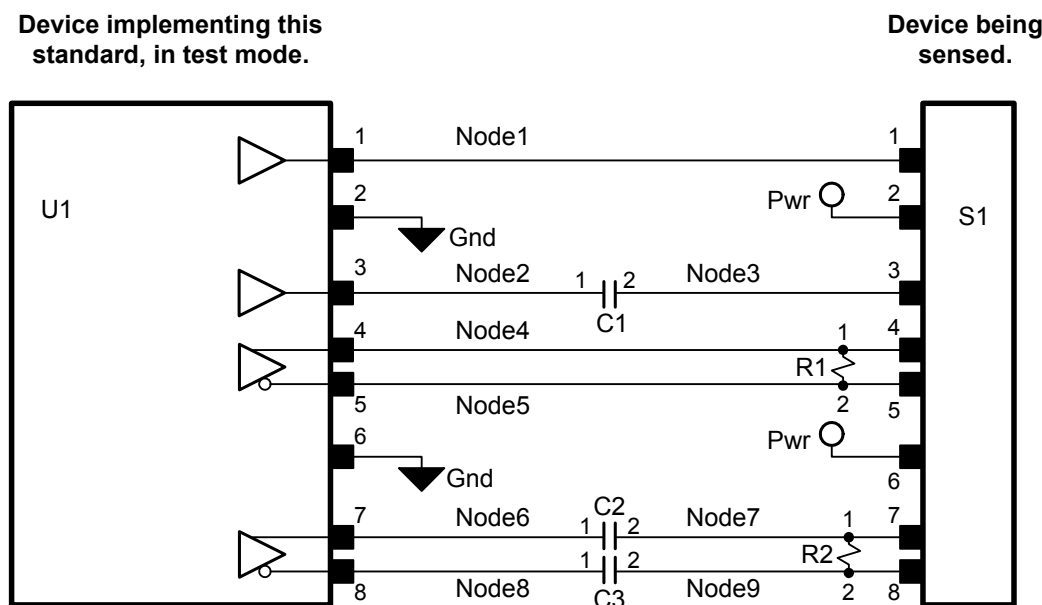


Figure 7—Interconnects between a stimulating device and a device being tested

Figure 7 and Table 2 show a group of interconnect defects between a device U1 that implements this standard and device S1 that is being capacitively sensed. U1 is in test mode so all of its ST-pins have drive and self-monitor capability. Device S1 has a non-contact test sensor in close proximity. There are other devices such as coupling capacitors and termination resistors in the network. A listing of possible defects and their effects is shown in Table 2.

Table 2—Potential defects for the circuit in Figure 7

Defect ID	Defect site (NOTE 1)	Possible defect cause	Typical failure syndrome (NOTE 2)
1	Node1 shorted to fixed voltage (power or ground)	Excess solder	Detected by EXTEST self-monitor; reduced signal at sense plate
2	U1 pin 1 open	Missing solder, bent pin	Reduced signal at sense plate
3	C1 pin 1 open (NOTE 3)	Missing solder, missing capacitor	Reduced signal at sense plate
4	Node1 shorted to Node2	Excess solder	Detected by EXTEST self-monitor
5	Node3 shorted to fixed voltage (power or ground)	Excess solder	Reduced signal at sense plate
6	Node2 shorted to Node3	Excess solder, defective capacitor	Not detected
7	Node4 shorted to Node5	Excess solder, defective resistor	Detected by EXTEST self-monitor (depends on monitor's characteristics).
8	R1 pin 1 open	Missing solder, missing resistor	Possibly detected, dependent on driver technology. (NOTE 4)

Table 2—Potential defects for the circuit in Figure 7 (continued)

Defect ID	Defect site (NOTE 1)	Possible defect cause	Typical failure syndrome (NOTE 2)
9	U1 pin 4 open	Missing solder, bent pin	Signal pair does not cancel at sense plate in balanced mode; phase identifies pin.
10	U1 pin 7 open	Missing solder	Signal pair does not cancel at sense plate in balanced mode; phase identifies pin.
11	Node5 shorted to Node7	Excess solder	Signal pair does not cancel at sense plate in balanced mode when testing U1 pins 4-5. Same result when testing U1 pins 7-8.
12	S1 pin 7 open	Missing solder, bent pin	Signal pair does not cancel at sense plate in balanced mode; phase identifies pin.
13	Node7 shorted to Node9	Excess solder, defective resistor	Not detected.
14	R2 pin 1 open	Missing solder, missing resistor	Possibly detected, dependent on driver technology. (NOTE 4)
15	Both U1 pins 4 and 5 open	Missing solder, bent pins	Reduced signal at sense plate in unbalanced mode.
16	Node1 shorted to Node7	Excess solder	Increased signal at sense plate when testing U1 pin 1. Some out-of-phase signal detected when testing U1 pins 7 and 8 in balanced mode. Attenuated in-phase signal detected at U1 pins 7 and 8 in unbalanced mode.
NOTE 1—Defects that are equivalent or symmetric in behavior have only one entry in this table. NOTE 2—Some syndromes will depend on termination impedance. NOTE 3—Assumes the coupling capacitance is large compared to the sensing capacitance. This is typically true by several orders of magnitude. NOTE 4—For example, detectability might depend on whether the differential driver is LVDS or CML.			

In Table 2 all defects except 6, 8, 13, and 14 are testable with conventional boundary-scan and/or capacitive sensing. Note that defects 8 and 14 might be detectable in some cases but could be false calls if the measured readings are too close to defect-free measurements.

Defects 1–6 affect only single-ended signals. Defects 7–16 affect differential cases.

Defects 1, 4–7, 11, 13 and 16 all involve shorts, as follows:

- Defect 1 involves a signal on a single-ended driver being shorted to a fixed node such as ground or power. In these cases the driver is incapacitated by the short such that the self-monitor capability on the driver will detect the short during EXTEST-based testing. During capacitive sensing, the driven signal would also be greatly attenuated.
- Defect 4 shorts two self-monitored drivers together. This should be detected during EXTEST testing, when thresholds are chosen according to recommendation b) in 6.3.1.2.
- Defect 5 shorts a signal to power or ground, but on the decoupled side of a decoupling capacitor. This short cannot be seen by the self-monitor of the driver for normally small capacitances. The only way to detect it is by the reduction in the signal at a sense plate.
- Defect 6 is undetected as there will be almost no change in sensed signaling and the self-monitor will not see any significant loading.
- Defect 7 is detectable by the self-monitor capability added by this standard for differential drivers using a hysteretic comparator across the two pins. (See 6.3.4.3.)

- Defect 11 shorts one pin of a differential driver to the capacitively isolated side of another differential path. When the pin-5 driver is toggling, its signal appears at S1 pin 5 and also S1 pin 7 so a signal does appear at a sense plate instead of being canceled. But later, when testing the path from U1 pin 7 through to S1 pin 7, the short to U1 pin 5 will hold that half of the pair constant, again producing a signal at the sensor. This could lead to a diagnosis of two opens, when in reality there is one short.
- Defect 13 is not detectable. The short kills the decoupled driver signals but is not observable by self-monitoring. The short will not likely change the signal level enough at a sense plate to be detected in unbalanced mode testing.
- Defect 16 is similar to defect 11, except the stimulated node shorted to a decoupled differential pin is single-ended.

The remaining defects are open pins, as follows:

- Defect 2 disconnects a signal to the sense plate, greatly reducing the observed signal.
- Defect 3 opens a signal at a capacitor, greatly reducing the observed signal at the sense plate.
- Defect 8 opens a parallel termination resistance across a dc-coupled differential pair. This is not counted as detected but might be observable as a small change in signal level at a sense plate during unbalanced mode testing.
- Defect 9 opens one side of a dc-coupled differential pair. During differential mode testing, the signal cancelation of the defect-free case is replaced by an observable signal. The phase of the signal can be used to identify which of the pins is open.
- Defect 10 opens one side of an ac-coupled differential pair. The effect is the same as for defect 9.
- Defect 12 opens one side of an ac-coupled differential pair after the capacitor. The effect is the same as for defect 9.
- Defect 14 opens a parallel termination resistance across an ac-coupled differential pair after the capacitors. This is not counted as detected but might be observable as a somewhat increased signal at a sense plate during unbalanced testing.
- Defect 15 opens both pins of a differential pair. During differential mode testing where signal cancelation occurs at the sense plate, there is no observable effect. This defect will attenuate an observed signal at the sense plate when testing in unbalanced mode.

4.5 Selective toggle theory of operation

This is a high-level discussion of how board testing for manufacturing defects, using boundary-scan and capacitive sensing measurements, is facilitated by *selective toggle*. Rules, permissions, recommendations, and description of details follow in Clause 5 and Clause 6.

4.5.1 Board test background

Before boundary-scan-type tests are conducted, many board testers will conduct tests with the board in an unpowered state. Such testers depend on nodal access to many points on surface(s) of the board. Shorts testing is conducted at this time, as well as the measurement of many passive component values, as supported by nodal access. In some cases, access limitations will not allow some components or potential shorts to be tested. These are then left for other test techniques to follow that require the board to be powered. Defects found while in the unpowered state (particularly shorts) may be repaired before proceeding.

As with all boundary-scan-type tests, a PCA is first properly conditioned to support the test. Conditioning includes powering up the necessary portions of the board in an appropriate sequence, and then asserting control states on important nodes, such as power-on reset signals, oscillator disables and bus disables as needed to bring the board to a stable state conducive to the test. Note that part of a boundary-scan test strategy may be to use boundary-scan driver resources to condition and maintain certain board nodes to high or low states to further support the needs of the test during its execution. This becomes a “conditioning pattern” of node states needed to support the test. This conditioning pattern is then held constant for the duration of the test and thus supersedes testing of those nodes. Analysis and identification of such cases is a part of board test engineering. The conditioning and holding of nodes to high or low states is typically done with the EXTEST or CLAMP instruction depending on board connectivity and the objective of the test being performed.

Conventional boundary-scan testing using the IEEE 1149.1 EXTEST instruction may then be run since it focuses on finding shorted paths and open connections between boundary-scan devices. If shorts are indeed detected, power may be quickly removed from the board to prevent damage. These may be repaired before continuing; a decision made by the test engineer. The detection of opens may not precipitate such action since they are less likely to cause damage. Indeed, a test engineer may run a selection of boundary-scan tests that focus on various defects, ordered to find dangerous shorts quickly, and followed by tests focused on less damaging defects later. Each such test may be “stand-alone,” meaning it is entirely responsible for setup of the test conditions it needs and is not dependent on other preceding tests to leave these conditions behind. Such tests can be rearranged in order, or even skipped if desired. Such tests will start and end in the Test-Logic-Reset TAP controller state.

4.5.2 Basic differences between normal pins and ST-pins

There are critical differences between normal pins and ST-pins with how they operate with respect to the EXTEST and the SELECTIVE_TOGGLE instruction. This understanding is needed when conditioning nodes to high or low states for the test duration, as explained in 4.5.1, and testing the remaining nodes with the SELECTIVE_TOGGLE capability. A board design will contain components that could have a mix of normal pins and ST-pins. With the SELECTIVE_TOGGLE instruction loaded, normal pins function as defined by EXTEST. The differences between normal pins and ST-pins with SELECTIVE_TOGGLE active are given in Table 3.

An important difference with SELECTIVE_TOGGLE in effect is that for ST-pins, data transfers from the Capture flip-flops to the Update flip-flops is suppressed in the Update-DR TAP state. The Capture flip-flop data is then treated as a “toggle pointer” where “1” data indicates “selected” ST-pins that will toggle (in the Run-Test/Idle TAP state) and “0” data indicates ST-pins that hold their states during that time. ST-pin Update flip-flops do not load data from their Capture flip-flops in the Update-DR TAP state the way normal pins do. Thus, ST-pins have their drivers set to an initial state at the Update-IR state (step 2) when SELECTIVE_TOGGLE first becomes effective. After that, the only way ST-pins change state is in Run-Test/Idle (step 5) when they are selected to toggle. When exiting the Run-Test/Idle state (step 6) the ST-pin driver state is restored to the initial state. If several pins are to be successively toggled, then the test algorithm will progress from step 6 back to step 3 where the ST-pin capture flip-flops are loaded with a new toggle-hold selection pattern and the normal pins are simply reloaded with the same data from step 1. Some of the ST-pins may be involved in toggling pins during a test and some may not, as required by the needs of the test. Those pins that are not toggled retain their static states for the duration of the test.

With SELECTIVE_TOGGLE in effect, a data scan-in in the Shift-DR TAP state will also shift data out of the Capture flip-flops. There is no requirement for what should be captured by SELECTIVE_TOGGLE given by this standard, so the device designer may choose whatever is expedient. Test algorithms will ignore this data.

Table 3—Selective toggle test actions for normal and ST-pins in a device.

Step	TAP controller action	Normal pin action	ST-pin action
1	Starting in Test-Logic-Reset state, shift in PRELOAD instruction, then Update-IR; shift in boundary register data, then Update-DR.	Boundary data loaded into Update flip-flop to be its initial state, pin driver is in non-test mode.	Same as for normal pin.
2	Shift in SELECTIVE_TOGGLE instruction, then Update-IR.	Pin driver state controlled by Update flip-flop.	Same as for normal pin.
3	Shift in boundary register data.	No change in pin driver state. (Data shifted into Capture flip-flop Shift should be same as in step 1 to avoid signal step on pin.)	No change in pin driver state. Data shifted into Capture flip-flop is “1” if pin is selected to toggle and “0” if pin should not toggle.
4	Update-DR	Transfer data from Capture flip-flop to Update flip-flop (driver does not change state since data should be same as in step 1.).	No transfer from Capture flip-flop to Update flip-flop (therefore, no state change).
5	Run-Test/Idle	No change in pin’s state.	Toggle pin if “1” in Capture flip-flop. No change in pin’s state if “0” in Capture flip-flop.
6	Exit Run-Test/Idle.	No change in pin’s state.	Pin that toggled is returned to its initial state set up in steps 1 and 2.

4.5.3 Testing with SELECTIVE_TOGGLE

When a boundary-scan test that makes use of the features in this standard is first initiated, all the ICs that participate begin in system mode, meaning their I/O pins are controlled by their system functionality. Using the PRELOAD instruction, boundary register states are set up as will be needed as a conditioning pattern by the test when it enters test mode, controlled by either EXTEST or the SELECTIVE_TOGGLE instruction provided by this standard. In a multi-device chain, some ICs might be held in static states by EXTEST, and one or more other ICs will have SELECTIVE_TOGGLE in effect to support the requirements of the device-under-test (DUT).

NOTE—The CLAMP instruction may serve in place of the EXTEST instruction for devices in a chain that are exclusively holding constant states on I/O pins during a selective-toggle-based test.

To simplify this discussion, assume there is only one IC being used to test a set of pins on one DUT with the SELECTIVE_TOGGLE instruction. The normal pins will behave as per EXTEST, but the ST-pins will perform as specified by SELECTIVE_TOGGLE.

Before commencing a test using SELECTIVE_TOGGLE, the TOGGLE_SETUP instruction is used to enter an integer into the Toggle_Control register. Note TOGGLE_SETUP is a normal mode instruction and does not affect component behavior while active. The integer loaded into the Toggle_Control register, and the TCK frequency, control the time between transitions of ST-pins that are used during a test.

Referring to Table 3, the preload sequence (step 1) is used to set the board nets up to perform a reliable test by isolating conflicts and disabling noise sources. The preload sequence can be a simple all-zero or all-one pattern for the ST-pins, or a more random-looking pattern, if needed to enhance test performance. For example, some nodes connected to ST-pins might fan out to an array of memory ICs, and it is necessary to assure that all the chip-select lines of this array are all deselected to avoid driver conflicts among these devices during test, when individual ST-pins are being toggled. This would become part of an initial state shifted in by PRELOAD. Then, as toggling proceeds one pin at a time, only one memory IC would be selected at a time and no driver conflicts would ensue.

Figure 8 shows the timing diagram for preloading the boundary register with data and then loading either the SELECTIVE_TOGGLE or EXTEST instructions (step 2). (Notice that “Tags” are used in Figure 8 and