

IEEE Standard for VMA Extensions for Instrumentation: VXIbus

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Abstract: A technically sound modular instrument standard based on IEEE Std 1014-1987, which is open to all manufacturers and is compatible with present industry standards, is defined. The VXIbus specification details the technical requirements of VXIbus compatible components, such as mainframes, backplanes, power supplies, and modules.

Keywords: common modular instrument architecture, VMEbus, VXIbus

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Introduction

(This introduction is not a part of IEEE Std 1155-1992, IEEE Standard for VMEbus Extensions for Instrumentation: VXIbus.)

The architectural concept of the *VMEbus Extensions for Instrumentation: VXIbus* standard has its basis in IEEE Std 1014-1987, *IEEE Standard for a Versatile Backplane Bus: VMEbus* (ANSI). The VXIbus standard further develops and extends the concepts and capabilities of the VMEbus, with particular emphasis on support of an open instrumentation system.

There have been numerous requests for multivendor, modular instrumentation, particularly from the US Department of Defense towards Instruments-on-a-Card (IAC). The US Air Force, Navy, and Army have programs addressing these issues, known respectively as MATE, CASS, and IFTE. To date, the Air Force has adopted VXIbus as the basis for the MATE IAC Standard, MATE-STD-IAC. The Army has also specified VXIbus to be used for updates to IFTE and the Contact Test Set.

The marketplace has demonstrated the advantages of an open system such as VMEbus, with thousands of VMEbus cards available from a multitude of vendors. In June 1987, technical representatives from five instrumentation companies, Colorado Data Systems, Hewlett Packard, Racal Dana, Tektronix, and Wavetek, formed a consortium to engineer the additional standards necessary for an open architecture instrumentation bus based on IEEE Std 1014-1987, IEEE Std 1101.2-1992, *IEEE Standard for Mechanical Core Specifications for Conductor-Cooled Eurocards* (ANSI), and other instrumentation standards, such as IEEE Std 488.1-1987, *IEEE Standard Digital Interface for Programmable Instrumentation* and its companion IEEE Std 488.2-1992, *IEEE Standard Codes, Formats, Protocols and Common Commands*. In July 1987, the VXIbus Consortium announced their agreement to support a common modular instrument architecture, known as VXIbus, and released Revision 9.9 of the document. This group of instrument manufacturers has continued to refine and enhance the standard, resulting in the release of Revision 1.3, dated July 14, 1989.

Concurrent with the actions of, and supported by the VXIbus Consortium, the P1155 Working Group was established in August 1987 under the auspices of the Microprocessors and Microcomputers Standards Subcommittee of the IEEE Computer Society. The IEEE Instrumentation and Measurement Society also became closely involved with its development. The P1155 Working Group has reviewed Revision 1.4 of the VXIbus specification and used it as the basis for the standard defined herein.

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CLAUSE	PAGE
1. Introduction	1
1.1 VMEbus background	1
1.2 The VXIbus extensions	2
1.3 Document structure	3
1.4 Specification objectives	3
1.5 Terminology	4
1.6 References	4
1.7 Definitions	5
1.8 Abbreviations	7
2. VXIbus implementation of VMEbus specifications	7
2.1 Introduction	7
2.2 Data transfer bus	7
2.3 Data transfer bus arbitration	8
2.4 Priority interrupt	8
2.5 Utilities	8
2.6 Electrical specifications	8
2.7 Mechanical specifications	34
2.8 EMC and system power	73
3. System architecture	89
3.1 VXIbus system architecture overview	89
3.2 Device operation	91
3.3 Device communication protocols	133
3.4 System resources	141
4. VXIbus device implementations	148
4.1 VXIbus instruments	148
4.2 IEEE 488 VXIbus interface	152
5. Command and event formats	158
5.1 Word-serial commands	159
5.2 Longword-serial commands	176
5.3 Extended longword-serial commands	177
5.4 Protocol events	177

STABILIZED

CLAUSE	PAGE
6. Dynamic configuration	178
6.1 Definitions.....	178
6.2 DC device requirements.....	179
6.3 DC system requirements	181
Annex A (Informative) VXIbus register overviews	184
Annex B (Informative) Suggested backplane design.....	194
Annex C (Informative) Support of early VXIbus devices	197
Annex D (Informative) Manufacturer ID numbers	198
Annex E (Informative) Bibliography	199

IEEE Standard for VMEbus Extensions for Instrumentation: VXIbus

1. Introduction

The goal of the VXIbus is to define a technically sound modular instrument standard based on IEEE Std 1014-1987¹ that is open to all manufacturers and is compatible with present industry standards.

VXIbus is an acronym for VMEbus extensions for instrumentation. The VXIbus specification details the technical requirements of VXIbus compatible components, such as mainframes, backplanes, power supplies, and modules. Before studying the VXIbus architecture, one should become familiar with the VMEbus and its specification.

1.1 VMEbus background

The VMEbus is an open system architecture primarily focused at computer systems. VMEbus modules are approximately 15 cm (6 in) deep and come in two heights, about 10 cm (4 in) and 23 cm (9 in). The VXIbus specification refers to these as the A and B sizes, respectively. The precise dimensions are specified by IEEE Std 1101-1987, which describes a printed-circuit boards (PCB) family and their associated backplane connector locations. VMEbus modules are designed for 0.8 in slot-to-slot spacing. The A-size board has a single 96-pin connector known as P1, while the B-size board may include a P1 and a P2 connector. Each of these connectors consists of three rows of 32 pins apiece on 0.1 in centers. Typically, these boards are positioned vertically in a frame with the P1 connector closest to the top. Neither the VMEbus nor the VXIbus mandates a physical orientation, since orientation is only an implementation issue and is not needed for compatibility. Many VMEbus and VXIbus systems are designed to accept boards horizontally.

The VMEbus specification allows a maximum of 21 modules. However, if installed vertically in a main-frame intended for mounting in a standard 19 in rack, 20 is the practical maximum. VMEbus makes no particular provision for an extension chassis or frame-to-frame communication. Multiple frame systems can be created by electrically buffering the VMEbus (at the loss of some bandwidth between cages) or by using standard data communication links entirely different from the VMEbus architecture. There are no electromagnetic compatibility (EMC) requirements dictated by VMEbus, either conducted or radiated, nor are there power dissipation limits or cooling requirements. VMEbus has left these issues to the system integrator, while VXIbus addresses these issues more rigorously.

¹Information on references can be found in 1.6.

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Although electrically and logically similar to the 68000 microprocessor architecture, the VMEbus interface has been specified broadly enough that it is not dependent on any particular processor, and many processors are already supported on VMEbus, including the 80386. Many of the simpler VMEbus boards do not have processors at all.

A minimum VMEbus system requires only the P1 connector. All handshaking, arbitration, and interrupt support exists on P1, with P2 used to expand the system to 32 bits of address and data (A32 and D32). P1 will support 16-bit and 24-bit addressing (A16 and A24) as well as 8- and 16-bit data paths (D08 and D16). The extra lines needed for A32 and D32 are contained on the center row of P2, while the outer rows are user defined. These undefined pins are typically used for interface connections, such as allowing a module to drive a chassis-mounted connector, access an internal disk drive, or provide for module-to-module communication. The VMEbus subsystem bus (VSB) is a “subsystem bus” specification that has defined P2 as an additional communication path for up to six modules. Multiple VSBs may exist within any one VMEbus system. This is important to note, because VXIbus defines a subsystem of up to 13 modules and, like VSB, multiple VXIbus subsystems may exist within any one VXIbus system.

1.2 The VXIbus extensions

VXIbus retains P1 and the center row of P2 exactly as defined by VMEbus. This includes the 5 V and ± 12 V power pins on P1, and the additional 5 V pins on P2. VXIbus includes the A and B card sizes, and these modules remain totally VMEbus compatible. However, VXIbus has made substantial additions to the VMEbus specification oriented towards instrumentation that can best be described as an electromechanical superset and a logical subset.

1.2.1 VXIbus modules

VXIbus has added two module sizes of about a 33 cm (13 in) depth referred to as the C and D sizes. These modules are 23 cm (9 in) and 35.5 cm (14 in) high, respectively, and are placed on 3 cm (1.2 in) centers. The C-size module is the same height as the VMEbus B-size board, and may sport both the P1 and P2 connectors. The D-size module is a triple-high module that may include a P3 connector in addition to P1 and P2. The 3 cm (1.2 in) module width allows feasible implementation of high-density instrumentation modules while allowing enough space for shielding both sides of a module and inserting an optional chassis shield. It also has the added benefit of allowing a high degree of compatibility with the shorter and narrower A and B sizes by allowing them to be mounted on full-length board carders or adapters. These carriers/adapters may also shield the sides of standard VMEbus cards, giving them a high degree of electromagnetic compatibility with VXIbus systems.

1.2.2 VXIbus subsystems

A VXIbus system may have up to 256 devices, including one or more VXIbus subsystems. A VXIbus subsystem consists of a central timing module referred to as Slot 0 with up to 12 additional instrument modules. P2 and P3 are completely defined in a VXIbus subsystem. These 13 modules conveniently fill a standard 19 in cabinet when mounted vertically on 3 cm (1.2 in) centers. Many VXIbus systems will consist only of a single frame with these 13 modules. A common configuration will load the Slot 0 module with system resources, such as the VXIbus mandated timing generation, the VMEbus required system controller 0 subfunctions, and a data communication port, such as IEEE 488 or RS-232. Slot 0 may also include optional instrumentation. The other positions are general purpose slots for the user to mix and match modules. A single VXIbus subsystem may have less than 12 additional slots, but may not have more. Any combination of VXIbus subsystems may exist within a VXIbus system. For instance, one VXIbus system may consist of a frame with one Slot 0 and 12 VXIbus modules extended to another frame that has a Slot 0 adjacent to three instrument slots, another Slot 0 with five instrument slots, and four standard VMEbus slots of undefined P2.

1.2.2.1 P2 connector definition

As mentioned previously, a VXIbus subsystem defines all P2 and P3 pins. The VXIbus P2 adds a 10 MHz ECL clock, ECL and analog supply voltages, ECL and TTL trigger lines, an analog summing bus, a module identification line, and a daisy-chain structure known as the local bus. The trigger lines serve primarily as resources for signaling between instruments in a VXIbus subsystem, while the local bus lines are preferred for use within a multiple module instrument

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set (adjacent slots). The daisy-chain local bus use is left to the module manufacturer to define, and several classes of electrical signals are permitted. Allowed signals are TTL, ECL, low-voltage analog, and analog up to 42 V. A keying mechanism near the faceplate indicating that module's local bus class prevents incompatible classes from accidentally being placed adjacently and potentially causing a destructive condition. Typical uses of the local bus include creating an internal analog bus or a chain of serial digital signal processors. There are a total of 24 local bus pins on P2, 12 lines in and 12 lines out for each slot; thus creating a 12-line bus that may or may not be passed on to adjacent slots.

1.2.2.2 P3 connector definition

The VXIbus P3 connector adds many of the same resource types as described for P2, but it is aimed at higher performance instrumentation. Included on P3 is a 100 MHz clock and sync signal, additional power pins of the same supply voltages, more ECL trigger lines, and 24 additional lines (48 pins) of daisy-chain local bus. Also defined on P3 is a “star” trigger system where precision ECL trigger signals are routed through Slot 0 acting as a cross-point switch. This allows very precisely matched trigger timing between modules regardless of module position.

1.2.3 VXIbus system architecture

The VXIbus device protocols define how modules are granted nonconflicting portions of the VMEbus address space. A device is typically a single module, but this is not required. Several devices may exist on a single module, and a single device may consist of multiple modules. Two hundred fifty-six devices may exist in any one VXIbus system, and are referred to by logical device addresses ranging from 0 to 255. A VXIbus system configuration space is defined in the upper 16 kbytes of the 64 kbyte A16 address space. Each device is granted a total of 64 bytes in this space, which is sufficient for many devices. Devices requiring additional address space have their address requirements readable in a defined register in the A16 address space. A “resource manager” reads this value shortly after power-on, and then assigns the requested memory space by writing the module's new VMEbus address into the device's offset register. This method positions a device's additional memory space in the A24 (16 Mbyte) or A32 (4 Gbyte) address space. If present day VMEbus cards are used in a system, the resource manager must position the VXIbus devices around the space taken by the standard VMEbus cards.

Higher level communication protocols are defined to allow sharing of interface modules and other devices by multiple manufacturers.

1.2.4 Manufacturer ID numbers

The VXIbus specification provides a mechanism for identifying the manufacturer of every VXIbus device. This consists of a 12-bit manufacturer ID number (0 → 4095), which may be read over the VMEbus (see 3.2.1.1.2, Configuration registers). The list of ID numbers is maintained by the VXIbus Consortium, and is available to the public upon request. Each VXIbus device manufacturer has exactly one manufacturer ID number. Numbers are assigned to manufacturers in decreasing order beginning with number 4095. The VXIbus Consortium's address, along with an application for a manufacturer ID number, is given in annex D to this specification.

1.3 Document structure

This document is organized in clauses, with each clause discussing a particular independent level of the implementation. In the event where a clause parallels another standard document (such as IEEE Std 1014-1987), subclauses will have corresponding numbers. Several informative annexes, containing clarifications and extensions, follow the body of the specification.

1.4 Specification objectives

This document defines a set of *rules* and *recommendations* for constructing a component that will interface to the VXIbus family. The specifications cover the complete spectrum, from basic hardware issues such as card dimensions to communications protocols. This specification has the following objectives:

- a) To allow communication among devices in an unambiguous fashion.
- b) To allow for physical size reduction of standard rack-and-stack instrumentation systems.
- c) To allow for software cost reduction in test system integration by the use of common interfaces to analogous capabilities.
- d) To provide higher system throughput for test systems through the use of higher bandwidth channels for interdevice communication, and the use of new protocols specifically designed to enhance throughput.
- e) To provide test equipment that could be used in military Instrument-on-a-Card (IAC) systems.
- f) To provide the ability to implement new functionality in test systems through the use of virtual instruments.
- g) To define how to implement multimodule instruments within the framework of this standard.

1.5 Terminology

This standard uses the keywords defined in IEEE Std 1014-1987, 1.4, in order to avoid confusion and maintain consistency. These keywords are used to indicate the nature of the trailing information as follows:

Rule. Rules shall be followed to ensure compatibility for cards in the system. A rule is characterized by the use of the words *shall* and *shall not*. These words are not used for any purpose other than stating rules.

Recommendation. Recommendations consist of advice to implementors that will affect the usability of the final device. Discussions of particular hardware to enhance throughput would fall under a recommendation. These should be followed to avoid problems and to obtain optimum performance.

Suggestion. A suggestion contains advice that is helpful but not vital. The reader is encouraged to consider the advice before discarding it. Suggestions are included to help the novice designer with areas of design that can be problematic.

Permission. Permissions are included to clarify the areas of the specification that are not specifically prohibited. Permissions reassure the reader that a certain approach is acceptable, and will cause no problems. The word *may* is reserved for indicating permissions.

Observation. Observations spell out implications of rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules, so that the reader understands why the rule must be followed.

Any text that appears without heading should be considered as description of the standard.

1.6 References

IEEE Std 488. 1-1987, IEEE Standard Digital Interface for Programmable Instrumentation (ANSI).²

IEEE Std 488.2-1992, IEEE Standard Codes, Formats, Protocols, and Common Commands for Use With IEEE Std 488.1-1987, IEEE Standard Digital Interface for Programmable Instrumentation (ANSI).

IEEE Std 1014-1987, IEEE Standard for a Versatile Backplane Bus: VMEbus (ANSI).

IEEE Std 1101-1987, IEEE Standard for Mechanical Core Specifications for Microcomputers (ANSI).

²IEEE publications are available from the Institute of Electrical and Electronics Engineers, Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.

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1.7 Definitions

1.7.1 488-VXIbus interface device: A message-based device that provides communication between an IEEE 488 interface and the VXIbus instruments.

1.7.2 backplane: An assembly, typically a PCB, with 96-pin connectors and signal paths that bus the connector pins. VXIbus systems will have up to three sets of bussed connectors, called the J1, J2, and J3 backplanes.

1.7.3 board: A blank PCB.

1.7.4 board assembly: A board and its associated electrical components and connectors.

1.7.5 chassis shield: A shield that resides between two modules and attaches to the mainframe.

1.7.6 command: Any communication from a commander to a message-based servant, consisting of a write to the servant's data low register, possibly preceded by a write to the data high or data high and data extended registers.

1.7.7 commander: A message-based device that is also a bus master and can control one or more servants.

1.7.8 configuration registers: A device's A16 registers that are required for the system configuration process.

1.7.9 DC device: A device whose logical address can be programmed by a dynamic configuration (DC) resource manager.

1.7.10 DC resource manager: A resource manager that supports dynamic configuration.

1.7.11 DC system: A VXIbus system that includes a DC resource manager and one or more DC devices.

1.7.12 device: A component of an VXIbus system. Normally, a device will consist of one VXIbus board. However, multiple-slot devices and multiple-device modules are permitted. Some examples of devices are computers, multimeters, multiplexers, oscillators, operator interfaces, and counters.

1.7.13 DIR violation: A word-serial protocol error that occurs when a servant receives a DIR synchronized command (such as *byte available*) and is unable to process that command because the DIR bit is zero (0).

1.7.14 DOR violation: A word-serial protocol error that occurs when a servant receives a DOR synchronized command (such as *byte request*) and is unable to process that command because the DOR bit is zero (0).

1.7.15 dynamic configuration (DC): An optional, alternative method of automatically assigning logical addresses to VXIbus devices at system power-on or other configuration times, using the MODID lines. It allows for each slot to contain one or more devices as well as different devices within a slot to share address decoding hardware.

1.7.16 events: Signals or interrupts generated by a device to notify another device of an asynchronous event. The contents of events are device dependent.

1.7.17 extended devices: A device that has VXIbus configuration registers and a subclass register. This category is intended to allow for definition of additional device types.

1.7.18 extended longword serial: A form of word-serial communication that allows 48-bit data transfers between commanders and servants.

1.7.19 fast handshake: A high-speed mode of operation that uses the same communication registers as the word-serial protocol and allows data transfer without the need for polling after each transfer.

1.7.20 hybrid device: A VMEbus compatible device that includes application-specific subsets of VXIbus protocols.

1.7.21 location monitor: A function that monitors data transfers over the VMEbus in order to detect accesses to the locations it has been assigned to watch. When an access occurs to one of these assigned locations, the location monitor generates a local signal.

1.7.22 logical address: An 8-bit number that uniquely identifies each VXIbus device in a system. It defines a device's A 16 register addresses, and indicates commander/servant relationships.

1.7.23 longword serial: A form of word-serial communication that allows 32-bit data transfers between commanders and servants.

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1.7.24 mainframe: A rigid framework that provides mechanical support for modules inserted into the backplane, ensuring that connectors mate properly and that adjacent modules do not contact each other. It also provides cooling airflow, and ensures that modules do not disengage from the backplane due to vibration or shock.

1.7.25 memory device: A device that contains only memory and implements configuration registers.

1.7.26 message-based device: An intelligent device that implements the defined VXIbus registers and communication protocols.

1.7.27 module: Typically a board assembly and its associated mechanical parts, front panel, optional shields, etc., which contains everything required to occupy a slot in a mainframe. A module may occupy one or more slots.

1.7.28 multiple query error: A word-serial protocol error that occurs when a servant receives a command requiring it to output a response to its data low register, and is unable to respond because of an unread response to a previous command.

1.7.29 operational register: Any register on a device that is not required for the system configuration process.

1.7.30 read ready violation: A word-serial protocol error that occurs when data is read from a servant while its read ready bit is zero (0).

1.7.31 register-based device: A servant-only device that supports VXIbus configuration registers. Register-based devices are typically controlled by message-based devices via device-dependent register reads and writes.

1.7.32 resource manager: A message-based commander located at logical address 0 that provides configuration management services, such as address map configuration, commander/servant mappings, self-test, and diagnostics management.

1.7.33 responses: Signals or interrupts generated by a device to notify another device of an asynchronous event. Responses contain the information in the sender's response register.

1.7.34 SC device: A static configuration device, whose logical address is set manually and cannot be changed by DC protocols.

1.7.35 SC resource manager: A resource manager that supports static configuration and does not support dynamic configuration of VXIbus devices.

1.7.36 SC system: A VXIbus system with no DC devices.

1.7.37 serial protocol: Any communication protocol in which data is transferred serially to or from a fixed location.

1.7.38 servant: A device that is controlled by a commander. There are message-based and register-based servants.

1.7.39 signal: Any communication between message-based devices consisting of a write to a signal register.

1.7.40 slot: A position where a module can be inserted into an VXIbus backplane. Each slot provides the 96-pin J connectors to interface with the board P connectors. It may have to provide one, two, or three connectors.

1.7.41 system: One or more mainframes that are connected, having a common resource manager. Each device in a system has a unique logical address.

1.7.42 unsupported command: A word-serial protocol error that occurs when a servant receives a command that it does not support.

1.7.43 VXIbus: VMEbus extensions for instrumentation.

1.7.44 VXIbus instrument: A message-based device that supports the VXIbus instrument protocols.

1.7.45 VXIbus subsystem: A central timing module referred to as Slot 0, with up to 12 additional adjacent VXIbus modules. The VXIbus subsystem bus defines the lines on the P2 and P3 connectors.

1.7.46 word serial: The simplest required communication protocol supported by message-based devices in the VXIbus system. It utilizes the A16 communication registers to transfer data using a simple polling handshake method.

1.7.47 write ready violation: A word-serial protocol error that occurs when data is written to a servant while its *write ready* bit is zero (0).

1.8 Abbreviations

DC	Dynamic Configuration
DIR	Data In Ready
DOR	Data Out Ready
ECL	Emitter-Coupled Logic
IC	Integrated Circuit
LAN	Local Area Network
PCB	Printed Circuit Board
SC	Static Configuration
TTL	Transistor-Transistor Logic

2. VXIbus implementation of VMEbus specifications

This document describes additions to and recommendations for the VMEbus specification, IEEE Std 1014-1987. This clause is organized in a parallel fashion to the IEEE Std 1014-1987 document. Subclauses 2.1-2.7 are additions to the corresponding Sections 1-7 of IEEE Std 1014-1987, and 2.8 is new material.

2.1 Introduction

The intent of the VXIbus implementation of the VMEbus specifications is to produce an electromechanical superset and logical subset of the VMEbus specifications in order to establish compatibility for all VXIbus systems.

It is expected that all boards designed to the VMEbus specification will be compatible with this implementation mechanically and electrically. However, a subset of VMEbus protocols relating to data transfer, arbitration, and interrupts has been specified, and may limit the utility of some standard VMEbus products in a VXIbus system. Mechanical extensions are defined to allow for a superset of board sizes.

2.2 Data transfer bus

2.2.1 Address modifiers

Recommendation 2.2.1. It is recommended that the address modifiers listed in the VMEbus specification as user defined not be used.

2.2.2 DTACK* operation

Rule 2.2.1. A slave shall pull DTACK* or BERR* low within 20 μ s after a data strobe goes low.

Recommendation 2.2.2. A SLAVE should pull DTACK* low within 1 μ s after a data strobe goes low.

Rule 2.2.2. A slave shall release DTACK* and BERR* within 5 μ s after the data strobe(s) goes high.

Recommendation 2.2.3. A slave should release DTACK* and BERR* within 0.5 μ s after the data strobe(s) goes high.

2.2.3 Bus timer operation

Rule 2.2.3. The bus timer shall be BTO (≥ 100).

Observation 2.2.1. The BTO(100) capability minimum is to allow for chassis-to-chassis communication. There is a potential for each chassis to take up to 20 μ s to respond to a data transfer.

2.3 Data transfer bus arbitration

Rule 2.3.1. The bus grant daisy-chain lines shall be used or passed by all single boards and board assemblies.

Recommendation 2.3.1. The arbiter should implement priority-based arbitration between the four bus request/grant levels.

2.4 Priority interrupt

Rule 2.4.1. The interrupt acknowledge daisy-chain lines shall be used or passed by all single boards and board assemblies.

2.5 Utilities

2.5.1 Power monitor

The power monitor, defined by IEEE Std 1014-1987, is a function that asserts the SYSRESET* line at power-on, and asserts both the aCFAIL* and SYSRESET* lines immediately prior to power-removal. This is a required VXIbus capability closely linked to the mainframe power supply. Each mainframe is required to provide this function.

Rule 2.5.1. Every VXIbus mainframe shall provide a VMEbus power monitor.

Recommendation 2.5.1. A power monitor should drive ACFAIL* low a minimum of 8 ms before driving SYSRESET* low, and a minimum of 10 ms before +5 Vdc power drops below 4.875 V, when a power failure is detected. See Fig 65 of IEEE Std 1014-1987.

2.5.2 Power pins

See 2.8, EMC and system power, for power pin specifications.

2.6 Electrical specifications

Rule 2.6.1. All conductors on P1, P2, and P3 shall meet the requirements of Section 6 of IEEE Std 1014-1987.

2.6.1 The P1 connector

The P1 connector shall remain as defined by IEEE Std 1014-1987.

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2.6.2 The VXIbus subsystem P2 connector

The VXIbus subsystem bus defines the outer rows (user-defined pins) for instrumentation use. The center row retains the VMEbus specification. Alternate definitions of the outer two rows of P2 are permitted in VXIbus systems (not VXIbus subsystems) with a “segmented backplane” architecture where other VMEbus subsystem buses, such as VSB, may exist. A VXIbus subsystem bus consists of a system resource module defined as Slot 0 with up to 12 adjacent modules in increasing slot numbers. VXIbus and VXIbus subsystem bus are used interchangeably in this subclause of the VXIbus specification.

The VXIbus P2 connector delivers resources to modules particularly oriented toward instrumentation. On P2 it adds the following:

- a) -5.2 V , -2 V , $\pm 24\text{ V}$, and additional $+5\text{ V}$ power
- b) Ten MHz differential clock
- c) Two parallel emitter-coupled logic (ECL) trigger lines
- d) Eight parallel transistor-transistor logic (TTL) trigger lines
- e) Module identification pin
- f) Twelve lines of manufacturer-defined local bus lines that connect to adjacent modules
- g) Fifty-ohm terminated analog summing bus

The Slot 0 module serves as a system resource and has a modified P2 functionality for central handling of the module identification pins. The Slot 0 module, while providing these common resources, may also contain other devices and instrumentation.

2.6.2.1 CLK10

CLK10 is a 10 MHz system clock. It is sourced from Slot 0 and distributed to Slots 1-12 on P2 (see tables 2-1 and 2-2). The Slot 0 output is differential ECL. It is buffered on the backplane and distributed to each module slot as a single-source, single-destination differential ECL signal. The CLK10 is individually buffered on the backplane for each slot position to provide a high level of intermodule isolation and relax the loading rules for modules. See figure 2-1.

Rule 2.6.2. The CLK10 frequency sourced from Slot 0 shall be 10 MHz. Its accuracy shall be equal to or better than $\pm 100\text{ ppm}$ (.01%), over its specified operating temperature and time.

Recommendation 2.6.1. A Slot 0 module should allow CLK10 to be derived from an external frequency source.

Observation 2.6.1. An external frequency source would permit the use of an accurate frequency reference, such as a Rubidium Standard, and would facilitate synchronization of multiple VXIbus mainframes.

Rule 2.6.3. CLK10 duty cycle shall be $50\% \pm 5\%$ when measured at the 50% transition level.

Rule 2.6.4. If CLK10 is switched between different clock sources, then the minimum pulse width, high or low, shall not be less than 30 ns or more than 10 μs during switching. The minimum time between two successive transitions of the same polarity shall not be less than 80 ns.

Rule 2.6.5. Each slot's CLK10 shall be driven by a unique backplane buffer output.

Rule 2.6.6. CLK10 shall be distributed differentially from Slot 0.

Rule 2.6.7. The backplane CLK10 distribution traces shall be designed for 50 Ω .

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Rule 2.6.8. If a module accesses the CLK10 signals, then it shall provide 50 Ω termination on CLK10+ and CLK10-, with no more than two (2) equivalent ECL loads.

Rule 2.6.9. The absolute delay of CLK10 from Slot 0 to any module shall not exceed 8 ns.

Observation 2.6.2. Either single-ended input buffers or differential input buffers can be used to buffer and fan out CLK10 on the backplane. Typical components are the 10H101 and 10H116 buffers.

Table 2-1—P2 pin definitions: Slots 1-12

Pin number	ROWa signal mnemonic	ROWb signal mnemonic	ROWc signal mnemonic	Pin number
1	ECLTRG0	+5 V	CLK 10+	1
2	–2 V	GND	CLK 10–	2
3	ECLTRG1	RSV1	GND	3
4	GND	A24	–5.2 V	4
5	LBUSA00	A25	LBUSC00	5
6	LBUSA01	A26	LBUSC01	6
7	–5.2 V	A27	GND	7
8	LBUSA02	A28	LBUSC02	8
9	LBUSA03	A29	LBUSC03	9
10	GND	A30	GND	10
11	LBUSA04	31	LBUSC04	11
12	LBUSA05	GND	LBUSC05	12
13	–5.2 V	+5 V	–2 V	13
14	LBUSA06	D16	LBUSC06	14
15	LBUSA07	D17	LBUSC07	15
16	GND	18	GND	16
17	LBUSA08	D19	LBUSC08	17
18	LBUSA09	D20	LBUSC09	18
19	–5.2 V	D21	–5.2 V	19
20	LBUSA10	D22	LBUSC10	20
21	LBUSA11	D23	LBUSC11	21
22	GND	GND	GND	22
23	TTLTRG0*	D24	TTLTRG1*	23
24	TTLTRG2*	D25	TTLTRG3*	24
25	+5 V	D26	GND	25
26	TTLTRG4*	D27	TTLTRG5*	26
27	TTLTRG6*	D28	TTLTRG7*	27
28	GND	D29	GND	28
29	RSV2	D30	RSV3	29
30	MODID	D31	GND	30
31	GND	GND	+24 V	31
32	SUMBUS	+5 V	–24 V	32

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Table 2-2 —P2 pin definitions: Slots 0

Pin number	ROWa signal mnemonic	ROWb signal mnemonic	ROWc signal mnemonic	Pin number
1	ECLTRG0	+5 V	CLK10+	1
2	–2 V	GND	CLK10–	2
3	ECLTRG1	RSV1	GND	3
4	GND	A24	–5.2 V	4
5	MODID12	A25	LBUSC00	5
6	MODID11	A26	LBUSC01	6
7	–5.2 V	A27	GND	7
8	MODID10	A28	LBUSC02	8
9	MODID09	A29	LBUSC03	9
10	GND	A30	GND	10
11	MODID08	A31	LBUSC04	11
12	MODID07	GND	LBUSC05	12
13	–5.2 V	+5 V	–2 V	13
14	MODID06	D16	LBUSC06	14
15	MODID05	D17	LBUSC07	15
16	GND	D18	GND	16
17	MODID04	D19	LBUSC08	17
18	MODID03	D20	LBUSC09	18
19	–5.2 V	D21	–5.2 V	19
20	MODID02	D22	LBUSC10	20
21	MODID01	D23	LBUSC11	21
22	GND	GND	GND	22
23	TTLTRG0*	D24	TTLTRG1*	23
24	TTLTRG2*	D25	TTLTRG3*	24
25	+5 V	D26	GND	25
26	TTLTRG4*	D27	TTLTRG5*	26
27	TTLTRG6*	D28	TTLTRG7*	27
28	GND	D29	GND	28
29	RSV2	D30	RSV3	29
30	MODID00	D31	GND	30
31	GND	GND	+24 V	31
32	SUMBUS	+5 V	–24 V	32

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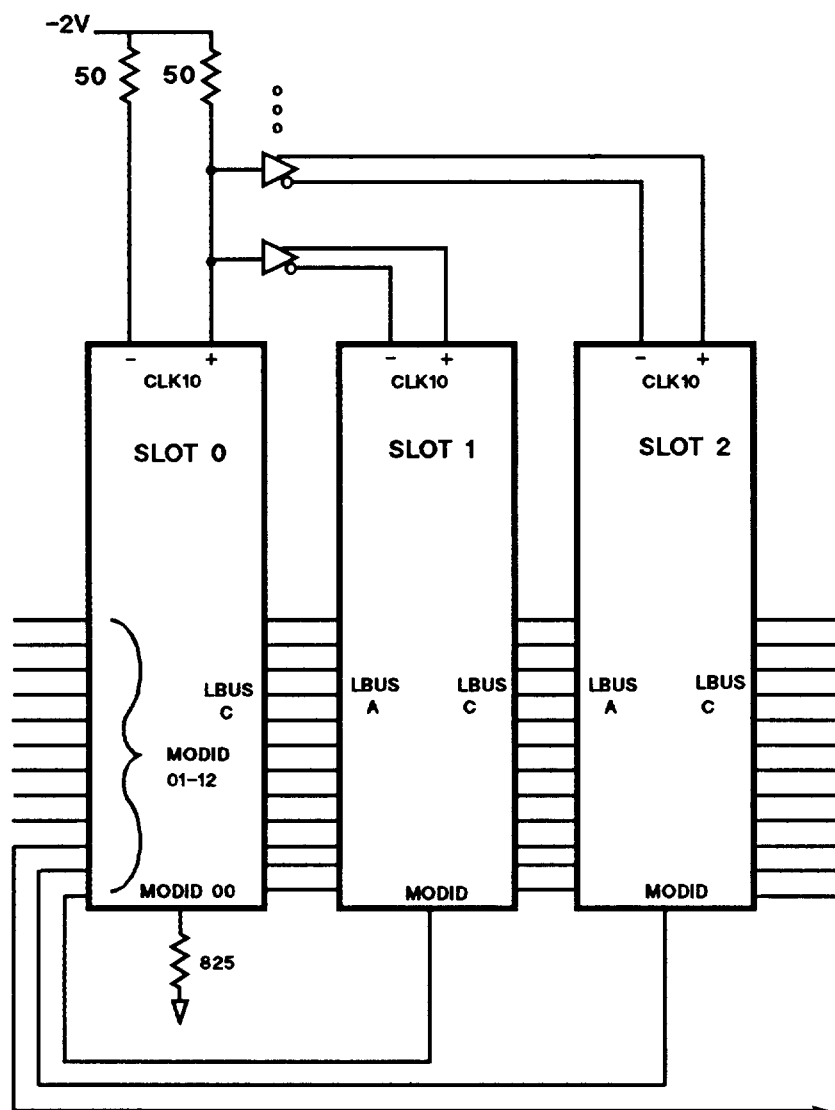


Figure 2-1 —CLK10, MODID, and LBUS signal routing

2.6.2.2 MODID lines

The MODID lines allow a logical device to be identified with a particular physical location or slot. These lines are sourced from the VXIbus Slot 0 module to the Slot 1 and higher modules. There is one line to each module, located on P2 pin A30. A total of 12 MODID lines will connect between Slot 0 and the other modules in a maximally configured VXIbus subsystem. In addition to these 12 lines, Slot 0 has its own MODID line (MODID00). The purpose of the MODID lines is to

- Detect the presence of a module in a slot, even if that module has failed.
- Identify the geographical location (slot number) of a particular device.
- Indicate by lamp or other means the actual physical location of the module.

Slot 0 detects the presence of a module by the module pulling down its MODID line with a fixed resistor to ground. This allows any module, even if failed and unpowered, to be detected.

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The slot number of a device is identified by the Slot 0 module asserting a particular MODID line, and polling the MODID bit in each module's A16 configuration space to detect the selected device.

A visual indicator, such as a lamp, may be placed adjacent to a slot (or even on the module) to illuminate when that particular MODID line is driven true. This may be used to quickly identify the location of any module, including failed modules. Refer to figure 2-2 for rules for loading and driving the MODID lines.

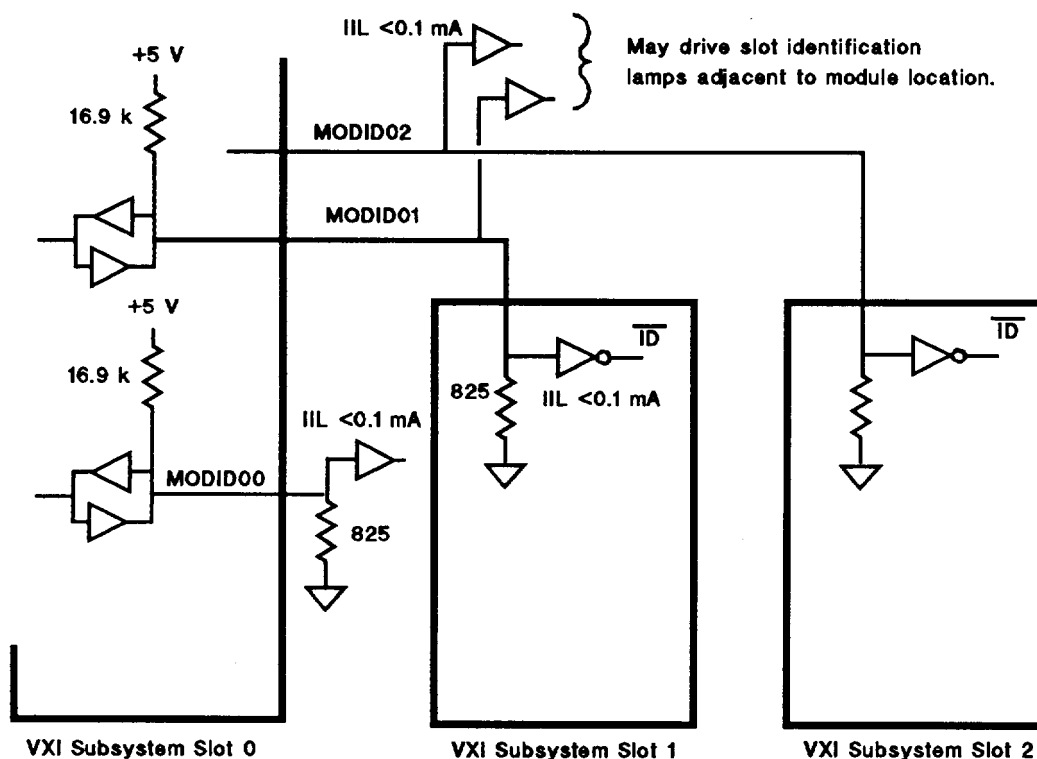


Figure 2-2 —Module ID lines

Rule 2.6.10. Each Slot 0 MODIDxx receiver shall comply with the VMEbus loading rules for High Current 3 State lines (IEEE Std 1014-1987 , Rule 6.14).

Rule 2.6.11. Each Slot 0 MODIDxx driver shall comply with the VMEbus driving rules for Standard 3 State lines (IEEE Std 1014-1987 , Rule 6.15).

Rule 2.6.12. Each Slot 0 device shall provide a 16.9 kΩ pull-up resistor from each MODID line to +5 V.

Rule 2.6.13. If a non-Slot 0 module accesses the MODID pin, then it shall provide an 825 Ω pull-down to ground in parallel with no more than 100 μA of leakage current on its MODID line.

Observation 2.6.3. 16.9 kΩ and 825 Ω are standard 1% metal film resistor values.

Rule 2.6.14. A VXIbus subsystem backplane shall provide an 825 Ω pull-down to ground on the MODID00 line.

Rule 2.6.15. The backplane shall not sink or source more than 100 μ A of leakage current to any MODID line.

Permission 2.6.1. VXIbus subsystem Slot 0 module may drive its MODID line true to illuminate its own module location lamp.

Observation 2.6.4. The proper placement of a Slot 0 module in a Slot 0 position may be verified by a read of its MODID00 state when all Slot 0 MODID drivers are disabled. A low state indicates that the module is in a Slot 0 position. A high state indicates that it is in another position.

2.6.2.3 TTLTRG0-7* (TTL trigger lines)

The TTLTRG* lines are open collector TTL lines used for intermodule communication. Any module, including Slot 0, may drive these lines and receive information on these lines. They are general purpose lines that may be used for trigger, handshake, clock, or logic state transmission. They are in a nonasserted (high) state until allocated by the user under program control. Some standard allocation procedures are defined. Standard protocols, synchronous (SYNC), asynchronous (ASYNCR), and start/stop (STST) are defined. To compensate for the larger rise time caused by the passive pullup termination, these protocols specify separate timing requirements for trigger sources and trigger acceptors. When used for logic state transmission, setup and hold times with respect to a clock edge are defined. Other protocols may be defined by a manufacturer.

Observation 2.6.5. IEEE Std 1014-1987 (VMEbus) recommends a 100 Ω system impedance for open-collector lines. Although the TTLTRG* lines will be terminated and meet the drive and load requirements for the VMEbus, the characteristic impedance of the traces on the backplane may be closer to 50 Ω . This allows ECL traces to share the same backplane layer, and may keep backplanes at a manufacturable number of planes and thickness for component insertion. This should not significantly affect performance of the TTLTRG* lines.

Rule 2.6.16. The backplane shall terminate all TTLTRG* lines as specified by IEEE Std 1014-1987, Fig 70.

Rule 2.6.17. A module's interface to any TTLTRG* signal line shall conform to the driving and loading rules for open collector lines (IEEE Std 1014-1987, 6.4.2.5).

Rule 2.6.18. Upon the assertion of SYSRESET*, all TTLTRG drivers shall become unasserted within 1 s after SYSRESET* becomes unasserted.

Rule 2.6.19. A module shall allocate any TTLTRG* lines to specific functions in groups of 1, 2, or 4.

Rule 2.6.20. If a module uses single-line TTLTRG* groups, then that module shall be user-programmable to connect to any TTLTRG* line.

Rule 2.6.21. If a module uses two-line TTLTRG* groups, then that module shall be user-programmable to connect all defined TTLTRG* group pairs. The defined TTLTRG* group pairs are lines 0 and 1, lines 2 and 3, lines 4 and 5, and lines 6 and 7.

Rule 2.6.22. If a module uses four-line TTLTRG* groups, then that module shall be user-programmable to connect to all defined TTLTRG* four-line groups. The defined TTLTRG* four-line group are lines 0, 1, 2, and 3; and lines 4, 5, 6, and 7.

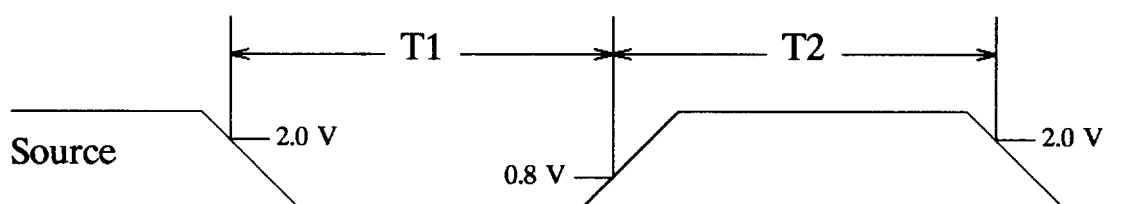
2.6.2.3.1 Standard TTLTRG* protocols

2.6.2.3.1.1 TTLTRG* synchronous (SYNC) trigger protocol

The TTLTRG* SYNC trigger protocol is a single-line broadcast trigger that does not require an acknowledge from any acceptors.

Rule 2.6.23. A TTLTRG* SYNC trigger source shall assert the trigger for a minimum time of T1 and shall not reassert the trigger for a minimum time of T2 as shown in figure 2-3.

Rule 2.6.24. A TTLTRG* SYNC trigger acceptor shall accept any trigger asserted for ≥ 10 ns, following a ≥ 10 ns deassertion.



Parameter label	Min	Max	Description
T1	30 ns		Minimum source assertion time
T2	50 ns		Minimum source nonassertion time

Figure 2-3 —TTLTRG* synchronous (SYNC) trigger protocol

2.6.2.3.1.2 TTLTRG * asynchronous (ASYNC) trigger protocol

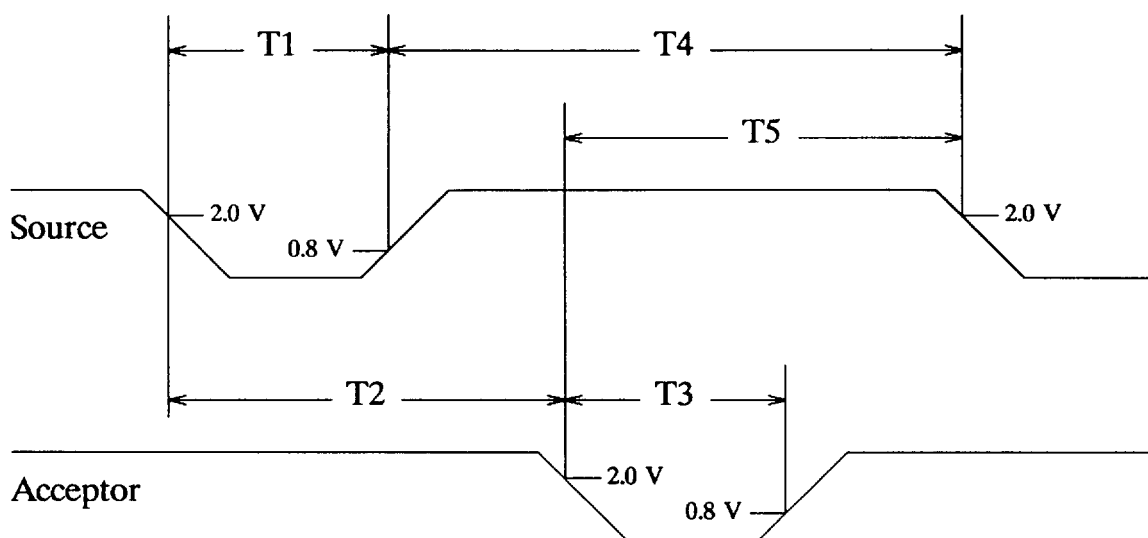
The TTLTRG * ASYNC trigger protocol is a two-line single-source, single-acceptor protocol. The source initiates an operation by asserting the lower numbered line of the allocated TTLTRG* line pair, while the acceptor acknowledges by asserting the higher numbered line of the TTLTRG* line pair. This is a useful trigger mode for handshaking between VXIbus modules and external instruments or between VXIbus mainframes.

Rule 2.6.25. A module implementing the TTLTRG* ASYNC trigger protocol shall source only on the lower numbered line of a TTLTRG* line pair.

Rule 2.6.26. A module implementing the TTLTRG* ASYNC trigger protocol shall acknowledge only on the higher numbered line of a TTLTRG * line pair.

Rule 2.6.27. If a module implements the TTLTRG* ASYNC trigger protocol, then it shall meet the timing requirements shown in figure 2-4.

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Parameter label	Min	Max	Description
T1	30 ns		Minimum source assertion time
T2	0 ns		Minimum acceptor response time
T3	30 ns		Minimum acceptor assertion time
T4	50 ns		Minimum source nonassertion time
T5	0 ns		Minimum acceptor acknowledge to source reassertion time

Figure 2-4 —Asynchronous (ASync) trigger protocol

Rule 2.6.28. A TTLTRG* ASync trigger source or acceptor shall accept any trigger asserted for ≥ 10 ns following a ≥ 10 ns deassertion.

2.6.2.3.1.3 TTLTRG* clock transmission

A TTLTRG* line may be used for a clock signal transmission.

Rule 2.6.29. If A TTLTRG* line is used for clock transmission, then it shall meet the timing requirements described for the TTLTRG* SYNC trigger protocol.

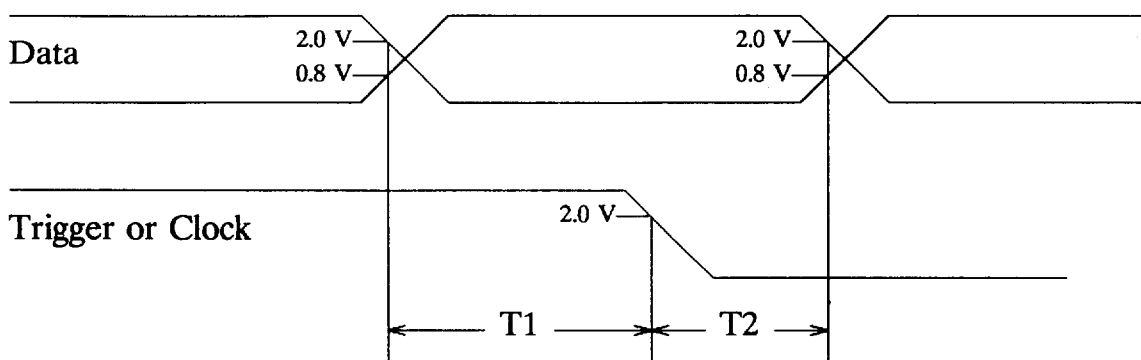
Observation 2.6.6. In a fully loaded VXIbus subsystem, the TTLTRG* rise time will approach 40 ns. For this reason, the falling edge is used for triggering.

2.6.2.3.1.4 TTLTRG* data transmission

The TTLTRG* lines can also be used for data transmission, where one of the TTLTRG* lines is used as a clock. Data may be synchronized to either the rising or falling edge of the clock, or both.

Rule 2.6.30. If a source uses TTLTRG* lines for data transmission on a falling clock edge, then the source shall meet the timing requirements shown in figure 2-5.

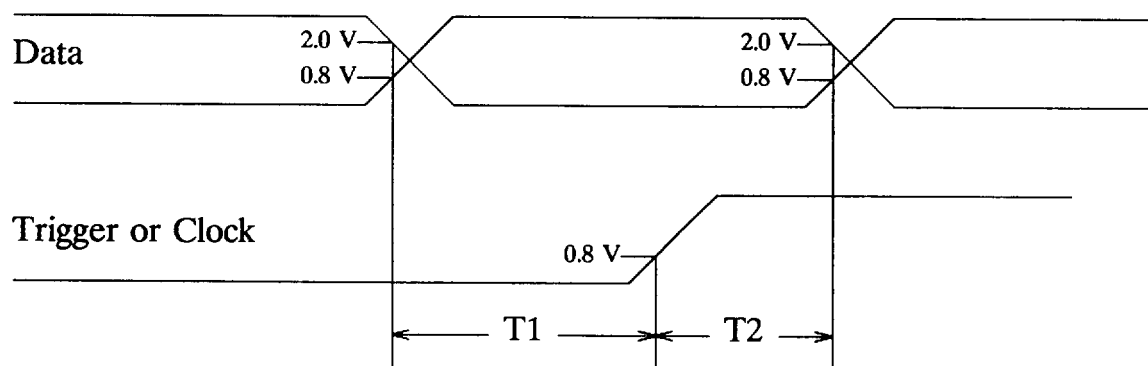
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Parameter label	Min	Max	Description
T1	40 ns		Data setup time
T2	10 ns		Data hold time

Figure 2-5 —TTLTRG* data transmission on falling clock edge

Rule 2.6.31. If a source uses TTLTRG* lines for data transmission on a rising clock edge, then the source shall meet the timing requirements shown in figure 2-6.



Parameter label	Min	Max	Description
T1	40 ns		Data setup time
T2	40 ns		Data hold time

Figure 2-6 —TTLTRG* data transmission on rising clock edge

Rule 2.6.32. A TTLTRG* data acceptor shall accept any data having data setup and hold times of ≥ 7 ns each.

2.6.2.3.1.5 Start/stop (STST) protocol

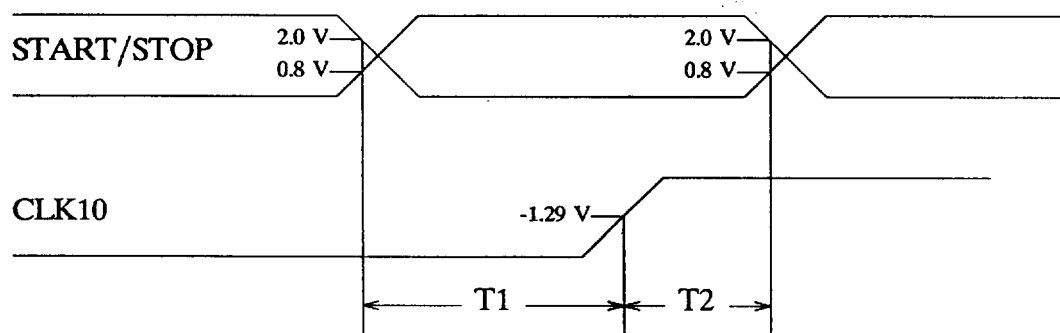
The start/stop (STST) protocol provides a method for starting and stopping module clusters synchronously. One TTLTRG* line is driven from the Slot 0 module and its state signifies start or stop operation. All participating modules respond to this line synchronously at the next CLK10 rising edge. Slot 0 has the responsibility to synchronize the start/stop signal with CLK10 so that setup and hold times are guaranteed for all acceptors. This may require an arbiter in Slot 0 to synchronize external events.

Rule 2.6.33. If a module implements STST protocol, then the start/stop line shall be user-programmable to connect to any TTLTRG* line.

Rule 2.6.34. If a Slot 0 module implements the STST protocol, then it shall meet the timing requirements shown in figure 2-7.

Rule 2.6.35. A TTLTRG* STST acceptor shall accept any STST command having data setup and hold times of ≥ 7 ns each.

Rule 2.6.36. When implementing the STST protocol, start shall be represented by a low (asserted) state on the START/STOP TTLTRG* line, and stop shall be represented by a high (unasserted) state on the START/STOP TTLTRG* line.



Parameter label	Min	Max	Description
T1	50 ns		Start/stop setup time
T2	15 ns		Start/stop hold time

Figure 2-7 —TTLTRG* start/stop timing

2.6.2.3.1.6 External trigger buffering

Observation 2.6.7. The TTLTRG* loading and driving rules require that these lines be buffered when extended outside a mainframe.

Recommendation 2.6.2. When extending a trigger operation external to a VXIbus chassis, the buffer module should source and accept signals as described in the standard external trigger buffer below.

2.6.2.3.1.6.1 Standard external trigger buffer

To maximize the compatibility between multiple VXIbus mainframes or a VXIbus mainframe and external instruments, a standard buffering scheme for TTLTRG* lines is recommended. A source has an output series impedance of $50\ \Omega$. Its open-circuit low-level output is $\leq 0.4\text{ V}$, and its open-circuit high-level output is $\geq 4.2\text{ V}$. Fifty-ohm cable is recommended for connection from the source module to other VXIbus mainframes or instruments. For highest performance, terminate the cable with $50\ \Omega$ at the furthest point from the source. The acceptor's threshold level is centered at 1.5 V with a loading impedance of $\geq 5\text{ k}\Omega$. The TTLTRG* sense remains uninverted (asserted state is low). See figure 2-8.

Observation 2.6.8. The standard external trigger buffer requires only simple buffering to implement the SYNC and ASYNC trigger protocols.

2.6.2.4 ECLTRG0-1 (ECL trigger lines)

The ECLTRG lines are intended to be an intermodule timing resource. These two lines are bussed the length of the VXIbus subsystem backplane. Any module, including the Slot 0 module, may drive these lines and receive information from these lines. These lines are single-ended ECL, and have a system impedance of $50\ \Omega$. The asserted state is defined as logical high.

Rule 2.6.37. Each ECLTRG line shall be terminated with $50\ \Omega$ to -2 V at each end of the backplane. This requires that any driver be able to drive $25\ \Omega$.

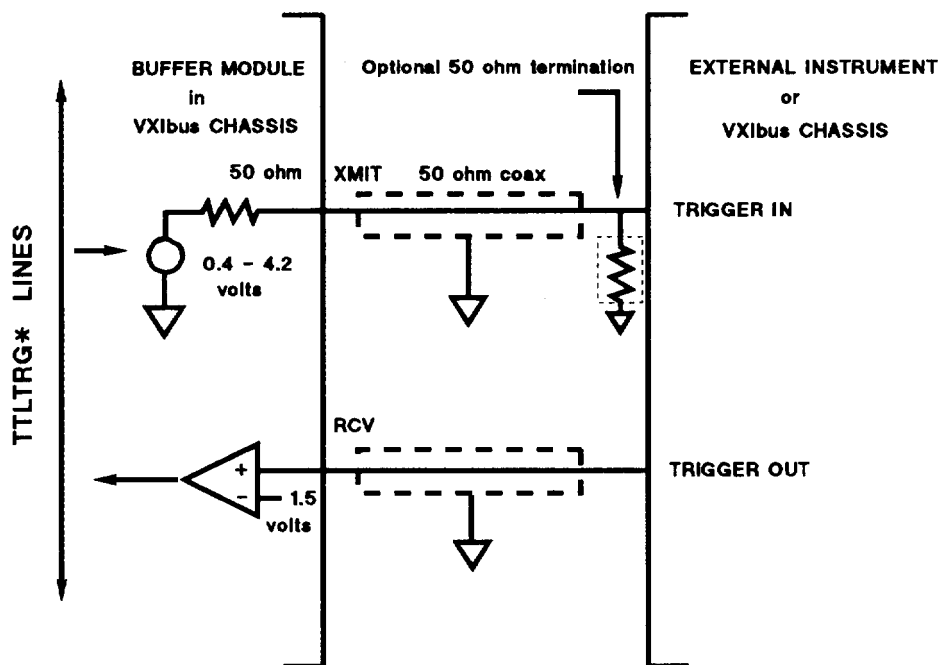


Figure 2-8 —External trigger buffering

Rule 2.6.38. The maximum ECLTRG trace length from the P2 connector pad on any module shall not exceed 2.54 cm (1.0 in.).

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Recommendation 2.6.3. The transmission line impedance connecting the P2 connector to the ECLTRG receiver/driver circuitry should be 50 Ω .

Recommendation 2.6.4. A module that senses the ECLTRG lines should have a 150 Ω resistor in series with the transmission line connecting the ECL trigger lines on the P2 connector to the line receiver.

Rule 2.6.39. Each module shall not have more than one equivalent driver/receiver load on any ECLTRG line.

Rule 2.6.40. If a module drives the ECLTRG bus, then it shall use ECL drivers that provide a low output level that is less (more negative) than the -2 V termination supply, e.g., 10H123.

Observation 2.6.9. Using drivers that produce a high-impedance low level for ECLTRG lines eliminates the glitching that occurs when ECL devices are WIRE-OR'ed.

Rule 2.6.41. Upon the assertion of SYSRESET*, all ECLTRG drivers shall become unasserted within one (1) second after SYSRESET * becomes unasserted.

Rule 2.6.42. ECLTRG lines shall be allocated in groups of one or two and meet the same allocation rules as defined for the TTLTRG* lines.

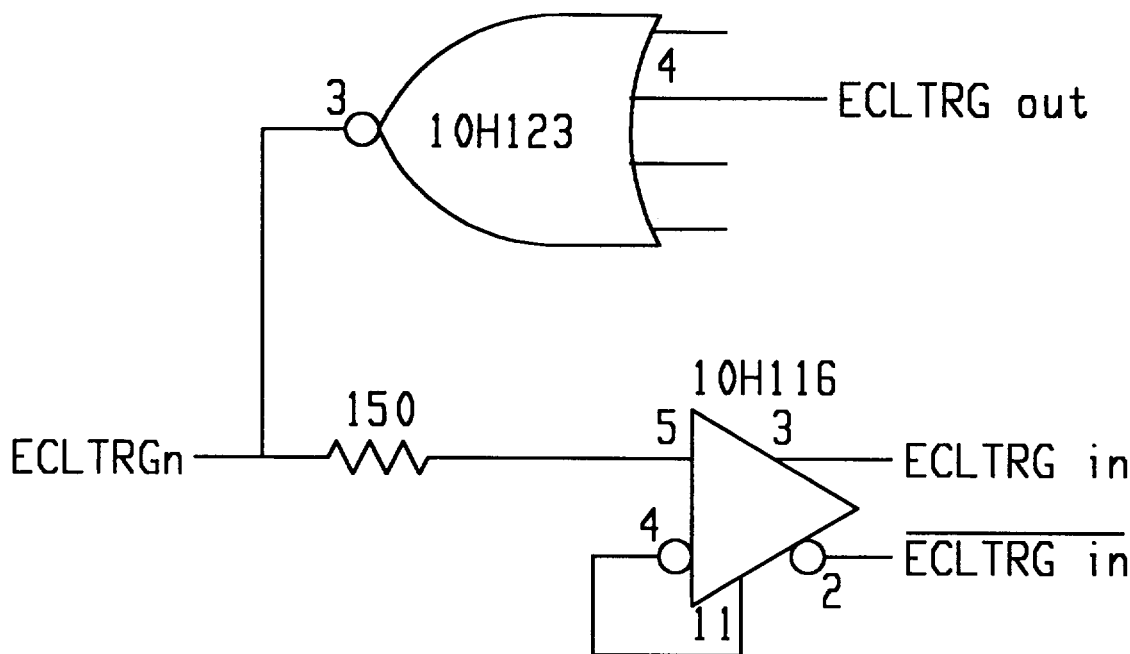


Figure 2-9 —Typical ECLTRG interface

2.6.2.4.1 Standard ECLTRG protocols

The ECLTRG lines have a set of defined protocols corresponding to the TTLTRG* protocols. These protocols are defined in the following subclauses.

2.6.2.4.1.1 ECLTRG synchronous (SYNC) trigger protocol

The ECLTRG SYNC trigger protocol is a single-line broadcast trigger that does not require an acknowledge from any acceptors.

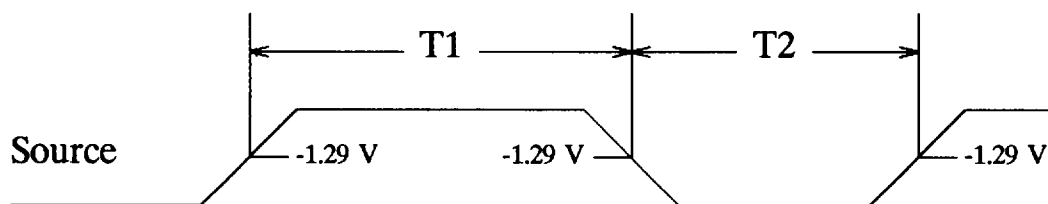
Rule 2.6.43. An ECLTRG SYNC trigger source shall assert the trigger for a minimum time of T_1 and shall not reassert the trigger for a minimum time of T_2 as shown in figure 2-10.

Rule 2.6.44. An ECLTRG SYNC trigger acceptor shall accept any trigger asserted for ≥ 6 ns following a ≥ 6 ns deassertion.

2.6.2.4.1.2 ECLTRG asynchronous (ASYNC) trigger protocol

The ECLTRG ASYNC trigger protocol is a two-line, single-source, single-acceptor protocol. The source initiates an operation by asserting the lower numbered line of the allocated ECLTRG line pair, while the acceptor acknowledges by asserting the higher numbered line of the ECLTRG line pair. This is a useful trigger mode for handshaking between VXIbus modules and external instruments.

Rule 2.6.45. A module implementing the ECLTRG ASYNC trigger protocol shall source only on the lower numbered line of an ECLTRG line pair.



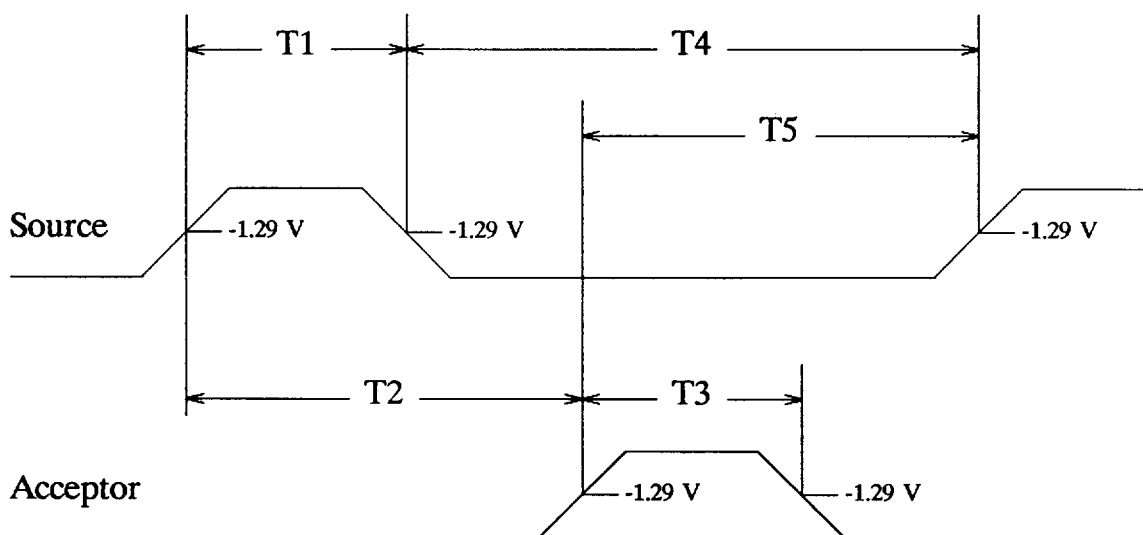
Parameter label	Min	Max	Description
T1	8 ns		Minimum source assertion time
T2	8 ns		Minimum source nonassertion time

Figure 2-10 — ECLTRG synchronous (SYNC) trigger protocol

Rule 2.6.46. A module implementing the ECLTRG ASYNC trigger protocol shall acknowledge only on the higher numbered line of a ECLTRG line pair.

Rule 2.6.47. If a module implements the ECLTRG ASYNC trigger protocol, then it shall meet the timing requirements shown in figure 2-11.

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Parameter label	Min	Max	Description
T1	8 ns		Minimum source assertion time
T2	0 ns		Minimum acceptor response time
T3	8 ns		Minimum acceptor assertion time
T4	8 ns		Minimum source nonassertion time
T5	0 ns		Minimum acceptor acknowledge to source reassertion time

Figure 2-11 —ECLTRG asynchronous (ASYNC) trigger protocol

Rule 2.6.48. An ECLTRG ASYNC trigger source or acceptor shall accept any trigger asserted for ≥ 6 ns following a ≥ 6 ns deassertion.

2.6.2.4.1.3 ECLTRG clock transmission

An ECLTRG line may be used for a clock signal transmission.

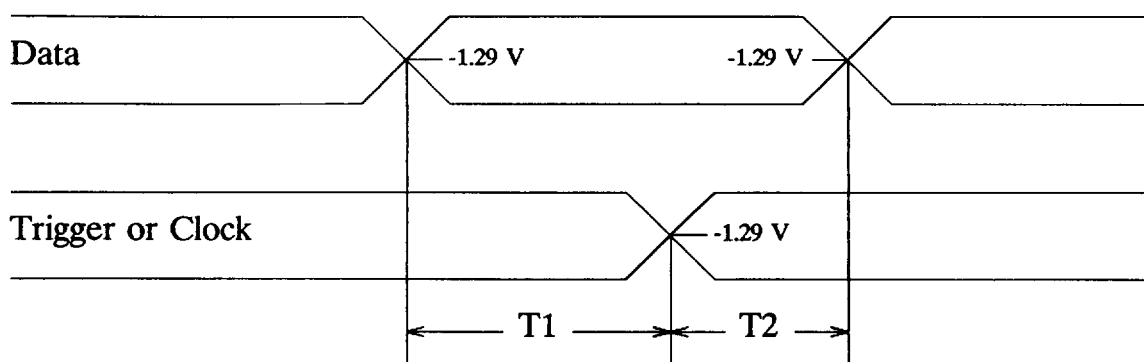
Rule 2.6.49. If an ECLTRG line is used for clock transmission, then it shall meet the timing requirements described for the ECLTRG SYNC trigger protocol.

2.6.2.4.1.4 ECLTRG data transmission

The ECLTRG lines can also be used for data transmission, where one of the ECLTRG lines is used as a clock. Data may be synchronized to either the rising or falling edge of the clock, or both.

Rule 2.6.50. If a source uses ECLTRG lines for data transmission, then the source shall meet the timing requirements shown in figure 2-12.

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Parameter label	Min	Max	Description
T1	8 ns		Data setup time
T2	4 ns		Data hold time

Figure 2-12 —ECLTRG data transmission

Rule 2.6.51. An ECLTRG data acceptor shall accept any data with a setup time of ≥ 6 ns and a hold time of ≥ 2 ns.

2.6.2.4.1.5 Extended start/stop (ESTST) protocol

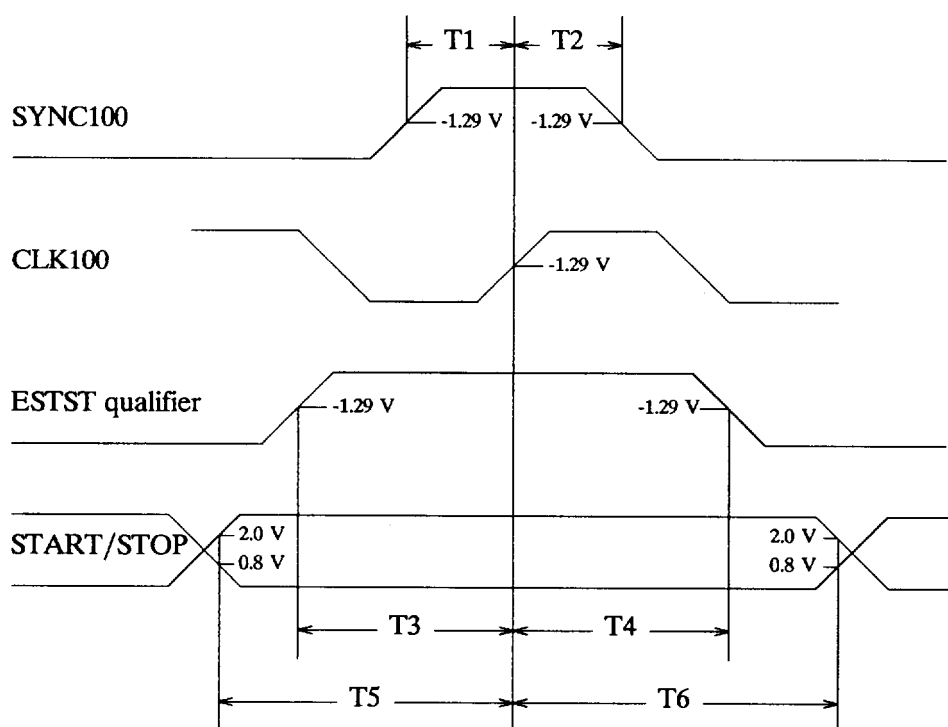
Extended start/stop (ESTST) protocol is the natural extension of the start/stop (STST) protocol to D-size modules. Because the modules may contain P3 and utilize CLK100 as their instrument clock, three additional signals have been added to the STST protocol (CLK100, SYNC100, and an ECLTRG line). The ECLTRG line determines whether an ESTST operation is initiated, while the same TTLTRG line used to transmit the start/stop value for STST devices also determines the start or stop operation for ESTST devices.

In the ESTST protocol, a Slot 0 SYNC100 driver (see 2.6.3.2, SYNC100) selects a particular CLK100 clock edge to initiate the START or STOP command. An ECLTRG line indicates whether the SYNC100 pulse is related to the ESTST protocol. This line is known as the ESTST qualifier line. Since the CLK10 and CLK100 signals are synchronized, the Slot 0 module can always qualify a CLK100 edge having a fixed-phase relationship to CLK10. This fixed-phase relationship, over a series of ESTST operations, guarantees fixed and repeatable delays between modules paced by CLK10 (STST) and those paced by CLK100 (ESTST). The TTLTRG* line used to indicate start/stop for the STST protocol also determines start or stop for the ESTST protocol.

Rule 2.6.52. If a module implements the ESTST protocol, then the module shall be user programmable to select any ECLTRG line as the ESTST qualifier line.

Rule 2.6.53. ESTST qualifier true shall be represented by a high state of the selected ECLTRG ESTST qualifier line, and ESTST qualifier false shall be represented by a low state.

Rule 2.6.54. A Slot 0 module implementing the ESTST protocol shall meet the timing requirements of figure 2-13.



Parameter label	Min	Max	Description
T1	4.0 ns	7.5 ns	SYNC100 setup time
T2	3.5 ns	6.0 ns	SYNC100 hold time
T3	13.0 ns		ESTST qualifier setup time
T4	11.0 ns		ESTST qualifier hold time
T5	50.0 ns		Start/stop setup time
T6	15.0		Start/stop hold time

Figure 2-13 —CLK100, SYNC100, and ECLTRG start/stop timing

Rule 2.6.55. A Slot 0 module implementing the ESTST protocol shall meet the timing requirements for the STST protocol.

Rule 2.6.56. An ESTST acceptor shall accept a SYNC100 setup value for ≥ 2 ns and held for ≥ 0.5 ns, an ESTST qualifier value setup for ≥ 4 ns and held for ≥ 2 ns, and an STST value setup ≥ 7 ns and held for ≥ 7 ns with respect to the CLK100 edge.

2.6.2.4.1.6 External trigger buffering

Recommendation 2.6.5. Since the ECLTRG asserted sense is opposite the TTLTRG* asserted sense, the ECLTRG signal should be inverted by the standard external trigger buffer. This allows compatibility of external ECLTRG and TTLTRG* signals.

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Observation 2.6.10. By meeting the loading and driving rules for ECLTRG lines, a module is prohibited from extending these lines external to the chassis without buffering these lines. See 2.6.2.3.1.6.1, Standard external trigger buffer.

2.6.2.5 SUMBUS

The SUMBUS is a $25\ \Omega$, $\pm 0.8\text{ V}$ analog summing node that is bussed the length of the VXIbus subsystem backplane. It is intended that any module be able to drive or receive from this line. Each module can drive this line using an analog current source driver. Each module may receive information from this bus through a high-impedance receiver, such as a high-impedance analog buffer amplifier.

2.6.2.5.1 SUMBUS backplane requirements

Rule 2.6.57. The SUMBUS shall be terminated to signal ground through $50 \pm 1\ \Omega$ at each end of the backplane.

Rule 2.6.58. The backplane shall supply a SUMBUS protection network that clamps the SUMBUS voltage within the range $\pm 3.0\text{ V}$ for all SUMBUS input currents in the range of $\pm 520\text{ mA}$.

Rule 2.6.59. The SUMBUS protection network shall not source or sink more than $\pm 1.0\ \mu\text{A}$ nor load with greater than 30 pF for SUMBUS voltages in the range $\pm 1.0\text{ V}$.

Observation 2.6.11. Low leakage diodes may be required to meet the SUMBUS leakage requirement.

2.6.2.5.2 SUMBUS module driver and receiver requirements

Rule 2.6.60. A receiver on the SUMBUS shall have an equivalent input impedance of $\geq 10\text{ k}\Omega$ in parallel with $\leq 3\text{ pF}$.

Rule 2.6.61. A SUMBUS output current source shall have an equivalent output impedance of $\geq 10\text{ k}\Omega$ in parallel with $\leq 4\text{ pF}$.

Rule 2.6.62. A SUMBUS output current source shall have $\pm 0.8\text{ V}$ minimum compliance.

Rule 2.6.63. A SUMBUS output current source shall not source or sink more than 40 mA .

Recommendation 2.6.6. Because all modules may drive the SUMBUS at the same time, a module designer should consider the total dynamic range of a SUMBUS output current source and be able to adjust the maximum output current accordingly. This will keep the signal within the compliance ($\pm 0.8\text{ V}$) region.

Rule 2.6.64. SUMBUS output current sources and receivers shall not be located more than 2.54 cm (1.0 in) from the P2 SUMBUS pad.

Rule 2.6.65. When a module's SUMBUS module output current source is disabled, the module shall not source more than $\pm 1.0\ \mu\text{A}$ into the SUMBUS.

2.6.2.6 Local bus

The local bus is a daisy-chained bus that is defined by adjacently installed modules. The backplane connects from the LBUSC pins of Slot N to the LBUSA pins of Slot N+1 (see figure 2-1). No local bus lines are extended beyond Slot 12. Several classes of signal level are allowed and may be transmitted via this bus. To ensure that modules that produce incompatible levels are not installed in adjacent slots, a keying mechanism has been provided. The local bus key provides support for TTL, ECL, and analog communication. Each module indicates with the mechanical key on the faceplate which classes of signals it may source or accept nondestructively on each side of its local bus. The particular key position for each of the signal classes, as well as sensor-only devices, is specified in 2.7, Mechanical specifications. Sensor-only devices are modules that can nondestructively accept signals of a number of classes, but do not source any signals of their own. See table 2-3.

Table 2-3 —Logical classes of LBUS signals

Number	Class	–limit	+limit	Drive limit
1	TTL	–0.5 V	+5.5 V	200 mA
2	ECL	–5.46 V	0.0 V	50 mA
3	ANALOG LOW	–5.5V	+5.5V	50Ω drive
4	ANALOG MED	–16.0 V	+16.0 V	500 mA
5	ANALOG HIGH	–42.0 V	+42.0 V	500 mA
6	RESERVED			

Rule 2.6.66. Modules shall not drive more than ± 42 V onto any LBUS line.

Rule 2.6.67. Modules shall not drive more than 500 mA dc current into any LBUS line.

Rule 2.6.68. The backplane resistance between any LBUS line and any adjacent pin shall be greater than 10.0 MΩ.

Rule 2.6.69. The di/dt on any LBUS line shall not exceed ± 100 mA/ns.

Recommendation 2.6.7. Multimodule instrument systems that utilize the local bus for intrasystem communications should be built with anchor and expander protocol. An anchor module has no connections on LBUSA lines. It may drive or receive LBUSC lines. An expander module may drive or receive LBUSA or LBUSC lines. Expanders should be placed in adjacent slots (of higher number) to the anchor. This protocol always guarantees compatibility between adjacent module groups without empty slots.

Rule 2.6.70. Any module that accesses the LBUS lines shall indicate its class on its local bus keys.

Rule 2.6.71. A module shall not exceed the voltage specified for its class under any loading conditions.

Observation 2.6.12. If a module provides a direct connection (an electrical short) between LBUSA lines and LBUSC lines, the keying mechanism should indicate that the module will source on LBUSA and LBUSC any class it accepts on either LBUSA or LBUSC, respectively.

Rule 2.6.72. A module shall not indicate on its key the reserved signal class.

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Observation 2.6.13. The keying mechanism cannot prevent a destructive condition in all situations. It is good practice for a module manufacturer to protect modules from destruction by any signals within the class it accepts.

Rule 2.6.73. The Slot 0 P2 LBUSA key shall indicate TTL class.

Rule 2.6.74. The Slot 0 P3 LBUSA and LBUSC keys shall indicate ECL class.

Rule 2.6.75. The mainframe (if it supports VXIbus Subsystem P2) shall provide a Slot 0 P2 LBUSC key that indicates TTL class.

Rule 2.6.76. The mainframe (if it supports VXIbus Subsystem P3) shall provide a Slot 0 P3 LBUSC key that indicates ECL class.

Permission 2.6.2. A device that nondestructively senses signals up to ± 16 V, but does not source any signals or provide direct connection between LBUSA and LBUSC, may provide a single local bus key tab for ± 16 V sensor-only operation.

Permission 2.6.3. A device that nondestructively senses all classes of signals up to ± 42 V, but does not source any signals or provide direct connection between LBUSA and LBUSC, may provide no local bus key tabs for ± 42 V sensor-only operation. Such a device cannot cause a destructive condition.

Observation 2.6.14. A device that does not access the local bus does not provide any local bus keys.

Observation 2.6.15. Size A, B, and C modules do not provide P3 local bus keys.

2.6.2.7 RSV2-3 (RESERVED)

These pins are reserved.

Rule 2.6.77. Modules and backplanes shall not make any connections to RSV pins.

2.6.3 The VXIbus subsystem P3 connector

For higher performance instrumentation, the VXIbus also defines the P3 connector. As with P2, alternate pin definitions of P3 may coexist in VXIbus systems, but any one VXIbus subsystem must exist in contiguous slots. Again, Slot 0 plays a unique role in delivering system resources on P3, such as high-speed clocking and trigger routing. In particular, VXIbus P3 adds the following:

- a) Additional +5 V, -5.2 V, -2 V, ± 24 V, and ± 12 V power
- b) One hundred MHz differential clock that is synchronous with the P2 10 MHz clock
- c) A synchronizing signal for 100 MHz clock edge selection
- d) Four additional ECL trigger lines, for a total of 6
- e) Twenty-four additional local bus lines, for a total of 36
- f) “Star trigger” lines for precision module-to-module timing

See table 2-4.

2.6.3.1 CLK100

CLK100 is a 100 MHz system clock. It is sourced from Slot 0 and distributed to Slots 1-12 on P3 (see table 2-5). The Slot 0 CLK100 output is differential ECL. It is buffered on the backplane and distributed to each module slot as a

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single-source, single-destination differential ECL signal in a manner similar to that of CLK10. The distribution delays are matched to provide a tight timing relationship between modules. The backplane buffering provides a high level of intermodule isolation.

Rule 2.6.78. The CLK100 frequency sourced from Slot 0 shall be 100 MHz. Its accuracy shall be equal to or better than ± 100 ppm (.01%), over its specified operating temperature and time.

Observation 2.6.16. A Slot 0 module may generate CLK100 internally, or it may derive CLK100 from an external frequency source.

Rule 2.6.79. CLK100 duty cycle shall be 50% $\pm 20\%$ when measured at the 50% transition level.

Rule 2.6.80. If CLK100 is switched between different clock sources, then the minimum clock width, high or low, shall not be less than 2.5 ns or more than 1.0 μ s during switching. The minimum time between two successive transitions of the same polarity shall not be less than 9.5 ns.

Rule 2.6.81. CLK100 shall be synchronous to CLK10.

Observation 2.6.17. The absolute timing relationship between CLK10 and CLK100 is not specified. This relationship may be produced by deriving CLK10 from CLK100 or deriving CLK100 from CLK10.

Rule 2.6.82. The CLK100 and SYNC100 backplane distribution network shall not insert more than 2.0 ns timing skew between CLK100 and SYNC100 at any slot.

Observation 2.6.18. If a 10H101 distribution buffer is used for CLK100 or SYNC100, the trace lengths should be matched within 1 ns (approximately 15 cm [6 in]).

Rule 2.6.83. Each slot CLK100 shall be driven by a unique backplane buffer output.

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Table 2-4 —P3 pin definitions

Pin Number	ROWa signal mnemonic	ROWb signal mnemonic	ROWc signal mnemonic	Pin Number
1	ECLTRG2	+24 V	+12 V	1
2	GND	−24 V	−12 V	2
3	ECLTRG3	GND	RSV4	3
4	−2V	RSV5	+5 V	4
5	ECLTRG4	−5.2 V	RSV6	5
6	GND	RSV7	GND	6
7	ECLTRG5	+5 V	−5.2 V	7
8	−2V	GND	GND	8
9	LBUSA12	+5 V	LBUSC12	9
10	LBUSA13	LBUSC15	LBUSC13	10
11	LBUSA14	LBUSA15	LBUSC14	11
12	LBUSA16	GND	LBUSC16	12
13	LBUSA17	LBUSC19	LBUSC17	13
14	LBUSA18	LBUSA19	LBUSC18	14
15	LBUSA20	+5 V	LBUSC20	15
16	LBUSA21	LBUSC23	LBUSC21	16
17	LBUSA22	LBUSA23	LBUSC22	17
18	LBUSA24	−2 V	LBUSC24	18
19	LBUSA25	LBUSC27	LBUSC25	19
20	LBUSA26	LBUSA27	LBUSC26	20
21	LBUSA28	GND	LBUSC28	21
22	LBUSA29	LBUSC31	LBUSC29	22
23	LBUSA30	LBUSA31	LBUSA30	23
24	LBUSA32	+5 V	LBUSC32	24
25	LBUSA33	LBUSC35	LBUSC33	25
26	LBUSA34	LBUSA35	LBUSC34	26
27	GND	GND	GND	27
28	STARX+	−5.2V	STARY+	28
29	STARX−	GND	STARY−	29
30	GND	−5.2 V	−5.2 V	30
31	CLK100+	−2 V	SYNC100+	31
32	CLK 100−	GND	SYNC 100−	32

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Rule 2.6.84. CLK100 shall be distributed differentially from Slot 0.

Rule 2.6.85. The backplane CLK100 distribution traces shall be designed for 50 Ω .

Rule 2.6.86. The CLK100 backplane distribution network shall not insert more than 2.0 ns timing skew between CLK100 signals at any two slots.

Rule 2.6.87. The absolute delay of CLK100 from Slot 0 to any module shall not exceed 8 ns.

Rule 2.6.88. If a module accesses the CLK100 signals, then it shall provide 50 Ω termination on CLK100+ and CLK100–, with no more than two equivalent ECL loads.

Recommendation 2.6.8. Use a 10H101 to buffer and fan out CLK100.

Table 2-5—P3 Slot 0 pin definitions

Pin Number	ROWa signal mnemonic	ROWb signal mnemonic	ROWc signal mnemonic	Pin number
1	ECLTRG2	+24 V	+12 V	1
2	GND	–24 V	–12 V	2
3	ECLTRG3	GND	RSV4	3
4	–2 V	RSV5	+5 V	4
5	ECLTRG4	–5.2 V	RSV6	5
6	GND	RSV7	GND	6
7	ECLTRG5	+5 V	–5.2 V	7
8	–2 V	GND	GND	8
9	STARY12+	+5 V	STARX01+	9
10	STARY12–	STARY01–	STARX01–	10
11	STARX12+	STARX12–	STARY01+	11
12	STARY11+	GND	STARX02+	12
13	STARY11–	STARY02–	STARX02–	13
14	STARX11+	STARX11–	STARY02+	14
15	STARY10+	+5 V	STARX03+	15
16	STARY10–	STARY03–	STARX03–	16
17	STARX10+	STARX10–	STARY03+	17
18	STARY09+	–2 V	STARX04+	18
19	STARY09–	STARY04–	STARX04+	19
20	STARX09+	STARX09–	STARY04+	20

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Table 2-5—P3 Slot 0 pin definitions (Continued)

Pin Number	ROWa signal mnemonic	ROWb signal mnemonic	ROWc signal mnemonic	Pin number
21	STARY08+	GND	STARX05+	21
22	STARY08–	STARY05–	STARX05–	22
23	STARX08+	STARX08–	STARY05+	23
24	STARY07+	+5 V	STARX06+	24
25	STARY07–	STARY06–	STARX06–	25
26	STARX07+	STARX07–	STARY06+	26
27	GND	GND	GND	27
28	STARX+	–5.2 V	STARY+	28
29	STARX–	GND	STARY–	29
30	GND	–5.2 V	–5.2 V	30
31	CLK100+	–2 V	SYNC100+	31
32	CLK100–	GND	SYNC100–	32

2.6.3.2 SYNC100

The synchronization signal SYNC 100 is used to synchronize multiple devices with respect to a given rising edge of CLK100. This provides very tight time coordination between modules. The SYNC100 signal is distributed from Slot 0 to Slots 1–12, with individual backplane buffers for each slot. The SYNC100 signal can be compared to the GPIB group execute trigger command in function, but with greatly improved time coordination. As the Slot 0 module drives the SYNC100 and CLK100 signals, it may also may be programmed to drive one or more ECLTRG lines in order to qualify the SYNC100 action. An example of this protocol is the ESTST protocol described under ECLTRG trigger protocols.

A Slot 0 module implementing the SYNC 100 function will provide an arbiter to synchronize external events to CLK100 and meet the guaranteed setup and hold times for the SYNC100 signal. This guarantees that all affected modules will trigger on the same CLK100 clock edge. SYNC100 is a nominally 10 ns pulse and may be initiated by any type of external or internal event—an external BNC trigger; a software register write; the state of any of the TTLTRG*, ECLTRG, LBUS, or STAR lines; or any other signal synchronized by the Slot 0 arbiter. Refer to the timing diagram on figure 2-13.

Observation 2.6.19. SYNC 100 delay matching relative to CLK100 is called out under CLK100 matching rules.

Recommendation 2.6.9. Use a 10H101 to buffer and fan out SYNC100.

Rule 2.6.89. Slot 0 modules shall provide ≥ 4.0 ns of setup time from SYNC100 to the rising edge of CLK100.

Rule 2.6.90. Slot 0 modules shall provide ≥ 3.5 ns of hold time from rising edge of CLK100 to SYNC 100.

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Recommendation 2.6.10. Slot 0 modules that provide SYNC100 support should be designed such that the SYNC100 recycle rate is ≤ 50 ns.

Rule 2.6.91. Each module slot SYNC100 shall be driven by a unique backplane buffer output.

Rule 2.6.92. SYNC 100 shall be distributed differentially from Slot 0.

Rule 2.6.93. The backplane SYNC100 distribution traces shall be designed for $50\ \Omega$.

Rule 2.6.94. The SYNC100 backplane distribution network shall not insert more than 2.0 ns timing skew between SYNC100 signals at any two slots.

Rule 2.6.95. If a module accesses the SYNC100 signals, then it shall provide $50\ \Omega$ termination on SYNC100+ and SYNC100-, with no more than two equivalent ECL loads.

2.6.3.3 STARX and STARY

STARX and STARY provide intermodule asynchronous communication. Two STAR lines are connected between each module slot and Slot 0. Slot 0 may provide a cross-matrix switch that can route signals between any two STARX or STARY lines. It may also broadcast a signal received on one STAR line to a group of STAR lines. The STAR lines are bidirectional, providing additional flexibility.

Rule 2.6.96. The STARX and STARY backplane distribution network shall not insert more than 2.0 ns timing skew between any two STAR signals.

Rule 2.6.97. STARX and STARY shall be driven differentially.

Rule 2.6.98. The backplane STAR distribution traces shall be designed for $50\ \Omega$.

Rule 2.6.99. If a module accesses the STAR signals, then it shall provide $50\ \Omega$ termination on STAR+ and STAR-, with no more than a single equivalent ECL driver load and a single equivalent ECL receiver load.

Rule 2.6.100. Modules that can both drive and receive STARX or STARY shall use bidirectional ECL drivers, e.g., 10H123. When the module is programmed to receive, the STAR+ and STAR- drivers shall be forced into the high-impedance state ($V_{ol} \leq -2.0$ V).

Rule 2.6.101. A D-size Slot 0 module shall provide a default differential signal to all STARX and STARY lines that are not being driven by another module.

Permission 2.6.4. If a Slot 0 module does not support STAR bus routing, it may meet the above rule by connecting a $50\ \Omega$ resistor between STAR+ lines and ground.

Rule 2.6.102. The absolute delay of any STAR line between Slot 0 and any module shall not exceed 5 ns.

Rule 2.6.103. The backplane shall not connect to the STARX+, STARX-, STARY+, and STARY- pins of the Slot 0 backplane connector.

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Permission 2.6.5. The Slot 0 module may access the STARX+, STARX–, STARY+, and STARY– pins.

Observation 2.6.20. Allowing all modules, including Slot 0, to access the STAR lines allows construction of modules that may operate in any slot position, including Slot 0.

2.6.3.4 ECLTRG2-5

These lines are functionally the same as the ECLTRG0-1 lines on P2 described in 2.6.2.4, ECLTRG0-1, and meet the same rules.

2.6.3.5 LBUS12-35

These lines are functionally the same as the LBUS00-11 lines on P2 described in 2.6.2.6, Local bus, and meet the same rules.

2.6.3.6 RSV4-7

These lines are functionally the same as the RSV2-3 lines on P2 described in 2.6.2.7, RSV2-3, and meet the same rules.

2.6.4 Backplane

The backplane is the common signal and power distribution network for all modules. As such, it must be very well designed so as not to introduce noise into the system.

Observation 2.6.21. Noise should be minimized on the ECLTRG lines, clock lines, and SUMBUS lines. It is desirable to maintain time jitter to ≤ 25 ps. This requires that noise be limited to ± 9 mV, assuming an ECL slew rate of 2.75 V/ns.

Rule 2.6.104. All backplane ECL transmission paths shall be designed for 50 Ω nominal characteristic impedance.

Observation 2.6.22. When TTL lines share a layer of the backplane with 50 Ω ECL transmission lines, the TTL signal characteristic impedance may also be near 50 Ω . This should provide satisfactory operation (see IEEE Std 1014-1987, Observation 6.13).

Suggestion 2.6.1. See the *MECL System Design Handbook* [B5]³, for more backplane and microstrip design information.

2.6.4.1 ECL signal levels

The signal levels present on the backplane ECL lines are summarized in table 2- 6.

³The numbers in brackets correspond to those of the bibliography in annex E.

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Table 2-6 —Backplane ECL signal levels

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{OH}	Output logic level “1” (HIGH)	−0.980	−0.9	−0.735	V
V_{OL}	Output logic level “0” (LOW)	−1.950	−1.75	−1.630	V
V_{BB}	Logic switching threshold		−1.29		V

2.7 Mechanical specifications

2.7.1 Introduction

Information is provided in this subclause to ensure that VXIbus modules, backplanes, mainframes, and associated mechanical accessories are dimensionally compatible. figure 2-14 through 2-39 show mechanical details for chassis, module, and backplane assemblies.

The mechanical dimensions given in this subclause are based on IEEE Std 1101-1987 and IEC Publications 297-3 [B3] and 603-2 [B4]. The electrical characteristics for VXIbus connectors, as specified here, supersede Publication 603-2 where they differ.

IEC publication 603-2 describes a family of connector types that are identified by labels of the form:

603-2-IEC-xxxxxx-xxx

All of the P1/J1, P2/J2, and P3/J3 connectors used on VXIbus modules and backplanes are members of this family. In this subclause, the label 603-2-IEC-xxxxxx-xxx is used in references to all of these connector types as a group. The label 603-2-IEC-C096Mx-xxx is used when referring to the 96-pin male connector types within this family that are used on the VXIbus modules. 603-2-IEC-C096Fx-xxx is used when referring to the 96-pin female connector types that are used on backplanes.

Figure 2-14 is a front view of a typical VXIbus mainframe. In the mainframe shown, modules are inserted into the mainframe from the front, in a vertical plane, with the component face of the module board on the right.

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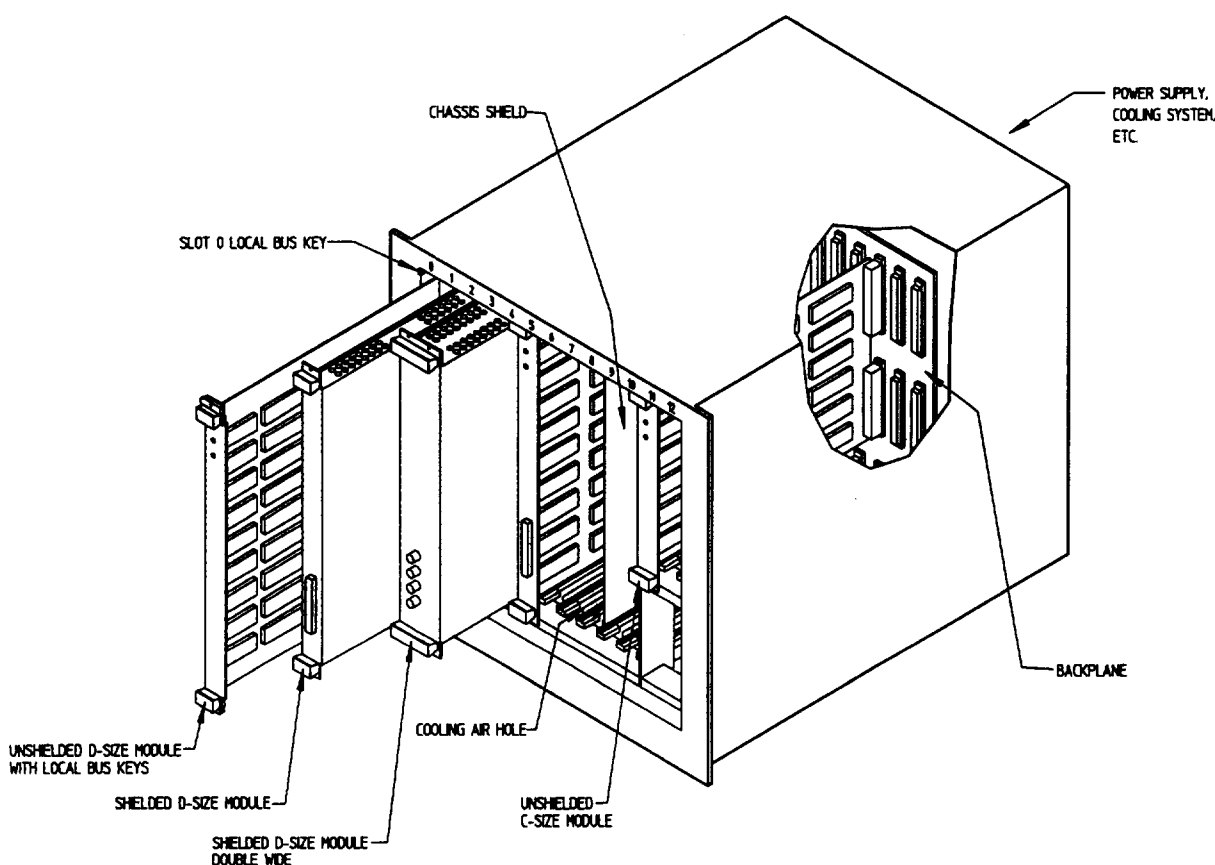


Figure 2-14 —Typical D-size mainframe

2.7.2 Module specifications

2.7.2.1 VXIbus boards and modules

Rule 2.7.1. VXIbus modules shall fit into one of the following four size classifications:

- Single-height module *typically* containing a board with dimensions 100 mm (3.937 in) high $\times$ 160 mm (6.299 in) deep will be referred to as a “size A” module.
- Double-height module *typically* containing a board with dimensions 233.35 mm (9.187 in) high $\times$ 160 mm (6.299 in) deep will be referred to as a “size B” module.
- Double-height module *typically* containing a board with dimensions 233.35 mm (9.187 in) high $\times$ 340 mm (13.386 in) deep will be referred to as a “size C” module.
- Triple-height module *typically* containing a board with dimensions 366.7 mm (14.437 in) high $\times$ 340 mm (13.386 in) deep will be referred to as a “size D” module.

Rule 2.7.2. Size A and size B boards and board assemblies shall be designed according to the dimensions given in IEEE Std 1014-1987.

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Observation 2.7.1. Size A and size B boards and board assemblies are designed for a mainframe with 20.32 mm (0.8 in) spacing between slots.

Rule 2.7.3. Size C and size D modules shall be contained within the envelope specified in figures 2-17, 2-18, and 2-21.

Rule 2.7.4. Size C and size D modules shall be designed for a mainframe with 30.48 mm (1.2 in) spacing between slots.

Observation 2.7.2. Typical size C and size D modules will contain a board as shown in figures 2-15 and 2-16.

Rule 2.7.5. Modules shall provide the board edge feature as specified in figure 2-21 to allow proper insertion into a mainframe. This feature shall be $1.6 + 0.2$ mm (0.063 ± 0.008 in) thick.

Recommendation 2.7.1. Size C and D modules should be designed around a board as specified in figures 2-15 and 2-16. This will ensure proper position of connectors, front panel, card edge, etc.

2.7.2.1.1 Board connectors

Size A modules have only one backplane connector, called the P1 connector. Size B and C modules have either one or two backplane connectors, called the P1 and P2 connectors. Size D modules have one, two, or three connectors, called the P1, P2, and P3 connectors. In all modules, the P1 connector is mandatory; P2 and P3 are optional.

Rule 2.7.6. P1, P2, and P3 connectors shall meet or exceed the mechanical specifications of a 603-2IEC-C096Mx-xxx class 2 connector.

Observation 2.7.3. 603-2-IEC class 2 connectors have a minimum mechanical endurance of 400 insertion/extraction cycles.

Rule 2.7.7. The mounting location of the P1, P2, and P3 connectors shall be consistent with the hole patterns specified in figures 2-15 and 2-16.

Rule 2.7.8. The P1, P2, and P3 connectors shall be positioned as shown in figures 2-19 and 2-20.

2.7.2.1.2 Board assemblies

The board assembly typically consists of a PCB and connectors, as defined above, and electronic components.

Rule 2.7.9. Solder fillets, traces, shielding, and components on VXIbus boards shall not be closer than 2.5 mm (0.098 in) from the top and bottom edges of the board to guarantee clearance between them and the board guides. Figures 2-15 and 2-16 show these dimensions for size C and D modules.

Rule 2.7.10. If a module contains components sensitive to orientation (e.g., mercury switches), then that module's specifications and labels shall clearly state its limitations.

Recommendation 2.7.2. An orientation-sensitive module should be designed to be installed vertically with its component side to the right, or horizontally with its component side up.

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2.7.2.1.3 Module width

Permission 2.7.1. Size C or D modules that require more than the standard spacing may be designed to occupy more than one slot, adding an integer multiple of 30.48 mm (1.2 in) to the module width.

Observation 2.7.4. Component height, lead length, shield positions, etc., of the typical module are shown in figure 2-18.

Permission 2.7.2. Module shields as shown in figures 2-17 and 2-18 may be omitted or their positions changed, but must remain within the defined envelope.

Recommendation 2.7.3. Include module shields to improve electromagnetic compatibility (EMC), ease of handling, etc.

2.7.2.1.4 Board warpage, lead length, shield height, and component height

Rule 2.7.11. All size A and B board assemblies shall meet IEEE Std 1014-1987, 7.2.6.

Rule 2.7.12. For shielded size C and D modules, the outer surface of the solder-side shield, including warpage, shall be greater than or equal to 1.57 mm (0.062 in) from the intermodule separation plane when installed. The outer surface of the component-side shield, including warpage, shall be greater than or equal to 0.15 mm (0.006 in) from the intermodule separation plane when installed. Refer to figure 2-18.

Recommendation 2.7.4. To account for warpage, the nominal solder-side shield should be greater than 2.07 mm (0.082 in) from the intermodule separation plane. The nominal component-side shield should be greater than 0.65 mm (0.026 in) from the intermodule separation plane. Refer to figure 2-18.

Rule 2.7.13. For unshielded size C and D modules, leads and solder-side components, including warpage, shall be greater than or equal to 3.96 mm (0.156 in) from the intermodule separation plane when installed. Components, including warpage, shall be greater than or equal to 2.54 mm (0.100 in) from the intermodule separation plane when installed. Refer to figure 2-18.

2.7.2.2 Front panel

This subclause provides the mechanical specifications for the double- and triple-height module front panels and associated hardware. Figure 2-22 shows a double-height, single-width (C size) front panel. Figure 2-23 shows a triple-height, single-width (D size) front panel.

Rule 2.7.14. All modules shall include a front panel.

Rule 2.7.15. Each module, regardless of size, shall have a front panel conforming to the size of the mainframe in which it is used.

Permission 2.7.3. Additional hardware may be utilized to fill a front-panel gap when inserting a small module into a larger mainframe.

Rule 2.7.16. front-panel screws shall be provided to secure the top and bottom of the panel to the mainframe, and their screw threads shall be M2.5 × 0.45 pitch. See figure 2-22.

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Rule 2.7.17. Front panels shall make contact with chassis ground in the area surrounding the retention screws as shown in figures 2-22 and 2-23. This surface shall be conductive, smooth, and free of all protrusions.

2.7.2.2.1 Front-panel mounting

Rule 2.7.18. All modules shall comply with the test dimension shown in figures 2-26 and 2-27. This dimension is from the rear face of the front panel to the rear face of the backplane connector.

2.7.2.2.2 Front-panel dimensions

Rule 2.7.19. Single-width size C and D front panels shall be designed to the dimensions shown in figures 2-22 and 2-23, respectively.

Rule 2.7.20. If a size C or D module occupies more than one slot, then the width of the front panel shall be 30.18 mm (1.188 in) plus an integral multiple (N) of 30.48 mm (1.200 in), where N is the number of slots that the module occupies minus one.

Rule 2.7.21. If local bus lockout keys are required on a module, then the front panel shall be notched as shown in figures 2-22 and 2-23.

Suggestion 2.7.1. Include the lockout key notch on all front panels. This will simplify removal of a module when the adjacent module is keyed.

2.7.2.2.3 Filler panels

Rule 2.7.22. Filler panels shall be used in any empty slots.

Observation 2.7.5. Filler panels are often required by safety regulations, and may be necessary for cooling and EMC performance.

Rule 2.7.23. Size C and D filler panels shall conform to dimensions given in figures 2-24 and 2-25, respectively.

Rule 2.7.24. Size A and B filler panels shall conform to IEEE Std 1014-1987, 7.3.4.

2.7.2.2.4 Board injectors/ejectors

Insertion and extraction forces of the module relative to the mainframe may be very high. These forces are greatest for size D modules that use all three backplane connectors.

Recommendation 2.7.5. Modules using three or more of the 96-pin 603-2-IEC-C096Mx-xxx connectors should provide an injector/ejector system.

Observation 2.7.6. The insertion force for three 96-pin 603-2-IEC-C096Mx-xxx connectors can be as high as 270 N (60.69 lbf).

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Permission 2.7.4. An injector and/or ejector system may be provided on any module size.

Rule 2.7.25. Modules equipped with ejectors or injectors shall not interfere with mainframes designed to the VXIbus specification or IEEE Std 1014-1987. See figures 2-37 and 2-38.

Observation 2.7.7. Refer to 7.3.3, Injection/ejection, for more information.

2.7.2.2.5 Front-panel interface

Rule 2.7.26. External wiring to a module, if any, shall exit the module only through the front-panel I area.

Observation 2.7.8. External wiring is defined as any connectors, cables, etc., that carry signals or interfaces out of the mainframe in which the module is installed. The above rule does not exclude module-to-module wiring.

Rule 2.7.27. Connector and front-panel interfaces shall not leave significant gaps in the front panel, or disrupt proper airflow within the system.

Observation 2.7.9. Although the terms “significant gaps” and “proper air flow” can be rather broadly interpreted, it is intended that a manufacturer be very cautious about the front-panel components chosen.

2.7.2.2.6 Front-panel handles

Rule 2.7.28. Handles shall not interfere with the local bus lockout keys of adjacent modules.

Suggestion 2.7.2. Handle width and position should comply with the dimensions shown in figures 2-22 and 2-23. This will prevent interference with local bus lockout keys.

Observation 2.7.10. Injection and ejection constraints may require the use of a handle with dimensions different from those in figures 2-22 and 2-23.

2.7.2.3 Module shielding

Shields are often included in modules to improve EMC performance, ease of handling, etc. Refer to figures 2-17 and 2-18.

Permission 2.7.5. Module shields may be tied to chassis ground or circuit ground.

Rule 2.7.29. Size C and D modules shall provide room for the optional mainframe chassis shield as shown in figures 2-17 and 2-18.

Observation 2.7.11. The envelope as defined in figure 2-17 ensures that module shields do not contact adjacent modules.

Observation 2.7.12. The use of box type plug-in units as specified by IEC 297-3 [B3] and IEEE Std 1101-1987 may be limited. Maximum module length, injector surfaces, and nonremovable card guides may be incompatible. Refer to figures 2-17, 2-21, and 2-38.

Permission 2.7.6. A grounding shield may be provided around each 96-pin connector as shown in figure 2-34. This will be referred to as the connector shield.

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Observation 2.7.13. Connector shield contacts may or may not be removable. However, removable contacts may be advisable for some modules. The module manufacturer should evaluate the applicability of removable contacts for each module.

Permission 2.7.7. A module may make electrical contact with a compatible adjacent module at any point in the area near the front panel as specified in figure 2-17. This contact may be implemented by means of gasketing, clips, etc.

Rule 2.7.30. If gasketing is installed for contact with a compatible adjacent module, then it shall be installed on the solder side only, and it shall be compressible to fit within the intermodule separation plane.

Recommendation 2.7.6. Gasketing installed for contact with a compatible adjacent module should be removable. This will allow installation adjacent to unshielded or otherwise incompatible modules.

Recommendation 2.7.7. The areas specified in figure 2-17 for contact with adjacent modules should be chassis-ground and conductive.

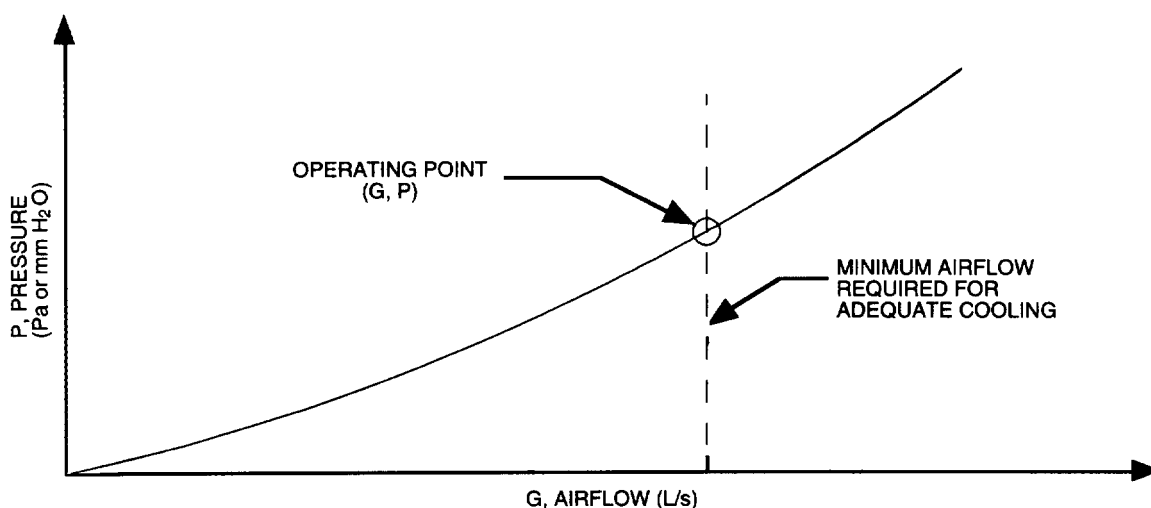
2.7.2.4 Module cooling

Rule 2.7.31. Cooling air shall flow as shown in figures 2-29, 2-30, and 2-39. Airflow direction is from P3 to P1.

Rule 2.7.32. Cooling requirements shall be established for all modules and included in product specifications. The specification shall include the maximum ambient operating temperature and the operating point. (*Example:* 55 °C ambient maximum operating temperature. For 10 °C internal rise, 4.9 Pa (0.5 mm H₂O @ 1.5 L/s.)

Recommendation 2.7.8. Label the module with the cooling specification. This will facilitate system integration (see figure 2-42).

Recommendation 2.7.9. A “resistance” pressure drop versus airflow graph should be established and included in the product specifications. This is useful for more detailed system integration. For example:



Observation 2.7.14. An example of simplified test setup and procedures for establishing module cooling requirements is shown in figure 2-40.

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Observation 2.7.15. Great care must be taken with the design of modules that require cooling air to flow in parallel paths. Examples are modules with multiple boards and modules with components on the solder side of the main board. In particular, the power dissipation of solder-side components may be limited by the restricted access of cooling air. The module designer is responsible for assuring that resistance to air flow is consistent with the cooling requirements for each parallel path.

2.7.2.5 Module power

Recommendation 2.7.10. Attach an abbreviated version of the power-supply voltage and current requirements to the module. This will facilitate system integration.

2.7.2.6 Module keying

Lockout keys are provided to serve as an impediment to local bus incompatibilities.

Rule 2.7.33. If modules access a local bus, then lockout keys shall be provided, consistent with the particular bus accessed. The lockout keys shall conform to the specifications in figure 2-28.

Rule 2.7.34. If lockout keys are required on a module, then they shall be installed by the manufacturer, consistent with the definition of the product.

Observation 2.7.16. Lockout keys are not intended to provide failsafe protection. Accidental damage may still occur if incompatible modules are forced next to each other on the local bus.

2.7.2.7 Module environmental

Recommendation 2.7.11. Modules should be tested for temperature, humidity, vibration, shock, etc., according to the procedures described in IEC Publication 68 [B2]. The results should be included in product specifications, along with module mass.

Observation 2.7.17. It is a system integrator's responsibility to select modules and mainframes that are appropriate for the environmental requirements of the application.

2.7.3 Mainframe specifications

Rule 2.7.35. VXIbus mainframes shall fit into one of four size classifications:

- a) A mainframe that provides the J 1 backplane and allows the insertion of an A-size module only will be referred to as a "A-size" mainframe, and conform to IEEE Std 1014-1987 requirements for subracks.
- b) A mainframe that allows the insertion of a B-size module, maximum, will be referred to as a "B-size" mainframe, and conform to IEEE Std 1014-1987 requirements for subracks. The J1 backplane is mandatory; J2 is optional.
- c) A mainframe that allows the insertion of a C-size module, maximum, will be referred to as a "C-size" mainframe. The J1 backplane is mandatory; J2 is optional.
- d) A mainframe that allows the insertion of a D-size module, maximum, will be referred to as a "D-size" mainframe. The J1 backplane is mandatory; J2 and J3 are optional.

Recommendation 2.7.12. Allowances should be made for the insertion of A-size modules into B-size mainframes, the insertion of A- and B-size modules into C-size mainframes, and the insertion of A-, B-, and C-size modules into D-size mainframes.

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Observation 2.7.18. Additional hardware and removable card guides may be required to allow the insertion of smaller modules into a larger mainframe.

Rule 2.7.36. If the insertion of smaller modules is allowed into a larger mainframe, then the mainframe manufacturer shall specify a procedure and/or means for the insertion of the smaller modules.

Permission 2.7.8. Mechanical and/or electrical means may be used for the adaptation of a smaller module to a larger mainframe.

Rule 2.7.37. C- and D-size mainframes shall be designed for 30.48 mm (1.2 in) slot spacing, as shown in figures 2-29 and 2-30.

Rule 2.7.38. A- and B-size mainframes shall be designed to 20.32 mm (0.8 in) spacing.

Rule 2.7.39. C- and D-size mainframes shall conform to the dimensions and tolerances shown in figures 2-29, 2-30, 2-35, and 2-36. This ensures that connectors mate properly and that modules will fit in the mainframe without interference.

Rule 2.7.40. With the mainframe oriented with the modules vertical, P1 at the top, component side of module boards to the right; Slot 0 shall be the leftmost slot of any VXibus subsystem.

Observation 2.7.19. This rule does not mandate mainframe orientation; it only establishes the position of Slot 0 relative to mainframe orientation.

Suggestion 2.7.3. If vertical orientation of the modules is desired, then Slot 0 should be at the left. If horizontal orientation of the modules is desired, then Slot 0 should be at the bottom.

Rule 2.7.41. Card guides shall be made of nonconductive material, or be isolated from chassis ground.

Observation 2.7.20. Removable card guides may permit the use of box style plug-in units as specified by IEC 297-3 [B3] and IEEE Std 1101-1987.

2.7.3.1 Backplanes

Rule 2.7.42. Each backplane shall be a single monolithic board, within any slot position.

Rule 2.7.43. Backplane connectors for C- and D-size mainframes shall be positioned as shown in figures 2-31 and 2-32.

Permission 2.7.9. Backplanes may deviate from figures 2-31 and 2-32 in structure and mounting methods.

Observation 2.7.21. Typical C- and D-size backplanes are shown in figures 2-31 and 2-32 for reference. Adherence to these drawings will ease the task of mounting and aligning the backplane within the mainframe.

Rule 2.7.44. If components other than connectors are placed on the component side of a C- or D-size backplane, then they shall be placed outside the shaded areas specified in figure 2-33. Nonconductive components shall be less than 12.2 mm (0.480 in) in height. Conductive components shall be less than 10.0 mm (0.394 in) in height.