

IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164)

Sponsor

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of the
IEEE Computer Society**

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IEEE Standards Board

Abstract: This standard is embodied in the Std_logic_1164 package declaration and the semantics of the Std_logic_1164 body. An annex is provided to suggest ways in which one might use this package.

Keywords: Std_logic_1164, VHDL model interoperability

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Introduction

[This introduction is not a part of IEEE Std 1164-1993, IEEE Standard Multivalued Logic System for VHDL Model Interoperability (Std_logic_1164).]

This package provides a standard datatype system for the declaration of ports and signals used in modeling digital components in VHDL. Use of this package with its defined logic values and operators is intended to provide a mechanism for writing VHDL component models that have well-defined behavior when connected to other models adhering to this standard.

Development of the Std_logic_1164 package:

The work of this committee is the culmination of efforts by several groups with the same goals working over a period of over three years. The EIA (Electronic Industries Association) and the VDEG (VHDL Design Exchange Group) have been working on the problem of interoperable VHDL component models since the standardization of VHDL by the IEEE in 1987. The work at the EIA has been guided by John Wilner, Jack Kinn, and Len Finegold in their efforts to produce a specification for procuring interoperable VHDL component models. The work at the VDEG was guided by Moe Shahdad, Ghulam Nurie, and its last chair, Victor Berman, who merged this group with the IEEE Model Standards Group in order to promote a unified standard. The VDEG group has since disbanded. At present there is agreement by the IEEE P1164 and EIA 567 groups on this standard.

Between 1989 and this date, many individuals made valuable contributions to the development of this standard. At the time of approval of the standard, the members of the working group were:

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1. Overview

1.1 Scope

This standard is embodied in the Std_logic_1164 package declaration and the semantics of the Std_logic_1164 package body along with this clause 1 documentation. The information annex A is a guide to users and is not part of this standard, but suggests ways in which one might use this package.

1.2 Conformance with this standard

The following conformance rules shall apply as they pertain to the use and implementation of this standard:

- a) No modifications shall be made to the package declaration whatsoever.
- b) The Std_logic_1164 package body represents the formal semantics of the implementation of the Std_logic_1164 package declaration. Implementers of this package body may choose to simply compile the package body as it is; or they may choose to implement the package body in the most efficient form available to the user. Users shall not implement a semantic that differs from the formal semantic provided herein.