

IEEE Recommended Practice for Latchup Test Methods for CMOS and BiCMOS Integrated-Circuit Process Characterization

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IEEE Recommended Practice for Latchup Test Methods for CMOS and BiCMOS Integrated-Circuit Process Characterization

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of the
IEEE Electron Devices Society

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Abstract: Recommendations are provided for the layout and test methods required to characterize properly latchup behavior in CMOS and BiCMOS integrated circuit processes or other processes that have similar lateral PNPN topographical layout characteristics. The aim is to allow the characterization of an integrated circuit process architecture so that different approaches can be scientifically compared. This allows the evaluation of the process capabilities on a "worst-case" recommended structure and test method independent of actual integrated circuit product topographical latchup layout practices. Test structures and test philosophy are covered.

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Foreword

(This Foreword is not a part of IEEE Std 1181-1991, IEEE Recommended Practice for Latchup Test Methods for CMOS and BiCMOS Integrated-Circuit Process Characterization.)

The need for this document was primarily initiated by semiconductor fabrication foundries. Customers who had an interest in CMOS Latchup would invariably ask what were the latchup characteristics of the process. One answer was that it depended on the structure used. There was no standard way, however, of defining a latchup structure, and no defacto standard of any kind had emerged. Companies with in-house fabrication and merchant semiconductor suppliers had the same question from their own internal needs.

The Latchup Committee was formed by semiconductor technology engineers from foundries, captive suppliers, and merchant suppliers to come to a consensus on what structures should be used and how they should be tested.

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IEEE Recommended Practice for Latchup Test Methods for CMOS and BiCMOS Integrated-Circuit Process Characterization

1. General

1.1 Scope. This document provides recommendations for the layout and test methods required to properly characterize the latchup behavior in CMOS and BiCMOS¹ integrated-circuit processes or other processes that have similar lateral PNPN topographical layout characteristics.

1.2 Purpose. This recommended practice is intended to provide recommendations to enable the characterization of an integrated-circuit process architecture.² This document describes how to characterize “worst-case” CMOS integrated-circuit layout topography for PNPN latchup. This document is intended to be used to test the behavior of a CMOS *process*, and not a CMOS *product*.

Establishing a recommended practice allows the scientific comparison of different approaches to processes or process architectures by establishing a workable methodology of topographical layout and electrical measurement procedures. By doing so, technical papers can be written so that comparisons of different engineering approaches can be better made.

Establishing a recommended practice allows the scientific comparison of similar CMOS processes so that a purchaser of custom integrated circuits can use a common test methodology to evaluate and compare the *processes* of one or more vendors or foundries of custom integrated circuits. This allows the evaluation of the process capabilities on a worst-case recommended structure and test method independent of actual integrated-circuit *product* topological latchup layout practices (which should be topographically best-case layouts, and not worst-case layouts).

It is *not* the purpose of this recommended practice to be applied to semiconductor products. For product testing, EIA/JEDEC JC-40.2-87-16 [1]³ should be used.

2. References

- [1] EIA/JEDEC JC-40.2-87-16, “A Standardized Test Procedure for the Characterization of LATCHUP in CMOS Integrated Circuits,” Draft 3.2 (January 29, 1987), EIA/JEDEC JC-40.2 CMOS Logic Standardization Committee.⁴

¹BiCMOS is a process that, at the very minimum, combines an isolated, high-performance NPN transistor along with a CMOS process. The test methods described in this document illustrate the CMOS-based latchup structures only. Currently, this document does not address the contribution of an isolated NPN transistor to CMOS latchup phenomenon. However, the basic approach described in this document is applicable to generating a valid structure for an NPN/CMOS latchup structure.

²Architecture, in this context, is sometimes called “process integration” or just simply a “process.” It refers to the way in which the structure of the process is put together.

³The numbers in brackets correspond to the References in Section 2.

⁴JEDEC publications are available from JEDEC, 2001 I Street NW, Washington, DC 20006, USA.

3. Definitions and Nomenclature

3.1 Definitions

3.1.1 Latchup. A malfunction of a CMOS integrated circuit caused by a parasitic PNPN structure.

Junction-isolated CMOS integrated-circuit technologies inherently have parasitic PNPN structures. In order to achieve high packing density in integrated-circuit products, the circuit design engineer or layout designer often does the topological layout such that the N-Channel MOSFETs are placed as close as possible to P-Channel MOSFETs. In so doing, the worst-case PNPN parasitic structure is created. In normal operation with a properly-developed process, this PNPN parasitic structure is inactive and has no detrimental effect on the integrated circuit.

If a fault condition occurs, it is possible to forward bias one of the junctions in the PNPN structure, and, if there is sufficient fault voltage and current available, the PNPN structure will turn on. When the PNPN structure turns on (latchup is initiated), the voltage across it collapses to a series summation of

- (1) A forward diode drop
- (2) A bipolar transistor collector-to-emitter saturation voltage
- (3) IR drop in parasitic resistance(s) of the PNPN structure

Typically, this voltage may be in the 1–2 V range. Depending on the character of the PNPN structure and the external electrical conditions, latchup may be either sustained or transient. In either case, the CMOS integrated circuit will normally malfunction. It may also cause other electronic devices used along with the CMOS integrated circuit to malfunction as well.

CMOS latchup is normally caused by fault conditions external to the integrated-circuit product. Topological layout solutions, which sometimes add to the chip area, are usually effective at mitigating latchup on input and output pins of CMOS integrated circuits. The effectiveness of such topological solutions (such as guard rings) are both process architecture and layout related and, thus, are beyond the scope of this document. It is also possible, however, to initiate latchup *internally* in an integrated circuit. Therefore, it is important to be able to properly characterize process-related CMOS latchup phenomena in order to improve process designs and not solely rely on topological layout solutions.

If a latchup stimulus is applied to the input node of a test device; the output-node current simply increases from its initial value (approximately zero current for the devices described in this standard); the output-node voltage does not drop; and, upon removal of the input-node stimulus, the output-node current returns to its initial value (taking into account current increase due to junction temperature increase); then the device can be defined as “latchup immune” to that stimulus.

Figs 1 and 2 illustrate some of the basic SCR definitions as used in this document.

3.1.2 Overvoltage. A voltage between any pins that exceeds the related positive power supply; specifically in cases where a P+ to N- diode may be forward biased.

3.1.3 Undervoltage. A voltage between any pins that exceeds (in the negative direction) the related negative power supply; specifically in cases where an N+ to P- diode may be forward biased.

3.1.4 Trigger Voltage. The voltage required to trigger an SCR structure at the terminal that initiates a latchup condition.

3.1.5 Trigger Current. The current required to trigger an SCR structure at the terminal that initiates a latchup condition.

3.1.6 Trigger Source. The source of trigger voltage or current.

3.1.7 Trigger Duration. The duration of trigger voltage or current.

3.1.8 Holding Current. The dc current that will sustain the holding voltage condition.

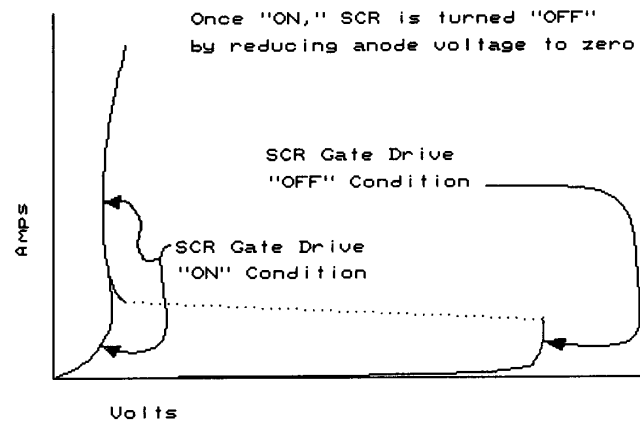


Fig 1
IV Characteristic of a Four-Layer SCR Device

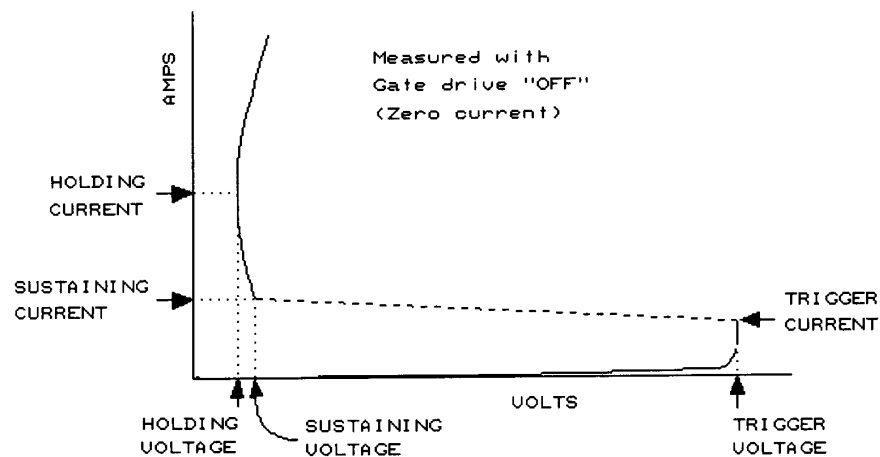


Fig 2
Holding Current and Holding Voltage at the End Terminals of a PNP Structure

3.1.9 Holding Voltage. The sum of a forward diode drop plus a $V_{ce(sat)}$ of a bipolar transistor plus IR drop in the device under test. It is measured at the holding current value. It is the minimum voltage at which sustained latchup current will flow.

3.1.10 Minimum Sustaining Current. The minimum sustained latchup current that will flow. It is important to point out that measurement of this current is *test-setup dependent*.

3.1.11 Sustaining Voltage. The voltage at which minimum sustaining current will flow.

3.1.12 Bipolar Latching Voltage. A reduced breakdown voltage occurring when the intrinsic base voltage is higher than the emitter voltage.

Bipolar transistors exhibit two forms of breakdown voltage from collector to emitter. One is avalanche voltage, which is normally observed with the base connected to the emitter, or BV_{ces} . The other is latching voltage, which is normally observed with the base terminal open circuited. In this condition, very low current breakdown is approximately equal to BV_{ces} , but increasing current causes the collector-emitter voltage to drop substantially. This voltage is known as LV_{ceo} or BV_{ceo} . Latching voltage can also occur with a resistance connected from base to emitter, or when the extrinsic or intrinsic base voltage is allowed to be greater than the emitter voltage. See Fig 3.

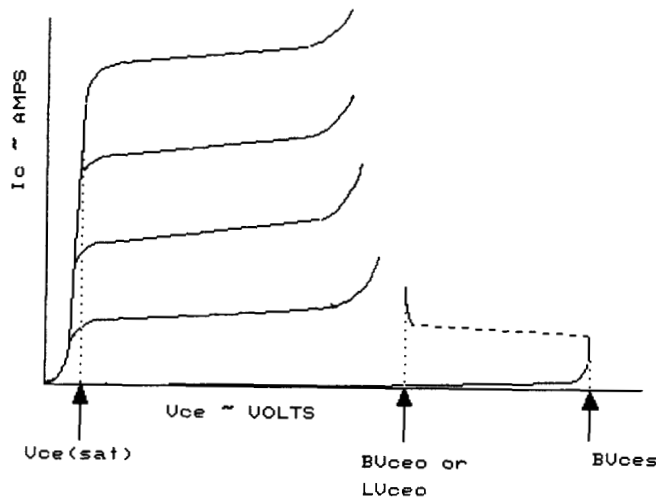


Fig 3
Bipolar LV_{ceo} Latching Voltage is not SCR Latchup

3.1.13 MOS Snapback Voltage. A reduced breakdown voltage occurring when channel current is flowing.

MOS snapback voltage is not SCR latchup. MOS snapback voltage is initiated in a lateral MOS device by channel hot-electron hole-electron pair production in the drain region of the transistor. The minority carriers (holes for N-Channel transistors) expelled from the drain region into the substrate (base) region trigger a lateral parasitic bipolar transistor and create a breakdown condition similar to collector-emitter latching voltage (known as LV_{ceo} or BV_{ceo}) in normal bipolar transistors. This latching voltage is not SCR latchup. See Fig 4.

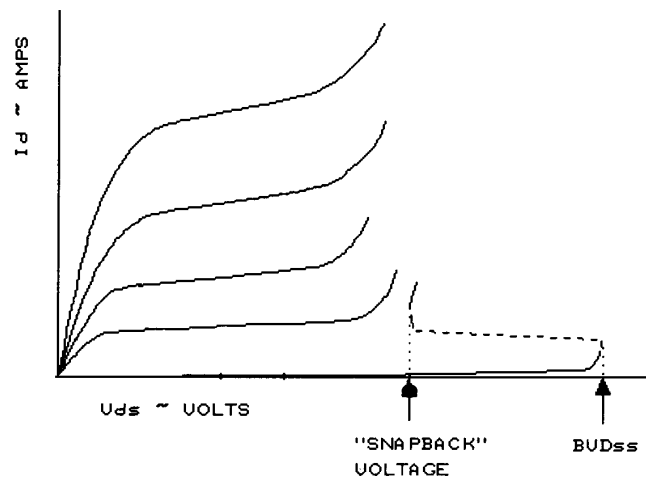


Fig 4
MOS Snapback Voltage is not SCR Latchup

3.1.14 Cool-Down Time. The period of time between successive applications of trigger pulses, or the period of time between the removal of the supply voltage and the application of the next trigger pulse.

3.1.15 Test Conditions. The ambient temperature, supply voltage, current limits, radiation source, input/output dc bias voltages, and the pulse voltage/current conditions applied to the device during the test.

3.1.16 Architecture. Architecture, in the context of this document, is sometimes called "process integration" or just simply "a process." This refers to the way in which the structure of the process is put together.

3.1.17 BiCMOS. A process that, at the very minimum, combines an isolated, high-performance NPN transistor along with a CMOS process.

3.2 Nomenclature

3.2.1 DUT. Device under test.

3.2.2 V_{dd} . The normal positive supply voltage applied to the DUT.

3.2.3 V_{ss} . The normal negative supply voltage applied to the DUT.

3.2.4 Gnd or Ground. This is the ground potential of the system. It may be the same as V_{ss} or V_{dd} or any other specified potential.

3.2.5 I_{dd} . DUT total dc supply current.

3.2.5 Output. The pin on the SCR test structure that simulates the output pin of a CMOS output buffer.

3.2.6 I_{to} . Trigger current from output overvoltage above V_{dd} .

3.2.7 I_{tu} . Trigger current from output undervoltage below V_{ss} .

3.2.8 V_{to} . Trigger voltage output overvoltage above V_{dd} .

3.2.9 V_{tu} . Trigger voltage output undervoltage below V_{ss} .

3.2.10 I_{so} . The maximum dc value of I_{dd} for the SCR still in its OFF state when triggered into latchup by overvoltage on an input or output pin.

3.2.11 I_{su} . The maximum dc value of I_{dd} for the SCR still in its OFF state when triggered into latchup by undervoltage on an input or output pin.

3.2.12 I_h . The value of SCR latchup holding current where $dV/dI = 0$.

3.2.13 V_h . The SCR holding voltage measured when I_h is flowing.