

IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

IEEE Instrumentation & Measurement Society

Sponsored by the
Waveform Generation Measurement and Analysis Technical Committee

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USA

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IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

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Waveform Generation Measurement and Analysis Technical Committee
of the
IEEE Instrumentation & Measurement Society

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Abstract: The material presented in this standard is intended to provide common terminology and test methods for the testing and evaluation of analog-to-digital converters (ADCs). This standard considers only those ADCs whose output values have discrete values at discrete times, i.e., they are quantized and sampled. In general, this quantization is assumed to be nominally uniform (the input-output transfer curve is approximately a straight line) as discussed further in 1.3, Analog-to-digital converter background, and the sampling is assumed to be at a nominally uniform rate. Some but not all of the test methods in this standard can be used for ADCs that are designed for non-uniform quantization.

Keywords: ADC, analog-to-digital converter, code transition level, coherent sampling, DNL, ENOB, histogram, INL, LSB, missing codes, noise power ratio, noncoherent sampling, quantization error, quantization noise, SAR, SFDR, sine fitting

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Introduction

This introduction is not part of IEEE Std 1241-2010, IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters.

This standard defines the terms, definitions, and test methods used to specify, characterize, and test analog-to-digital converters (ADCs). It is intended for the following:

- Individuals and organizations who specify ADCs to be purchased
- Individuals and organizations who purchase ADCs to be applied in their products
- Individuals and organizations whose responsibility is to characterize and write reports on ADCs available for use in specific applications
- Suppliers interested in providing high-quality and high-performance ADCs to acquirers

This standard is designed to help organizations and individuals

- Incorporate quality considerations during the definition, evaluation, selection, and acceptance of supplier ADCs for operational use in their equipment
- Determine how supplier ADCs should be evaluated, tested, and accepted for delivery to end users

This standard is intended to satisfy the following objectives:

- Promote consistency within organizations in acquiring third-party ADCs from component suppliers
- Provide useful practices on including quality considerations during acquisition planning
- Provide useful practices on evaluating and qualifying supplier capabilities to meet user requirements
- Provide useful practices on evaluating and qualifying supplier ADCs
- Assist individuals and organizations judging the quality and suitability of supplier ADCs for referral to end users

Several standards have previously been written that address the testing of analog-to-digital converters either directly or indirectly. These include

- IEEE Std 1057-2007, which describes the testing of waveform recorders. This standard has been used as a guide for many of the techniques described in this standard.
- IEEE Std 746-1984, which addresses the testing of analog-to-digital and digital-to-analog converters used for PCM television video signal processing.
- JESD99-1, which deals with the terms and definitions used to describe analog-to-digital and digital-to-analog converters. This standard does not include test methods.

IEEE Std 1241-2009 for analog-to-digital converters is intended to focus specifically on terms and definitions as well as test methods for ADCs for a wide range of applications.

This standard is a revision of IEEE Std 1241-2000. This version has added additional test methods, improved guidance for selecting tests, and additional terms. Some terminology pertaining to signal-to-noise ratio and related terms has been changed to be consistent with other standards.

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Contents

1. Overview	1
1.1 Scope	1
1.2 Purpose	1
1.3 Document organization.....	2
1.4 Analog-to-digital converter background.....	2
1.5 Guidance to the user	6
1.6 Manufacturer-supplied information.....	7
2. Normative references.....	11
3. Definitions and symbols	11
3.1 Definitions	11
3.2 Symbols and acronyms.....	18
4. General test methods	20
4.1 Introductory information on test methods.....	20
4.2 Test setup.....	20
4.3 Taking a record of data	22
4.4 Equivalent-time sampling and undersampling.....	23
5. Sine-wave testing and fitting	28
5.1 Introductory information on sine-wave testing and fitting	28
5.2 Curve fitting test method	28
5.3 Comment on three-parameter versus four-parameter sine fit	29
5.4 Choice of frequencies and record length	29
5.5 Selecting signal amplitudes	31
5.6 Presenting sine-wave data.....	31
5.7 Impurities of sine-wave sources	31
5.8 Estimating impurity problems from sine-fitting results.....	32
5.9 Measuring and controlling sine-wave impurities.....	33
6. Locating code transitions.....	34
6.1 Introductory information on locating code transitions.....	34
6.2 Locating code transitions using a feedback loop	35
6.3 Alternate code transition location method based on ramp histogram	37
6.4 Alternate code transition location method, based on sine-wave histogram	39
6.5 Determining the static transfer curve.....	42
7. Analog input	43
7.1 Input characteristics	43
7.2 Static input impedance versus input signal level	44
7.3 Static input current.....	44
7.4 Static gain and offset	44

8. Linearity	46
8.1 General comments on linearity	46
8.2 Integral nonlinearity	46
8.3 Absolute accuracy error	47
8.4 Differential nonlinearity and missing codes	47
8.5 Example INL and DNL data	48
8.6 Monotonicity	49
8.7 Hysteresis	50
8.8 Harmonic and spurious distortion	51
8.9 Intermodulation distortion	57
8.10 Noise power ratio	60
9. Noise (total)	65
9.1 General comments concerning noise	65
9.2 Signal-to-noise-and-distortion ratio (SINAD)	65
9.3 Signal-to-noise ratio (SNR)	66
9.4 Effective number of bits (ENOB)	67
9.5 Random noise	70
10. Step response parameters	73
10.1 Step response definition	73
10.2 Test method for acquiring an estimate of the step response	73
10.3 Slew rate limit	73
10.4 Settling time parameters	74
10.5 Transition duration of step response	75
10.6 Overshoot and precursors	75
11. Frequency response parameters	76
11.1 Bandwidth (BW)	76
11.2 Gain error (gain flatness)	78
11.3 Frequency response and gain from step response	78
12. Differential gain and phase	81
12.1 Introductory information on differential gain and phase	81
12.2 Method for testing a general purpose ADC	81
12.3 Method for testing a special purpose ADC	84
12.4 Comments on differential phase and differential gain testing	85
13. Aperture effects	86
13.1 Introductory information on aperture effects	86
13.2 Aperture duration	86
13.3 Aperture delay	91
13.4 Aperture jitter	92
14. Additional tests and specification	94
14.1 Digital logic signals	94
14.2 Pipeline delay	94

14.3 Out-of-range recovery	94
14.4 Differential input specifications.....	95
14.5 Comments on reference signals.....	97
14.6 Power supply parameters.....	98
Annex A (informative) ADC architectures.....	101
A.1 Integrating ADCs.....	101
A.2 Flash ADCs.....	102
A.3 Pipelined and Subranging ADCs	103
A.4 SAR ADCs	104
A.5 Σ - Δ ADCs	105
A.6 Time-Interleaved ADCs.....	106
A.7 Folding and Interpolating ADCs.....	107
Annex B (informative) Sine-wave fitting algorithms	108
B.1 An algorithm for three-parameter (known frequency) least-squares fit to sine-wave data	108
B.2 An algorithm for four-parameter least-squares fit to sine-wave data.....	109
Annex C (normative) Discrete Fourier transforms and windowing	112
C.1 The windowed DFT and spectral leakage.....	114
C.2 Some useful windows and their characteristics.....	116
C.3 Window selection.....	117
Annex D (informative) Presentation of sine-wave data.....	118
D.1 ENOB presentation.....	118
D.2 Presentation of residuals	119
D.3 Other examples of presentations of sine-wave test results.....	121
Annex E (informative) Bibliography.....	125

IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

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1. Overview

1.1 Scope

The material presented in this standard is intended to provide common terminology and test methods for the testing and evaluation of analog-to-digital converters (ADCs). This standard considers only those ADCs whose output values have discrete values at discrete times, i.e., they are quantized and sampled. In general, this quantization is assumed to be nominally uniform (the input-output transfer curve is approximately a straight line) as discussed further in 1.3, and the sampling is assumed to be at a nominally uniform rate. Some but not all of the test methods in this standard can be used for ADCs that are designed for non-uniform quantization.

1.2 Purpose

This standard identifies ADC error sources and provides test methods with which to perform the required error measurements. The information in this standard is useful both to manufacturers and to users of ADCs in that it provides a basis for evaluating and comparing existing devices, as well as providing a template for writing specifications for the procurement of new ones. In some applications, the information provided by the tests described in this standard can be used to correct ADC errors, e.g., correction for gain and offset errors. The reader should note that this standard has many similarities to IEEE Std 1057. Many of the tests and terms are nearly the same, since ADCs are a necessary part of digitizing waveform recorders.

1.3 Document organization

This standard is divided into fourteen clauses plus annexes. Clause 1 is a basic orientation. For further investigation, users of this standard can consult Clause 2, which contains references to other IEEE standards on waveform measurement and relevant International Standardization Organization (ISO) documents. The definitions of technical terms and symbols used in this standard are presented in Clause 3. Clauses 4 through 14 present a wide range of tests that measure the performance of an analog-to-digital converter. Annexes, containing the bibliography and informative comments on the tests presented in Clauses 4 through 14, augment the standard.

1.4 Analog-to-digital converter background

This standard considers only those ADCs whose output values have discrete values at discrete times, i.e., they are quantized and sampled. Although different methods exist for representing a continuous analog signal as a discrete sequence of binary words, an underlying model implicit in many of the tests in this standard assumes that the relationship between the input signal and the output values approximates the ideal staircase transfer curve depicted in Figure 1(a). Applying this model to a voltage-input ADC, the full-scale input range (FSR) of the ADC is divided into uniform intervals, known as code bins, with nominal width Q . The number of code transition levels in the discrete transfer function is equal to $2^N - 1$, where N is the number of digitized bits of the ADC. Note that there are ADCs that are designed such that N is not an integer, i.e., the number of code transition levels is not an integral power of two. Inputs below the first transition or above the last transition are represented by the most negative and positive output codes, respectively. Note, however, that two conventions exist for relating $V_{\min}$ (often called $-FS$, or negative full scale) and $V_{\max}$ (often called $+FS$, or positive full scale) to the nominal transition points between code levels, *mid-tread* and *mid-riser*.

The dotted lines at $V_{\min}$, $V_{\max}$, and $(V_{\min} + V_{\max})/2$ indicate what is often called the *mid-tread* convention, where the first transition is $Q/2$ above $V_{\min}$ and the last transition is $3Q/2$, below $V_{\max}$. This convention gets its name from the fact that the midpoint of the range, $(V_{\min} + V_{\max})/2$, occurs in the middle of a code, i.e., on the *tread* of the staircase transfer function. The second convention, called the *mid-riser* convention, is indicated in the figure by dashed lines at $V_{\min}$, $V_{\max}$, and $(V_{\min} + V_{\max})/2$. In this convention, $V_{\min}$ is $-Q$ from the first transition, $V_{\max}$ is $+Q$ from the last transition, and the midpoint, $(V_{\min} + V_{\max})/2$, occurs on a staircase riser. The difference between the two conventions is a displacement along the voltage axis by an amount $Q/2$.

For all tests in this standard, this displacement has no effect on the results and either convention may be used. The one place where it does matter is when a device provides or expects user-provided reference signals. In this case, the manufacturer must provide the necessary information relating the reference levels to the code transitions. In both conventions the number of code transitions is $2^N - 1$ and the full-scale range, FSR, is from $V_{\min}$ to $V_{\max}$. Even in an ideal ADC, the quantization process produces errors. These errors contribute to the difference between the actual transfer curve and the ideal straight-line transfer curve, which is plotted as a function of the input signal in Figure 1(b).

To use this standard, the user must understand how the transfer function maps its input values to output codewords, and how these output codewords are converted to the code bin numbering convention used in this standard. As shown in Figure 2(a), the lowest code bin is numbered 0, the next is 1, and so on up to the highest code bin, numbered $(2^N - 1)$. In addition to unsigned binary [Figure 1(a)], ADCs may use 2's complement, sign-magnitude, Gray, binary-coded decimal (BCD), or other output coding schemes. In these cases, a simple mapping of the ADC's consecutive output codes to the unsigned binary codes can be used in applying various tests in this standard. Note that in the case of an ADC whose number of distinct output codes is not an integral power of 2 (e.g., a BCD-coded ADC), the number of digitized bits N is still defined, but will not be an integer.

Real ADCs have other errors in addition to the nominal quantization error shown in Figure 1(b). All errors can be divided into the categories of static and dynamic, depending on the rate of change of the input signal at the time of digitization. A slowly varying input can be considered a static signal if its effects are equivalent to those of a constant signal. Static errors, which include the quantization error, usually result from non-ideal spacing of the code transition levels. Dynamic errors occur because of additional sources of error induced by the time variation of the analog signal being sampled. Sources include harmonic distortion from the analog input stages, signal-dependent variations in the time of samples, dynamic effects in internal amplifier and comparator stages, and frequency-dependent variation in the spacing of the quantization levels.

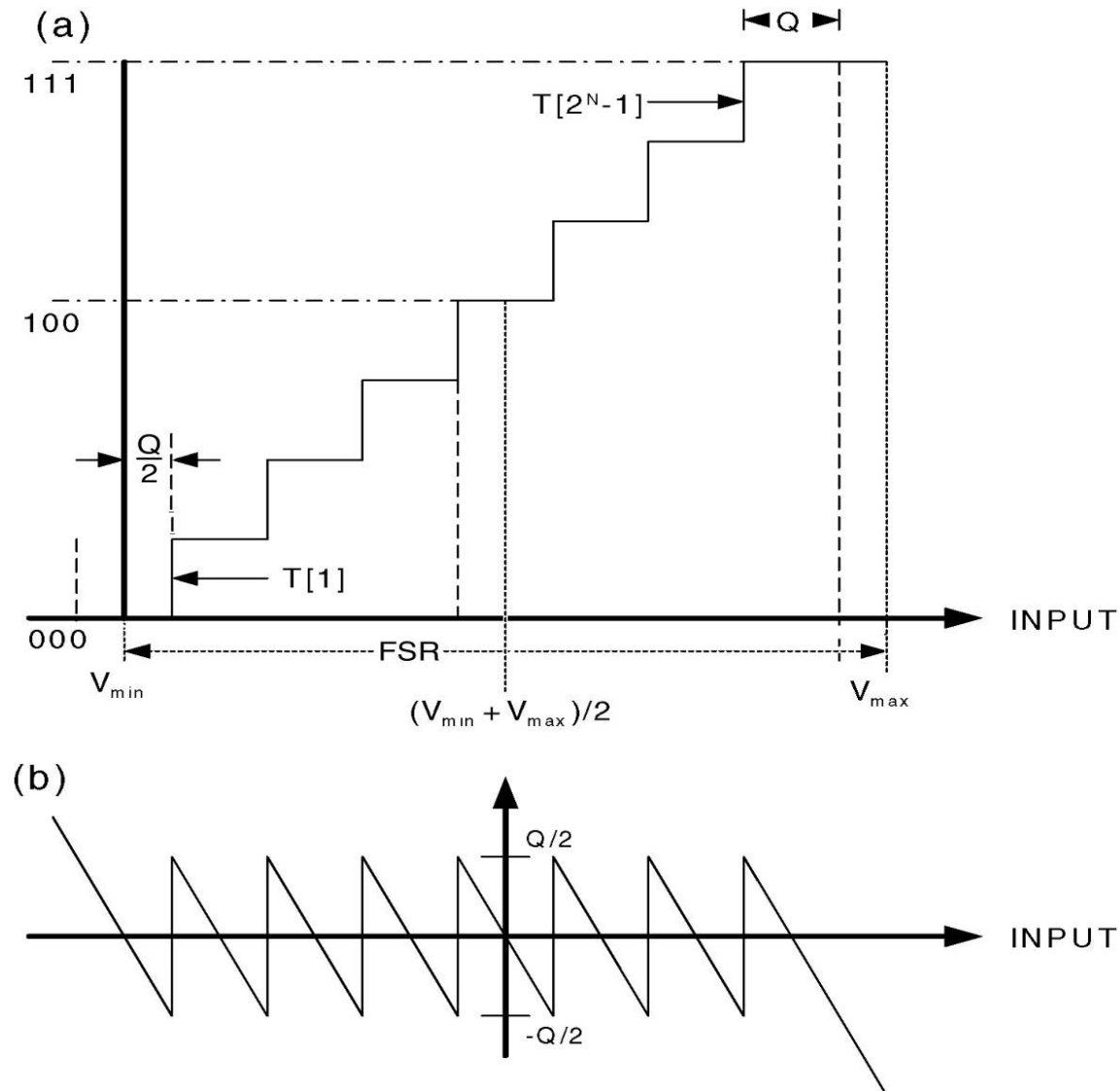


Figure 1—Staircase ADC transfer function, having full-scale range (FSR) and $2^N - 1$ levels, corresponding to N -bit quantization

There are two standard methods for characterizing the error of an ADC:

- a) The transition levels are evaluated as $T[1]$ through $T[2^N - 1]$.
 - For $i = 1$ to $2^N - 2$, the quantity $T'[i] = (T[i] + T[i + 1])/2$ is evaluated.
 - The deviations from nominal of $T'[i]$ are used to define the errors of the ADC.
- b) The transition levels are evaluated as $T[1]$ through $T[2^N - 1]$.
 - The deviations from nominal of $T[i]$ are used to define the errors of the ADC.

The two methods are shown graphically in Figure 2. The ADC characteristics shown in Figure 2 help illustrate the two methods of describing ADC errors. The following should be noted:

- 1) The location of the code edges $T[1]$, $T[2]$, $T[3]$, $T[4]$, $T[5]$, and $T[7]$ are the same as the ideal code edges illustrated in Figure 1.
- 2) The location of $T[6]$ is shifted from the nominal position by $+Q/2$.
- 3) Figure 2(b) shows the error in the ADC output for any input. Note that the maximum error ranges from $-Q/2$ to $+Q/2$ in the area where the code transitions are ideal. In the region around $T[6]$ the error peaks at a value of $+Q$ before returning to a value of 0.
- 4) The ADC is assumed to be noise-free. The ADC is assumed to be end-point calibrated.
- 5) Figure 2(c) is a plot of the ADC error based on code edges. The error is 0 for all codes except for code 1102 where the error is $+Q/2$.
- 6) Figure 2(d) is a plot of the ADC errors based on code centers.

The data for Figure 2 is tabulated below.

Code	Ideal $T[\text{code}]$	Actual $T[\text{code}]$	Figure 2(c)	Mid-step ideal	Mid-step actual	Figure 2(d)
0	NA	NA	NA	NA	NA	NA
1	$0.5Q$	$0.5Q$	$0.0Q$	$1.0Q$	$1.0Q$	$0.0Q$
2	$1.5Q$	$1.5Q$	$0.0Q$	$2.0Q$	$2.0Q$	$0.0Q$
3	$2.5Q$	$2.5Q$	$0.0Q$	$3.0Q$	$3.0Q$	$0.0Q$
4	$3.5Q$	$3.5Q$	$0.0Q$	$4.0Q$	$4.0Q$	$0.0Q$
5	$4.5Q$	$4.5Q$	$0.0Q$	$5.0Q$	$5.25Q$	$0.25Q$
6	$5.5Q$	$6.0Q$	$0.5Q$	$6.0Q$	$6.25Q$	$0.25Q$
7	$6.5Q$	$6.5Q$	$0.0Q$	NA	NA	NA

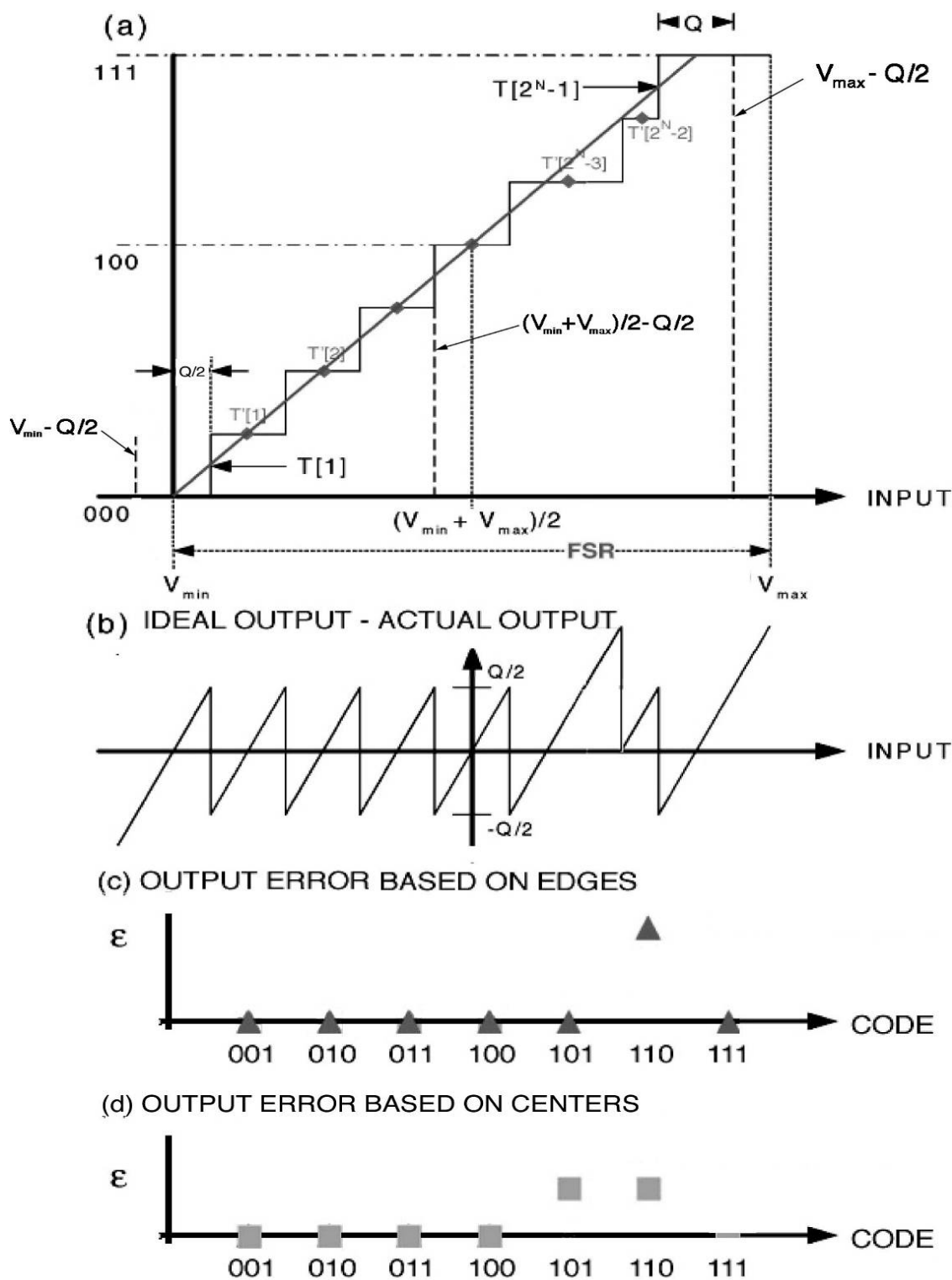


Figure 2—Methods for characterizing the error of an ADC

There are advantages and disadvantages to both methods of analyzing ADC errors

- a) Code center error analysis (mid-tread):
 - 1) AC analyses such as THD, SINAD, and SNR are better defined by code center error analyses.
 - 2) For a given converter, INL errors are smaller when based on code centers.
 - 3) Histogram error analyses are more closely related to code center error analysis.
- b) Code edge error analysis (mid-riser):
 - 1) ADCs that are used for instrumentation are better defined by code edge analysis.
 - 2) Servo measurement techniques of an ADC transfer function identify code edges.

1.5 Guidance to the user

Conditions described in this section are a general overview of the test environment. More detailed conditions about the environment will be included in relevant sections of the standard.

1.5.1 Interfacing

ADCs present unique interfacing challenges, and without careful attention users can experience substandard results. As with all mixed-signal devices, ADCs perform as expected only when the analog and digital domains are brought together in a well-controlled fashion. The user should fully understand the manufacturer's recommendations with regard to proper signal buffering and loading, input signal connections, transmission line matching, circuit layout patterns, power supply decoupling, and operating conditions. Edge characteristics for start-convert pulse(s) and clock(s) must be carefully chosen to maintain input signal purity with sufficient margin up to the analog input pin(s). Most manufacturers now provide excellent ADC evaluation boards, which demonstrate recommended layout techniques, signal conditioning, and interfacing for their ADCs. If the characteristics of a new ADC are not well understood, then these boards should be analyzed or used before starting a new layout.

1.5.2 Test conditions

ADC test specifications can be split into two groups: test conditions and test results. Typical examples of the former are: temperature, power supply voltages, clock frequency, and reference voltages. Examples of the latter are: power dissipation, effective number of bits, spurious free dynamic range (SFDR), and integral non-linearity (INL). The test methods defined in this standard describe the measurement of test results for given test conditions.

ADC specification sheets will often give allowed ranges for some test condition (e.g., power supply ranges). This implies that the ADC will function properly and that the test results will fall within their specified ranges for all test conditions within their specified ranges.

Since the test condition ranges are generally specified in continuous intervals, they describe an infinite number of possible test conditions, which obviously cannot be exhaustively tested. It is up to the manufacturer or tester of an ADC to determine, from design knowledge and/or testing, the effect of the test conditions on the test result, and from there to determine the appropriate set of test conditions needed to accurately characterize the range of test results. For example, knowledge of the design may be sufficient to know that the highest power dissipation (test result) will occur at the highest power supply voltage (test condition), so the power dissipation test need be run only at the high end of the supply voltage range to check that the dissipation is within the maximum of its specified range. It is very important that relevant test conditions be stated when presenting test results.

1.5.3 Electrical environment

When designing a test setup, one should consider the electrical environment. Prevent external disturbances from affecting the test results. Examples of external disturbances include common-mode noise and poor grounding in the set-up. Computers and high-power radio frequency (RF) signals like TV and radio transmitters can be sources of interference.

1.5.4 Test equipment

One must verify that the performance of the test equipment used for these tests significantly exceeds the desired performance of the ADC under evaluation. Users will likely need to include additional signal conditioning in the form of filters and pulse shapers. Accessories such as terminators, attenuators, delay lines, and other such devices are usually needed to match signal levels and to provide signal isolation to avoid corrupting the input stimuli.

Quality testing requires following established procedures, most notably those specified in IEEE Std ISO 9001: 2000 [B26]. In particular, traceability of instrumental calibration to a known standard is important. Commonly used test setups are described in 4.2.

1.5.5 Test selection

When choosing which parameters to measure, one should follow the outline and hints in this clause to develop a procedure that logically and efficiently performs all needed tests on each unique setup. The standard has been designed to facilitate the development of these test procedures. In this standard the discrete Fourier transform (DFT) is used extensively for the extraction of frequency domain parameters because it provides numerous evaluation parameters from a single data record. DFT testing is the most prevalent technique used in the ADC manufacturing community, although the sine-fit test, also described in the standard, provides meaningful data. Nearly every user requires that the ADC should meet or exceed a minimum signal-to-noise-and-distortion ratio (SINAD) limit for the application and that the nonlinearity of the ADC be well understood. Certainly, the extent to which this standard is applied will depend upon the application; hence, the procedure should be tailored for each unique characterization plan.

1.6 Manufacturer-supplied information

1.6.1 General information

Manufacturers shall supply the following general information:

- a) ADC part identification
- b) Physical characteristics: dimensions, packaging, pinouts
- c) Power requirements
- d) Environmental conditions: Reliable operating, non-operating, and specified performance temperature range; altitude limitations; humidity limits, operating and storage; vibration tolerance; and compliance with applicable electromagnetic interference specifications
- e) Any special or peculiar characteristics
- f) Compliance with other specifications
- g) Control signal characteristics
- h) Output signal characteristics
- i) Pipeline delay (if any)
- j) Exceptions to the above parameters where applicable

1.6.2 Minimum specifications

The manufacturer shall provide the following specifications (see Clause 3 for definitions):

- a) Absolute accuracy (total unadjusted error)
- b) Analog bandwidth (minimum, maximum, and/or typical)
- c) Clock and digital control signals and level specifications
- d) Input impedance (as applicable)
- e) Input signal full-scale range with nominal reference signal levels (minimum, maximum, and/or typical)
- f) Number of digitized bits (resolution)
- g) Output coding format (binary, two's complement, etc.)
- h) Output logic levels
- i) Power dissipation (minimum, maximum, and/or typical)
- j) Range of allowable sample rates (minimum, maximum)
- k) Reference signal levels to be applied as required (minimum, maximum, and/or typical)
- l) Supply currents (minimum, maximum, and/or typical)
- m) Supply voltages (minimum, maximum, and/or typical)
- n) Timing requirements for inputs and outputs

1.6.3 Additional specifications

- a) Aperture delay time
- b) Aperture uncertainty (aperture short-term time-base instability/jitter) (maximum, typical)
- c) Common-mode rejection ratio (minimum, maximum, and/or typical)
- d) Crosstalk (minimum, maximum, and/or typical)
- e) Differential gain and differential phase (minimum, maximum, and/or typical)
- f) Differential input impedance (as required)
- g) Differential nonlinearity (minimum, maximum, and/or typical)
- h) Effective number of bits (minimum, maximum, and/or typical)
- i) Frequency response (minimum, maximum, and/or typical)
- j) Gain error (minimum, maximum, and/or typical)
- k) Harmonic distortion (minimum, maximum, and/or typical)
- l) Hysteresis (maximum, typical)
- m) Integral nonlinearity (minimum, maximum, and/or typical)
- n) Intermodulation distortion (minimum, maximum, and/or typical)
- o) Maximum common-mode signal levels (minimum, maximum, and/or typical)
- p) Maximum static error (minimum, maximum, and/or typical)
- q) Monotonicity
- r) No missing codes resolution (minimum, maximum, and/or typical)

- s) Random noise (maximum, typical)
- t) Noise power ratio (NPR) (minimum, maximum, and/or typical)
- u) Offset error (minimum, maximum, and/or typical)
- v) Out-of-range/Overdrive recovery time (voltage or current)
- w) Overshoot and precursors
- x) Settling time (minimum, maximum, and/or typical)
- y) Signal-to-noise ratio (minimum, maximum, and/or typical)
- z) Slew rate limit (minimum, maximum, and/or typical)
- aa) Spurious-free dynamic range (minimum, maximum, and/or typical)
- bb) Transition duration of step response (rise time) (minimum, maximum, and/or typical)
- cc) Word error rate

1.6.4 Pertinent ADC parameters

Table 1 is presented as a guide for many of the most common ADC applications. The wide range of ADC applications makes a comprehensive listing impossible. This table is intended to be a helpful starting point for users to apply this standard to their particular applications.

Table 1—Critical ADC parameters

Typical applications	Critical ADC parameters	Performance issues
Audio	SINAD, THD, noise	— Power consumption — Crosstalk and gain matching
Automatic control	Monotonicity Short-term settling, long-term stability, noise	— Transfer function — Crosstalk and gain matching — Temperature stability
Data acquisition	DNL, INL, gain, offset, noise, out-of-range recovery, settling time, full-scale step response, channel-to-channel crosstalk	— Channel-to-channel interaction — Accuracy, traceability (Sol Max)
Digital oscilloscope/waveform recorder	SINAD, ENOB, noise Bandwidth Out-of-range recovery Word error rate	— SINAD for wide bandwidth amplitude resolution — Low thermal noise for repeatability — Bit error rate
Geophysical	THD, SINAD, long-term stability, noise	— Millihertz response
Imaging	DNL, INL, SINAD, ENOB, noise Out-of-range recovery Full-scale step response	— DNL for sharp-edge detection — High-resolution at switching rate — Recovery from blooming
Radar and sonar	SINAD, IMD, ENOB SFDR Out-of-range recovery, noise	— SINAD and IMD for clutter cancellation and Doppler processing
Spectrum analysis	SINAD, ENOB SFDR, noise	— SINAD and SFDR for high linear dynamic range measurements
Spread spectrum communication	SINAD, IMD, ENOB SFDR, NPR Noise-to-distortion ratio, noise	— IMD for quantization of small signals in a strong interference environment — SFDR for spatial filtering — NPR for interchannel crosstalk
Telecommunication personal communications	SINAD, NPR, SFDR, IMD Bit error rate Word error rate, noise	— Wide input bandwidth channel bank — Interchannel crosstalk — Compression — Power consumption
Video	DNL, SINAD, SFDR, DG, DP, noise	— Differential gain and phase errors — Frequency response
Wideband digital receivers SIGINT, ELINT, COMINT	SFDR, IMD SINAD, noise	— Linear dynamic range for detection of low-level signals in a strong interference environment — Sampling frequency
COMINT = communications intelligence DG = differential gain error DNL = differential nonlinearity DP = differential phase error ELINT = electronic intelligence ENOB = effective number of bits IMD = intermodulation distortion INL = integral nonlinearity NPR = noise power ratio SFDR = spurious free dynamic range SIGINT = signal intelligence SINAD = signal-to-noise-and-distortion ratio THD = total harmonic distortion		

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated referenced, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 181™-2003, IEEE Standard on Transitions, Pulses, and Related Waveforms.^{1, 2}

3. Definitions and symbols

For the purposes of this standard, the following terms and definitions apply. *The IEEE Standards Dictionary: Glossary of Terms & Definitions* should be referenced for terms not defined in this clause.³

3.1 Definitions

ac-coupled analog-to-digital converter: An analog-to-digital converter utilizing a network that passes only the varying ac portion, not the static dc portion, of the analog input signal to the quantizer.

alternation band: The range of input levels which causes the converter output to alternate between two adjacent codes. A property of some analog-to-digital converters, it is the complement of the hysteresis property.

analog-to-digital converter (ADC): A device that converts a continuous time signal into a discrete-time discrete-amplitude signal.

aperture: The interval during which the input to the ADC affects the output or the weighting function that determines the sampled output from the input signal.

aperture delay: The delay from a threshold crossing of the analog-to-digital converter clock which causes a sample of the analog input to be taken to the center of the aperture for that sample.

aperture duration ($p\%$): The $[50 - (p/2)]\%$ to $[50 + (p/2)]\%$ transition duration of the step response of the ADC. If ringing of the step response causes multiple crossings of either of the levels, the $p\%$ aperture duration is the time from the first crossing of the first level to the last crossing of the second level. Note: The significance is that the output of the ADC is determined, with an error of $(100 - p)\%$ or less, by the input signal in an interval of this duration. Common values of p are 50, 80, and 99.9. For $p = 80$, this is the 10% to 90% transition duration of the step response.

aperture jitter: See: **aperture uncertainty**.

aperture uncertainty: The standard deviation of the apparent sampling time. *Syn:* **aperture jitter; timing jitter; timing phase noise**.

asynchronous sampling: Refers to sampling an input signal that is not phase locked to the analog-to-digital converter sampling frequency.

¹ The IEEE standards or products referred to in this clause are trademarks of the Institute of Electrical and Electronics Engineers, Inc.

² IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854, USA (<http://standards.ieee.org/>).

³ The *IEEE Standards Dictionary: Glossary of Terms & Definitions* is available at <http://shop.ieee.org/>.

clock signal duty cycle: The fraction of the time the clock signal spends in excess of the logic threshold.

clock signal slew rate: The time derivative of the clock signal at the point where it crosses the logic threshold.

code bin k : A digital output that corresponds to a particular set of input values.

code bin width ($W[k]$): The difference of the code transition levels, $T[k + 1]$ and $T[k]$, that delimit the k^{th} bin:

$$W[k] = T[k + 1] - T[k] \quad (1)$$

code transition level: The boundary between two adjacent code bins.

code transition level ($T[k]$): The value of the converter-input parameter at the transition point between two given adjacent code bins. The transition point is defined as the input value that causes 50% of the output codes to be greater than or equal to the upper code of the transition, and 50% to be less than the upper code of the transition. The transition level $T[k]$ lies between code bin $k - 1$ and code bin k .

coherent sampling: Sampling of a periodic waveform such that there is an integer number of waveform cycles in the data record. Coherent sampling occurs when the following relationship exists:

$$Mf_i = Jf_s \quad (2)$$

where

f_s is the sampling frequency
 J is the integer number of cycles of the waveform in the data record
 f_i is the frequency of the input waveform
 M is the number of samples in the data record

common-mode out-of-range: A signal level whose magnitude is less than the specified maximum common-mode signal but greater than the maximum operating common-mode signal.

common-mode out-of-range recovery time: The time required for the analog-to-digital converter under test to return to its specified characteristics after the end of a common-mode out-of-range input signal.

common-mode range: The range of analog input signal swing at each differential input over which the common-mode rejection is specified. Common-mode range is also the sum of the largest simultaneously applied common-mode signal and differential signal.

common-mode rejection ratio (CMRR): The ratio of the input common-mode signal to the effect produced at the output of the analog-to-digital converter under test, in units of the input signal.

common-mode signal: The average value of the signals at the positive input and the negative input of a differential-input analog-to-digital converter. If the signal at the positive input is designated V_+ , and the signal at the negative input is designated V_- , then the common-mode signal V_{cm} is:

$$V_{\text{cm}} = \frac{V_+ + V_-}{2} \quad (3)$$

conversion (clock) rate (f_s): The frequency at which digital output words are provided by the analog-to-digital converter on its output.

crosstalk: Undesired energy appearing in a signal as a result of coupling from other signals.

data valid time: A measure of the time, in analog-to-digital converter clock cycles, between the first clock transition after the data becomes valid at the digital outputs and the last clock transition before it becomes invalid.

differential-input impedance to ground: For a differential-input analog-to-digital converter, the impedance between the positive input and the negative input.

differential nonlinearity (DNL): The difference between a specified code bin width and the average code bin width, divided by the average code bin width.

differential signal: The difference between the signal at the positive and negative inputs of a differential-input analog-to-digital converter. If the signal at the positive input is designated V_+ , and the signal at the negative input is designated V_- , then the differential signal (V_{dm}) is

$$V_{dm} = V_+ - V_- \quad (4)$$

effective number of bits (ENOB): A measure of the signal-to-noise-and-distortion ratio used to compare actual analog-to-digital converter (ADC) performance to an ideal ADC.

epoch: The duration of time corresponding to a data record. For instance, for an M -sample record acquired at the uniform sampling period T_s , the epoch is MT_s .

equivalent-time sampling: A process by which consecutive samples of a repetitive waveform are acquired and assembled from multiple repetitions of the waveform, to produce a record of samples representing a single repetition of the waveform.

fall time (t_f): The time for the desired signal to go from 90% to 10% of the transition range.

full-scale range (FSR): The difference between the most positive and most negative analog inputs of a converter's operating range. For an N -bit converter, FSR is given by:

$$\text{FSR} = (2^N)(\text{ideal code width}) \quad (5)$$

in analog input units.

full-scale signal: A full-scale signal is one whose peak-to-peak amplitude spans the entire range of input values recordable by the analog-to-digital converter under test.

full width at half maximum (FWHM): The width of a distribution measured at an amplitude of one half of the maximum amplitude.

gain and offset: (A) (independently based) Gain and offset are the values by which the input values are multiplied and then to which the input values are added, respectively, to minimize the mean squared deviation from the output values. **(B) (terminal based)** Gain and offset are the values by which the input values are multiplied and then to which the input values are added, respectively, to cause the deviations from the output values to be zero at the terminal points, that is, at the first and last codes.

harmonic distortion: For a pure sine-wave input, output components at frequencies that are an integer multiple of the applied sine-wave frequency which are induced by the input sine wave.

hysteresis: The maximum difference in values of a code transition level, when the transition level is approached by a changing input signal from either side of the transition.

ideal code bin width (Q): The ideal full-scale input range divided by the total number of code bins.

input impedance: The impedance between the signal input of the analog-to-digital converter under test and ground.

integral nonlinearity (INL): The maximum difference between the ideal and actual code transition levels after correcting for gain and offset.

k^{th} code transition level ($T[k]$): The input value corresponding to the transition between codes $k - 1$ and k .

NOTE—See Figure 3.

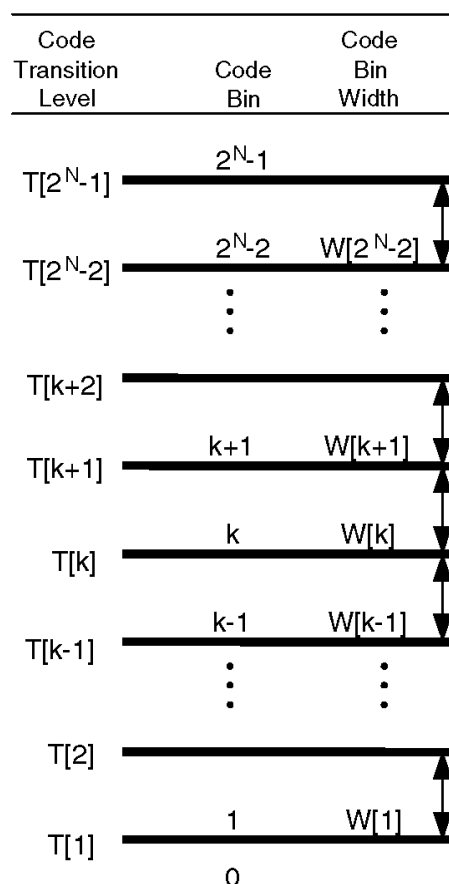


Figure 3—Definitions pertaining to input quantization

large signal: One whose peak-to-peak amplitude is as large as practical but is recorded by the instrument within, but not including, the maximum and minimum amplitude data codes. As a minimum, the signal must span at least 90% of the full-scale range of the analog-to-digital converter under test.

least significant bit (LSB): With reference to analog-to-digital converter input signal amplitude, an LSB is synonymous with one ideal code bin width.

logic level: Any level within one of two (or more) non-overlapping ranges of values, of a physical quantity, used to represent the logic.

long-term settling error: The absolute difference between the final value specified for short-term settling time and the value 1 s after the beginning of the step, expressed as a percentage of the step amplitude.

maximum common-mode signal level: The maximum level of the common-mode signal at which the common-mode rejection ratio is still valid.

maximum operating common-mode signal: The largest common-mode signal for which the analog-to-digital converter will meet its specifications when recording a simultaneously applied, normal-mode signal.

maximum input signal level: The input level beyond which damage to the device may occur.

monotonic analog-to-digital converter: An analog-to-digital converter that has output codes that do not decrease (increase) for a uniformly increasing (decreasing) input signal, disregarding random noise.

noise power ratio (NPR): The ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the discrete Fourier transform spectrum of the analog-to-digital converter output sample set.

noise (total): Any deviation between the output signal (converted to input units) and the input signal except deviations caused by linear time-invariant system response (gain and phase shift), or a dc level shift. For example, noise includes the effects of random errors (random noise), fixed pattern errors, nonlinearities (e.g., harmonic or intermodulation distortion), and aperture uncertainty. *See also:* **random noise**.

noncoherent sampling: Sampling of a waveform such that the relationship between the input frequency, sampling frequency, number of cycles in the data record, and the number of samples in the data record does not meet the definition of coherent sampling.

normal mode signal: The difference between the signal at the positive input and the negative input of a differential input analog-to-digital converter. *Syn:* differential signal.

offset: *See:* **gain and offset**.

out-of-range input: Any input whose magnitude is less than the maximum input signal of the analog-to-digital converter but greater than the full-scale range.

overshoot: The maximum amount by which the step response exceeds the high state, specified as a percentage of (recorded) pulse amplitude.

passband: The band of input signal frequencies that the analog-to-digital converter is intended to digitize with nominally constant gain.

phase nonlinearity: The deviation in phase response from a perfectly linear-phase response as a function of frequency.

pipeline delay: A measure of the latency in terms of analog-to-digital converter clock cycles between the clock transition that initiates sampling of the input and the presentation of the digitized value of that sample at the digital output.

precursor: In a step or pulse waveform, any deviation from the base state prior to the pulse transition.

probability density function (PDF): For a random variable, x , a positive real function, $f_x(x)$, which has the interpretation that $f_x(x) dx$ is the probability that the random variable, X , lies in the interval $(x, x + dx)$.

quantization: A process in which the continuous range of values of an input signal is divided into non-overlapping sub-ranges, and to each sub-range a discrete value of the output is uniquely assigned. Whenever the signal value falls within a given sub-range, the output has the corresponding discrete value. (*IEEE Standards Dictionary* [B21])

quantization error/quantization noise: The error caused by conversion of a variable having a continuous range of values to a quantized form having only discrete values, as in analog-to-digital conversion. The error is the difference between the original (analog) value and its quantized (digital) representation. (*IEEE Standards Dictionary* [B21])

random noise: A non-deterministic fluctuation in the output of an analog-to-digital converter, described by its frequency spectrum and its amplitude statistical properties. *See also:* **noise**.

record of data: A sequential collection of samples acquired by the analog-to-digital converter.

relatively prime: Describes integers whose greatest common divisor is 1.

residuals: In curve fitting, the differences between the recorded data and the fitted function.

rise time (t_r): The time for the signal to go from 10% to 90% of the transition range.

root-mean-square (rms): For a given set of data, the square root of the arithmetic mean of the squared values of each of the data.

root-sum-square (rss): For a given set of data, the square root of the sum of the squared values of each of the data.

sampling: The process of assigning discrete time values to a continuous time signal.

settling time: The time at which the step response enters and subsequently remains within a specified error band around the final value, measured from the mesial point (50%) of the response. The final value is defined to occur 1 s after the beginning of the step.

short-term settling time: Measured from the mesial point (50%) of the output, the time at which the **step response** enters and subsequently remains within a specified error band around the final value. The final value is defined to occur at a specified time less than 1 s after the beginning of the step.

signal-to-noise-and-distortion ratio (SINAD): For a pure sine-wave input of specified amplitude and frequency, the ratio of the root-mean-square (rms) amplitude of the analog-to-digital converter output signal to the rms amplitude of the output noise, where noise is defined as above to include not only random errors but also nonlinear distortion and the effects of sampling time errors.

single-ended analog-to-digital converter: A non-differential analog-to-digital converter, i.e., one that does not subtract the signals at two input terminals. Such a converter may add multiple inputs.

slew limit: The value of output transition rate of change for which an increased amplitude input step signal causes no change.

small signal: A signal whose peak-to-peak amplitude spans no more than 10% of the full range of the analog-to-digital converter under test.

signal-to-noise-ratio (SNR): For a pure sine-wave input of specified amplitude and frequency, the ratio of the root-mean-square (rms) amplitude of the analog-to-digital converter output signal to the rms amplitude of the output noise, this does not include the harmonic distortion components that are used for the estimate of THD. Note: This was called signal-to-non-harmonic ratio (SNHR) in the previous version of this standard.

spurious components: Persistent sine waves at frequencies other than the harmonic frequencies. *See: harmonic distortion.*

spurious-free dynamic range (SFDR): For a pure sine-wave input of specified amplitude and frequency, the ratio of the amplitude of the analog-to-digital converter's output averaged spectral component at the input frequency, f_i , to the amplitude of the largest harmonic or spurious spectral component observed over the full Nyquist band, $\max\{|X(f_h)| \text{ or } |X(f_s)|\}$:

$$\text{SFDR(dB)} = 20 \log_{10} \left(\frac{|X_{\text{avm}}(f_i)|}{\max_{f_s, f_h} \{|X_{\text{avm}}(f_h)| \text{ or } |X_{\text{avm}}(f_s)|\}} \right) \quad (6)$$

where

X_{avm} is the averaged spectrum of the ADC output
 f_i is the input signal frequency
 f_h and f_s are the frequencies of the set of harmonic and spurious spectral components

step (or pulse) base state: The magnitude reference line at the base magnitude [IEEE Std 181-2003].

step (or pulse) high state: The magnitude reference line at the top magnitude [IEEE Std 181-2003].

step response: The recorded output response for an ideal input step with designated base state and high state.

synchronous sampling: Refers to sampling an input signal that has been phase locked to the analog-to-digital converter sampling frequency.

timing jitter: *See: aperture uncertainty.*

timing phase noise: *See: aperture uncertainty.*

total harmonic distortion (THD): For a pure sine-wave input of specified amplitude and frequency, the root-sum-of-squares (rss) of all the harmonic distortion components including their aliases in the spectral output of the analog-to-digital converter. Unless otherwise specified, THD is estimated by the rss of the second through the tenth harmonics, inclusive. THD is often expressed as a decibel ratio with respect to the root-mean-square amplitude of the output component at the input frequency.

total spurious distortion (TSD): For a pure sine-wave input of specified amplitude and frequency, the root-sum-square of the spurious components in the spectral output of the analog-to-digital converter. TSD is often expressed as a decibel ratio with respect to the root-mean-square amplitude of the output component at the input frequency.

transfer curve: The representation of the average digital output code of an analog-to-digital converter as a function of the input signal value.

transition duration of a step response: The duration between the 10% point and the 90% point on the recorded step response transition, for an ideal input step with designated base state and high state.

useful power bandwidth: The large signal analog input frequency at which a record of the analog-to-digital converter's output data will be degraded by less than a specified amount.

voltage standing wave ratio (VSWR): The ratio of the mismatch between the actual impedance and the desired or nominal impedance.

window: A set of coefficients with which corresponding samples in a data record are multiplied so as to more accurately estimate certain properties of the signal, particularly frequency domain properties. Generally the coefficient values increase smoothly toward the center of the record.

word error rate: The probability of receiving an erroneous code for an input after correction is made for gain, offset, and linearity errors, and a specified allowance is made for random noise. Typical causes of word errors are metastability and timing jitter of comparators within the analog-to-digital converter.

3.2 Symbols and acronyms

ε	error, used for total error and error band
ε_{rms}	root-mean-square value of ε
$\varepsilon[k]$	difference between $T[k]$ and ideal value of $T[k]$ computed from G and V_{os}
θ	phase, expressed as radians
π	ratio of the circumference of a circle to the diameter (constant)
ρ	reflection coefficient
σ	standard deviation; sometimes used as noise amplitude, which is the standard deviation of the random component of a signal
σ_{σ}	standard deviation of the standard deviation (e.g., standard deviation of the noise amplitude)
σ_t	aperture uncertainty
σ^2	variance; sometimes used to describe random noise power
τ	sampling period, the inverse of f_s
ω	$2\pi f$ = angular frequency, expressed in radians per second
ω_i	angular input frequency expressed in radians per second
a	general purpose real number
A	sinusoidal amplitude
B	test tolerance in fractions of a least significant bit (Q); also used as an amplitude
C	offset
CMR	common-mode range
D	general purpose integer
dBc	decibels referenced to the output fundamental frequency level
dBFS	decibels referenced to a full-scale sine wave
DNL	maximum differential nonlinearity over all k
$d[n]$	dither component of output sample $y[n]$
$\text{DNL}[k]$	differential nonlinearity of code k
$d_{\text{est}}[n]$	estimate of the dither component $d[n]$
$E_G(f)$	gain flatness error of frequency f
ENBW	equivalent noise bandwidth
ENOB	effective number of bits
$e_m[f]$	aliasing and first differencing magnitude errors
$e_p[f]$	aliasing and first differencing phase errors
FSR	full-scale range
f	frequency

$f(n)$	sine-wave component of output sample $y(n)$
f_{co}	upper frequency for which the amplitude response is -3 dB
f_{d}	sampling frequency of a record after decimation by an integer
f_{eq}	equivalent sampling rate
f_h	frequency of a harmonic of the input frequency
f_i	actual input frequency or approximate desired input frequency
f_{imf}	frequency of intermodulation distortion products
f_m	frequency of the m th component of a magnitude spectrum produced by a DFT
f_{opt}	optimum input frequency for testing
f_r	input signal reference frequency or input signal repetition rate
f_s	sampling frequency
f_{sp}	frequency of a persistent spurious tone
G	static gain of the ADC under test
$G(f)$	dynamic gain of the ADC under test, as a function of frequency f
H	average number of histogram samples received in two code bins sharing the same transition level
$H(f)$	frequency response of the ADC under test, as a function of frequency f
$H(f_k)$	DFT of $h(n)$
$H(i)$	number of histogram samples in bin i
$H_c(j)$	number in the j th bin of the cumulative histogram of samples
$h(n)$	discrete time impulse response of a system
INL	integral nonlinearity
INL(k)	integral nonlinearity at output code k
i	general purpose index
J	number of cycles in a record
k	code bin
L	general purpose integer
l	general purpose factor
M	number of sequential samples in a record
$M_+(x), M_-(x)$	number of measurements of the output value at the input value x for increasing and decreasing inputs respectively
M_D	number of samples in one period of pseudorandom dither
M_d	number of samples in a record after decimation
mod	the standard function for which $\text{mod}(I, J)$ is the remainder when I is divided by J (e.g., $\text{mod}(12, 10) = 2$).
mse	mean square error
N	number of digitized bits. (Note that for certain ADCs, N may not be an integer value.)
NPR	noise power ratio
n	sample index within a record
p	probability
Q	ideal code bin width, expressed in input units
R	error parameter; also used as minimum number of records required
r	general purpose integer
S	set of samples collected over more than one record, also used as an error parameter or as total number of samples used in a histogram
$T[k]$	code transition level between code $k - 1$ and code k
THD	estimate of total harmonic distortion
t_{eq}	average equivalent-time sampling period

t_f	top to base transition time; fall time
t_n	discrete sample times
t_r	base to top transition time; rise time
t_{wc}	the center point of the aperture time associated with an output sample
u	confidence level expressed as a fraction
V_{cm}	common-mode signal
V_{dm}	differential mode signal
V_o	input signal overdrive; the amount by which an input signal exceeds the ADC full-scale range
V_{os}	input offset of ADC, ideally = 0
VSWR	voltage standing wave ratio
$W[k]$	code bin width of code bin k
w	estimated word error rate
w'	worst-case word error rate
$w(n)$	window function coefficient (for a DFT)
X	number of standard deviations of a Gaussian distribution
$X_{avm}(f_m)$	the averaged magnitude spectral component at discrete frequency f_m after a DFT
x	ADC input signal value; or number of errors detected
$Y[k]$	the M -point discrete Fourier transform of the M -sample record $y[n]$
$y[n] = y_n$	the n th output data sample within a record
$\bar{y}[n]$	average of y_n over M samples
Z_0	transmission line impedance
Z_t	ADC input impedance
$Z_{u/2}$	number of standard deviations that encompass $100(1 - u)\%$ of a Gaussian distribution about the center

4. General test methods

4.1 Introductory information on test methods

It is assumed that the user/manufacture has defined operating limits for the device under test. These limits are categorized as *absolute* (the limit beyond which the device will be destroyed) and *operating* (the limit beyond which the device will not operate properly). These limits will vary from device to device, depending on the design. It is not the intention of this document to describe the method of setting these limits, only to verify the operation within them. All test procedures described herein apply only to parameters of a device that is operated within its specified limits.

The type of circuitry used to capture the digital data samples produced by the ADC is determined largely by the data rate. Slower ADCs may be interfaced directly to the computer. ADCs often require a buffer memory to acquire data at the ADC sample rate and then download accumulated samples to the computer at a slower rate. Even faster ADCs may require latches and/or de-multiplexers between the ADC and the buffer memory, and perhaps data decimation, as described in 4.2.2. A logic analyzer might be used as a buffer memory to capture data for some tests.

4.2 Test setup

A few general test setups can be used to perform most of the ADC tests presented in this standard. Test setups that use sine waves, arbitrary waveforms, and pulses are described in the following subclauses.

Some tests, such as those for VSWR and out-of-range signals, require setups other than those discussed in the following subclauses.

4.2.1 Sine-wave test setup

Figure 4 shows the sine-wave test setup. Sine waves are commonly used in ADC testing because appropriate sine-wave sources are readily available and because it is relatively easy to establish the quality of the sine wave (e.g., with a spectrum analyzer). A sine-wave generator provides the test signal while a clock generator provides the clock (or conversion) signal. Also, combining the output of two (or three) sine-wave generators can produce two-tone (or three-tone) test signals for intermodulation distortion testing. Additionally, a noise generator's output can be combined with a signal to provide low-level dither (Gray and Stockham [B17]).

If frequency synthesizers are used to generate the test and clock signals, the synthesizers can often be phase-locked to maintain precise phase relationships between the signal and the sampling clock. Phase-locking of synthesizers facilitates testing and simplifies subsequent digital signal processing, by preventing clock/signal walkthrough (beat patterns) that may artificially increase or reduce measured spurious output.

Both the clock and the test signals must be suitable for the test being performed. Filters may be required in either the clock or signal paths to reduce noise or harmonic distortion. For example, sub-harmonics in the clock path will degrade ADC performance, so the clock signal may require filtering to smooth edges which might otherwise feed through to the signal path. Also, low-pass or band-pass filters may be required in the signal path to eliminate noise or other undesirable signals (e.g., harmonics). The relative jitter between the clock and test signals must be low enough to prevent jitter artifacts from affecting the measured noise floor as described in 9.4.4.

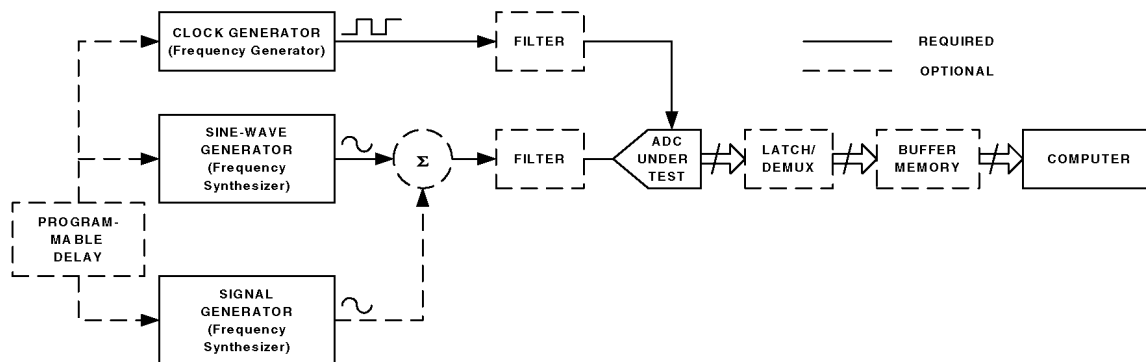


Figure 4—Setup for sine-wave testing

4.2.2 Arbitrary signal test setup

The arbitrary waveform test setup of Figure 5 can be used for arbitrary test signals, such as ramps, chirps, and steps. In this setup, the test signal is generated digitally and then converted to analog. Care must be taken to quantify the performance of the digital-to-analog converter (DAC) and filter in order to assess (or remove) its impact on the measured performance of the ADC under test. See 4.2.1 for comments on filters and data capture. It may be suitable to use an arbitrary waveform generator for the DAC and filter functions for some ADCs.

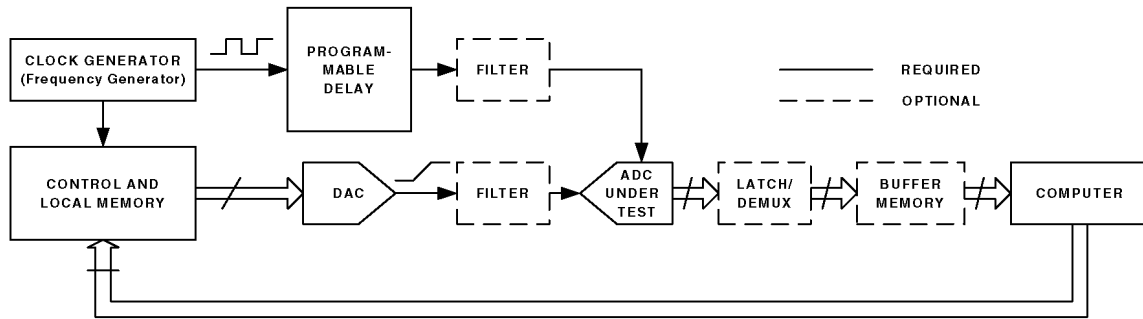


Figure 5—Setup for arbitrary signal testing

4.2.3 Step signal setup

Figure 6 shows a step waveform test setup to be used for testing with precision step signals that are not digitally generated. Precision pulses and step signals can be used to measure both time domain parameters (such as impulse response, transition duration, overshoot, and settling time) and frequency domain parameters (such as frequency response amplitude and phase, bandwidth, and gain flatness). Equivalent-time sampling can be employed, and certain data analysis tasks can be simplified, if the optional step repetition generator is phase locked to the sampling clock. See 4.2.1 for comments on data capture and on filters. Careful attention must be paid to the phase linearity of any filters placed in the pulse/step signal path.

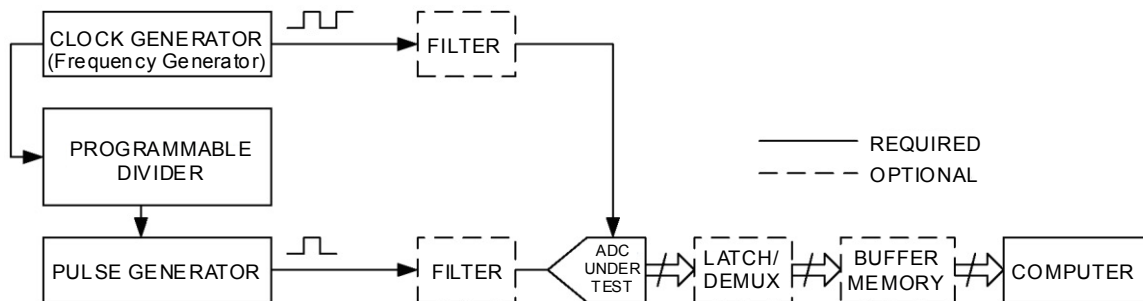


Figure 6—Setup for pulse and step signal testing

4.3 Taking a record of data

A record of data is a sequential series of samples acquired by test equipment interfaced to the ADC. The action of taking a record of data is defined as accumulating a set of samples from the ADC using the interfaced test equipment and transferring the sample set to a computer for analysis.

4.3.1 Use of output decimation in taking a record of data

For ADCs with very high sample rate, the limits of interfaced memory may make it impractical and/or uneconomical to store sequential samples from the ADC. In this case, output decimation may be used to take a record of data at a slower effective sample rate while still clocking the ADC at the high sample rate. A decimated record is a collection of every D th sequential sample acquired by the ADC. To do this, a divide-by- D counter is driven by the (high-frequency) ADC clock, and the output of the divider in turn

drives a bank of data latches (flip-flops), or triggers a logic analyzer to sample the data outputs of the ADC and pass every D th sample along to the memory system.

Output decimation may also be applied on tests that do not directly record the output data, for instance when recording histograms of output code occurrences or feeding back the output code to control the input signal level (see 6.2 and 6.3). The user should note that decimation involves a loss of information, which in special cases, such as hysteresis testing (see 8.7), may affect test results. When output decimation is used, the decimated sample rate, f_s/D , shall be used for any equations relating sample rate to input frequency (e.g., for equivalent-time sampling) or time measurements (e.g., step response parameters), but the actual ADC sample rate f_s shall be quoted as the sample rate in the test results.

For decimation of the output of an ADC system that has a time-interleaved architecture (i.e., L ADCs each sampling at f_s/L), the output decimation ratio D should be made relatively prime to the interleave ratio L ; otherwise, the decimated output data stream will not contain data from all of the L interleaved converters.

4.4 Equivalent-time sampling and undersampling

The maximum sampling rate of a converter limits its useful measurement bandwidth. Furthermore, if the sampling rate is not at least twice the frequency of the highest frequency component of the input signal, then aliasing errors can result. If the input signal is repetitive, equivalent-time sampling can reduce these limitations. Equivalent-time sampling is a process by which consecutive samples of a repetitive waveform are acquired and assembled from multiple repetitions of the waveform, to produce a record of samples representing a single repetition of the waveform.

Several methods of equivalent-time sampling exist:

- a) Apply a known delay between the input signal and the converter's time base
- b) Independently measure the relative delay between the signal and the (time base) sample commands
- c) Extract equivalent time samples from a single record using the converter's internal time base, provided that the input signal's repetition rate is selected appropriately

The method in 4.4.1 implements the extraction method.

4.4.1 Extraction method

The method below shows how to use equivalent-time sampling to increase the effective sampling rate by an integer factor D . By appropriate choice of the repetition rate of the input signal (f_i), D periods of the input waveform are recorded in a single record; then, upon rearranging the samples with a simple algorithm, a single period of the input signal is obtained which is effectively sampled at D times the real-time sampling rate. This is illustrated in Figure 7 for $D = 4$. To implement this method, choose integer D based on the required equivalent sample rate, f_{eq} , such that $f_{eq} = Df_s$, where f_s is the ADC sampling frequency. Next, L , the number of real-time samples taken during each repetition of the input waveform, is given by $L = \text{INT}(M/D)$, i.e., the integer value of M/D , where M is the number of samples in a record. Finally, the input signal's repetition rate, f_i , is set [as shown in Equation (7)] such that

$$f_i = f_s \frac{D}{LD - 1} \text{ with } LD \leq M \quad (7)$$

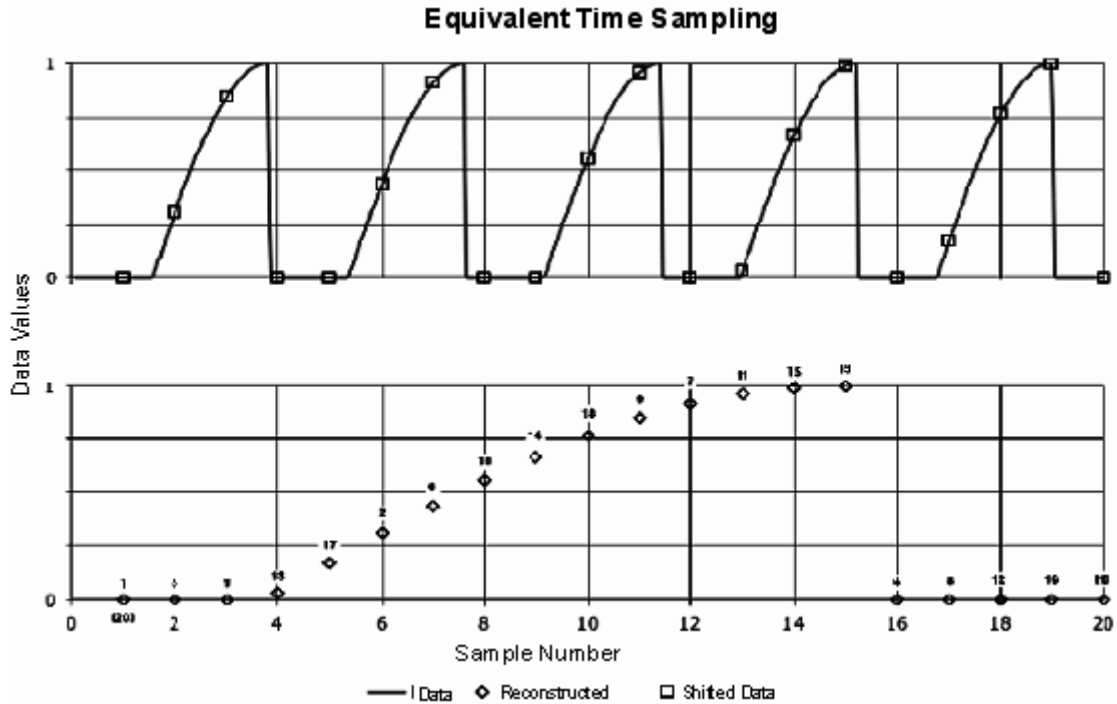


Figure 7—Equivalent-time sampling extraction

For the example of Figure 7, $D = 4$, $L = 5$, M could be 20, 21, 22, or 23, and $f_i = 4f_s/19$. (Note that data points between LD and M are not useable). The following pseudo-code implements the algorithm to rearrange the samples in equivalent time:

```

LET F = 0
FOR I = 1 TO L
  FOR J = 1 TO D
    F = F + 1
    I2 = I + (J - 1)*L
    E(F) = R(I2)
  NEXT J
NEXT I

```

where

- D is the sample rate multiplier
- M is the record length
- L is the $\text{INT}(M/D)$ where $\text{INT}(*)$ designates the integer part of *
- E(*) is the array containing LD equivalent-time samples
- F is the equivalent-time sampling index
- R(*) is the array containing real-time samples
- I2 is the real-time sampling index

4.4.2 Comments on the extraction method for equivalent-time sampling

This method of achieving higher equivalent sampling rates requires that the repetition rate, f_i , of the input signal be precisely controlled. While the average equivalent-time sample rate is just Df_s , independent of f_i , the relative spacing of the equivalent-time samples becomes non-uniform when f_i deviates from the value

given by Equation (7). If f_i is too great, $D - 1$ out of D successive samples will occur too late while one sample will be correctly placed; if f_i is too small, $D - 1$ samples will occur too soon. In either case, the maximum sampling time error (Δt_{eq}) is given, to a good approximation, by Equation (8).

$$\Delta t_{eq} \approx \frac{M(D-1)}{Df_s} \frac{\Delta t_i}{t_i} \quad (8)$$

where

- t_{eq} is the average equivalent-time sampling period, i.e., $1/(D \cdot f_s)$
- Δt_{eq} is the maximum sampling time offset
- $\Delta t_i/t_i$ is the proportional error in the repetition period (or repetition rate)

Note, however, that the errors are not cumulative; the average equivalent-time sampling period is still given by $1/Df_s$.

Of course, the assumption is made in Equation (7) that f_s is exactly known; if it is not exactly known, then the additional error given by an expression similar to Equation (8) will accrue. As an example, if $D = 4$, $M = 1024$, and the equivalent sampling period is known to 5%, then the repetition rate must be set, and the sampling rate must be known, each with an accuracy of $0.05/(1024 \times 3) = 16$ parts in 10^6 .

To achieve such accuracy it is usually necessary to use a frequency-synthesized source. It may sometimes be necessary to measure the frequency of the input signal as well as the frequency of the ADC's clock generator with an accurate frequency counter to ensure that they are set with sufficient accuracy. If sufficient accuracy cannot be guaranteed for a specific record length, the accuracy might be improved by decreasing the record length. However, since the lowest frequency component that is represented in a record of length M is given by f_{eq}/M , this limits the range of frequencies that can be represented.

4.4.3 Alternate extraction method

This alternate method of extracting an equivalent time record is based upon a simple keep-one-of-each- D -samples decimation of an input record. While the decimation operation could be performed in either hardware or software, the method as outlined here implicitly assumes that the decimation is done in software.

At a sampling frequency, f_s , it is possible to adjust the input frequency, f_i , of a repetitive waveform to obtain exactly one cycle in a record of length M , as shown in Equation (9).

$$f_i = nf_s + \frac{f_s}{M} \quad n = 0, 1, 2, 3, \dots \quad (9)$$

Intentional aliasing of the input occurs when n is greater than or equal to one. The usual concern about not being able to tell which alias is observed does not apply in the practical case, as the input signal is known a priori.

When an ADC output data record is decimated by the factor D , the decimated output is sampled at a sampling frequency f_d ; when a record of length M is decimated by keeping only one of every D samples it will be of length M_d , as shown in Equation (10) and Equation (11).

$$f_d = \frac{f_s}{D} \quad (10)$$

$$M_d = \frac{M}{D} \quad (11)$$

When f_d is substituted for f_s and M_d for M in Equation (9), and using the relation $f_d/M_d = f_s/M$, then one cycle in a record of length M_d results from the input frequency chosen using Equation (12).

$$f_i = nf_d + \frac{f_s}{M} \quad n = 0, 1, 2, 3, \dots \quad (12)$$

When a decimated record of length M_d contains a single cycle of f_i , the equivalent sampling rate, f_{eq} , is the number of points in the decimated record divided by the period of the single cycle. Thus f_{eq} is equivalent to the frequency f_i times the length M_d , as shown in Equation (13).

$$f_{eq} = f_i M_d \quad (13)$$

This method uses input frequencies determined by Equation (12) with n chosen to be an appropriate integer in order to yield an equivalent time record of M_d samples at various frequencies of interest. The resulting records contain a single cycle in a record of length M_d . Each increment of n yields a proportional increase in f_{eq} . If fast Fourier transform (FFT) testing is to be performed on the decimated record, then some integer number of cycles greater than one is usually desired. The input frequency, modified to provide exactly J cycles per record, is given by Equation (14):

$$f_i = nf_d + \frac{Jf_s}{M} \quad n = 0, 1, 2, 3, \dots \quad (14)$$

where J is the number of cycles in record of length M_d

and the equivalent sampling rate f_{eq} is found by Equation (15):

$$f_{eq} = \frac{f_i M_d}{J} \quad (15)$$

Thus increasing J simultaneously increases the number of cycles in the decimated record and decreases the effective sampling rate. The parameter J is not necessarily an integer; it could be adjusted to give a non-integer number of cycles and exact integer equivalent sampling rate increases if that were desired.

4.4.4 Comments on alternate extraction method

This method uses simple keep-one-of- D samples decimation of the ADC output data stream to produce the equivalent-time data samples. Figure 8 depicts this operation. For $D = 2$, one ADC output sample is discarded, while the next is retained in the decimated record. If the decimation is done in software, then this method requires acquiring D times more ADC output samples than will be used. However, this method does not require complicated data reshuffling. Also, small frequency errors result in small errors in the equivalent sampling rate increase, but do not result in apparent systematic jitter of the equivalent-time output samples. This method is useful when an ADC is to be characterized for operation near a given frequency. It does not yield exact integer times increase in effective sampling frequency.

ILLUSTRATION OF UNDERSAMPLING

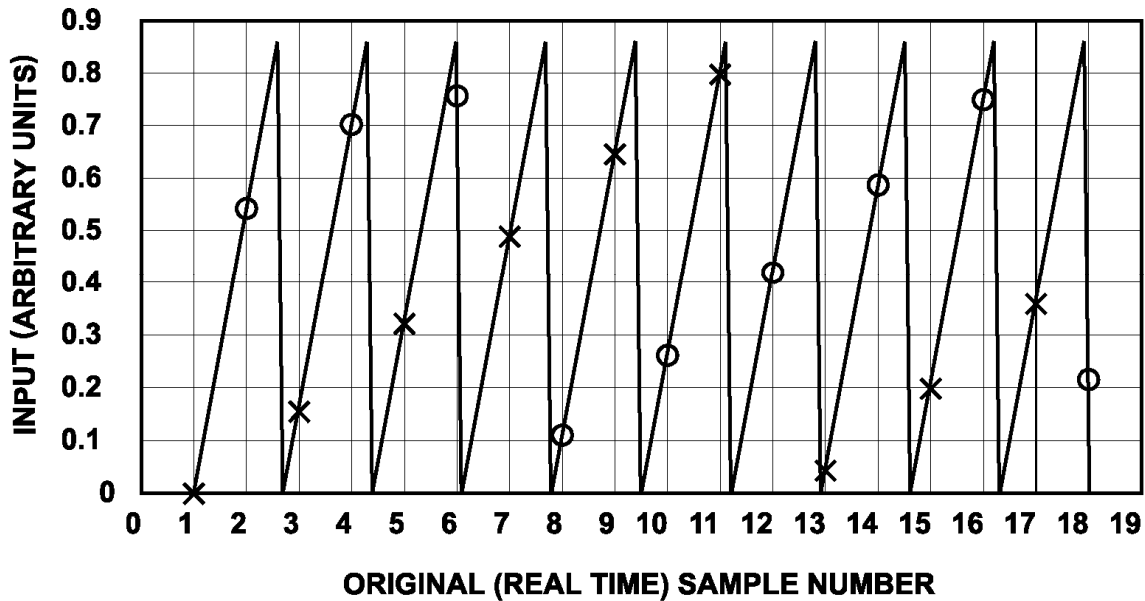


Figure 8—Continuous time waveform showing samples to be kept after decimation-by-2; samples marked “x” are kept; those marked “o” are discarded

This alternate extraction is a simple method for generating equivalent time records of arbitrary numbers of cycles per record which can utilize the same set of analog input frequencies required for coherent FFT-based tests. See 3.1 and 12.2 for coherent FFT input frequency discussions.

Specifically, when the integer M is a power of 2 and the integer D is also chosen to be a power of two, then the input frequencies chosen by Equation (14) will also be optimum input frequencies as described by 5.4.1, when the parameter J is chosen to be an odd integer. It is thus possible to generate a coherent DFT of both the real-time signal and the equivalent-time signal from the same length M data record if this alternate extraction method is used with these restrictions upon M , D , and J .

As in any under-sampled application, small errors due to inclusion of undesired signals from the unwanted base band, or other aliases, may pollute the signal. For narrowband or sine signals, the use of a band-pass filter at the ADC input minimizes any aliased artifacts.

One application of equivalent-time sampling is reconstructing an equivalent-time record to readily observe ADC anomalies, especially dynamic anomalies that become apparent only at input frequencies approaching or above the Nyquist frequency of the ADC. The equivalent-time record can also be used to measure settling times when a non-sinusoidal periodic waveform is used as the input signal. When the equivalent-sampling frequency is chosen to be much greater than the original sampling frequency the equivalent-time record can be used to measure settling times with much greater resolution. This is especially useful when the expected settling time is actually a fraction of one real-time sampling period.

FFTs of the equivalent-time signal are normalized to the equivalent-sampling rate. This can be used to *unscramble* aliased harmonics. This eases the differentiation of harmonics from any spurious tones.

5. Sine-wave testing and fitting

5.1 Introductory information on sine-wave testing and fitting

There are a number of tests that use sine waves as input signals, and there are often questions as to why sine waves are used to test instruments that are often intended to record transients. The primary reason is that very accurate sine-wave signals can be produced, and the accuracy of the signals can be readily tested with a spectrum analyzer. Another reason for the usefulness of sine waves as test signals is that they are eigenfunctions for linear time invariant (LTI) systems. This means that when a pure sine wave is supplied to the input of an LTI system, the output is a pure sine wave of the same frequency but with altered amplitude and phase. Since the analysis of the test results usually assumes that both the amplitude and phase are unknown, the LTI system distortion is ignored. The test results give the nonlinear and time-varying errors.

5.2 Curve fitting test method

Apply a sine-wave signal with appropriate amplitude, frequency, and spectral purity to the input of the ADC. Trigger the ADC to collect a record of data. The trigger does not have to be synchronized to the signal. For the four-parameter method, calculate the values of A_0 , B_0 , C_0 and f_0 that give the best fit, in the least squares sense, to the recorded signal to a function of the form

$$x[n] = A_0 \cos(2\pi f_0 t_n) + B_0 \sin(2\pi f_0 t_n) + C_0 \quad (16)$$

where

t_n is the nominal time associated with the n th data value

For the three-parameter fit, the known frequency is substituted for the parameter f_0 . Subtract the fitted signal from the recorded signal to obtain the residuals.

There are many algorithms for performing the least squares curve fits above. This standard describes methods for both the three- and four-parameter fit.

The sine-wave curve fit is used in several specific test methods described later in this document. Analyze the residuals and fit parameters using methods described for the specific test being performed.

The fitted signal may be converted to the amplitude and phase representation of the function using

$$A_0 \cos(2\pi f_0 t) + B_0 \sin(2\pi f_0 t) = A \cos(2\pi f_0 t + \phi) \quad (17)$$

where

$$A = \sqrt{A_0^2 + B_0^2}$$

$$\phi = \arctan(B_0, A_0)$$

where

$\arctan$ is the standard inverse tangent of two arguments, called ATAN2 in many programming languages, and returns a value in the range of 0 to 2π or in the range from $-\pi$ to π

5.3 Comment on three-parameter versus four-parameter sine fit

The recommended method is the four-parameter method with a record containing at least five cycles of the signal. Even if the input frequency is accurately known a priori, the four-parameter method usually determines it to even better accuracy. The computations are more complicated with the four-parameter method. For records containing less than five cycles, the four-parameter method can underestimate harmonic distortion by compensating for it with a change in frequency. In this case, the three-parameter method may be more appropriate. When frequencies are chosen precisely as recommended for coherent sampling, with an exact integer number of cycles in a record, a DFT will give the same results as a three-parameter sine-wave fit.

5.4 Choice of frequencies and record length

Typically ADCs are tested at several different frequencies. There are several factors that enter into the selection of frequencies. These factors affect frequency selection on three different scales: fine, medium, and coarse. Although the frequency selection decisions are made in the order: coarse, medium, then fine, the criteria are described in the reverse order.

5.4.1 Fine-scale frequency selection

On the fine scale, one wants to select a frequency for which the sampled values will all be different. For example, if a frequency of 200 kHz was used to test an ADC with a sampling rate of 1 MHz, the same five different phases of the sine wave would be sampled many times. The recommended approach is to use a record length, M , and a frequency, f_i such that M uniformly distributed phases will be sampled. This is easily accomplished by choosing f_i as follows:

$$f_i = \left(\frac{J}{M} \right) f_s \quad (18)$$

where

J is an integer which is relatively prime to M
 f_s is the sampling frequency
 M is the record length

The condition of being relatively prime means that M and J have no common factors, i.e., their greatest common divisor is one. For the recommended frequency there are exactly J cycles in a record (called coherent sampling in this standard). If M is a power of two, then any odd value for J meets the relatively prime condition.

If the signal frequency meets the above conditions exactly, the maximum phase difference between successive sampled phases will be $2\pi/M$. The accuracy required of the signal frequency depends strongly on the frequency and on whether the frequency deviation is in the positive or negative direction from the nominal value.

For any value of J , relatively prime to M , there is a unique value, I , between 0 and $M - 1$, which satisfies $\text{mod}(IJ, M) = 1$. The number I is the multiplicative inverse (mod M) of J , and its value determines the frequency accuracy required.

For an exact input frequency, the maximum difference between successive sampled phases is $2\pi/M$. *If the frequency does not have the exact value specified in Equation (18), then the maximum magnitude of the phase difference will be larger.* If the larger value is written in the form $(1 + \rho) \times (2\pi/M)$, then the error, ε_f , in the frequency must satisfy:

$$\left| \frac{\varepsilon_f}{f_i} \right| \leq \begin{cases} \frac{\rho f_s}{IMf_i} & \text{for } \varepsilon_f > 0 \\ \frac{\rho f_s}{(M-1)IMf_i} & \text{for } \varepsilon_f < 0 \end{cases} \quad (19)$$

where

- ε_f is the error in input frequency
- ρ $(1 + \rho)$ is the error limit factor between successively sample phases as defined above
- f_i is the input frequency
- f_s is the sampling frequency
- I is chosen such that $\text{mod}(IJ, M) = 1$
- M is the record length

For positive frequency deviations, I should be as small as possible. For negative frequency deviations, I should be as large as possible (the maximum value is $M - 1$). Tables are available, Blair [B9], that give values of J corresponding to small values of I and small values of $M - I$ for all power-of-two record lengths between 2^8 and 2^{20} . One can choose a frequency from these tables that is close to the desired frequency and determine the accuracy requirement and required direction of deviation from information in the table. If the tables do not contain values of J with acceptable frequencies, one can compute the value for I for an interval of acceptable values of J and select the value with the smallest values of I or $M - I$. The actual deviation of the frequency from the ideal value can be determined from the sine-wave fitting result.

For an ADC with N bits of resolution and an ideal transfer characteristic, the minimum record size that will produce a representative sample in every code bin (in the absence of random noise) is $2^N \times \pi$, when the input frequency is chosen as above. The smallest power-of-two record length is 4×2^N . To achieve one sample in each code bin with this slightly longer record length one can let $1 + \rho = 2\pi/4$, or $\rho = 0.57$.

At low input frequencies, the accuracy requirement for the input frequency becomes much less stringent. However, if a four-parameter fit is being used, the frequency should be chosen large enough that there are at least five cycles in the record. Otherwise, errors may be underestimated.

5.4.2 Medium-scale frequency selection

The rules for fine-scale frequency selection give many frequencies that optimize the spacing between the samples recorded. On the medium scale, one selects frequencies to cause errors from different sources to occur at different frequencies. For example, for an ADC with a sampling rate of 2 GSa/s if a frequency of 400 MHz were selected, third harmonic distortion would be at a frequency of 1200 MHz. Since this is above the Nyquist frequency of 1000 MHz it would be aliased down to 800 MHz. This is the same frequency as second harmonic distortion, so the two would be indistinguishable. With a frequency of 420 MHz, the second harmonic is at 840 MHz while the third harmonic aliases down to 760 MHz, allowing one to distinguish between the two.

In the coarse-scale frequency selection, one normally selects nice round numbers (e.g., 250 MHz, 500 MHz). These round numbers then have to be modified to separate the errors from different harmonics and, perhaps, from interleaving. It is important to take aliasing into account in this step. The resulting frequencies should then be modified a second time to meet the criteria for fine-scale frequency selection.

5.4.3 Coarse-scale frequency selection

Select several test frequencies spanning the range of major expected frequency components in the final-use input signal. The highest frequency signal should have at least as large of a maximum slew rate (derivative with respect to time) as the maximum slew rate of final-use input signal.