



IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

IEEE Instrumentation and Measurement Society

Developed by the
Waveform Generation Measurement and Analysis Committee

IEEE Std 1241™-2023
(Revision of IEEE Std 1241™-2010)

STANDARDS

IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

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Waveform Generation Measurement and Analysis Committee
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Approved 6 May 2023

IEEE SA Standards Board

Abstract: The material presented in this standard is intended to provide common terminology and test methods for the testing and evaluation of analog-to-digital converters (ADCs). This standard considers only those ADCs whose output values are extracted (sampled) and then digitized at known time intervals. In general, this quantization is assumed to be nominally uniform (the input-output transfer curve is approximately a straight line) and the sampling is assumed to be at a nominally uniform rate. Some but not all of the test methods in this standard can be used for ADCs that are designed for non-uniform quantization.

Keywords: ADC, analog-to-digital converter, code transition level, coherent sampling, DNL, ENOB, histogram, IEEE 1241™, INL, LSB, missing codes, noise power ratio, noncoherent sampling, quantization error, quantization noise, SAR, SFDR, sine fitting

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Introduction

This introduction is not part of IEEE Std 1241-2023, IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters.

This standard defines the terms, definitions, and test methods used to specify, characterize, and test analog-to-digital converters (ADCs). It is intended for use by the following:

- Individuals and organizations who specify ADCs to be purchased
- Individuals and organizations who purchase ADCs to be applied in their products
- Individuals and organizations whose responsibility is to characterize and write reports on ADCs available for use in specific applications

This standard is designed to help organizations and individuals to:

- Incorporate quality considerations during the definition, evaluation, selection, and acceptance of supplier ADCs for operational use in their equipment
- Determine how supplier ADCs should be evaluated, tested, and accepted for delivery to end users

This standard is intended to satisfy the following objectives:

- To promote consistency within organizations in acquiring third-party ADCs from component suppliers
- To provide useful practices on including quality considerations during acquisition planning
- To provide useful practices on evaluating and qualifying supplier capabilities to meet user requirements
- To provide useful practices on evaluating and qualifying supplier ADCs
- To assist individuals and organizations judging the quality and suitability of supplier ADCs for referral to end users

Several standards have been previously written that address the testing of analog-to-digital converters either directly or indirectly. These include:

- IEEE Std 1057™-2017 [B23],¹ which describes the testing of waveform recorders. This standard has been used as a guide for many of the techniques described in this standard.
- IEEE Std 746™-1984 [B22], which addresses the testing of analog-to-digital and digital-to-analog converters used for PCM television video signal processing.
- JESD 99-1:1989 [B31], which deals with the terms and definitions used to describe analog-to-digital and digital-to-analog converters. This standard does not include test methods.

IEEE Std 1241™-2010 for analog-to-digital converters is intended to focus specifically on terms and definitions as well as test methods for ADCs for a wide range of applications.

¹ The numbers in brackets correspond to those of the bibliography in Annex E.

Acknowledgements

Portions of Annex A, including text and Figure A.1 through Figure A.8, have been reprinted with permission from “ADC Parameters and Characteristics,” which was written by Sergio Rapuano, Pasquale Daponte, Eulalia Balestrieri, Luca De Vito, Steven J. Tilden, Solomon Max, and Jerome Blair. The article can be found in *IEEE Instrumentation and Measurement Magazine*, vol. 8, no. 5, pp. 44–54, Dec. 2005 [B47]. © 2005 IEEE.

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IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

1. Overview

1.1 Scope

The material presented in this standard is intended to provide common terminology and test methods for the testing and evaluation of analog-to-digital converters (ADCs). This standard considers only those ADCs whose output values are extracted (sampled) and then digitized at known time intervals. In general, this quantization is assumed to be nominally uniform (the input-output transfer curve is approximately a straight line) as discussed further in 1.4, and the sampling is assumed to be at a nominally uniform rate. Some but not all of the test methods in this standard can be used for ADCs that are designed for non-uniform quantization.

1.2 Purpose

This standard identifies ADC error sources and provides test methods with which to perform the required error measurements. The information in this standard is useful both to manufacturers and to users of ADCs in that it provides a basis for evaluating and comparing existing devices, as well as providing a template for writing specifications for the procurement of new ones. In some applications, the information provided by the tests described in this standard can be used to correct ADC errors, e.g., correction for gain and offset errors. The reader should note that this standard has many similarities to IEEE Std 1057™. Many of the tests and terms are nearly the same, since ADCs are a necessary part of digitizing waveform recorders.

1.3 Word usage

The word *shall* indicates mandatory requirements strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*).^{2, 3}

The word *should* indicates that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required (*should* equals *is recommended that*).

The word *may* is used to indicate a course of action permissible within the limits of the standard (*may* equals *is permitted to*).

The word *can* is used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

² The use of the word *must* is deprecated and shall not be used when stating mandatory requirements, *must* is used only to describe unavoidable situations.

³ The use of *will* is deprecated and shall not be used when stating mandatory requirements, *will* is only used in statements of fact.

1.4 Document organization

This standard is divided into fourteen clauses plus annexes. Clause 1 is a basic orientation. For further investigation, users of this standard should consult Clause 2, which contains references to other IEEE standards on waveform measurement and relevant International Standardization Organization (ISO) documents. The definitions of technical terms and symbols used in this standard are presented in Clause 3. Clause 4 through Clause 14 present a wide range of tests that measure the performance of an analog-to-digital converter. Annexes, containing the bibliography and informative comments on the tests presented in Clause 4 through Clause 14, augment the standard.

1.5 Analog-to-digital converter background

This standard considers only those ADCs whose output values are extracted (sampled) and then digitized at known time intervals. Although different methods exist for representing a continuous analog signal as a discrete sequence of binary words, an underlying model implicit in many of the tests in this standard assumes that the relationship between the input signal and the output values approximates the ideal staircase transfer curve depicted in Figure 1(a). Applying this model to a voltage-input ADC, the full-scale input range (FSR) of the ADC is divided into uniform intervals, known as code bins, with nominal width Q . The number of code transition levels (CTLs) in the discrete transfer function is equal to $2^N - 1$, where N is the number of digitized bits of the ADC. Note that there are ADCs that are designed such that N is not an integer, i.e., the number of CTLs is not an integral power of two. Inputs below the first transition or above the last transition are represented by the most negative and positive output codes, respectively. Note, however, that two conventions exist for relating $V_{\min}$ (often called $-FS$, or negative full scale) and $V_{\max}$ (often called $+FS$, or positive full scale) to the nominal transition points between code levels, namely, *mid-tread* and *mid-riser*.

The dotted lines at $V_{\min}$, $V_{\max}$, and $(V_{\min} + V_{\max})/2$ in Figure 1(a) indicate what is often called the *mid-tread* convention, where the first transition occurs at $V_{\min} + Q/2$ and the last transition occurs at $V_{\max} - 3Q/2$. This convention gets its name from the fact that the midpoint of the range, $(V_{\min} + V_{\max})/2$, occurs in the middle of a code, i.e., on the *tread* of the staircase transfer function. The second convention, called the *mid-riser* convention, is indicated in the figure by dashed lines at $V_{\min}$, $V_{\max}$, and $(V_{\min} + V_{\max})/2$. In this convention, the first transition occurs at $000 + Q$, the last transition occurs at $000 + FSR - Q$ from the last transition, and the midpoint, $(V_{\min} + V_{\max})/2$, occurs on a staircase riser. The difference between the two conventions is a voltage offset by an amount $Q/2$.

For all tests in this standard, this voltage offset has no effect on the results and either convention may be used. The one place where it does matter is when a device provides or expects user-provided reference signals. In this case, the manufacturer should provide the necessary information relating the reference levels to the code transitions. In both conventions the number of code transitions is $2^N - 1$ and the FSR is from $V_{\min}$ to $V_{\max}$. Even in an ideal ADC, the quantization process produces errors. These errors contribute to the difference between the actual transfer curve and the ideal straight-line transfer curve and are plotted as a function of the input signal in Figure 1(b).

To use this standard, the user should understand how the transfer function maps its input values to output codewords, and how these output codewords are converted to the code bin numbering convention used in this standard. As shown in Figure 2(a), the lowest code bin is numbered 0, the next is 1, and so on up to the highest code bin, numbered $(2^N - 1)$. In addition to unsigned binary [Figure 1(a)], ADCs may use 2's complement, sign-magnitude, Gray, binary-coded decimal (BCD), or other output coding schemes. In these cases, a simple mapping of the ADC's consecutive output codes to the unsigned binary codes may be used in applying various tests in this standard. Note that in the case of an ADC whose number of distinct output codes is not an integral power of 2 (e.g., a BCD-coded ADC), the number of digitized bits N is still defined, but is not an integer.

Real ADCs have other errors in addition to the nominal quantization error shown in Figure 1(b). All errors shall be segregated into the categories of static and dynamic, and this segregation depends on the rate of

change of the input signal at the sampling instant that it is digitized. A slowly varying input shall be considered a static signal if its effects are equivalent to those of a constant signal. Static errors, which include the quantization error, usually result from non-ideal intervals between the CTLs. Dynamic errors occur because of additional sources of error induced by the time variation of the analog signal being sampled. Sources of dynamic error include harmonic distortion from the analog input stages, signal-dependent variations in the time of samples, dynamic effects in internal amplifier and comparator stages, and frequency-dependent variation in the spacing of the quantization levels.

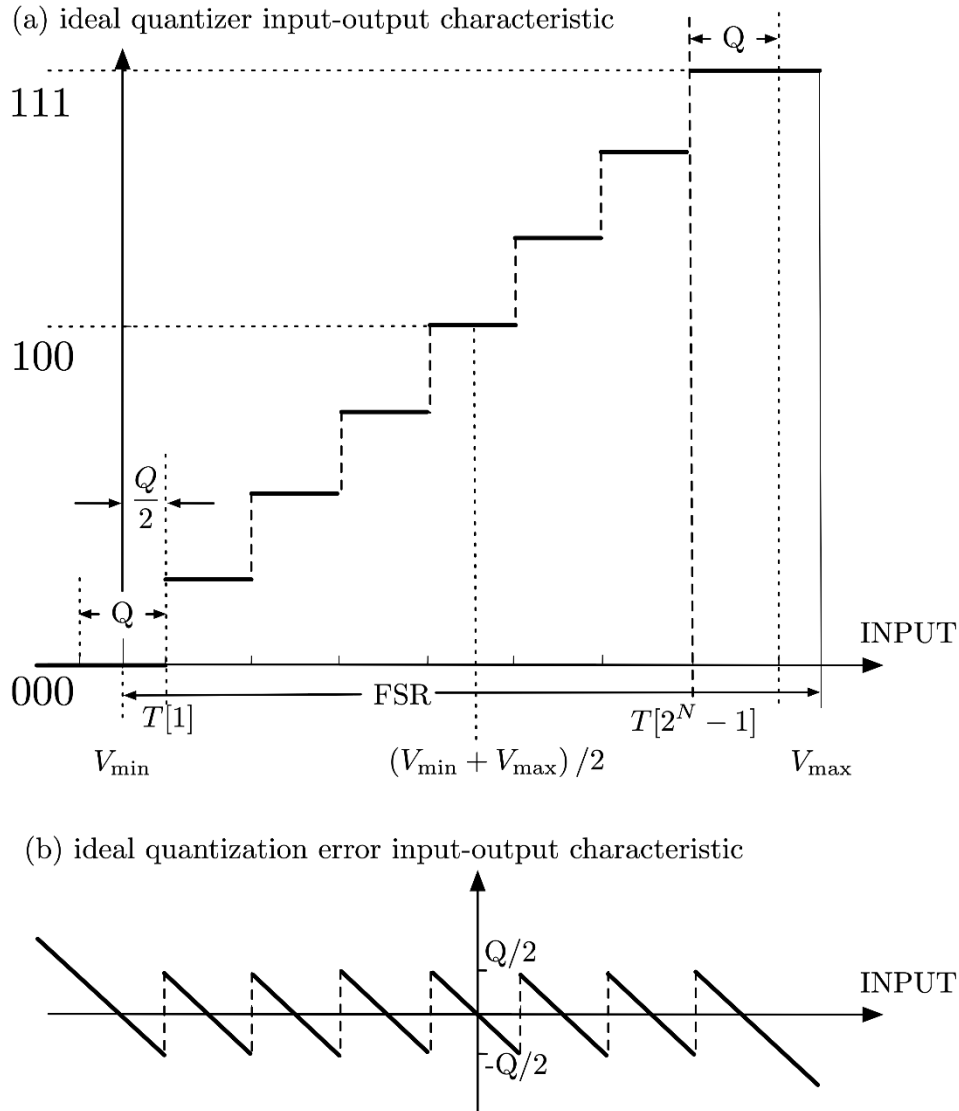


Figure 1—Staircase ADC transfer function, having full-scale range (FSR) and $2^N - 1$ levels, corresponding to N -bit quantization

There are two standard methods for characterizing the error of an ADC:

- a) The CTLs are evaluated as $T[1]$ through $T[2^N - 1]$.
 - 1) For $i = 1$ to $2^N - 2$, the quantity $T'[i] = (T[i] + T[i + 1])/2$ is evaluated.
 - 2) The deviations from nominal of $T'[i]$ are used to define the errors of the ADC.
- b) The CTLs are evaluated as $T[1]$ through $T[2^N - 1]$.
 - 1) The deviations from nominal of $T[i]$ are used to define the errors of the ADC.

The two methods are shown graphically in Figure 2. The ADC characteristics shown in Figure 2 help illustrate the two methods of describing ADC errors. The following should be noted:

- c) The voltages of the CTLs $T[1]$, $T[2]$, $T[3]$, $T[4]$, $T[5]$, and $T[7]$ are those for the ideal CTLs, such as illustrated in Figure 1.
- d) The voltage of $T[6]$ is offset from nominalist ideal value by $+Q/2$.
- e) Figure 2b) shows the error in the ADC output for any input. Note that the maximum error ranges from $-Q/2$ to $+Q/2$, where the code transitions are ideal. Around $T[6]$ the error peaks at a value of $+Q$ before returning to a value of 0.
- f) The ADC is assumed to be noise-free. The ADC is assumed to be calibrated at V_{min} and V_{max} .

The data for Figure 2 is tabulated below.

Code	Ideal $T[\text{code}]$	Actual $T[\text{code}]$	Mid-step ideal $T'[\text{code}]$	Mid-step actual $T'[\text{code}]$	Figure 2(b)
0	NA	NA	NA	NA	NA
1	$0.5Q$	$0.5Q$	$1.0Q$	$1.0Q$	$0.0Q$
2	$1.5Q$	$1.5Q$	$2.0Q$	$2.0Q$	$0.0Q$
3	$2.5Q$	$2.5Q$	$3.0Q$	$3.0Q$	$0.0Q$
4	$3.5Q$	$3.5Q$	$4.0Q$	$4.0Q$	$0.0Q$
5	$4.5Q$	$4.5Q$	$5.0Q$	$5.25Q$	$0.25Q$
6	$5.5Q$	$6.0Q$	$6.0Q$	$6.25Q$	$0.25Q$
7	$6.5Q$	$6.5Q$	NA	NA	NA

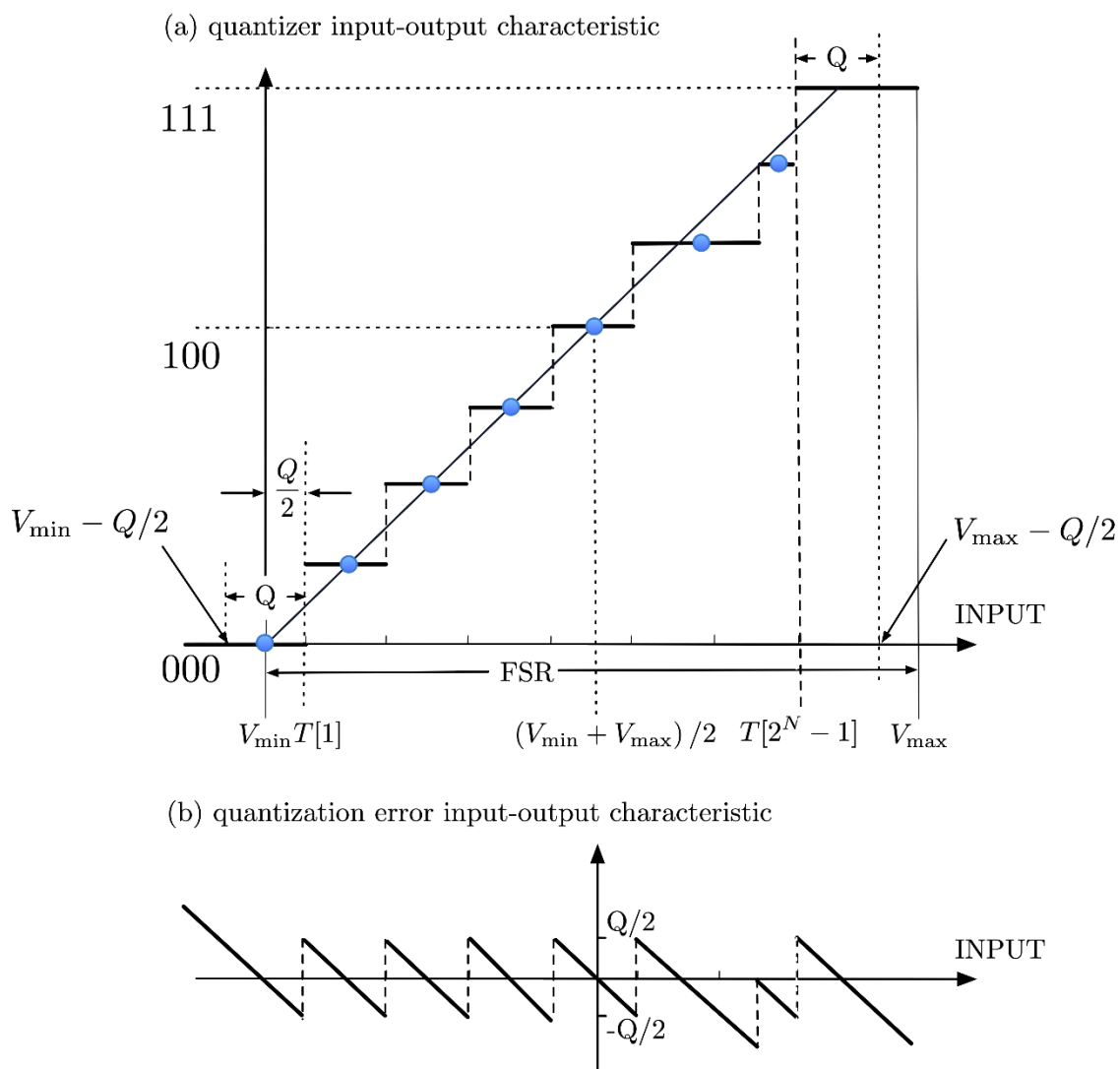


Figure 2—Methods for characterizing the error of an ADC

There are advantages and disadvantages to both methods of analyzing ADC errors:

- a) Code center error analysis (mid-tread):
 - 1) AC analyses such as THD, SINAD, and SNR are better defined by code center error analyses.
 - 2) For a given converter, INL errors are smaller when based on code centers.
 - 3) Histogram error analyses are more closely related to code center error analysis.
- b) CTL error analysis (mid-riser):
 - 1) ADCs that are used for instrumentation are better defined by CTL analysis.
 - 2) Servo measurement techniques of an ADC transfer function identify CTLs.

1.6 Guidance to the user

Conditions described in this section are a general overview of the test environment. More detailed conditions about the environment are included in relevant sections of the standard.

1.6.1 Interfacing

ADCs present unique interfacing challenges, and without careful attention users may experience substandard results. As with all mixed-signal devices, ADCs perform as expected only when the analog and digital domains are brought together in a well-controlled fashion. The user should fully understand the manufacturer's recommendations with regard to proper signal buffering and loading, input signal connections, transmission line matching, circuit layout patterns, power supply decoupling, and operating conditions. Pulse transition characteristics for start-convert pulse(s) and clock(s) should be carefully chosen to maintain input signal integrity with sufficient margin (operational tolerance) for propagation of the signals up to the analog input pin(s) of the ADC. Most manufacturers now provide excellent ADC evaluation boards, which demonstrate recommended layout techniques, signal conditioning, and interfacing for their ADCs. If the characteristics of a new ADC are not well understood, then these boards should be analyzed or used before starting a new layout.

1.6.2 Test conditions

ADC test specifications shall be split into two groups: test conditions and test results. Typical examples of the former are: temperature, power supply voltages, clock frequency, and reference voltages. Examples of the latter are: power dissipation, effective number of bits, spurious free dynamic range (SFDR), and integral non-linearity (INL). The test methods defined in this standard describe the measurement of test results for given test conditions.

ADC specification sheets often give allowed ranges for some test condition (e.g., power supply ranges). This implies that the ADC functions properly and that the test results fall within their specified ranges for all test conditions within their specified ranges.

Since the test condition ranges are generally specified for continuous intervals, they describe an infinite number of possible test conditions for which an ADC obviously cannot be exhaustively tested. It is up to the manufacturer or tester of an ADC to determine, from design knowledge and/or testing, the effect of the test conditions on the test result, and from there to determine the appropriate set of test conditions needed to accurately characterize the range of test results. For example, knowledge of the design may be sufficient to know that the greatest power dissipation (test result) occurs at the greatest power supply voltage (test condition). Accordingly, the power dissipation test need be run only at the high end of the supply voltage range to check that the dissipation is within the maximum of its specified range. It is very important that relevant test conditions be stated when presenting test results.

1.6.3 Electrical environment

When designing a test setup, one should consider the electrical environment. The test setup should be designed so that external disturbances do not affect the test results. Examples of external disturbances include common-mode noise and poor grounding in the set-up. Computers and high-power radio frequency (RF) signals like TV and radio transmitters may be sources of interference.

1.6.4 Test equipment

One should verify that the performance of the test equipment used for these tests significantly exceeds the desired performance of the ADC under evaluation. Users may need to include additional signal conditioning in the form of filters and pulse shapers. Accessories such as terminators, attenuators, delay lines, and other such devices are usually needed to match signal levels and to provide signal isolation to help avoid corrupting the input stimuli.

Quality testing requires following established procedures, most notably those specified in ISO/IEC 17021:2015 [B26]. In particular, traceability of instrumental calibration to a known standard, per ISO/IEC 17025:2017 [B27], is important. Commonly used test setups are described in 4.2.

1.6.5 Test selection

When choosing which parameters to measure, one should follow the outline and hints in this clause to develop a procedure that logically and efficiently performs all needed tests on each unique setup. The standard has been designed to facilitate the development of these test procedures. In this standard, the discrete Fourier transform (DFT) is used extensively for the extraction of frequency domain parameters because it provides numerous evaluation parameters from a single waveform epoch. DFT testing is the most prevalent technique used in the ADC manufacturing community, although the sine-fit test, also described in the standard, provides meaningful data. Nearly every user requires that the ADC should meet or exceed a minimum signal-to-noise-and-distortion ratio (SINAD) limit for the application and that the nonlinearity of the ADC be well understood. Certainly, the extent to which this standard is applied depends upon the application; hence, the procedure should be tailored for each unique characterization plan.

1.7 Manufacturer-supplied information

1.7.1 General information

Manufacturers shall supply the following general information:

- a) ADC part identification
- b) Physical characteristics: dimensions, packaging, pinouts
- c) Power requirements
- d) Environmental conditions: Reliable operating, non-operating, and specified performance temperature range; altitude limitations; humidity limits, operating and storage; vibration tolerance; and compliance with applicable electromagnetic interference specifications
- e) Any special or peculiar characteristics
- f) Compliance with other specifications
- g) Control signal characteristics
- h) Output signal characteristics
- i) Pipeline delay (if any)
- j) Exceptions to the above parameters where applicable

1.7.2 Minimum specifications

The manufacturer shall provide the following specifications (see Clause 3 for definitions):

- a) Absolute accuracy (total unadjusted error)
- b) Analog bandwidth (minimum, maximum, and/or typical)
- c) Clock and digital control signals and level specifications
- d) Input impedance (as applicable)
- e) Input signal full-scale range with nominal reference signal levels (minimum, maximum, and/or typical)
- f) Number of digitized bits (resolution)
- g) Output coding format (binary, two's complement, etc.)
- h) Output logic levels
- i) Power dissipation (minimum, maximum, and/or typical)
- j) Range of allowable sample rates (minimum, maximum)
- k) Reference signal levels to be applied as required (minimum, maximum, and/or typical)
- l) Supply currents (minimum, maximum, and/or typical)
- m) Supply voltages (minimum, maximum, and/or typical)
- n) Timing requirements for inputs and outputs

1.7.3 Additional specifications

- a) Aperture delay time
- b) Aperture uncertainty (aperture short-term time-base instability/jitter) (maximum, typical)
- c) Common-mode rejection ratio (minimum, maximum, and/or typical)
- d) Crosstalk (minimum, maximum, and/or typical)
- e) Differential gain and differential phase (minimum, maximum, and/or typical)
- f) Differential input impedance (as required)
- g) Differential nonlinearity (minimum, maximum, and/or typical)
- h) Effective number of bits (minimum, maximum, and/or typical)
- i) Frequency response (minimum, maximum, and/or typical)
- j) Gain error (minimum, maximum, and/or typical)
- k) Harmonic distortion (minimum, maximum, and/or typical)
- l) Hysteresis (maximum, typical)
- m) Integral nonlinearity (minimum, maximum, and/or typical)
- n) Intermodulation distortion (minimum, maximum, and/or typical)
- o) Maximum common-mode signal levels (minimum, maximum, and/or typical)
- p) Maximum static error (minimum, maximum, and/or typical)
- q) Monotonicity
- r) No missing codes resolution (minimum, maximum, and/or typical)

- s) Random noise (maximum, typical)
- t) Noise power ratio (NPR) (minimum, maximum, and/or typical)
- u) Offset error (minimum, maximum, and/or typical)
- v) Out-of-range/Overdrive recovery time (voltage or current)
- w) Overshoot and precursors
- x) Settling time (minimum, maximum, and/or typical)
- y) Signal-to-noise ratio (minimum, maximum, and/or typical)
- z) Slew rate limit (minimum, maximum, and/or typical)
- aa) Spurious-free dynamic range (minimum, maximum, and/or typical)
- bb) Transition duration of step response (minimum, maximum, and/or typical)
- cc) Word error rate

1.7.4 Pertinent ADC parameters

Table 1 is presented as a guide for many of the most common ADC applications. The wide range of ADC applications makes a comprehensive listing impossible. This table is intended to be a helpful starting point for users to apply this standard to their particular applications.

Table 1—Critical ADC parameters

Typical applications	Critical ADC parameters	Performance issues
Audio	SINAD, THD, noise	— Power consumption — Crosstalk and gain matching
Automatic control	Monotonicity Short-term settling, long-term stability, noise	— Transfer function — Crosstalk and gain matching — Temperature stability
Data acquisition	DNL, INL, gain, offset, noise, out-of-range recovery, settling time, full-scale step response, channel-to-channel crosstalk	— Channel-to-channel interaction — Accuracy, traceability (Sol Max)
Digital oscilloscope/waveform recorder	SINAD, ENOB, noise Bandwidth Out-of-range recovery Word error rate	— SINAD for wide bandwidth amplitude resolution — Low thermal noise for repeatability — Bit error rate
Geophysical	THD, SINAD, long-term stability, noise	— Millihertz response
Imaging	DNL, INL, SINAD, ENOB, noise Out-of-range recovery Full-scale step response	— DNL for detection of short-duration transitions — High-resolution at switching rate — Recovery from blooming
Radar and sonar	SINAD, IMD, ENOB SFDR Out-of-range recovery, noise	— SINAD and IMD for clutter cancellation and Doppler processing
Spectrum analysis	SINAD, ENOB SFDR, noise	— SINAD and SFDR for high linear dynamic range measurements
Spread spectrum communication	SINAD, IMD, ENOB SFDR, NPR Noise-to-distortion ratio, noise	— IMD for quantization of small signals in a strong interference environment — SFDR for spatial filtering — NPR for interchannel crosstalk
Telecommunication personal communications	SINAD, NPR, SFDR, IMD Bit error rate Word error rate, noise	— Wide input bandwidth channel bank — Interchannel crosstalk — Compression — Power consumption
Instrumentation	DNL, SINAD, SFDR, DG, DP, noise	— Differential gain and phase errors — Frequency response
Wideband digital receivers SIGINT, ELINT, COMINT	SFDR, IMD SINAD, noise	— Linear dynamic range for detection of low-level signals in a strong interference environment — Sampling frequency
COMINT= communications intelligence DG = differential gain error DNL = differential nonlinearity DP = differential phase error ELINT = electronic intelligence ENOB = effective number of bits IMD = intermodulation distortion INL = integral nonlinearity NPR = noise power ratio SFDR = spurious free dynamic range SIGINT = signal intelligence SINAD = signal-to-noise-and-distortion ratio THD = total harmonic distortion		

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they should be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 181TM-2011, IEEE Standard on Transitions, Pulses, and Related Waveforms.^{4, 5}

3. Definitions, acronyms, and abbreviations

3.1 Definitions

For the purposes of this document, the following terms and definitions apply. The *IEEE Standards Dictionary Online* should be consulted for terms not defined in this clause.⁶

ac-coupled analog-to-digital converter: An analog-to-digital converter utilizing a network that transmits only the time-varying ac portion, not the static dc portion, of the analog input signal to the quantizer.

aliasing: The phenomenon in sampled data systems whereby signal components at input frequencies greater than half the sampling frequency are converted to frequencies at less than half the sampling frequency in the output data record.

alternation band: The range of input levels that causes the ADC output to alternate between two consecutive code bins. A property of some analog-to-digital converters, it is the complement of the hysteresis property.

analog bandwidth: Unless otherwise specified, the difference between the upper and lower frequency at which the amplitude response as seen in the data record is 0.707 (−3 dB) of the response as seen in the data record at the specified reference frequency.

analog-to-digital converter (ADC): A device that converts a continuous time signal into a discrete-time discrete-amplitude signal.

aperture: The interval during which the input signal into the ADC affects the ADC's sampled output or the weighting function that determines the sampled output from the input signal.

aperture delay: The delay from the instant of a threshold crossing of the analog-to-digital converter clock to the aperture center instant at which the analog input signal is sampled.

aperture duration ($p\%$): The $[50 - (p/2)]\%$ to $[50 + (p/2)]\%$ transition duration of the step response of the ADC. If ringing of the step response causes multiple crossings of either of the levels, the $p\%$ aperture duration is the time from the first crossing of the first level to the last crossing of the second level. Note: The significance is that the output of the ADC is determined, with an error of $(100 - p)\%$ or less, by the input signal in an interval of this duration. Common values of p are 50, 80, and 99.9. For $p = 80$, this is the 10% to 90% transition duration of the step response.

aperture jitter: *See: aperture uncertainty.*

⁴ The IEEE standards or products referred to in Clause 2 are trademarks owned by The Institute of Electrical and Electronics Engineers, Incorporated.

⁵ IEEE publications are available from The Institute of Electrical and Electronics Engineers (<https://standards.ieee.org/>).

⁶ *IEEE Standards Dictionary Online* is available at: <http://dictionary.ieee.org>. An IEEE Account is required for access to the dictionary, and one can be created at no charge on the dictionary sign-in page.

aperture uncertainty: The standard deviation of the apparent sampling instant. *Syn:* **aperture jitter.**

asynchronous sampling: Refers to sampling an input signal that is not phase locked to the analog-to-digital converter sampling frequency.

clock signal duty cycle: The fraction of the clock period that the clock signal is greater than the logic threshold.

clock signal slew rate: The time derivative of the clock signal at the instant where it crosses the logic threshold.

code bin (k): A digital output that corresponds to a particular set of input values.

code bin width ($W[k]$): The difference between two consecutive code transition levels, $T[k + 1]$ and $T[k]$:

$$W[k] = T[k + 1] - T[k] \quad (1)$$

code transition level, k^{th} ($T[k]$) (CTL): The value of the ADC input representing the boundary of the ADC transfer function between code $k - 1$ and code k . It corresponds to the constant input signal value such that the probability of the output code to be greater than or equal to k is equal to 50%.

Code Transition Level	Code Bin	Code Bin Width
$T[2^N-1]$	2^N-1	
$T[2^N-2]$	2^N-2	$W[2^N-2]$
	$\vdots$	$\vdots$
$T[k+2]$		
$T[k+1]$	$k+1$	$W[k+1]$
$T[k]$	k	$W[k]$
$T[k-1]$	$k-1$	$W[k-1]$
	$\vdots$	$\vdots$
$T[2]$		
$T[1]$	1	$W[1]$
	0	

Figure 3—Definitions pertaining to input quantization

coherent sampling: Sampling of a periodic signal such that there is an integer number of signal cycles in the waveform epoch. Coherent sampling occurs when the following relationship exists:

$$Mf_i = Jf_s \quad (2)$$

where

f_s	is the sampling frequency
J	is the integer number of cycles of the signal in the waveform epoch
f_i	is the frequency of the input signal
M	is the number of samples in the waveform epoch

common-mode out-of-range: A signal level whose magnitude is less than the specified maximum common-mode signal but greater than the maximum operating common-mode signal.

common-mode out-of-range recovery interval: The interval required for the analog-to-digital converter under test to return to its specified transfer characteristics after the end of a common-mode out-of-range input signal.

common-mode range: The range of analog input signal swing at each differential input over which the common-mode rejection is specified. Common-mode range is also the sum of the largest simultaneously applied common-mode signal and differential-mode signal.

common-mode rejection ratio (CMRR): The ratio of the input common-mode signal to the effect produced at the output of the analog-to-digital converter under test, in units of the input signal.

common-mode signal: The average value of the signals at the positive input and the negative input of a differential-input analog-to-digital converter. If the signal at the positive input is designated V_+ , and the signal at the negative input is designated V_- , then the common-mode signal V_{cm} is:

$$V_{cm} = \frac{V_+ + V_-}{2} \quad (3)$$

conversion (clock) rate (f_s): The frequency at which digital output words are provided by the analog-to-digital converter on its output.

crosstalk: Undesired energy appearing in a signal as a result of coupling from other signals.

data valid time: A measure of the interval, in units of analog-to-digital converter clock cycles, between the first clock transition after the data becomes valid at the digital outputs and the last clock transition before it becomes invalid.

decibels full scale (dBFS): The root-mean-square (rms) amplitude of any signal in decibels relative to a sine wave that spans the entire input range of the ADC.

differential-input impedance: For a differential-input analog-to-digital converter, the impedance between the positive input and the negative input.

differential-mode signal: The difference between the signal at the positive and negative inputs of a differential-input analog-to-digital converter. *See also:* **normal-mode signal**. If the signal at the positive input is designated V_+ , and the signal at the negative input is designated V_- , then the differential-mode signal (V_{dm}) is:

$$V_{dm} = V_+ - V_- \quad (4)$$

differential nonlinearity (DNL): The difference between a specified code bin width and the average code bin width, divided by the average code bin width.

discrete Fourier transform (DFT): A mathematical operation that converts sampled data from the time domain to the frequency domain. *Contrast:* **inverse discrete Fourier transform (IDFT).**

effective number of bits (ENOB): A measure of the signal-to-noise-and-distortion ratio used to compare actual analog-to-digital converter (ADC) performance to an ideal ADC.

epoch (waveform epoch): An interval to which consideration of a waveform is restricted for a particular calculation, procedure, or discussion. Except when otherwise specified, it is assumed to be the span over which the waveform is measured or defined. As an example, for an M -sample record acquired at the uniform sampling period T_s , the epoch is MT_s . [IEEE Std 181-2011]⁷

equivalent-time sampling: A process by which consecutive samples of a repetitive signal are acquired and assembled from multiple repetitions of the signal, to produce a record of samples representing a single repetition of the signal.

frequency response: The complex gain (magnitude and phase) as a function of input frequency, or the Fourier transform of the impulse response.

full-scale range (FSR): The difference between the most positive and most negative analog inputs of a converter's operating range.

full-scale signal: A full-scale signal is one whose peak-to-peak amplitude spans the entire range of input values recordable by the analog-to-digital converter under test.

gain and offset: (A) (independently based) Gain and offset are the values by which the input values are multiplied and then to which the input values are added, respectively, to minimize the magnitude of the mean squared deviation from the output values. **(B) (terminal based)** Gain and offset are the values by which the input values are multiplied and then to which the input values are added, respectively, to cause the deviations from the output values to be zero at the terminal points, that is, at the first and last codes.

gain flatness: Variation of gain over a specified frequency range, usually expressed in decibels.

harmonic distortion (of a signal source): For an assumed sine-wave signal, the amplitudes of the components at frequencies that are multiples of the signal frequency by integers greater than 1.

harmonic distortion (of an ADC): For a sine-wave input signal, the amplitudes of the output signal components at frequencies that are at integer multiples, by a factor between 2 and a specified upper limit, of the input sine-wave frequency, or the aliases of these frequencies.

hysteresis: The maximum difference in the values of a CTL when the CTL is approached by an input signal whose value is first greater (less) than and then less (greater) than the value of the CTL.

ideal code bin width (Q): The ideal full-scale input range divided by the total number of code bins:

$$Q = \frac{FSR}{2^N - 1} \quad (5)$$

input impedance: The impedance between either the positive input and ground or the negative input and ground. This impedance may be specified at several different frequencies. When the frequency is not

⁷ Information on references can be found in Clause 2.

specified, the impedance given is the static value. Alternatively, the input impedance may be represented as the parallel combination of a resistance and a capacitance.

integral nonlinearity (INL): The maximum difference between the ideal and actual CTLs after correcting for gain and offset.

inverse discrete Fourier transform (IDFT): A mathematical operation that converts sampled data from the frequency domain to the time domain. *Contrast:* **discrete Fourier transform (DFT).**

large signal: One whose peak-to-peak amplitude is as large as practical but is recorded by the instrument within, but not including, the maximum and minimum amplitude data codes. As a minimum, the signal should span at least 90% of the full-scale range of the analog-to-digital converter under test.

least significant bit (LSB): With reference to analog-to-digital converter input signal amplitude, an LSB is synonymous with one ideal code bin width (Q).

level: Constant value having the same units as the input signal. [IEEE Std 181-2011]

logic level: Any level within one of two (or more) non-overlapping ranges of values, of a physical quantity, used to represent the logic.

long-term settling error: The absolute difference between the final signal value specified for short-term settling time and the signal value 1 s after the beginning of the step, expressed as a percentage of the step amplitude.

maximum common-mode signal level: The maximum level of the common-mode signal at which the common-mode rejection ratio is still valid.

maximum operating common-mode signal: The largest common-mode signal for which the analog-to-digital converter meets its specifications when recording a simultaneously applied, normal-mode signal.

maximum input signal level: The input level beyond which damage to the device may occur.

monotonic analog-to-digital converter: An analog-to-digital converter that has output codes that do not decrease (increase) for a uniformly increasing (decreasing) input signal, disregarding random noise.

noise power ratio (NPR): The ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the discrete Fourier transform spectrum of the ADC output sample set.

noise (total): Any deviation between the output signal (converted to input units) and the input signal except deviations caused by linear time invariant system response (gain and phase shift), a dc level shift, or harmonic distortion.

noise floor: Maximum power level over a given frequency band in the frequency domain of components that are not due to the applied signal, harmonics, or spurious signals. The level could be absolute (expressed in decibels with respect to a milliwatt per unit of bandwidth) or relative to the waveform recorder input full scale (expressed in decibels with respect to full scale per unit of bandwidth).

noncoherent sampling: Sampling of a signal such that the relationship between the input frequency, sampling frequency, number of cycles in the waveform epoch, and the number of samples in the waveform epoch does not meet the definition of coherent sampling.

normal-mode signal: The difference between the signal at the positive input and the negative input of a differential input analog-to-digital converter. *Syn:* differential-mode signal.

Nyquist frequency (f_N): Frequency equal to one-half the sampling frequency.

Nyquist zone, n^{th} : The frequency band from $(n - 1)f_N$ to nf_N .

offset: *See: gain and offset.*

out-of-range input: Any input whose magnitude is less than the maximum input signal of the analog-to-digital converter but greater than the full-scale range.

out-of-range recovery interval: The interval required for the analog-to-digital converter under test to return to its specified transfer characteristics after the end of an out-of-range input signal.

overshoot: A waveform aberration within a post-transition aberration region or pre-transition aberration region that is greater than the upper state boundary for the associated state level. [IEEE Std 181-2011]

passband: The band of input signal frequencies that the analog-to-digital converter is intended to digitize with nominally constant gain.

percent reference level: A *reference level* specified by:

$$y_{x\%} = y_{0\%} + \frac{x}{100}(y_{100\%} - y_{0\%})$$

where

$$0\% < x < 100\%$$

$y_{0\%}$ is the *level of low state*

$y_{100\%}$ is the *level of high state*

$y_{0\%}$, $y_{100\%}$, and $y_{x\%}$ are all in the same unit of measurement

Commonly used reference levels are 0%, 10%, 50%, 90%, and 100%. [IEEE Std 181-2011]

phase nonlinearity: The deviation in phase response from a perfectly linear-phase response as a function of frequency.

pipeline delay: A measure of the latency in terms of analog-to-digital converter clock cycles between the clock transition that initiates sampling of the input and the presentation of the digitized value of that sample at the digital output.

precursor: In a step or pulse waveform, any deviation from the base state prior to the pulse transition. The precursor includes both pre-transition overshoot and undershoot.

probability density function (PDF): For a random variable, a non-negative real function, $f_x(x)$, which has the interpretation that $f_x(x) dx$ is the probability that the random variable lies in the interval $(x, x + dx)$.

quantization: A process in which the continuous range of values of an input signal is divided into non-overlapping sub-ranges, and to each sub-range a discrete value of the output is uniquely assigned. Whenever the signal value falls within a given sub-range, the output has the corresponding discrete value. (*IEEE Standards Dictionary Online*)

quantization error/quantization noise: The error caused by conversion of a variable having a continuous range of values to a quantized form having only discrete values, as in analog-to-digital conversion. The error is the difference between the original (analog) value and its quantized (digital) representation. (*IEEE Standards Dictionary Online*)

random noise: A non-deterministic fluctuation in the output of an analog-to-digital converter, described by its frequency spectrum and its amplitude statistical properties. *See also:* **noise**.

record of data: A sequential collection of samples acquired by the analog-to-digital converter.

reference level: A user specified *level* that extends through all *instants* of the *waveform epoch*. [IEEE Std 181-2011] *See also:* **level**, **percent reference level**.

relatively prime: Describes integers whose greatest common divisor is 1.

residuals: In curve fitting, the differences between the recorded data and the fitted function.

root-mean-square (rms): For a given set of data, the square root of the arithmetic mean of the squared values of each of the data.

root-sum-square (rss): For a given set of data, the square root of the sum of the squared values of each of the data.

sampling: The process of assigning discrete time values to a continuous time signal.

settling time: The instant at which the step response enters and subsequently remains within a specified state boundary around its final value, measured from the 50% reference level of the response. The final value is defined to occur 1 s after the beginning of the step.

short-term settling time: Measured from the 50% reference level instant of the output, the time at which the **step response** enters and subsequently remains within a specified state boundary around its final value. The final value is defined to occur at a specified time less than 1 s after the beginning of the step.

signal-to-noise-and-distortion ratio (SINAD): For a single-frequency sine-wave input of specified amplitude, the ratio of the root-mean-square (rms) amplitude of the analog-to-digital converter output signal to the rms amplitude of its output noise, where this output noise includes the noise as defined in “noise (total)” and nonlinear distortion and the effects of sampling time errors.

single-ended analog-to-digital converter: A non-differential analog-to-digital converter, i.e., one that does not subtract the signals at two input terminals. Such a converter may add multiple inputs.

slew limit: The value of the output transition rate of change for which an increase in the amplitude of the input step signal causes no change.

small signal: A signal whose peak-to-peak amplitude is less than 10% of the full range of the analog-to-digital converter under test.

signal: A physical phenomenon that is a function of time and space. [IEEE Std 181-2011]

signal-to-noise-ratio (SNR): For a single-frequency sine-wave input of specified amplitude, the ratio of the root-mean-square (rms) amplitude of the analog-to-digital converter output signal to the rms amplitude of the output noise, where this noise does not include the harmonic distortion components that are used for the estimate of THD.

spectral leakage: Spectral lines near to the input line produced by the discrete Fourier transform (DFT) when the input is a pure sine wave whose frequency does not satisfy the coherent sampling condition and thus is not at the center of a DFT frequency bin.

spurious components: Persistent sine waves at frequencies other than the harmonic frequencies. *See:* **harmonic distortion**.

spurious-free dynamic range (SFDR): For a single-frequency sine-wave input of specified frequency and amplitude, the ratio of the amplitude of the analog-to-digital converter's output averaged spectral component at the input frequency, f_i , to the amplitude of the largest harmonic or spurious spectral component observed over the first Nyquist zone:

$$SFDR(\text{dB}) = 20 \log_{10} \left(\frac{X_{avm}(f_i)}{\max\{X_{avm}(f_h), X_{avm}(f_{sp})\}} \right) \quad (6)$$

where

$X_{avm}(f)$ is the averaged magnitude spectrum at frequency f of the ADC output
 f_i is the input signal frequency
 f_h and f_{sp} are the frequencies of the set of harmonic and spurious spectral components
 $\max\{X, Y\}$ returns the maximum of X and Y

step (or pulse) base state: The state of a waveform that, unless otherwise specified, possesses a level closest to zero [IEEE Std 181-2011].

step (or pulse) high state: The most positive state within the waveform epoch, unless otherwise specified [IEEE Std 181-2011].

step response: The recorded output response for an ideal input step with designated base state and high state.

synchronous sampling: Refers to sampling an input signal that has been phase locked to the analog-to-digital converter sampling frequency.

total harmonic distortion (THD): For a single-frequency sine-wave input of specified amplitude, the root-sum-of-squares (rss) of all the harmonic distortion components including their aliases in the spectral output of the analog-to-digital converter. Unless otherwise specified, THD is estimated by the rss of the second through the tenth harmonics, inclusive. THD is often expressed as a decibel ratio with respect to the root-mean-square amplitude of the output component at the input frequency.

total spurious distortion: For a pure sine-wave input of specified amplitude and frequency, the root-sum-square of the spurious components in the spectral output of the analog-to-digital converter. Total spurious distortion is often expressed as a decibel ratio with respect to the root-mean-square amplitude of the output component at the input frequency.

transfer curve: The representation of the average digital output code of an analog-to-digital converter as a function of the input signal value.

transition duration of a step response: The difference between the two reference level instants of the same transition. Unless otherwise specified, the two reference levels are the 10% and 90% reference levels. [IEEE Std 181-2011]

undershoot: A waveform aberration within a post-transition aberration region or a pre-transition aberration region that is less than the lower state boundary for the associated state level. [IEEE Std 181-2011]

useful power bandwidth: The large signal analog input frequency at which a record of the analog-to-digital converter's output data is degraded by less than a specified amount.

voltage standing wave ratio (VSWR): The ratio of the maximum voltage to the minimum voltage in standing wave pattern along the length of a transmission line structure.

waveform: A representation of a signal (for example, a graph, plot, oscilloscope presentation, discrete time series, equations, or table of values). This term refers to a measured or otherwise-defined estimate of the physical phenomenon or signal. [IEEE Std 181-2011]

waveform epoch: An *interval* to which consideration of a *waveform* is restricted for a particular calculation, procedure, or discussion. Except when otherwise specified, it is assumed to be the span over which the *waveform* is measured or defined. [IEEE Std 181-2011]

window: A set of coefficients with which corresponding samples in a waveform epoch are multiplied so as to more accurately estimate certain properties of the signal, particularly frequency domain properties. Generally, the coefficient values increase smoothly toward the center of the record.

word error rate: The frequency of erroneous codes for an input after correction is made for gain, offset, and linearity errors, and a specified allowance is made for random noise. Typical causes of word errors are metastability and timing jitter of comparators within the analog-to-digital converter.

3.2 Acronyms, abbreviations, and symbols

This subclause lists in 3.2.1 the acronyms, abbreviations, including those for units of measure, and operators and in 3.2.2 the symbols representing the variables used herein. The arguments of the operators are contained with curly brackets to distinguish them from the index of discrete functions, which are contained in square brackets. This segregation is intended to facilitate the use of this standard. In the event that a symbol is identical to an associated abbreviation, the former is italicized.

3.2.1 Acronyms, abbreviations, and operators

AAE	absolute accuracy error
ADC	analog-to-digital converter
AWG	arbitrary waveform generator
BCD	binary coded data
CMMR	common-mode rejection ratio
CTL	code transition level
dB	decibel
dB _c	decibel relative to carrier frequency
dBFS	a decibel ratio with respect to a full-scale signal
dc	direct current, refers to the constant level output by a source
dB _m	decibel relative to 1 mW
DAC	digital-to-analog converter
DFT	discrete Fourier transform
DMT	discrete multi-tone
DNL	differential nonlinearities
ENOB	effective number of bits
FDM	frequency-division multiplexed
FS	full scale
FSR	full scale range
GSa	giga sample
GSa/s	giga-samples-per-second
Hz	Hertz
IDFT	inverse discrete Fourier transform
IF	intermediate frequency
IMD	intermodulation distortion
INL	integral nonlinearities
INT{ <i>z</i> }	operator that returns the integer of its argument, <i>z</i>

kSa/s	kilo-samples-per-second
LSB	least significant bit
$\max\{z_i\}$	operator that returns the maximum of its arguments, z_i
$\min\{z_i\}$	operator that returns the minimum of its arguments, z_i
$\text{mod}\{z_1, z_2\}$	operator that returns the remainder of z_1/z_2
mW	milliwatt
MHz	megahertz
MTPR	multi-tone power ratio
MSa/s	mega-samples-per-second
nV	nanovolt
NAD	noise and distortion
NPR	noise power ratio
PAR	peak-to-average ratio
PDF	probability density function
PSD	power spectral distribution
PSRR	static PSRR
rms	root-mean square
rss	root sum of squares
s	second
RF	radio frequency
SADC	sub-ADC
SAR	successive-approximation-register
SDAC	sub-digital-to-analog converter
SFDR	spurious free dynamic range
SINAD	signal-to-noise-and-distortion ratio
SNR	signal-to-noise ratio
$\tan^{-1}(z)$	inverse tangent of argument, z
T/H	track-and-hold
THD	total harmonic distortion
VSWR	voltage standing wave ratio
$(\mathbf{Z})^T$	transpose of vector or matrix, $\mathbf{Z}$

3.2.2 Symbols

a	local variable
$a(t)$	time-varying amplitude modulation of a signal
ac_{out}	change in the rms output code due to imposed ripple
a_i	Fourier coefficients of the window function
A	amplitude of signal, primary use
A_0	cosine coefficient of sine fit
A_{fit}	amplitude of the fitted sine wave having the same units as FSR
A_h	amplitude of the h^{th} harmonic
$A_{c,\text{rms}}$	rms amplitude of the carrier signal
A_{mult}	amplitude multiplicative factor
$A_{\text{pk-pk}}$	peak-to-peak amplitude
A_{rms}	rms amplitude value
$A_{\text{tone,rms}}$	rms amplitude of the missing tone
A_H	amplitude of the dominant single harmonic distortion of ADC
b	local variable
B	tolerance on code bin width
B_H	amplitude of the dominant single harmonic distortion of input signal

B_N	Shift register bit
B_0	sine coefficient of sine fit
BW_a	3 dB attenuation bandwidth of signal with amplitude a
c	local variable
C	used as a local variable
C_0	offset of sine fit
$CMRR$	Common Mode Rejection Ratio
D	local variable
D_N	SAR ADC bits
D_i	matrix for four-parameter sine fit
D_0	matrix for three-parameter sine fit
$DNL[k]$	Differential nonlinearity
DNL_{RMS}	RMS value of the DNL
e	specified error
$e_m(f)$	upper bound for aliasing and first-differencing errors in magnitude response
$e_p(f)$	upper bound for aliasing and first-differencing errors in phase response
e_{rms}	root-mean-square error
$E_G(f)$	gain error as a function of frequency
$E(*)$	sequence of equivalent-time samples
$ENOB_{max}$	maximum effective number of bits
f	general frequency variable
f_c	carrier frequency
f_{co}	cutoff frequency
f_d	decimated sampling rate
f_{eq}	equivalent sample rate
f_h	frequencies of the set of harmonic spectral components
f_i	i^{th} frequency of the input signal
f_{imf}	intermodulation frequencies (sum and difference)
f_k	DFT frequency bins
f_r	repetition rate of the input signal
f_{ref}	reference frequency
f_{r1}, f_{r2}	frequencies of pure sine waves
f_s	sampling frequency
f_{sp}	the frequencies of spurious spectral components
$f_x(x)$	non-negative real-valued function of x
f_{CLK1}, f_{CLK2}	clock frequencies
f_N	Nyquist frequency
$f_{SYSTEM CLK}$	clock signal at twice the rate of $f_{CLK1}=f_{CLK2}$
f_0	frequency of sine fit or frequency of input sine wave
g_n	is the value of the n^{th} sample of the filtered step response
G	gain, static
$G(f)$	gain, frequency dependent
h	the harmonic frequency index
$h[n]$	discrete-time impulse response
hys_{max}	the maximum hysteresis
H	average histogram bin count for a given CTL
$H[i]$	is the number of histogram samples received in code bin i
$H(f_k)$	estimate of the frequency response of the ADC
i	index
I	an integer
J	an integer

k	code bin, ADC output
k_{in}	reference code
K	integer
L	local variable
m_1, m_2	means values of ADC output
M	is the number of samples in the waveform epoch
M_d	number of samples in decimated waveform epoch
M_1, M_2	average of the output codes
$M_+(x)$	number of measurements of output value for input x , for increasing x
$M_-(x)$	number of measurements of output value for input x , for decreasing x
n	counter, integer variable
n_h	corresponds to the chosen set of harmonics of the input test frequency
n_i	bin number of the input frequency
n_{nf}	set of frequency indices that are not at f_i or dc
n_1	index for the f_i
N_{cyc}	integer number of f_i cycles
N_H	the number of the highest order harmonic used
N_0	optimum step size for DAC output
N	number of bits, local integer
N_1, N_2	parameters to define magnitude of DAC input change for ADC output, k
NPR_{max}	theoretical maximum NPR
$p\%$	percent aperture duration
P_{No}	average power spectral density outside the notched frequency band
P_{Ni}	average power spectral density inside the notched band
PSRR_{ac}	power supply rejection ratio
PSRR_{dB}	PSRR in decibels units
Q	ideal code bin width
r	integer defining the width of the moving average window
$r[n]$	residuals
R	local variable
$R(*)$	sequence of real-time samples
$R[n]$	residuals to sine fit
$s[n]$	step response samples
s_i	vector of four-parameter sine-fit coefficients
$\hat{s}_i$	i^{th} least-square solution for four-parameter sine-fit
s_0	vector of three-parameter sine-fit coefficients
$\hat{s}_0$	least square solution for three-parameter sine-fit
S	total number of histogram samples
S_{eff}	effective slew rate of clock signal
S_0	set of all integers between 1 and $M - 1$
t	time
t_d	delay between reference waveform and delayed waveform
t_{eq}	average equivalent-time sampling period
t_n	nominal time associated with the n^{th} data value (discrete sample instants)
t_s	end of specified settling duration
t_{wc}	center of aperture delay
t_1, t_2	set values of delay
T	transition level
$T[k]$	code transition level for the k^{th} transition (between codes $k - 1$ and k)
$T'[k]$	calculated code transition level
$T[k_{\text{in}}]$	code transitions (p52)

T_M	measured transition level
T_{nom}	the nominal value of $T[k]$
T_s	nominal sampling period or sample interval
T_T	true transition level
T_1	the ideal value corresponding to $T[1]$
u	is equal to $1 - v$, with v the desired confidence level expressed as a fraction
$u(*)$	unit step function
v	the dummy integration variable
V	input signal level
$V(t)$	input signal
y_0	sampled output at t_0
V_{cm}	common-mode signal
V_{dm}	differential-mode signal
V_{rms}	the rms of the actual input to the ADC
V_{max}	positive full scale
V_{min}	negative full scale
V_{noise}	rms broadband noise
V_{out}	output code
V_p	peak amplitude of the sine wave
V_{ripple}	rms ripple voltage added to power supply
V_{FS}	full-scale range of the ADC input
V_{IN}	signal input into sample-and-hold amplifier
V_O	the input signal overdrive
V_{OS}	output offset
V_{PS}	Power supply voltage
V_{REF}	reference level for ADC test
$V(t_s)$	value at the end of the specified settling duration
V_-	signal at the negative input
V_+	signal at the positive input
$w[n]$	discrete weighting function or window function
$w(t)$	aperture weighting function
W	nominal code bin width
$W[k]$	code bin width
$W[0]$	width of the bin with the least value
$W[2^N - 1]$	width of the bin with the greatest value
W_M	measured code bin width
W_T	true code bin width
$W_w[f]$	DFT of the discrete window function
$x[n]$	samples
$\mathbf{x}$	vector
$x[n]$	is the waveform
$x_a[n], x_b[n]$	are the samples from the two noise waveforms
$x_k[n]$	represent the k^{th} waveform
x_{n-s}	is the value of the $(n-s)^{\text{th}}$ sample of the unfiltered step response
V_1, V_2	input levels
$X[f_h]$	complex value of the spectral component at frequency f_h
$X_{avm}(f)$	averaged magnitude spectrum at frequency f of the ADC output
$X_{avm}[n]$	averaged magnitude of the spectral component at frequency index n
$X_{wavg}[m]$	the spectrum averaged over K spectra of the windowed waveform epochs
$X_k[m]$	the complex value of the m^{th} spectral component of the k^{th} spectrum
$Xw[k]$	discrete Fourier transform of a windowed input sequence given by $w[i] x[i]$

$X_{w,k}[m]$	complex value of spectral component m for each windowed waveform, k
$y[n]$	fit to $x[n]$
$y_{x\%}$	percent reference level
$\bar{x}(V)$	output code value for input V
$\bar{x}_+(V)$	the mean output values measured at input level V for increasing input level
$\bar{x}_-(V)$	the mean output values measured at input level V for decreasing input level
$Z_{u/2}, Z_{N_u/2}$	local variable
α	local variable
δ	the mean squared difference between the two test waveforms
Δ_{out}	measured change in the ADC output for a change in ADC supply voltage
Δa	fractional frequency deviation between sampling frequency and signal frequency
Δf	frequency difference
Δf_i	frequency increment in four-parameter sine fit
Δt_{eq}	maximum equivalent-time sampling error
$\Delta t_i/t_i$	proportional error in the repetition period (or repetition rate)
ΔV_{PS}	change in power supply voltage
ε	uncertainty in LSB
$\varepsilon[k]$	residual error corresponding to the k^{th} code transition
ε_f	error in the input frequency of sine wave
ε_Q	rms ideal quantization error
η	rms noise estimate of the ADC output
κ	bin number, not necessarily an integer
θ_{adj}	phase adjustment factor
ρ	$(1 + \rho)$ is the error limit factor between successively sample phases
σ_A	standard deviation of the noise with a clock signal applied to analog input of the ADC
σ_B	standard deviation of the noise without a clock signal applied to analog input of the ADC
σ_{max}	maximum value of the standard deviation of the amplitude noise
σ_t	standard deviation of the jitter
σ_T	aperture uncertainty
σ_η	standard deviation of the estimate of the random noise amplitude
σ	standard deviation of the noise;
σ^*	local variable for the rms random noise value
σ_ϕ	rms random phase error of the input signal relative to the sampling instant
$\sigma_x(V)$	standard deviation of the output as a function of the input V
$\sigma_{x+}(V)$	standard deviation of the output, for increasing input levels of V
$\sigma_{x-}(V)$	standard deviation of the output, for decreasing input levels of V
$\varphi(t)$	phase modulation function
ϕ	phase of the sine-wave signal
τ	delay

4. General test methods

4.1 Introductory information on test methods

It is assumed that the user/manufacture has defined operating limits for the device under test. These limits are categorized as *absolute* (the limit beyond which the device is destroyed) and *operating* (the limit beyond which the device does not operate properly). These limits vary from device to device, depending on the design. It is not the intention of this document to describe the method of setting these limits, only to verify the operation within them. All test procedures described herein apply only to parameters of a device that is operated within its specified limits.

The type of circuitry used to capture the digital data samples produced by the ADC is determined largely by the data rate. Low-bandwidth ADCs may be interfaced directly to the computer. ADCs often require a buffer memory to acquire data at the ADC sample rate and then download accumulated samples to the computer at a slower rate. High-bandwidth ADCs may require latches and/or de-multiplexers between the ADC and the buffer memory, and perhaps data decimation, as described in 4.2.2. A logic analyzer might be used as a buffer memory to capture data for some tests.

4.2 Test setup

A few general test setups are used to perform most of the ADC tests presented in this standard. Test setups that use sine waves, arbitrary signals, and pulses are described in the following subclauses. Some tests, such as those for VSWR and out-of-range signals, require setups other than those discussed in the following subclauses.

4.2.1 Sine-wave test setup

Figure 4 shows the sine-wave test setup. Sine waves are commonly used in ADC testing because appropriate sine-wave sources are readily available and because it is relatively easy to establish the quality of the sine wave (e.g., with a spectrum analyzer). A sine-wave generator provides the test signal while a clock generator provides the clock (or conversion) signal. Also, combining the output of two (or three) sine-wave generators may produce two-tone (or three-tone) test signals for intermodulation distortion testing. Additionally, a noise generator's output may be combined with a signal to provide small-amplitude dither (Gray and Stockham [B18]).

If frequency synthesizers are used to generate the test and clock signals, the synthesizers are often phase-locked to maintain precise phase relationships between the signal and the sampling clock. Phase-locking of synthesizers facilitates testing and simplifies subsequent digital signal processing by helping to prevent clock/signal walkthrough (beat patterns) that may artificially increase or reduce measured spurious output.

Both the clock and the test signals should be suitable for the test being performed. Filters may be required in either the clock or signal paths to reduce noise or harmonic distortion. For example, sub-harmonics in the clock path degrade ADC performance, so the clock signal may require filtering to reduce the high-frequency content of the clock-pulse transitions that might otherwise couple to the signal path. Also, low-pass or band-pass filters may be required in the signal path to eliminate noise or other undesirable signals (e.g., harmonics). The relative jitter between the clock and test signals should be small enough so that jitter artifacts do not affect the measured noise floor as described in 9.4.4.

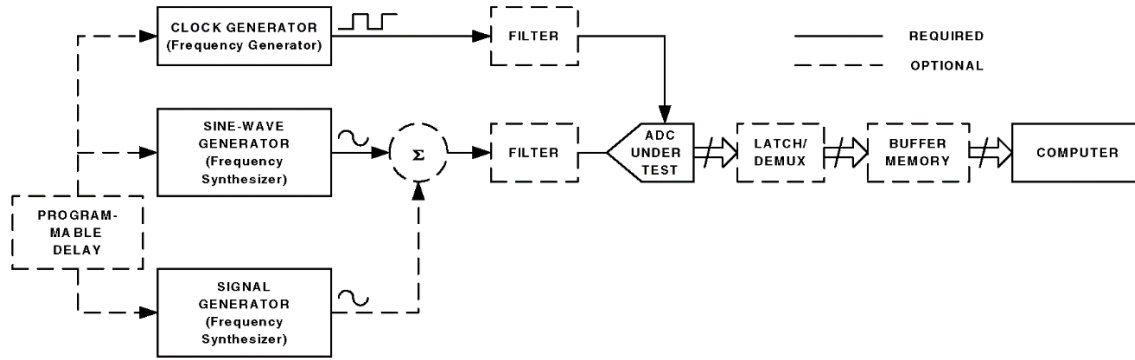


Figure 4—Setup for sine-wave testing

4.2.2 Arbitrary signal test setup

The arbitrary waveform test setup of Figure 5 may be used for arbitrary test signals, such as ramps, chirps, and steps. In this setup, the test signal is generated digitally and then converted to analog. Care should be taken to quantify the performance of the digital-to-analog converter (DAC) and filter in order to assess (or remove) its impact on the measured performance of the ADC under test. See 4.2.1 for comments on filters and data capture. It may be suitable to use an arbitrary waveform generator for the DAC and filter functions for some ADCs.

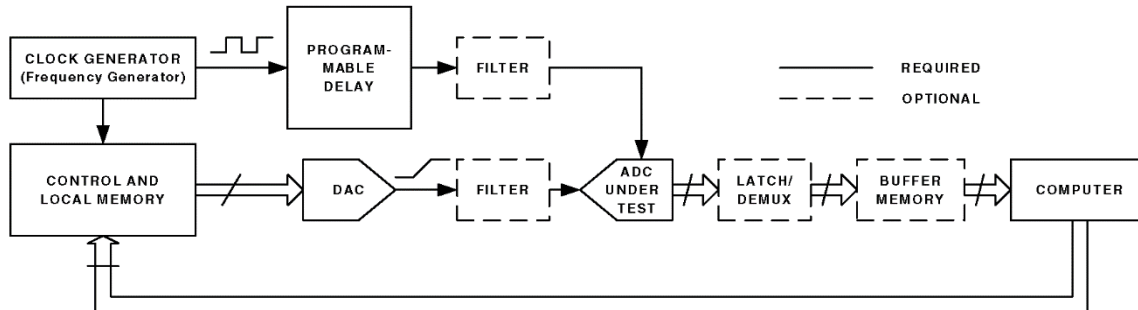


Figure 5—Setup for arbitrary signal testing

4.2.3 Step signal setup

Figure 6 shows a step waveform test setup to be used for testing with precision step signals that are not digitally generated. Precision pulses and step signals may be used to measure both time domain parameters (such as impulse response, transition duration, overshoot, and settling time) and frequency domain parameters (such as frequency response amplitude and phase, bandwidth, and gain flatness). Equivalent-time sampling may be employed, and certain data analysis tasks may be simplified, if the optional step repetition generator is phase locked to the sampling clock. See 4.2.1 for comments on data capture and on filters. Careful attention should be paid to the phase linearity of any filters placed in the pulse/step signal path.

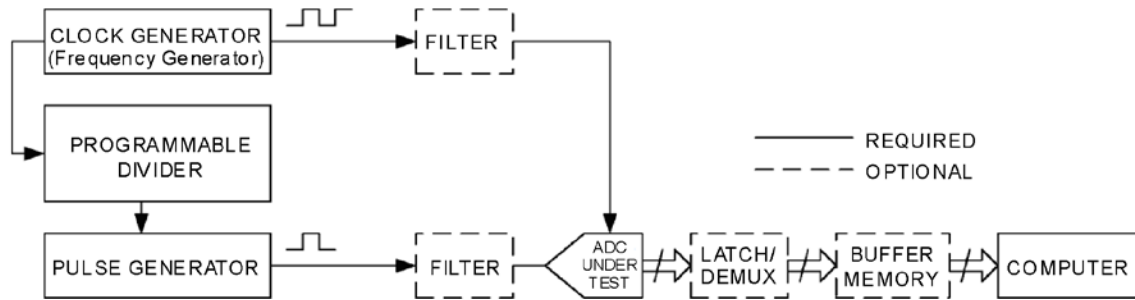


Figure 6—Setup for pulse and step signal testing

4.3 Taking a record of data

A waveform comprises a record of data that is a sequential series of samples acquired by test equipment that is interfaced to the ADC under test. The action of acquiring this data is defined as accumulating a set of samples from the ADC using the interfaced test equipment and then transferring that data to a computer for analysis.

4.3.1 Use of output decimation in taking a record of data

For ADCs with very high sample rate, the limits of interfaced memory may make it impractical and/or uneconomical to store sequential samples from the ADC. In this case, output decimation may be used to record data at a slower effective sample rate while still clocking the ADC at the high sample rate. A decimated waveform epoch is a collection of every D^{th} sequential sample acquired by the ADC. To do this, a divide-by- D counter is driven by the (high-frequency) ADC clock, and the output of the divider in turn drives a bank of data latches (flip-flops) or triggers a logic analyzer to sample the data outputs of the ADC and pass every D^{th} sample along to the memory system.

Output decimation may also be applied on tests that do not directly record the output data, for instance when recording histograms of output code occurrences or feeding back the output code to control the input signal level (see 6.2 and 6.3). The user should note that decimation involves a loss of information, which in special cases, such as hysteresis testing (see 8.7), may affect test results. When output decimation is used, the decimated sample rate, f_s/D , shall be used for any equations relating sample rate to input frequency (e.g., for equivalent-time sampling) or time measurements (e.g., step response parameters), but the actual ADC sample rate f_s shall be quoted as the sample rate in the test results.

For decimation of the output of an ADC system that has a time-interleaved architecture (i.e., L ADCs each sampling at f_s/L), the output decimation ratio D should be made relatively prime to the interleave ratio L ; otherwise, the decimated output data stream may not contain data from all of the L interleaved converters.

4.4 Equivalent-time sampling and undersampling

The maximum sampling rate of an ADC limits its useful measurement bandwidth. Furthermore, if the sampling rate is not at least twice the frequency of the highest frequency component of the input signal, then aliasing errors may result. If the input signal is repetitive, equivalent-time sampling may reduce these limitations. Equivalent-time sampling is a process by which consecutive samples of a repetitive signal are acquired and assembled from multiple repetitions of the signal to produce a record of samples representing a single repetition of the signal.

Several methods of equivalent-time sampling exist:

- Apply a known delay between the input signal and the ADC's time base
- Independently measure the relative delay between the signal and the (time base) sample commands

- c) Extract equivalent time samples from a single waveform using the ADC's internal time base, provided that the input signal's repetition rate is selected appropriately

Only the extraction method (4.4.1) is considered in this standard.

4.4.1 Extraction method

The method below shows how to use equivalent-time sampling to increase the effective sampling rate by an integer factor D . By appropriate choice of the repetition rate of the input signal (f_r), D periods of the input signal are recorded in a single waveform epoch; then, upon rearranging the samples with a simple algorithm, a single period of the input signal is obtained that is effectively sampled at D times the real-time sampling rate. This is illustrated in Figure 7 for $D = 4$. To implement this method, choose the integer D based on the required equivalent sample rate, f_{eq} , such that $f_{eq} = Df_s$, where f_s is the ADC sampling frequency. Next, L , the number of real-time samples taken during each repetition of the input signal, be given by $L = \text{INT}\{M/D\}$, i.e., the integer value of M/D , where M is the number of samples in a waveform epoch. Finally, the input signals repetition rate, f_r , is set such that:

$$f_r = f_s \frac{D}{LD - 1} \quad (7)$$

for $LD \leq M$

where

- D is the number of periods of f_r
- L is the number of real-time samples taken during each repetition of the input signal
- f_s is the sampling frequency
- f_r is the repetition frequency of the input signal

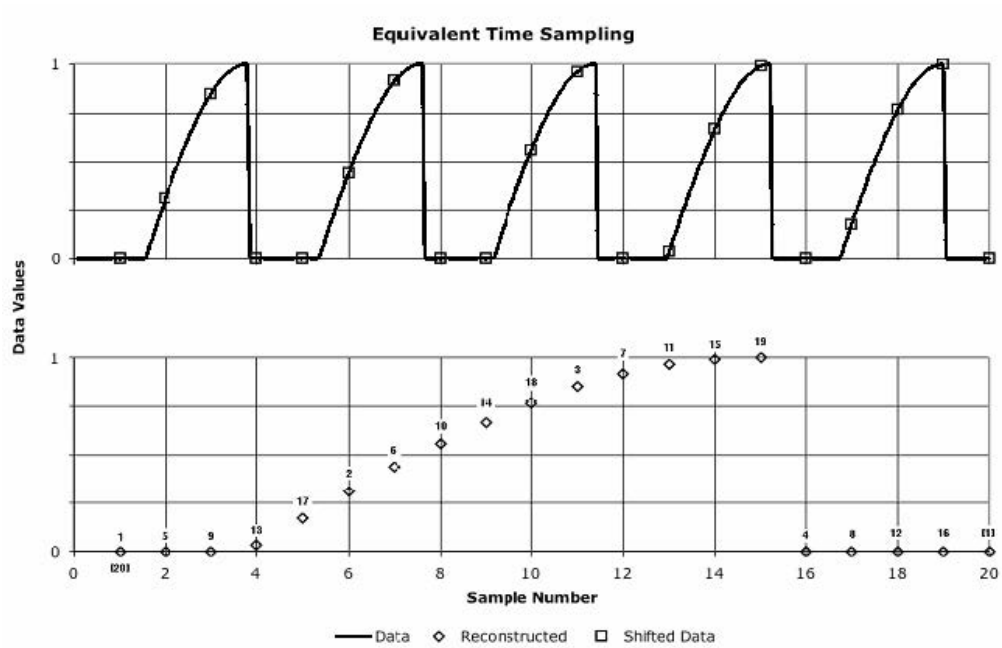


Figure 7—Equivalent-time sampling extraction

For the example of Figure 7, $D = 4$, $L = 5$, M could be 20, 21, 22, or 23, and $f_r = 4f_s/19$. (Note that data points between LD and M are not useable). The following pseudo-code implements the algorithm to rearrange the samples in equivalent time:

```

LET F = 0
FOR I = 1 TO L
    FOR J = 1 TO D
        F = F + 1
        I2 = I + (J - 1)*L
        E(F) = R(I2)
    NEXT J
NEXT I

```

where

D is the sample rate multiplier
 L is the $\text{INT}\{M/D\}$ which is the integer part of M/D
 M is the number of samples in the waveform epoch
 $E(*)$ is the sequence containing LD equivalent-time samples
 F is the equivalent-time sampling index
 $R(*)$ is the sequence containing real-time samples
 $I2$ is the real-time sampling index

4.4.2 Comments on the extraction method for equivalent-time sampling

This method of achieving higher equivalent sampling rates requires that f_r be precisely controlled. While the average equivalent-time sample rate is just Df_s , independent of f_r , the relative interval between the equivalent-time sampling instants becomes non-uniform when f_i deviates from the value given by Equation (7). If f_r is too great, $D - 1$ out of D successive samples occur too late while one sample is correctly timed; if f_r is too small, $D - 1$ samples occur too soon. In either case, the maximum equivalent-time sampling error (Δt_{eq}) is given, to a good approximation, by:

$$\Delta t_{eq} \approx \frac{M(D-1)}{Df_s} \frac{\Delta t_i}{t_i} \quad (8)$$

where

t_{eq} is the average equivalent-time sampling period, i.e., $1/(D \cdot f_s)$
 Δt_{eq} is the maximum equivalent-time sampling error
 $\Delta t_i/t_i$ is the proportional error in the repetition period (or repetition rate)
 M is the number of samples in the waveform epoch

Note, however, that the errors are not cumulative; the average equivalent-time sampling period is still given by $1/Df_s$.

Of course, the assumption is made in Equation (7) that f_s is exactly known; if it is not exactly known, then the additional error given by an expression similar to Equation (8) will accrue. As an example, if $D = 4$, $M = 1024$, and the equivalent sampling period is known to 5%, then the repetition rate should be set, and the sampling rate should be known, each with an accuracy of $0.05/(1024 \times 3) = 16$ parts in 10^6 .

To achieve such accuracy, it is usually necessary to use a frequency-synthesized source. It may sometimes be necessary to measure the frequency of the input signal as well as the frequency of the ADC's clock generator with an accurate frequency counter to help ensure that they are set with sufficient accuracy. If sufficient accuracy cannot be guaranteed for a specific M , the accuracy might be improved by decreasing

M . However, since the lowest frequency component that is represented in a M -long waveform epoch is given by f_{eq}/M , this limits the range of frequencies that may be represented.

4.4.3 Alternate extraction method

This alternate method of extracting an equivalent-time waveform is based upon a simple keep-one-of-each- D -samples decimation of an input record. While the decimation operation could be performed in either hardware or software, the method as outlined here implicitly assumes that the decimation is done in software.

At a sampling frequency, f_s , it is possible to adjust f_r , of a repetitive waveform to obtain exactly one cycle in a waveform epoch of length M , as shown in Equation (9).

$$f_r = nf_s + \frac{f_s}{M}, \text{ for } n = 0, 1, 2, 3, \dots \quad (9)$$

where M is the number of samples in the waveform.

Intentional aliasing of the input occurs when n is greater than or equal to one. The usual concern about not being able to tell which alias is observed does not apply in the practical case, as the input signal is known a priori.

When the waveform of an ADC measurement is decimated by the factor D , the decimated output is sampled at a sampling frequency f_d ; when a waveform epoch having M samples is decimated by keeping only one of every D samples, it will be of length M_d , as shown in Equation (10) and Equation (11).

$$f_d = \frac{f_s}{D} \quad (10)$$

$$M_d = \frac{M}{D} \quad (11)$$

When f_d is substituted for f_s and M_d for M in Equation (9), and using the relation $f_d/M_d = f_s/M$, then one cycle in a waveform epoch of length M_d results from the input repetition frequency chosen using:

$$f_r = nf_d + \frac{f_d}{M_d} \quad (12)$$

for $n = 0, 1, 2, 3, \dots$. When a decimated waveform epoch of length M_d contains a single cycle of f_r , the equivalent sampling rate, f_{eq} , is the number of samples in the decimated waveform epoch divided by the period of the single cycle. Thus, f_{eq} is equivalent to f_r multiplied by M_d :

$$f_{eq} = f_r M_d \quad (13)$$

This method uses input frequencies determined by Equation (12) with n chosen to be an appropriate integer in order to yield an equivalent-time waveform of M_d samples at various frequencies of interest. The resulting waveform epoch contain a single cycle of the sine wave with M_d samples. Each increment of n yields a proportional increase in f_{eq} . If discrete Fourier transform (DFT) testing is to be performed on the decimated waveform epoch, then some integer number of cycles greater than one is usually desired. The f_r modified to provide exactly J cycles per record is given by:

$$f_r = nf_d + \frac{Jf_s}{M} \quad (14)$$

where $n = 0, 1, 2, 3, \dots$; J is the number of cycles in the waveform epoch having M_d samples, and the equivalent sampling rate f_{eq} is found by:

$$f_{eq} = \frac{f_r M_d}{J} \quad (15)$$

Thus, increasing J simultaneously increases the number of cycles in the decimated waveform epoch and decreases the effective sampling rate. The parameter J is not necessarily an integer; it could be adjusted to give a non-integer number of cycles and exact integer equivalent sampling rate increases if that were desired.

4.4.4 Comments on alternate extraction method

This method uses simple keep-one-of- D samples decimation of the ADC output waveform epoch to produce the equivalent-time data samples. Figure 8 depicts this operation. For $D = 2$, one ADC output sample is discarded, while the next is retained in the decimated waveform epoch. If the decimation is done in software, then this method requires acquiring D times more ADC output samples than are used. However, this method does not require complicated data reshuffling. Also, small frequency errors result in small errors in the equivalent sampling rate increase, but do not result in apparent systematic jitter of the equivalent-time output samples. This method is useful when an ADC is to be characterized for operation near a given frequency. It does not yield exact integer times increase in effective sampling frequency.

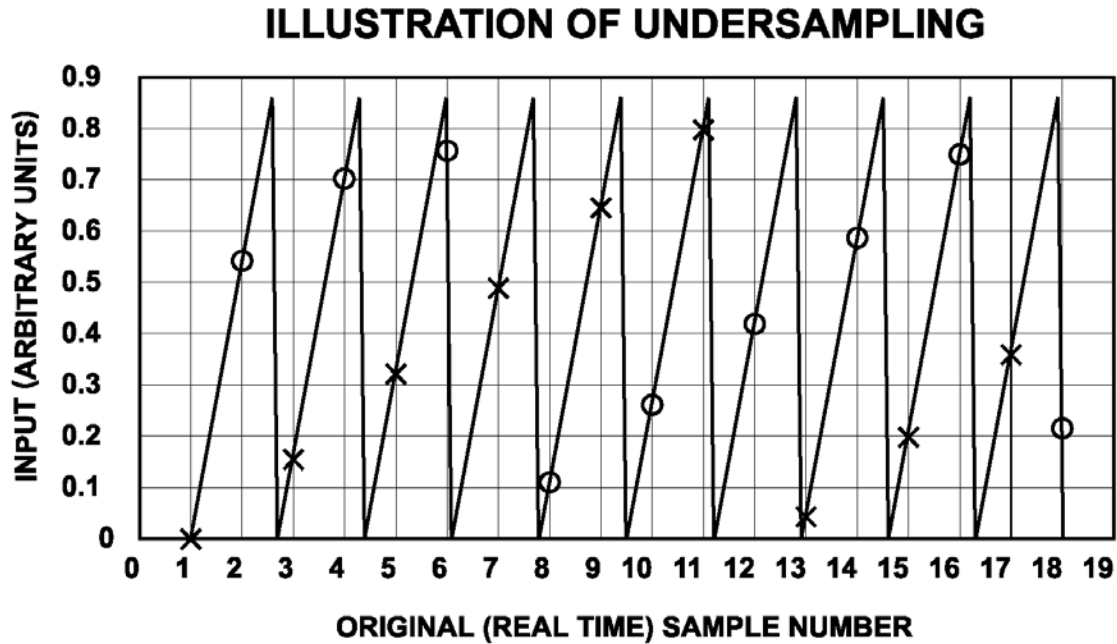


Figure 8—Continuous time waveform showing samples to be kept after decimation-by-2; samples marked “x” are kept; those marked “o” are discarded

This alternate extraction is a simple method for generating equivalent-time waveforms of arbitrary numbers of cycles per waveform epoch, which may utilize the same set of analog input frequencies required for coherent DFT-based tests. See 3.1 and 12.2 for coherent DFT input frequency discussions.