

# IEEE Standard for a High Performance Serial Bus—Amendment 1

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**Microprocessors and Microcomputers Standards Committee**  
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**IEEE Computer Society**

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**IEEE-SA Standards Board**

**Abstract:** Amended information for a high-speed Serial Bus that integrates well with most IEEE standard 32-bit and 64-bit parallel buses is specified. This amendment is intended to extend the usefulness of a low-cost interconnect between external peripherals, as described in IEEE Std 1394-1995. This amendment to IEEE Std 1394-1995 follows the ISO/IEC 13213:1994 Command and Status Register (CSR) Architecture.

**Keywords:** bus, computers, high-speed Serial Bus, interconnect

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# Introduction

(This introduction is not part of IEEE Std 1394a-2000, IEEE Standard for a High Performance Serial Bus—Amendment 1.)

Standards development is an ongoing process and is, perhaps, never complete. In 1994, the working group responsible for IEEE Std 1394-1995, IEEE Standard for a High Performance Serial Bus, reluctantly elected to close the door to new material. Although many enhancements were well understood in principle (some were even making their way into contemporary silicon designs), significant work remained to document the details. Consensus emerged to publish the completed work and later to prepare an amendment. This document is that amendment—it extends and corrects facilities of Serial Bus.

In January 1996, an informal study group was convened by Gerald Marazas, Chair of the IEEE P1394 Working Group. The meeting was held in Dallas, TX, at the same time as a quarterly meeting of the nascent 1394 Trade Association. The topic was unfinished business in Serial Bus; brainstorming quickly identified six major areas of interest. Some of the areas readily resolved into clusters of related activity, which became other Serial Bus standards projects still active at the time of writing—IEEE P1394.1, Draft Standard for High Performance Serial Bus Bridges and IEEE P1394b, Draft Standard for a High Performance Serial Bus—Amendment 2. The topics that were deemed essentially complete (e.g., the alternate 4-pin cable and connector, the PHY arbitration enhancements, and miscellaneous corrections to the 1995 standard) were gathered together under the banner of IEEE P1394a. During the next month, the IEEE P1394a Study Group met to select a chair and draft a Project Authorization Request (PAR). The first official meeting of IEEE P1394a took place in October 1996; the working group continued to meet monthly until its last meeting in February 1998.

The working group organized the new effort as an amendment rather than a new Serial Bus standard intended to replace IEEE Std 1394-1995 entirely. This decision was based upon the belief that the changes in IEEE P1394a were localized to a few areas and that we would be able to complete our work rapidly if we did not have to reissue the entire standard. In retrospect this was an awkward choice. The reader who wishes to be informed of the current Serial Bus standard is forced to consult both the original standard and this amendment. The working group hopes that in the process of international standardization that it is possible to editorially combine the two documents into a single volume.

IEEE P1394a, Draft 2.0 failed the sponsor ballot conducted by the IEEE and generated a large number of comments. In an effort to resolve these comments and pave the way for a successful recirculation ballot, the Ballot Response Committee (BRC) was convened by the IEEE P1394a Chair, Peter Johansson. The BRC first met in the fall of 1998 and continued meeting into 1999 to complete a revision of the draft standard, which was resubmitted to the balloting pool for approval.

IEEE P1394a, Draft 3.0 passed its recirculation and the editor prepared IEEE P1394a, Draft 4.0 for submission to the IEEE-SA Standards Board for approval. The IEEE Standards Review Committee (RevCom) recommended disapproval; as a consequence, the draft was recirculated for its third ballot. The IEEE P1394a Ballot Response Committee believes that there are no substantive changes to the draft between all of these revisions.

IEEE P1394a, Draft 5.0 passed the third and final ballot and was approved as a standard at the 30 March 2000 meeting of the IEEE-SA Standards Board.

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# IEEE Standard for a High Performance Serial Bus—Amendment 1

NOTE—The editing instructions contained in this amendment define how to merge the material contained herein into the existing base standard to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~striketrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make large changes in existing text, subclauses, tables, or figures by removing existing material and replacing it with new material. Editorial notes will not be carried over into future editions because the changes will be incorporated into the base standard.

## 0. Introduction

### 0.1 Scope

IEEE Std 1394a-2000 is a full-use standard whose scope is to amend IEEE Std 1394-1995 by defining or clarifying features and mechanisms that facilitate management of Serial Bus resources, at reconfiguration or during normal operation, and by defining alternate cables and connectors that may be needed for specialized applications.

The following are included in IEEE Std 1394a-2000:

- a) Cables and connectors for a 4-pin variant (from the 6-pin already standardized).
- b) Standardization of the physical layer (PHY)/link interface, previously published as an informative annex (Annex J) in IEEE Std 1394-1995.
- c) Performance enhancements to the PHY layer that are interoperable with the existing standard, e.g., a method to shorten the arbitration delay when the last observed Serial Bus activity is an acknowledge packet.
- d) A redefinition of the isochronous data packet, transaction code A<sub>16</sub>, to permit its use in either the asynchronous or isochronous periods.
- e) More stringent requirements on the power to be supplied by a cable power source and a clarification of electrical isolation requirements.
- f) Significant corrigenda and clarifications to the existing standard that do not clearly fall within any of the topics described above.

The preceding are arranged in no particular order.

## 0.2 Purpose

Experience with Serial Bus has revealed some areas in which additional features or improvements may result in better performance or usability. This amendment to IEEE Std 1394-1995 reflects the consideration of these features or improvements by a variety of users, and their refinement into generally useful facilities or features.

## 0.3 Document organization

IEEE Std 1394a-2000 contains this introduction, an overview, a list of definitions, an informative summary description, sections of technical specification, and application annexes. The new reader should read the informative summary in 3.9 and the clauses that precede it before the remainder of the document.

Most of the changes to IEEE Std 1394-1995, which begin with the editorial instructions, are preceded by background information that explains the scope and impact of the change. The background information should be read before implementing the change.

## 1. Overview

### 1.2 References

*Insert the following in 1.2, in alphabetical order, and renumber footnotes:*

ANSI/EIA 364-C-94, Electrical Connector/Socket Test Procedures Including Environmental Classifications.<sup>1</sup>

ANSI/EIA 364-06A-83 (Reaff 90), Contact Resistance Test Procedure for Electrical Connectors.

ANSI/EIA 364-09B-91, Durability Test Procedure for Electrical Connectors.

ANSI/EIA 364-13A-83 (Reaff 90), Mating and Unmating Forces Test Procedure for Electrical Connectors.

ANSI/EIA 364-17A-87, Temperature Life with or without Electrical Load Test Procedure for Electrical Connectors and Sockets.

ANSI/EIA 364-18A-84, Visual and Dimensional Inspection Procedure for Electrical Connectors.

ANSI/EIA 364-20A-83 (Reaff 90), Withstanding Voltage Test Procedure for Electrical Connectors, Sockets and Coaxial Contacts.

ANSI/EIA 364-21B-95, Insulation Resistance Test Procedure for Electrical Connectors.

ANSI/EIA 364-23A-85, Low Level Contact Resistance Test Procedure for Electrical Connectors.

ANSI/EIA 364-27B-96, Mechanical Shock (Specified Pulse) Test Procedure for Electrical Connectors.

ANSI/EIA 364-28C-97, Vibration Test Procedure for Electrical Connectors and Sockets.

ANSI/EIA 364-31A-83 (R90), Humidity for Electrical Connectors.

ANSI/EIA 364-32B-92, Thermal Shock Test Procedure for Electrical Connectors.

ANSI/EIA 364-41B-89, Cable Flexing Test Procedure for Electrical Connectors.

ANSI/EIA 364-46A-98, Microsecond Discontinuity Test Procedure for Electrical Connectors, Contacts and Sockets.

ANSI/EIA 364-65A-97, Mixed Flowing Gas.

IEC 60950 (1999-04), Safety of information technology equipment.<sup>2</sup>

IEC 61000-4-2 (1999-05) Edition 1.1, Electromagnetic compatibility (EMC)—Part 4-2: Testing and measurement techniques—Electrostatic discharge immunity test.

IEC 61883-1 (1998-02), Consumer audio/video equipment—Digital interface—Part 1: General.

<sup>1</sup>ANSI/EIA publications are available from Global Engineering Documents, 15 Inverness Way East, Englewood, Colorado 80112, USA (<http://global.ihs.com/>).

<sup>2</sup>IEC publications are available from the Sales Department of the International Electrotechnical Commission, Case Postale 131, 3, rue de Varembe, CH-1211, Genève 20, Switzerland/Suisse (<http://www.iec.ch/>). IEC publications are also available in the United States from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA. (<http://www.ansi.org/>)

**Replace 1.5 with the following:**

## 1.5 Service model

This standard uses a protocol model with multiple layers. Each layer provides services to the next higher layer and to Serial Bus management. These services are abstractions of a possible implementation; an actual implementation may be significantly different and still meet all the requirements. The method by which these services are communicated between the layers is not defined by this standard. The following four types of services are defined:

- a) *Request service.* A request service is a communication from a layer to a lower or adjacent layer in order to request some action. A request may also communicate parameters that may or may not be associated with an action. A request may or may not be confirmed. A data transfer request usually triggers a corresponding indication on peer node(s). (Since broadcast addressing is supported on Serial Bus, it is possible for the request to trigger a corresponding indication on multiple nodes.)
- b) *Indication service.* An indication service is a communication from a layer to a higher or adjacent layer in order to indicate a change of state or other event detected by the originating layer. An indication may also communicate parameters that are associated with the change of state or event. Indications are not necessarily triggered by requests; an indication may or may not be responded to by a response. A data transfer indication is originally caused by a corresponding request on a peer node.
- c) *Response service.* A response service is a communication from a layer to a lower or adjacent layer in response to an indication; a response is always associated with an indication. A response may communicate parameters that indicate its type. A data transfer response usually triggers a corresponding confirmation on a peer node.
- d) *Confirmation service.* A confirmation service is a communication from a layer to a higher or adjacent layer in order to confirm a request service; a confirmation is always associated with a request. A confirmation may communicate parameters that indicate the completion status of the request or that indicate other statuses. For data transfer requests, the confirmation may be caused by a corresponding response on a peer node.

If all four service types exist, they are related as shown by figure 1-2.

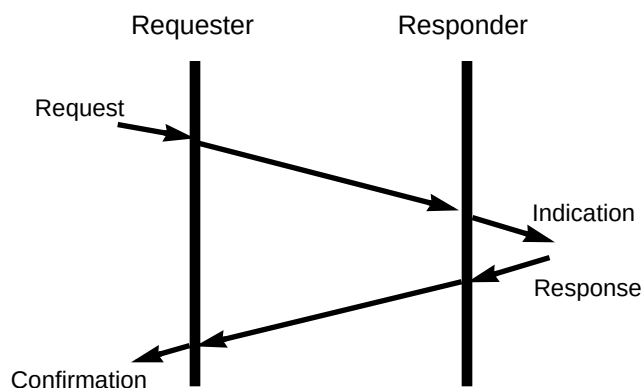


**Figure 1-2—Service model**

**Replace 1.6 with the following:**

## 1.6 Document notation

### 1.6.1 Mechanical notation

All mechanical drawings in this document use millimeters as the standard unit and follow ANSI Y14.2M-1992 [B1]<sup>3</sup> and ANSI Y14.5M-1994 [B2] formats.

### 1.6.2 Signal naming

All electrical signals are shown in all uppercase characters and active-low signals have the suffix “\*”. For example, TPA and TPA\* are the normal and inverted signals in a differential pair.

### 1.6.3 Size notation

This document avoids the terms *word*, *half-word*, and *double-word*, which have widely different definitions depending on the word size of the processor. In their place, processor-independent terms established by previous IEEE bus standards are used. These terms are illustrated in table 1-1.

**Table 1-1 — Size notation examples**

| Size (in bits) | 16-bit word notation | 32-bit word notation | IEEE standard notation<br>(used in this standard) |
|----------------|----------------------|----------------------|---------------------------------------------------|
| 4              | nibble               | nibble               | nibble                                            |
| 8              | byte                 | byte                 | byte                                              |
| 16             | word                 | half-word            | doublet                                           |
| 32             | long-word            | word                 | quadlet                                           |
| 64             | quad-word            | double               | octlet                                            |

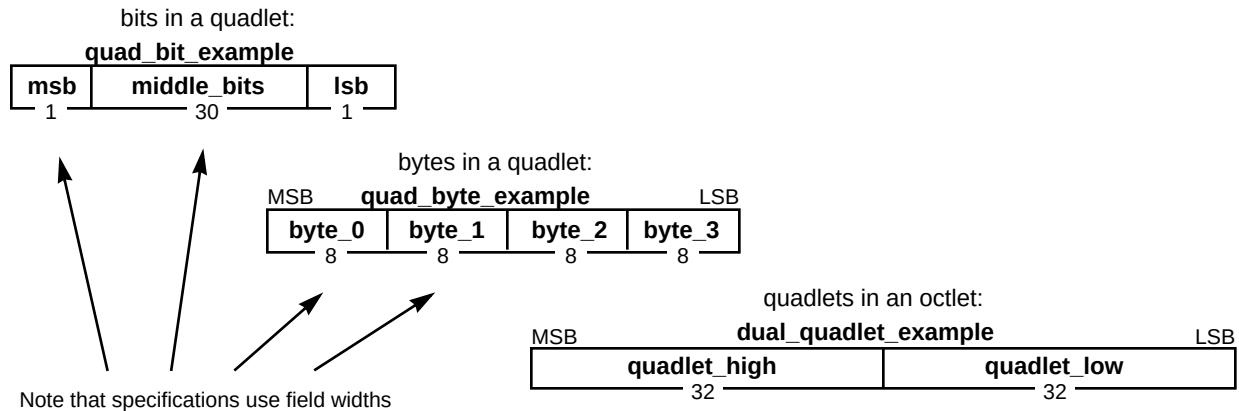
Serial Bus uses big-endian ordering for byte addresses within a quadlet, and quadlet addresses within an octlet. For 32-bit quadlet registers, byte 0 is always the most significant byte of the register. For a 64-bit quadlet-register pair, the first quadlet is always the most significant. The field on the left (most significant) is transmitted first; within a field, the most significant bit (msb) (the leftmost bit) is also transmitted first. This ordering convention is illustrated in figure 1-3.

Although Serial Bus addresses are defined to be big-endian, their data values may also be processed by little-endian processors. To minimize the confusion between conflicting notations, the location and size of bit fields are usually specified by width, rather than their absolute positions, as is also illustrated in figure 1-3.

When specific bit fields must be used, the CSR Architecture convention of consistent big-endian numbering is used. Hence, the most significant bit of a quadlet (“msb” in figure 1-3) is labeled “quad\_bit\_example[0],” the most significant byte of a quadlet (“byte\_0”) is labeled “quad\_byte\_example[0:7],” and the most significant quadlet in an octlet (“quadlet\_high”) is labeled “dual\_quadlet\_example[0:31].”

The most significant bit shall be transmitted first for all fields and values defined by this standard, including the data values read or written to control and status registers (CSRs).

<sup>3</sup>The numbers in brackets correspond to those of the bibliography in Annex N.

**Figure 1-3 — Bit and byte ordering**

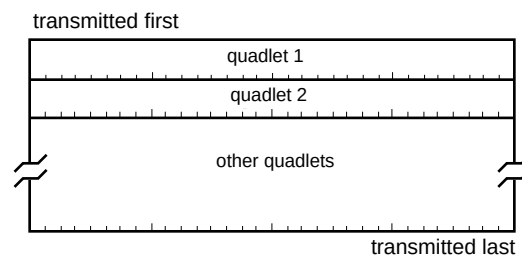
### 1.6.4 Numerical values

Decimal, hexadecimal, and binary numbers are used within this document. For clarity, the decimal numbers are generally used to represent counts, hexadecimal numbers are used to represent addresses, and binary numbers are used to describe bit patterns within binary fields.

Decimal numbers are represented in their standard 0, 1, 2, ... format. Hexadecimal numbers are represented by a string of one or more hexadecimal (0-9, A-F) digits followed by the subscript 16. Binary numbers are represented by a string of one or more binary (0,1) digits, followed by the subscript 2. Thus the decimal number “26” may also be represented as “1A<sub>16</sub>” or “11010<sub>2</sub>”. In C code examples, hexadecimal numbers have a “0x” prefix and binary numbers have a “0b” prefix, so the decimal number “26” would be represented by “0x1A” or “0b11010”.

### 1.6.5 Packet formats

Most Serial Bus packets consist of a sequence of quadlets. Packet formats are shown using the style given in figure 1-4.

**Figure 1-4 — Example packet format**

Fields appear in packet formats with their correct position and widths. Bits in a packet are transmitted starting with the upper leftmost bit and finishing with the bottom rightmost bit. Given the rules in 1.6.3, this means that all fields defined in this standard are sent most significant bit first.

### 1.6.6 Register formats

All Serial Bus registers are documented in the style used by the CSR Architecture.

### 1.6.7 C code notation

The conditions and actions of the state machines are formally defined by C code. Although familiar to software engineers, C code operators are not necessarily obvious to all readers. The meanings of C code operators, arithmetic, relational logical and bitwise, both unary and binary, are summarized in table 1-2.

**Table 1-2 — C code operators summary**

| Operator         | Description                                                                                                                                                 |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| +, -, *, and /   | Arithmetic operators for addition, subtraction, multiplication, and integer division                                                                        |
| %                | Modulus; $x \% y$ produces the remainder when $x$ is divided by $y$                                                                                         |
| >, >=, <, and <= | Relational operators for greater than, greater than or equal, less than, and less than or equal                                                             |
| == and !=        | Relational operators for equal and not equal; the assignment operator, =, should not be confused with ==                                                    |
| ++               | Increment; $i++$ increments the value of the operand after it is used in the expression while $++i$ increments it before it is used in the expression       |
| --               | Decrement; post-decrement, $i--$ , and pre-decrement, $--i$ , are permitted.                                                                                |
| &&               | Logical AND                                                                                                                                                 |
|                  | Logical OR                                                                                                                                                  |
| !                | Unary negation; converts a nonzero operand into 0 and a zero operand into 1                                                                                 |
| &                | Bitwise AND                                                                                                                                                 |
|                  | Bitwise inclusive OR                                                                                                                                        |
| ^                | Bitwise exclusive OR                                                                                                                                        |
| <<               | Left shift; $x << 2$ shifts the value of $x$ left by two bit positions and fills the vacated positions with zero                                            |
| >>               | Right shift; vacated bit positions are filled with zero or one according to the data type of the operand, but in this standard, are always filled with zero |
| ~                | One's complement (unary)                                                                                                                                    |

A common construction in C code is conditional evaluation, in the form  $(\text{expr}) ? \text{expr1} : \text{expr2}$ . This indicates that if the logical expression  $\text{expr}$  evaluates to a nonzero value, then  $\text{expr1}$  is evaluated, otherwise  $\text{expr2}$  is evaluated. For example,  $x = (q > 5) ? x + 1 : 14$  first evaluates  $q > 5$ . If nonzero (TRUE),  $x$  is incremented, otherwise  $x$  is assigned the value 14.

The descriptions above are casual; if in doubt, the reader is encouraged to consult ISO/IEC 9899:1990.

The C code examples assume the data types listed in table 1-3 are defined.

**Table 1-3 — Additional C data types**

| Data type | Description                                                                        |
|-----------|------------------------------------------------------------------------------------|
| timer     | A real number, in units of seconds, that autonomously increments at a defined rate |
| Boolean   | A single bit, where 0 encodes FALSE and 1 encodes TRUE                             |

All C code is to be interpreted as if it could be executed instantaneously, but time may elapse when conditional expressions are evaluated as part of iterated C code. Time elapses unconditionally only when the following function is called:

```
void wait_time(float time); // Wait for time, in seconds, to elapse
```

### 1.6.8 State machine notation

All state machines in this standard use the style shown in figure 1-5.

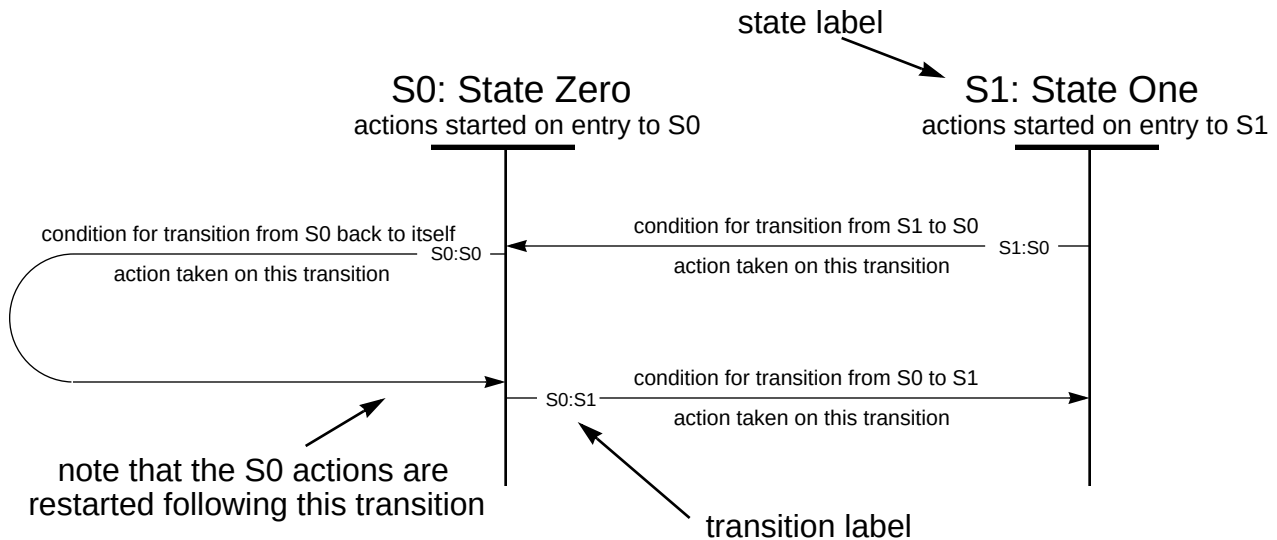


**Figure 1-5 — State machine example**

These state machines make the following three assumptions:

- Time elapses only within discrete states.
- State transitions are logically instantaneous, so the only actions taken during a transition are setting flags and variables, and sending signals. These actions complete before the next state is entered.
- Every time a state is entered, the actions of that state are started. Note that this means that a transition that points back to the same state causes the actions to be repeated from the beginning. All the actions started upon entry complete before any tests are made to exit the state.

### 1.6.9 CSR, ROM, and field notation

This standard describes CSRs and fields within them. To distinguish register and field names from node states or descriptive text, the register name is always capitalized. For example, the notation `STATE_CLEAR.lost` is used to describe the lost bit within the `STATE_CLEAR` register.

All CSRs are quadlets and are quadlet aligned. The address of a register is specified as the byte offset from the beginning of the initial register space and is always a multiple of four. When a range of register addresses is described, the ending address is the address of the last register.

This document describes a number of configuration ROM entries and fields within these entries. To distinguish ROM entry and field names from node states or descriptive text, the first character of the entry name is always capitalized. Thus, the notation Bus\_Info\_Block.cmc is used to describe the cmc bit within the Bus\_Info\_Block entry.

Entries within temporary data structures, such as packets, timers, and counters, are shown in lowercase (following normal C language conventions) and are formatted in a fixed-space typeface. Examples are arb\_timer and connected[i] .

NOTE—Within the C code, the character formatting is not used, but the capitalization rules are followed.

1.6.10 Register specification format

This document defines the format and function of Serial Bus-specific CSRs. Registers may be read only, write only, or both readable and writable. The same distinctions may apply to any field within a register. A CSR specification includes the format (the sizes and names of bit field locations), the initial value of the register, the value returned when the register is read, and the effect(s) when the register is written. An example register is illustrated in figure 1-6.

| definition     |                  |     |      |     |     |
|----------------|------------------|-----|------|-----|-----|
| unit_dependent | vendor_dependent | sig | resv | why | not |
| 12             | 16               | 1   | 1    | 1   | 1   |
| initial value  |                  |     |      |     |     |
| unit_dependent | zeros            | 1   | 0    | 0   | 0   |
| read value     |                  |     |      |     |     |
| last write     | last update      | w   | 0    | u   | u   |
| write effect   |                  |     |      |     |     |
| stored         | ignored          | s   | i    | i   | e   |

Figure 1-6 — CSR format specification (example)

The register definition lists the names of register fields. These names are descriptive, but the fields are defined in the text; their function should not be inferred solely from their names. However, the register definition fields in figure 1-6 have the meanings specified by table 1-5.

Table 1-5 — Register definition fields

| Name             | Abbreviation  | Definition                                                                                                                                                            |
|------------------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| unit dependent   | unit_depend   | The meaning of this field shall be defined by the unit architecture(s) of the node.                                                                                   |
| vendor dependent | vendor_depend | The meaning of this field shall be defined by the vendor of the node.<br>Within a unit architecture, the unit-dependent fields may be defined to be vendor dependent. |

A node's CSRs shall be initialized when power is restored (power reset), and may be initialized when a bus reset occurs or a quadlet is written to the node's RESET\_START register (command reset). If a CSR's bus reset or command reset values differ from its initial values, they shall be explicitly specified.

The read value fields in figure 1-6 have the meanings specified by table 1-6.

**Table 1-6 — Read value fields**

| Name        | Abbreviation | Definition                                                                                               |
|-------------|--------------|----------------------------------------------------------------------------------------------------------|
| last write  | w            | The value of the data field shall be the value that was previously written to the same register address. |
| last update | u            | The value of the data field shall be the last value that was updated by node hardware.                   |

The write effect fields in figure 1-6 have the meanings specified by table 1-7.

**Table 1-7 — Write effect fields**

| Name    | Abbreviation | Definition                                                                                                                                           |
|---------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| stored  | s            | The value of the written data field shall be immediately visible to reads of the same register.                                                      |
| ignored | i            | The value of the written data field shall be ignored; it shall have no effect on the state of the node.                                              |
| effect  | e            | The value of the written data field shall have an effect on the state of the node, but may not be immediately visible to reads of the same register. |

#### 1.6.11 Reserved CSR fields

Reserved fields within a CSR conform to the requirements of the conformance glossary in this standard (see 2.1). Within a CSR, a field that conforms to this standard is labeled *reserved* (sometimes abbreviated as lowercase *r* or *resv*). Reserved fields behave as specified by figure 1-7; they shall be zero and any attempt to write to them shall be ignored.

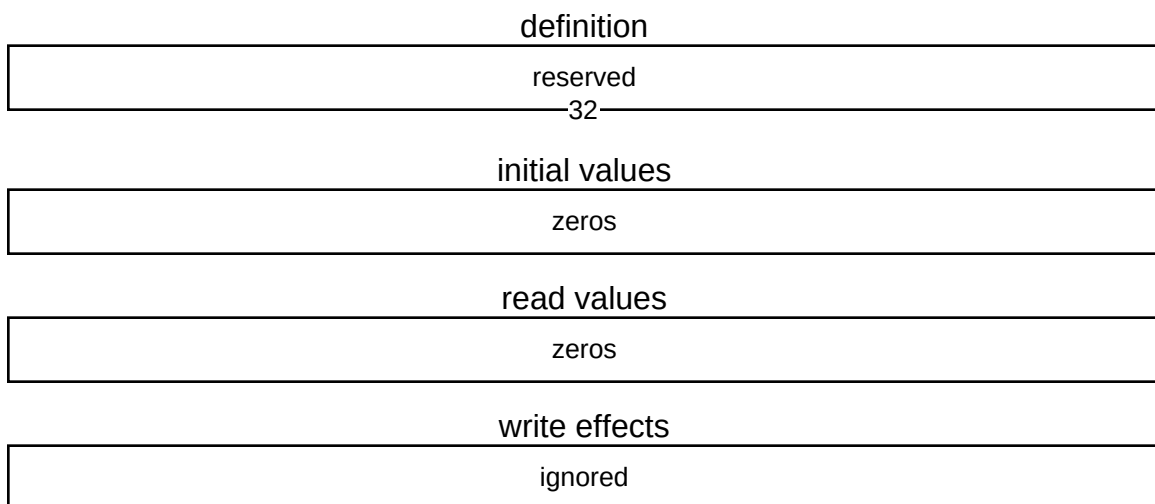


**Figure 1-7 — Reserved CSR field behavior**

This is straightforward as it applies to read and write requests. The same rules apply to lock requests, but the behaviors are less obvious; see 7.3.4.3 for details.

*Change the head for clause 2 as follows:*

## 2. Definitions and abbreviations

*Insert the following after the clause 2 title:*

For the purposes of this standard, the following definitions, terms, and notational conventions apply. The IEEE Dictionary of Electrical and Electronics Terms [B3] should be consulted for terms not defined in this clause.

*Replace 2.1 with the following:*

### 2.1 Conformance

The following keywords are used to differentiate between different levels of requirements and optionality in this standard.

**2.1.1 expected:** A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

**2.1.2 ignored:** A keyword that describes bits, bytes, quadlets, octlets, or fields whose values are not checked by the recipient.

**2.1.3 may:** A keyword that indicates flexibility of choice with no implied preference.

**2.1.4 reserved:** A keyword used to describe objects—bits, bytes, quadlets, octlets, and fields—or the code values assigned to these objects; the object or the code value is set aside for future standardization by the IEEE. A reserved object shall be zeroed by its originator or, upon development of a future IEEE standard, set to a value specified by such a standard. The recipient of a reserved object shall not check its value. The recipient of an object whose code values are defined by this standard shall check its value and reject reserved code values.

**2.1.5 shall:** A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products conforming to this standard.

**2.1.6 should:** A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “is recommended.”

*Change the head for 2.2 as follows:*

### 2.2 Technical glossary

*Replace the following in 2.2, in alphabetical order. Replace the “x” in 2.2.x with the appropriate numbers:*

**2.2.x acknowledge packet:** An 8-bit packet that may be transmitted in response to the receipt of a primary packet. The most and least significant nibbles are the one’s complement of each other. *Syn:* **acknowledge**.

**2.2.x arbitration:** The process by which nodes compete for control of the bus. Upon completion of arbitration, the winning node is able to transmit a packet or initiate a short bus reset.

**2.2.x arbitration reset gap:** The minimum period of idle bus (longer than a normal subaction gap) that separates fairness intervals.

**2.2.x asynchronous packet:** A primary packet transmitted in accordance with asynchronous arbitration rules (outside of the isochronous period).

**2.2.x base rate:** The lowest data rate used by Serial Bus in a backplane or cable environment. In multiple speed environments, all nodes are able to receive and transmit at the base rate. The base rate for the cable environment is 98.304 MHz  $\pm$  100 ppm.

**2.2.x bus manager:** The node that provides power management, sets the gap count in the cable environment, and publishes the topology of the bus and the maximum speed for data transmission between any two nodes on the bus. The bus manager node may also be the isochronous resource manager node.

**2.2.x concatenated transaction:** A split transaction comprised of concatenated subactions.

**2.2.x cycle master:** The node that generates the periodic cycle start packet 8000 times a second.

**2.2.x doublet:** Two bytes, or 16 bits, of data.

**2.2.x fairness interval:** A time period delimited by arbitration reset gaps. Within a fairness interval, the total number of asynchronous packets that may be transmitted by a node is limited. Each node's limit may be explicitly established by the bus manager or it may be implicit.

**2.2.x gap:** A period of idle bus.

**2.2.x initial register space:** A 2 kilobyte portion of initial node space with a base address of FFFF F000 0000<sub>16</sub>. This address space is reserved for resources accessible immediately after a bus reset. Core registers defined by ISO/IEC 13213:1994 are located within initial register space, as are Serial Bus-dependent registers defined by this standard.

**2.2.x isochronous:** Uniform in time (i.e., having equal duration) and recurring at regular intervals.

**2.2.x isochronous gap:** For an isochronous subaction, the period of idle bus that precedes arbitration.

**2.2.x isochronous resource manager:** A node that implements the BUS\_MANAGER\_ID, BANDWIDTH\_AVAILABLE, CHANNELS\_AVAILABLE, and BROADCAST\_CHANNEL registers (some of which permit the cooperative allocation of isochronous resources). Subsequent to each bus reset, one isochronous resource manager is selected from all nodes capable of this function.

**2.2.x isochronous subaction:** Within the isochronous period, either a concatenated packet or a packet and the gap that preceded it.

**2.2.x link layer:** The Serial Bus protocol layer that provides confirmed and unconfirmed transmission or reception of primary packets.

**2.2.x listener:** An application at a node that receives a stream packet.

**2.2.x node:** A Serial Bus device that may be addressed independently of other nodes. A minimal node consists of only a physical layer (PHY) without an enabled link. If the link and other layers are present and enabled they are considered part of the node.

**2.2.x octlet:** Eight bytes, or 64 bits, of data.

**2.2.x packet:** A sequence of bits transmitted on Serial Bus and delimited by DATA\_PREFIX and DATA\_END.

**2.2.x payload:** The portion of a primary packet that contains data defined by an application.

**2.2.x PHY packet:** A 64-bit packet where the most significant 32 bits are the one's complement of the least significant 32 bits.

**2.2.x physical layer (PHY):** The Serial Bus protocol layer that translates the logical symbols used by the link layer into electrical signals on Serial Bus media. The physical layer is self-initializing. Physical layer arbitration guarantees that only one node at a time is sending data. The mechanical interface is defined as part of the physical layer. There are different physical layers for the backplane and for the cable environment.

**2.2.x port:** The part of the physical layer (PHY) that allows connection to one other node.

**2.2.x primary packet:** Any packet that is not an acknowledge or a physical layer (PHY) packet. A primary packet is an integral number of quadlets and contains a transaction code in the first quadlet.

**2.2.x quadlet:** Four bytes, or 32 bits, of data.

**2.2.x request:** A primary packet (with optional data) sent by one node's link (the requester) to another node's link (the responder).

**2.2.x response:** A primary packet (with optional data) sent in response to a request subaction.

**2.2.x self-ID packet:** A physical layer (PHY) packet transmitted by a cable PHY during the self-ID phase or in response to a PHY ping packet.

**2.2.x speed code:** The code used to indicate bit rates for Serial Bus.

**2.2.x split transaction:** A transaction where unrelated subactions may take place on the bus between its request and response subactions.

**2.2.x subaction:** A complete link layer operation: optional arbitration, packet transmission, and optional acknowledgment.

**2.2.x subaction gap:** For an asynchronous subaction, the period of idle bus that precedes arbitration.

**2.2.x talker:** An application at a node that transmits a stream packet.

**2.2.x transaction:** A request and the optional, corresponding response.

**2.2.x transaction layer:** The Serial Bus protocol layer that defines a request-response protocol for read, write, and lock operations.

**2.2.x unit architecture:** The specification document that describes the interface to, and the behaviors of, a unit implemented within a node.

***Insert the following in 2.2, in alphabetical order. Replace the “x” in 2.2.x with the appropriate numbers:***

**2.2.x acronym:** A contrived reduction of nomenclature yielding mnemonics (ACRONYM).

**2.2.x active port:** A connected, enabled port that observes bias and is capable of detecting all Serial Bus signal states and participating in the reset, tree identify, self-identify, and normal arbitration phases.

**2.2.x arbitration signaling:** A protocol for the exchange of bidirectional, unclocked signals between nodes during arbitration.

**2.2.x boundary node:** A node with two or more ports, at least one of which is active and another suspended.

**2.2.x channel:** A relationship between a group of nodes, talkers, and listeners. The group is identified by a number between 0 and 63. Channel numbers are allocated cooperatively through isochronous resource management facilities.

**2.2.x disabled port:** A port configured to neither transmit, receive, or repeat Serial Bus signals. A disabled port shall be reported as disconnected in a physical layer's (PHY's) self-ID packet(s).

**2.2.x disconnected port:** A port whose connection detect circuitry detects no peer physical layer (PHY) at the other end of a cable. It is not important whether the peer PHY is powered or the peer port is enabled.

**2.2.x initial node space:** The 256 terabytes of Serial Bus address space that is available to each node. Addresses within initial node space are 48 bits and are based at zero. The initial node space includes initial memory space, private space, initial register space, and initial units space.

NOTE—See ISO/IEC 13213:1994 for more information on address spaces.

**2.2.x initial units space:** A portion of initial node space with a base address of FFFF F000 0800<sub>16</sub>. This places initial units space adjacent to and above initial register space. The CSR's and other facilities defined by unit architectures are expected to lie within this space.

**2.2.x isochronous period:** A period that begins after a cycle start packet is sent and ends when a subaction gap is detected. During an isochronous period, only isochronous subactions may occur. An isochronous period begins, on average, every 125  $\mu$ s.

**2.2.x isolated node:** A node without active ports; the node's ports may be disabled, disconnected, or suspended in any combination.

**2.2.x kilobyte:** A quantity of data equal to  $2^{10}$  bytes, or 1024 bytes.

**2.2.x nibble:** Four bits of data.

**2.2.x null packet:** A packet in which no clocked data is transmitted on Serial Bus between DATA\_PREFIX and DATA\_END.

**2.2.x originating port:** A transmitting port on a physical layer (PHY), which has no active receiving port. The source of the transmitted packet is either the PHY's local link or the PHY itself.

**2.2.x ping:** A term used to describe the transmission of a physical layer (PHY) packet to a particular node in order to time the response packet(s) provoked.

**2.2.x repeating port:** A transmitting port on a physical layer (PHY) that is repeating a packet from the PHY's receiving port.

**2.2.x resuming port:** A previously suspended port that has observed bias or has been instructed to generate bias. In either case, the resuming port engages in a protocol with its connected peer physical layer (PHY) in order to reestablish normal operations and become active.

**2.2.x suspended domain:** One or more suspended nodes linked by suspended connection(s). Two nodes are part of the same suspended domain if there is a physical connection between them and all ports on the path are suspended. A boundary node is adjacent to one or more suspended domain(s) but not part of the suspended domain(s).

**2.2.x suspended node:** An isolated node with at least one port that is suspended.

**2.2.x suspended port:** A connected port not operational for normal Serial Bus arbitration, but otherwise capable of detecting both a physical cable disconnection and received bias.

**2.2.x suspend initiator:** An active port that transmits the TX\_SUSPEND signal and engages in a protocol with its connected peer physical layer (PHY) to suspend the connection.

**2.2.x suspend target:** An active port that observes the RX\_SUSPEND signal. A suspend target requests all of the physical layer's (PHY's) other active ports to become suspend initiators while the suspend target engages in a protocol with its connected peer PHY to suspend the connection.

**2.2.x terabyte:** A quantity of data equal to  $2^{40}$ , or 1099511627776, bytes.

**2.2.x transmitting port:** Any port transmitting clocked data or an arbitration state. A transmitting port is further characterized as either originating or repeating.

**2.2.x unit:** A component of a Serial Bus node that provides processing, memory, input/output (I/O), or some other functionality. Once the node is initialized, the unit provides a Command and Status Register (CSR) interface. A node may have multiple units, which normally operate independently of each other.

*Change the following in 2.2. Replace the “x” in 2.2.x with the appropriate numbers after alphabetization:*

**2.2.x cycle start packet:** A primary packet sent by the cycle master that indicates the start of an isochronous eye period.

**2.2.x ~~node\_ID~~ node ID:** ~~This is a unique 16-bit number, which distinguishes the node from other nodes in the system. A 16-bit number that uniquely differentiates a node from all other nodes within a group of interconnected buses. The ten most significant bits of ~~node\_ID~~ node ID are the same for all nodes on the same bus; this is, i.e., the ~~bus\_ID~~ bus ID. The six least significant bits of ~~node\_ID~~ node ID are unique for each node on the same bus; this is called the ~~physical\_ID~~ physical ID. The physical ID is assigned as a consequence of bus initialization.~~

**2.2.x ~~physical\_ID~~ physical ID:** ~~The six least significant bits of the ~~node\_ID~~ node ID. This number is unique on a particular bus and is chosen by the physical layer during initialization. On a particular bus, each node's physical ID is unique.~~

### 3. Summary description

*Insert the following subclause after 3.8:*

#### 3.9 New features of IEEE Std 1394a-2000

The changes to IEEE Std 1394-1995 contained in IEEE Std 1394a-2000 are related to each other only in that they are incremental enhancements or extension to the existing standard. This clause provides an informative description of some of these new facilities; the clause is intended as a foundation for the reader's better understanding of the normative specifications that follow.

##### 3.9.1 Connection debounce

In the cable environment, Serial Bus configures itself and assigns a unique 6-bit physical ID to each of the 63 devices that may be interconnected within a single arbitration domain. The bus initialization and configuration process is triggered by a change in connection status at any PHY port—one or more devices have been added or removed and the connection topology has changed.

IEEE Std 1394-1995 specifies that a change in detected bias voltage causes an instantaneous connection status change and commences bus initialization. Unfortunately, this idealized model fails to account for two aspects of the physical world:

- The connection process is asymmetric. When two nodes are connected, it is extraordinary for bias to be detected by both at the same time. The node that detects bias first immediately commences a bus reset but is unable to complete bus initialization until the other node detects bias and also commences a bus reset. During this interval, which may be on the order of tens of milliseconds, the first node is unable to send or receive packets. If that node is connected to others, that entire Serial Bus is unable to operate normally; and
- The connection process is not smooth. As the plug and connector scrape together, electrical contact is made and broken many times. Bus initialization requires no more than approximately 200  $\mu$ s, but the completion of the insertion proceeds at a human pace. What appears to the user as one new connection may generate a storm of connections and disconnections.

All of this occurs quickly by human standards but the disruption caused to normal bus operations is particularly serious for isochronous data.

The problem of contact scrape is fairly simple to resolve—implement a connection time-out before new connections are confirmed. Disconnections may be detected immediately. There is no need to measure the connection time-out with great precision. An  $n$ -stage counter could derive a clock tick from the PHY's 24.576 MHz clock on the order of 5 ms; an overall time-out in the vicinity of 340 ms is adequate to debounce the contact scrape.

The problem of connection asymmetry is not solved by the connection timer. The first step in its solution is to require that all arbitration line states (except BUS\_RESET) be ignored during the connection time-out interval. If BUS\_RESET is observed, skip the remaining connection time-out interval and commence a bus reset. This works well when the connection is between two IEEE Std 1394a-2000 (new) PHYs or between an isolated node with a new PHY connected to an IEEE Std 1394-1995 (old) PHY of an operational bus.

In the case where an isolated node with an old PHY is connected to a new PHY of an operational bus, the old PHY generates a storm of bus resets which are propagated by the new PHY. This may be avoided if the new PHY implements an additional “reset detect” time-out of approximately 80 ms before it responds to BUS\_RESET.

### 3.9.2 Cable arbitration enhancements

At the time IEEE Std 1394-1995 was in the final steps toward becoming a standard, a number of valuable performance enhancements had been identified. Their overall effect is to reclaim Serial Bus bandwidth used unnecessarily in arbitration and make it available for data transmission. This both increases the throughput of the bus as a whole and reduces the latency of individual transactions.

#### 3.9.2.1 Arbitrated (short) bus reset

The addition of connection debounce, described in 3.9.1, does much to reduce the time the bus is unusable during bus initialization. However, even under ideal circumstances, e.g., a bus reset initiated by software, that involve no physical connection changes, bus initialization as specified by IEEE Std 1394-1995 is still more time consuming than it needs to be. Bus initialization is composed of three phases: reset, tree identify, and self-identify. The last phase, self-identify, requires approximately 1  $\mu$ s per node or about 70  $\mu$ s worst case when there are 63 nodes. Tree identify is also quite rapid and takes less than 10  $\mu$ s. The longest phase is bus reset and it lasts about 167  $\mu$ s while the BUS\_RESET signal is propagated. The total duration of bus initialization is longer than the nominal isochronous cycle time, 125  $\mu$ s, and may disrupt two isochronous periods. This compels device designers to add additional buffer depth to preserve the smooth flow of isochronous data from the perspective of their application. If sufficient time could be trimmed from bus initialization, the necessity for larger buffers could be reduced.

The reason for the long duration of BUS\_RESET is that a transmitting node is unable to detect this arbitration line state. It is only after packet transmission is complete that the node observes the reset. Hence, BUS\_RESET must be asserted longer than the longest possible packet transmission. This guarantees the success of bus reset regardless of the bus activity in progress.

Suppose a node arbitrates for and is granted control of Serial Bus, then all the other nodes are in the receive state. If BUS\_RESET is transmitted, all the nodes will detect it. In this case, the bus reset duration can be shortened to approximately 1.3  $\mu$ s. The worst case bus initialization time is improved from roughly 250  $\mu$ s to 80  $\mu$ s for a bus fully populated by 63 devices.<sup>4</sup> Typical bus initialization times would be shorter, e.g., approximately 20  $\mu$ s for a bus with 16 devices.

The concept is simple, but requires analysis for the following particular cases:

- a) *Parent port disconnection.* A prerequisite for arbitrated (short) bus reset is the ability to arbitrate. Since there is no longer a connection to the root, the long bus reset defined by IEEE Std 1394-1995 is all that is available.
- b) *Child port disconnection.* The node requests the bus and, if granted control of the bus, initiates a short reset. If the arbitration request ultimately fails because of an arbitration state time-out, a long bus reset is initiated.
- c) *New connection (root node or a node with a parent port).* After the connection time-out, the node requests the bus and, if granted control of the bus, initiates a short reset. If the arbitration request ultimately fails because of an arbitration state time-out, a long bus reset is initiated.
- d) *New connection (isolated node).* The isolated node should defer bus reset in anticipation that the other node, after its connection time-out, successfully arbitrates and initiates a short reset. If the isolated node fails to observe BUS\_RESET within 1 s, it initiates a long bus reset.

When two buses are connected, it is extremely unlikely that timings align to produce a short bus reset. Both nodes that sense the new connection are behaving as in item c), and one likely wins arbitration before the other. When the slower node observes BUS\_RESET, it initiates a long reset. Even in the event that the slower node fails to sense the reset, the other node's bus initialization process times-out and a long bus reset results.

### 3.9.2.2 Ack-accelerated arbitration

The timing strategy for asynchronous arbitration specified by IEEE Std 1394-1995 is straightforward—arbitration cannot start until the bus is idle for a subaction gap time. For a bus with few hops between nodes, the subaction gap might be little more than 1  $\mu$ s, while for the worst case topology, it could be slightly in excess of 13  $\mu$ s. This design was adopted when simplicity, proof of concept, and time to market were of greater importance to Serial Bus than the extraction of the last possible bit of bandwidth. However, the penalty of wasted bus idle time becomes increasingly onerous as transmission rates and the number of connected nodes increase.

The duration of a subaction gap is determined by bus topology; it is necessary for it to be greater than the worst case round-trip propagation time between any two nodes on the bus. This ensures that, after the transmission of an asynchronous primary packet, no node starts arbitration before the acknowledge packet has been transmitted and received. Unfortunately this makes no distinction between acknowledge packets and primary packets—an acknowledge packet never follows another acknowledge packet. Arbitration can start immediately after an acknowledge packet is observed.

NOTE—In a sense this is not a new form of arbitration but exactly the form of arbitration used for isochronous packets. Since there are no acknowledge packets during the isochronous period, isochronous arbitration starts as soon as an idle gap is detected after a packet.

<sup>4</sup>The calculation is based on the assumption that worst case PHY repeater delay and cable delay together are less than 500 ns. This would permit up to 100 m of cable.

### 3.9.2.3 Fly-by concatenation

IEEE Std 1394-1995 defines one arbitration enhancement—concatenated subactions. This is a method of completing a split transaction without relinquishing the bus in between the acknowledge packet and the response packet. From the standpoint of the link that receives both the acknowledge packet and the response packet, it is impossible to distinguish between concatenated subactions and closely spaced subactions separated by an intervening arbitration. This provides an opportunity to reclaim more Serial Bus bandwidth for data transmission.

Suppose a node has a packet ready for transmission when an unrelated packet addressed to the same node is received and acknowledged. Are there any consequences if the node concatenated the packet awaiting transmission to the acknowledge packet? This sequence of received packet, acknowledge packet, and transmitted packet is indistinguishable from the concatenated subactions permitted by IEEE Std 1394-1995, except for the content of the transmitted packet. Provided that fair arbitration is observed and some timing and topology issues are considered, Serial Bus operates as before.

One consideration is that fly-by concatenation may be used only when the candidate packet is received on a child port or is originated by the node's link. When a packet is received on a parent port it is likely that other nodes are simultaneously receiving the packet. If more than one node attempted fly-by concatenation, their transmitted packets would collide. When a packet is originated by the node's link or received on a child port, packet reception is unique—it is not possible for any other node to receive the same packet on a child port at the same time.

When a packet is received on a child port or is originated by the node's link, there are two opportunities for fly-by concatenation

- After an acknowledge packet, an unrelated asynchronous primary packet may be concatenated, or
- After a cycle start packet or isochronous packet, an isochronous packet may be concatenated.

Fly-by concatenation is illustrated by figure 3-32. The transmitted packet appears concatenated on the repeating ports, but as a separate packet transmitted by the child port. The figure shows a two-port PHY with a child port at the left. At the outset, a packet is about to be received by the child port. Moving down figure 3-32, the succeeding snapshots of Serial Bus state for both ports of the PHY are shown. As the received packet is repeated by the other port, it is seen to emerge, first the data prefix (now signaled as TX\_DATA\_PREFIX by the repeating port), then the clocked data of the packet. The packet retransmission is nearly complete as trailing TX\_DATA\_PREFIX is signaled by the repeating port; the use of data prefix instead of data end on retransmission signals concatenation. In the last snapshots, the concatenated packet is seen to emerge from both ports of the PHY; on the original receiving port the new packet appears as a single, unconcatenated packet.

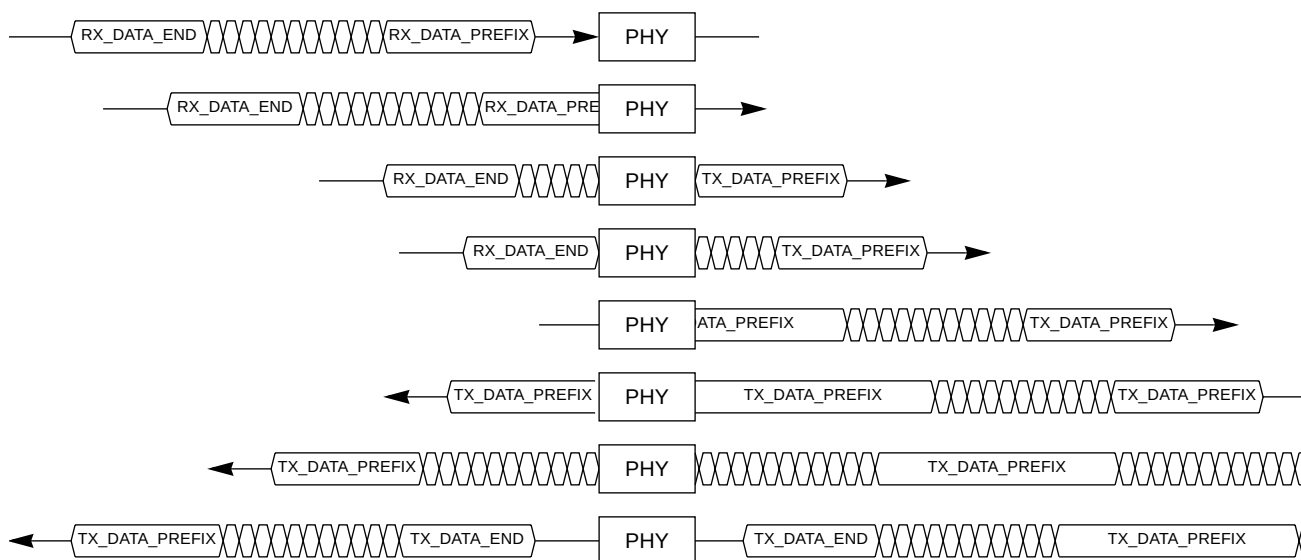


Figure 3-32 — Fly-by concatenation

### 3.9.2.4 Multi-speed-packet concatenation

IEEE Std 1394-1995 was published before 200 Mbit/s and faster PHYs were available. As a consequence, the details of operation at speeds other than S100 are sketchy and in some cases susceptible to multiple interpretations, each of which is arguably reasonable. As an example, IEEE Std 1394-1995 contains a contradictory requirement that PHYs signal speed only for the first packet of a multiple packet sequence but expect to observe a separate speed-signal for each received packet.

Apart from the interoperability problems, multi-speed-packet concatenation is an essential building block for the enhancements specified by IEEE Std 1394a-2000 because it permits the following:

- Concatenation of a read response of arbitrary speed after an acknowledge packet
- Concatenation of isochronous packets without regard to the speed of each
- Fly-by concatenation without regard to the speed of the concatenated packet

The deficiencies of IEEE Std 1394-1995, with respect to multi-speed-packet concatenation, are corrected in both the PHY/link interface specified in 4.2.1A and the PHY state machines and C language code in clause 5A. Complete interoperability with older PHYs cannot be guaranteed but is promoted by a requirement that S100 packets cannot be concatenated after faster packets.

### 3.9.2.5 Arbitration enhancements and cycle start

There are interoperability problems created by the enhancements described in 3.9.2.4 when utilized by nodes other than the cycle master (root). The problem arises when the cycle master needs to transmit a cycle start packet. Existing nodes give precedence to arbitration requests from child ports over their own requests. When none of the nodes implement arbitration enhancements, this is not a problem; a subaction gap appears at the end of any transaction in progress and the root, by virtue of its natural arbitration priority, wins arbitration and is able to send the cycle start packet. If some or all of the child nodes are employing arbitration enhancements, the root may be unable to win arbitration for a protracted period. IEEE Std 1394-1995 is designed to accommodate a delayed cycle start packet, but only up to the extent of the longest asynchronous primary packet. The delay caused by the root's children could violate isochronous timing assumptions and disrupt the flow of isochronous data.

The solution is to define new requests over the interface between the link and PHY so that the link may selectively disable and enable ack-accelerated and fly-by concatenation enhancements when a cycle start is due to be transmitted. All nodes except the cycle master are required to disable these accelerations from the time of their local cycle synchronization event until a cycle start packet is observed. Once the cycle start packet is observed, it is safe to reenable acceleration.

### 3.9.3 Performance optimization via PHY “pinging”

The simplest performance improvement that a bus manager can make is to tune the “gap count” to the topology of Serial Bus. The gap count determines the value of two fundamental time intervals—the subaction gap and the arbitration reset gap. The smaller the gap count, the less idle bus time consumed by these gaps.

IEEE Std 1394-1995 contains recommendations that permit the bus manager to reduce the gap count from the default  $3F_{16}$  in effect after bus reset. The bus manager<sup>5</sup> calculates the worst case round-trip propagation delay between any two nodes on the bus. The calculation should be based upon the greatest hop count between any two nodes (as determined from the self-ID packets) and an assumption that cable lengths do not exceed 4.5 m. Some implementations do not analyze the self-ID packets to determine the greatest hop count, but assume a maximum hop count of 16. Approximate as they are, neither the cable length nor maximum hop count assumption is reliable, since they are not normative requirements of IEEE Std 1394-1995.

<sup>5</sup>In the absence of a bus manager, the isochronous resource manager is permitted to optimize the gap count.

IEEE Std 1394a-2000 provides an alternate method for the bus manager to optimize gap count—the PHY “ping” packet. This is a packet that is addressed to any one of the 63 local nodes on a bus. In response, the addressed PHY returns a set of self-ID packets. The originator of the ping packet may time the transaction and calculate a round-trip time between itself and the targeted PHY.

With these tools, the bus manager can readily calculate the round-trip time between any two leaf nodes, as explained in more detail in annex M.

NOTE—For the purpose of calculating the round-trip time, the contents of the packet returned by the PHY are unimportant. The return of the self-ID packet(s) permit some additional diagnostic utility in the bus manager. Alternatively, the bus manager could address some other packet, such as the remote access packets defined for the suspend/resume facility, and time the packet sent in response.

### 3.9.4 Priority arbitration

A fundamental part of IEEE Std 1394-1995 is the concept of *fairness*, which ensures that all nodes on the bus are each able to arbitrate within a bounded time period; no node may starve another node’s arbitration requests. Within any particular period (called a *fairness interval*) the order in which nodes are granted the bus is arbitrary, but each node is guaranteed fair access.

This mechanism is useful to promote equal access to the bus, but individual nodes may consume bus time awaiting their chance to arbitrate. These inefficiencies can be significant, particularly in cases where there are few nodes attached to the bus.

One opportunity to improve efficiency concerns response subactions. Since each response subaction is originally triggered by a request subaction, it is arguably true that fair arbitration for requests inherently limits the number of responses. Hence the new provision of IEEE Std 1394a-2000 that responses are always permitted to use priority arbitration.

In the case where there are fewer nodes than the maximum of 63, the number of fair arbitration opportunities may be divided amongst them. For example, the system disk for a computer might be granted permission to use additional priority arbitration requests within a fairness interval. This would reduce the latency and increase the throughput for the transfer of data to and from the disk.

Finally, for reasons of simplicity, some infrequent subactions, such as the transmission of a PHY packet, are granted exemption from the normal requirements of fair arbitration.

### 3.9.5 Port disable, suspend, and resume

The cable PHY arbitration state machines in IEEE Std 1394-1995 describe the behavior of connected, fully functional ports in the four bus phases: reset, tree identify, self-identify, and normal arbitration. The only other port state is disconnected; it requires little or no description. IEEE Std 1394a-2000 defines additional port states, disabled and suspended, and the protocols for orderly transition between port states.

Each PHY port may independently be in one of the following four states:

- *Disabled*. The port generates no signals and is not capable of detecting signals. From the standpoint of a connected peer PHY, there is no observable difference between a disabled port and an unpowered PHY.
- *Disconnected*. There is no physical cable connection between the port and a peer PHY.

- *Suspended*. No bias is generated by this port but a physical connection exists with a peer PHY (which may or may not be generating bias). The absence of bias generated by this port permits a connection detect circuit to monitor the physical connection.
- *Active*. A physical connection exists with a peer PHY and bias is both generated and observed by this port. The active state is called *connected* in IEEE Std 1394-1995, but IEEE Std 1394a-2000 redefines *connected* to mean only the detection of a peer PHY, powered or unpowered, at the other end of a cable.

The preceding four states are fundamental; additional, transitional states are defined in the state diagrams in order to accurately describe PHY behavior.

An important motivation for the definition of these new states is to permit power savings in PHY implementations. In all states except active, many PHY components may be left unpowered. When all the ports of a PHY are either disabled, disconnected, or suspended, there are opportunities for substantial savings.

### 3.9.5.1 Connection detect circuit

Additional circuitry is required to detect the presence or absence of a physical connection. The circuit produces meaningful output only while the port itself is not generating bias.

### 3.9.5.2 Suspended connection

A suspended connection exists between two connected peer PHYs if the port at each end of the connection is suspended. The suspended connection is established by a protocol between the two ports, one of which is the suspend initiator and the other is the suspend target.

A port becomes a suspend initiator because of the receipt of a remote command packet that sets the port's suspend variable to one. The remote command packet may have been transmitted by the PHY's local link or by some other node. In either case, the originating PHY arbitrates for the bus; consequently the suspend initiator has ownership of the bus to transmit a remote response packet. Subsequent to the transmission of the remote response packet, the suspend initiator asserts the TX\_SUSPEND signal for a period equal to MIN\_DATA\_PREFIX.

A port becomes a suspend target when it observes RX\_SUSPEND while in the *Idle* state. In response to RX\_SUSPEND, the suspend target drives TpBias low and starts a timer.

In the meantime, the suspend initiator idles its transmitters after signaling TX\_SUSPEND for the required time. The suspend initiator then starts a timer and monitors bias. If the suspend initiator detects that bias has been removed by the suspend target, the suspend initiator in turn drives TpBias low and continues to do so for a fixed time, after which the suspend initiator enters the suspended state. If the suspend initiator's timer expires and bias is still present, the suspend initiator enters the suspended state in a faulted condition.

While the suspend target drives TpBias low it also monitors bias. If bias is removed by the suspend initiator, the handshake is complete and the suspend target enters the suspended state. Otherwise, the suspend target waits until its timer expires and then suspends even though bias is still observed.

Entry into the suspended state necessitates activation of the port's connection detect circuitry, which is usable only if the port itself does not generate bias. Each port, suspend initiator, or target delays entry into the suspended state until the output of the connection detect circuit becomes stable and indicates a physical connection.

Once a port is suspended it is capable of detecting either of the following two events:

- a) Physical disconnection
- b) The presence of bias

Physical disconnection causes the port to transition to the disconnected state. The effects of bias depend upon the fault state of the port. If the port completed the suspend initiator/target handshake normally and bias was removed, the presence of bias causes the port to resume normal operations. Otherwise, if the port entered the suspended state in a faulted condition (because bias was not removed by the connected peer PHY), the presence of bias has no effect until software clears the fault. Once the faulted condition is cleared, the port attempts to resume normal operations if bias is present.

### 3.9.5.3 Suspended domain

A suspended domain is a set of one or more suspended nodes that are physically connected through suspended nodes via suspended connections. A node without active ports and at least one suspended port is a suspended node. In order for two suspended nodes to be part of the same suspended domain, a path of suspended connections exists between them. It is possible for connected but disabled ports to split a group of physically connected suspended nodes into separate suspended domains.

A suspended domain propagates as the result of suspend target behavior. When a port becomes a suspend target (as a consequence of observing RX\_SUSPEND), it not only suspends the connection with its peer suspend initiator but also requests that all other active ports on the same PHY become suspend initiators. That is, during the same time that the suspend target observes RX\_SUSPEND, the formerly active ports transmit TX\_SUSPEND.

Unless blocked, the TX\_SUSPEND signal transmitted by a suspend initiator propagates until it reaches a leaf node. The propagation of the suspended domain may be blocked by a PHY compliant with IEEE Std 1394-1995 (but unmodified by IEEE Std 1394a-2000), a disabled port, or a suspended port. It is possible to control the extent of a suspended domain by disabling selected PHY ports prior to the activation of the suspend initiator.

NOTE—A Serial Bus configuration that includes nodes compliant with IEEE Std 1394-1995 (unmodified by IEEE Std 1394a-2000) as well as nodes capable of suspension requires careful analysis by a power manager or other application prior to the creation of a suspended domain. For example, if a remote PHY command packet is used to create a suspended domain and a legacy node lies on the path between the sender of the packet and the initiator of the suspended domain, the legacy node blocks the spread of the suspended domain from the suspend initiator toward the sender of the packet. In addition, the original sender of the packet subsequently has no means to cause the suspended domain to resume; it is unreachable because the legacy node perceives the connection to the suspended domain as disconnected.

### 3.9.5.4 Resumption

Any one of a number of events may cause a suspended port to attempt to resume normal operations

- Bias is detected and there is no fault condition.
- Except at a boundary node, another suspended (but unfaulted) port detects bias.
- A resume packet is received or transmitted by the PHY. The originator of the resume packet may be either the PHY's local link or another node.
- A remote command packet that sets the resume variable to one is addressed to the suspended port.
- At an isolated node, another disconnected (but enabled) port detects a new connection.

If a port is in the process of suspending, any of the previous events causes the port to resume after the completion of the suspend handshake.

Except for boundary nodes or the resumption of a single port by means of its resume variable, a resumption by one suspended port causes all of a PHY's other suspended ports to initiate resumption.

A suspended port initiates the resume process by generating TpBias and then waits to observe bias. Once bias is present at both ends of the cable, an active connection has been restored. Because topology changes may have occurred while connections were suspended, resumption of a connection always generates a bus reset. Heuristics are employed to minimize any proliferation of bus resets—delay a short time before initiating a bus reset, attempt to perform an arbitrated (short) bus reset if a boundary node, else delay a short while longer if not a boundary node—and in all cases defer to a detected bus reset.

### 3.9.5.5 Boundary nodes

Boundary nodes, on the border between an active Serial Bus and a suspended domain, behave differently than suspended nodes during resumption. The boundary node acts to minimize disruption of the active bus while the suspended domain resumes.

After a resume event on one of its suspended ports, a boundary node waits for three RESET\_DETECT intervals before it initiates an arbitrated (short) bus reset on the active bus. The delay is intended to permit all nodes in the suspended domain to resume before the active bus is made aware of their presence. If the boundary node experiences a resume event on more than one of its suspended ports, the delay is measured from the most recent resume event.

If a boundary node detects BUS\_RESET on any of its resumed ports during this interval, it initiates a long bus reset on the active bus. This is necessary because there is no time to arbitrate on the active bus and issue a short bus reset; bus reset is already underway on the resumed segment and must be propagated without delay.

The suspended nodes that have resumed wait seven RESET\_DETECT intervals before they initiate bus reset. This longer interval permits the entire suspended domain to resume and then allows time for the boundary node(s) to arbitrate on the active bus.

When a suspended domain that adjoins more than one boundary node is resumed, one of the boundary nodes likely arbitrates on its active bus before the other(s) and transmits BUS\_RESET into the resumed domain. When the bus reset is observed by the other boundary node(s), they respond by converting it to a long bus reset.

## 4. Cable PHY specification

### 4.2 Cable physical connection specification

#### Background

The facilities of Serial Bus, defined in IEEE Std 1394-1995, have found wide applicability in the consumer electronics industry for a new generation of digital products. For some of these product applications, the cable and 6-pin connectors specified by the standard are less than ideal:

- *Battery operated devices.* Because these devices draw no power from the cable, their design could be simplified and their cost reduced if electrical isolation were not required for the connector assembly. In addition, the cable's power conductors represent a potential source of analog noise—a significant concern for audio equipment.
- *Hand-held devices.* In contrast to the compactness of some consumer products, such as video camcorders, the cable and 6-pin connectors are relatively bulky. A more compact design is better suited to these products.

This subclause specifies alternative cables and connectors in addition to the cables and 6-pin connectors specified by IEEE Std 1394-1995. Except for the absence of power, these alternatives are intended to be interoperable with equipment that is compliant with either IEEE Std 1394-1995 or IEEE Std 1394a-2000. The remarks below apply to external (inter-crate) cabling, where extra care must be exercised for safety and EMC compliance. (Intra-crate connections are not standardized in this clause.)

Except as superseded by material in IEEE Std 1394a-2000, all subclauses in clause 4 of IEEE Std 1394-1995 apply to alternative cables and 4-pin connectors. With respect to these alternative cables and connectors only, the subclauses that follow apply. With respect to the cables with six conductors and 6-pin connectors at both ends, clause 4 of IEEE Std 1394-1995 is not affected in any way by IEEE Std 1394a-2000.

NOTE—This specification of alternative cables and connectors is intended to update and replace any and all earlier standards or draft standards that describe 4-pin variants of cable assemblies. Products in compliance with earlier standards (in particular, IEC 61883-1) may not operate at speeds faster than S100.

#### 4.2.1 Media attachment

##### 4.2.1.4 Signal propagation performance

##### 4.2.1.4.8 Shield ac coupling

#### Background

Although electrical isolation is an important system design issue for many Serial Bus devices, it is not possible to specify uniform isolation requirements for all devices. Electrical isolation is not a normative requirement of this standard so 4.2.1.4.8 should be removed from normative text.

**Delete 4.2.1.4.8 in its entirety.**

**Insert the following after 4.2.1:**

#### 4.2.1A Alternative cable media attachment specification

##### 4.2.1A.1 Connectors

In typical applications, computer, consumer electronic, or peripheral equipment boxes shall present one or more connector sockets for attachment to other boxes via cables. The detachable ends of the cable shall be terminated with connector plugs. Subclause 4.2.1 specifies connectors that have six contacts; this subclause specifies alternative connectors that have four contacts.

All dimensions, tolerances, and descriptions of features that affect the intermateability of the 4-pin shielded connector plugs and sockets are specified within this subclause. Features of connector plugs and sockets that do not affect intermateability are not specified and may vary at the option of the manufacturer. Connector features that are not directly controlled within this subclause shall be indirectly controlled by performance requirements in 4.2.1A.3 and 4.2.1A.4.

The holes and patterns (footprint) for the mounting of some of the possible versions of connectors to the printed circuit board are recommended in 4.2.1A.1.8.

##### 4.2.1A.1.1 Connector plug

The mating features of the connector plug are specified in figure 4-11A and figure 4-11B. The features assure the intermateability of the plug with the 4-pin sockets specified in 4.2.1A.1.

Figure 4-11A and figure 4-11B describe a plug intended to be used when only detent retention with the socket is required.

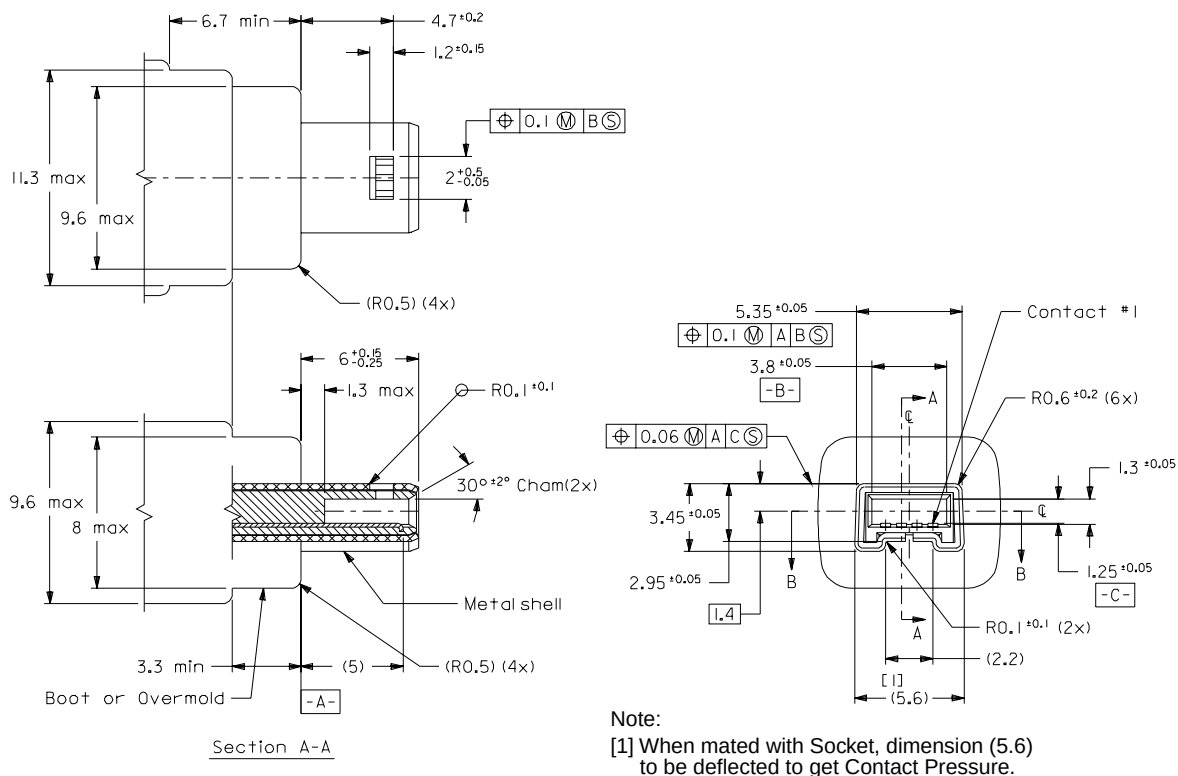
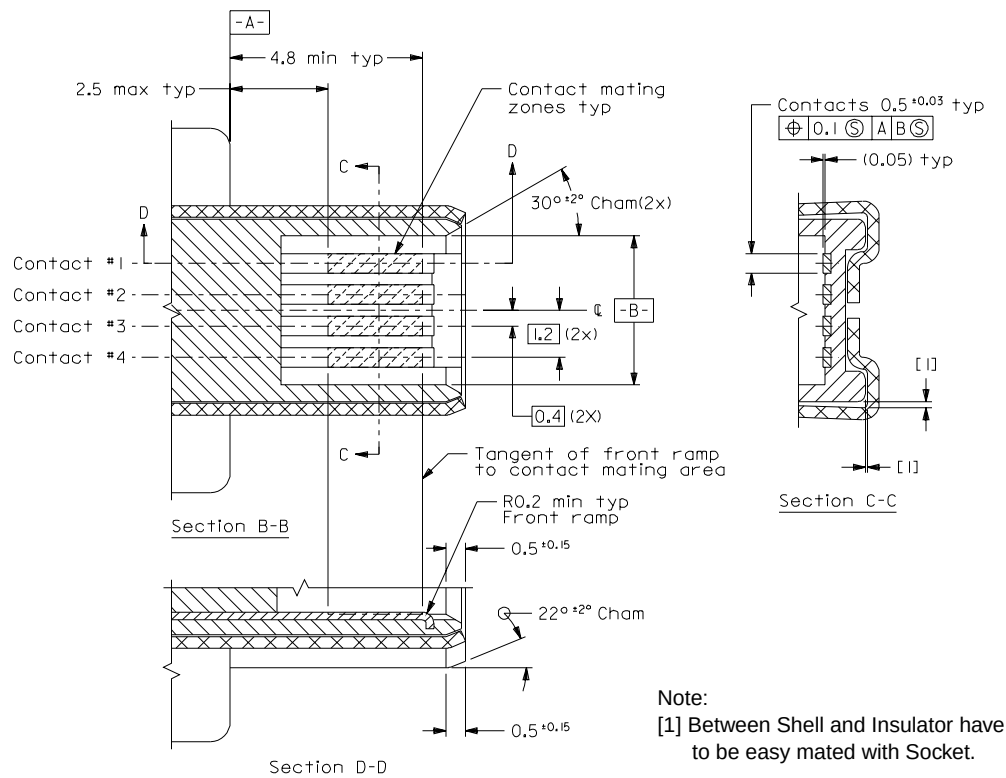


**Figure 4-11A — Plug body**



#### 4.2.1A.1.2 Connector plug terminations

The termination of the stranded wire to the plug contacts may be varied to suit the manufacturing process needs of the cable assembler.

For reference, the following methods are listed:

- Crimp
- Insulation displacement (IDC)
- Insulation piercing
- Welding and soldering

#### 4.2.1A.1.3 Connector socket

The mating features of the connector socket are described in figure 4-11C through figure 4-11E. They assure the intermateability of the socket with the 4-pin plugs specified in 4.2.1A.1.



### Table 4-11A — Connector socket signal assignment

| Contact number | Signal name | Comment                                                 |
|----------------|-------------|---------------------------------------------------------|
| 1              | TPB*        | Strobe on receive, data on transmit (differential pair) |
| 2              | TPB         |                                                         |
| 3              | TPA*        | Data on receive, strobe on transmit (differential pair) |
| 4              | TPA         |                                                         |
| Shell          | VG          | Necessary for ground reference                          |

When mounted on a printed circuit board, the socket should be at a fixed height, as illustrated by figure 4-11F.

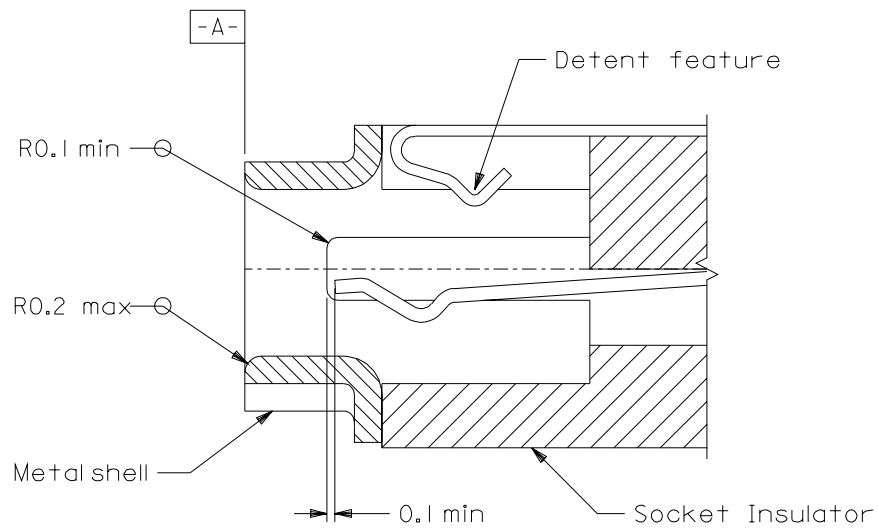


**Figure 4-11D — Socket cross-section A-A**

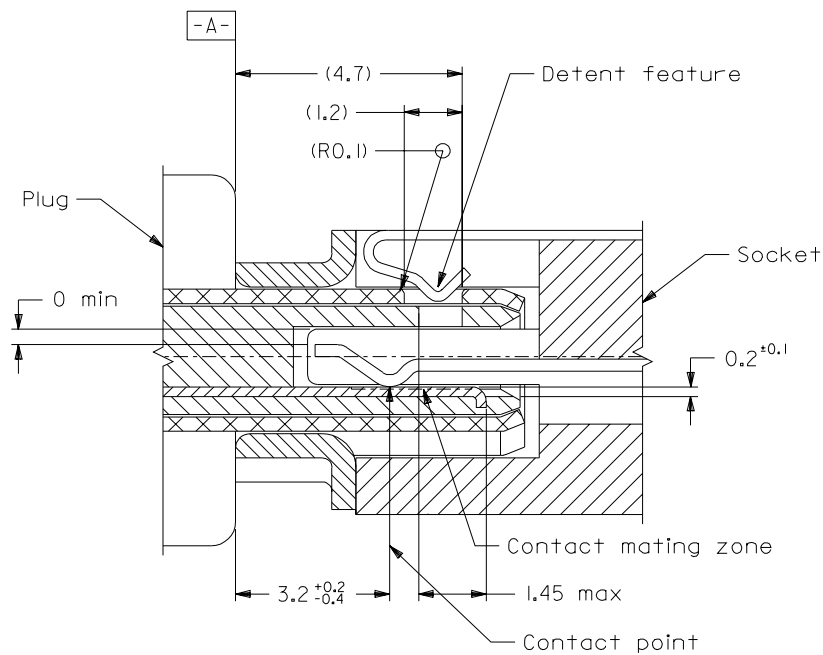


**Figure 4-11E — Cross-section of plug and socket contacts**

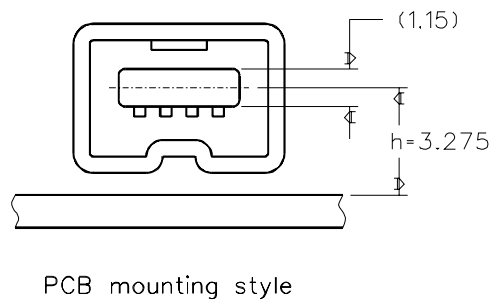


**Figure 4-11F — Socket position when mounted on a printed circuit board**

#### 4.2.1A.1.4 Contact finish on plug and socket contacts

It is necessary to standardize the electroplated finish on the contacts to assure the compatibility of plugs and sockets from different sources. The following standardized electroplatings are compatible, and one shall be used on contacts.

- a) 0.76  $\mu\text{m}$  (30  $\mu\text{in}$ ), minimum, gold, over 1.27  $\mu\text{m}$  (50  $\mu\text{in}$ ), minimum, nickel
- b) 0.05  $\mu\text{m}$  (2  $\mu\text{in}$ ), minimum, gold, over 0.76  $\mu\text{m}$  (30  $\mu\text{in}$ ), minimum, palladium, over 1.27  $\mu\text{m}$  (50  $\mu\text{in}$ ), minimum, nickel
- c) 0.05  $\mu\text{m}$  (2  $\mu\text{in}$ ), minimum, gold, over 0.76  $\mu\text{m}$  (30  $\mu\text{in}$ ), minimum, palladium-nickel alloy (80% Pd-20% Ni), over 1.27  $\mu\text{m}$  (50  $\mu\text{in}$ ), minimum, nickel

#### NOTES

1—Selective plating on contacts is acceptable. In that case, the above electroplating shall cover the complete area of contact, including the contact wipe area.

2—Either a copper or palladium strike is acceptable under the nickel electroplate.

#### 4.2.1A.1.5 Termination finish on plug and contact socket terminals

It is acceptable to use an electroplate of tin-lead with a minimum thickness of 3.04  $\mu\text{m}$  (120  $\mu\text{in}$ ) over 1.27  $\mu\text{m}$  (50  $\mu\text{in}$ ), minimum, nickel. A copper strike is acceptable under the nickel.

#### 4.2.1A.1.6 Shell finish on plugs and sockets

It is necessary to standardize the plated finish on the shells to ensure compatibility of products from different sources. Both shells shall be electroplated with a minimum of 3.03  $\mu\text{m}$  (120  $\mu\text{in}$ ) of tin or tin alloy over a suitable barrier underplate.

#### 4.2.1A.1.7 Connector durability

The requirements of different end-use applications call for connectors that can be mated and unmated a different number of times, without degrading performance beyond acceptable limits. Accordingly, this standard specifies minimum performance criteria of 1000 mating cycles.

#### 4.2.1A.1.8 Printed circuit board footprints

The dimensional specifications recommended for the footprint of a surface-mount printed circuit board socket are illustrated by figure 4-11G.

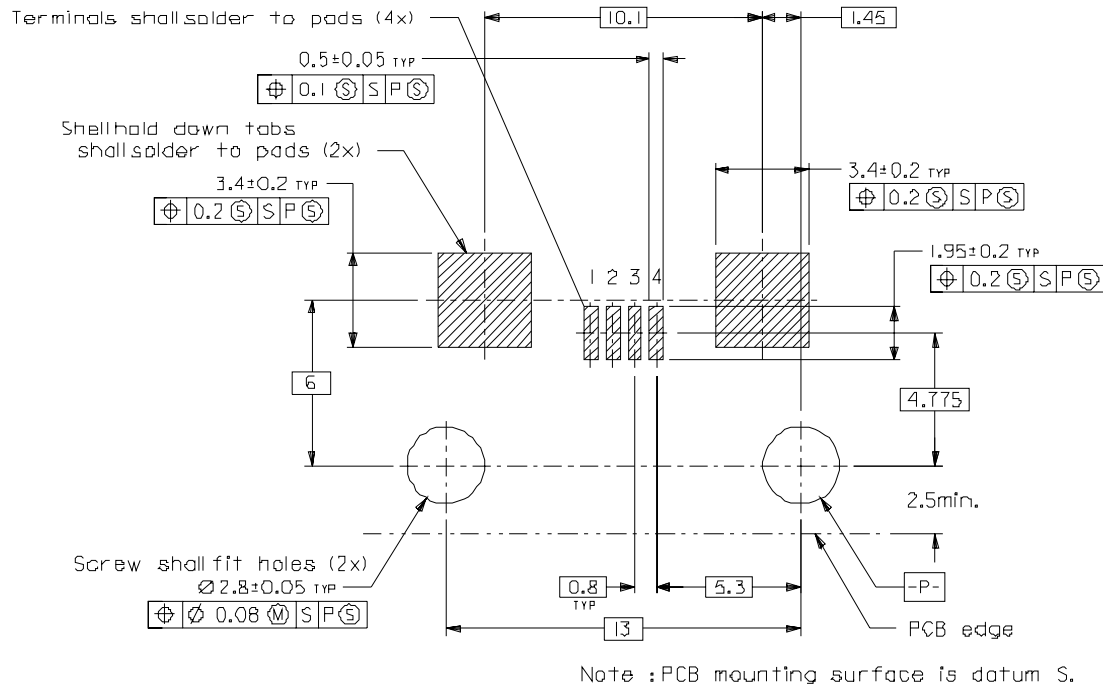


**Figure 4-11G — Flat surface-mount printed circuit board socket footprint**

The dimensional specifications recommended for the footprint of a through-hole printed circuit board socket are illustrated by figure 4-11H.

#### 4.2.1A.2 Cables

All cables and cable assemblies shall meet assembly criteria and test performance in the normative portions of this standard and should be tested in accordance with the procedures described in annex K.

##### 4.2.1A.2.1 Cable material (informative)

Linear cable material typically consists of two twisted-pair conductors. The two twisted pairs carry the balanced differential data signals. Figure 4-11I illustrates a *reference design* adequate for a 4.5 m cable. Subclause 4.2.1A.4 describes the performance requirements for the cable.

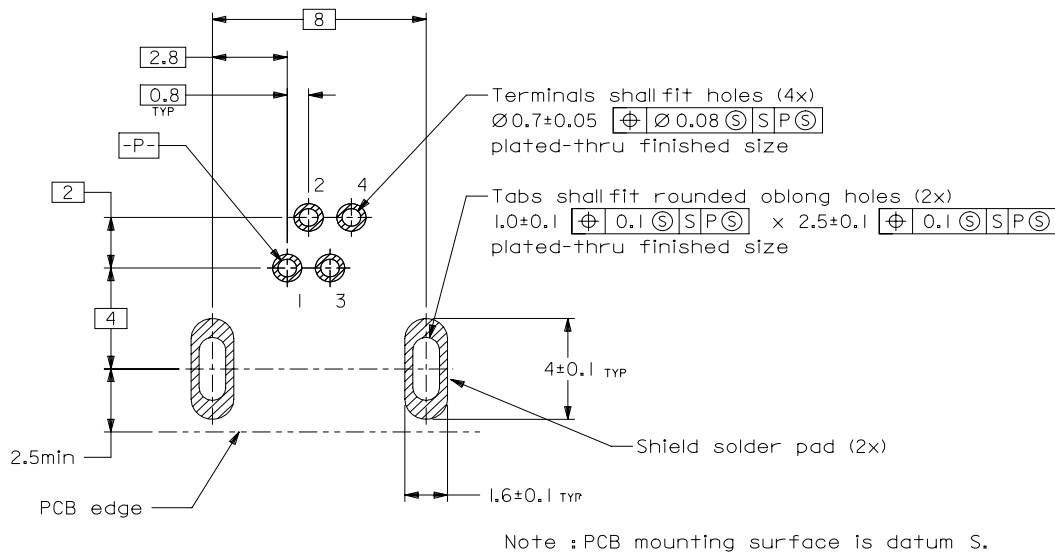
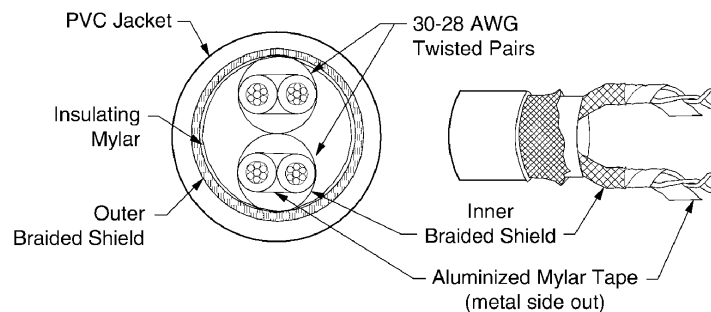


**Figure 4-11H — Flat through-hole mount printed circuit board socket footprint**



NOTE—This construction is illustrated for reference only; other constructions are acceptable as long as the performance criteria are met.

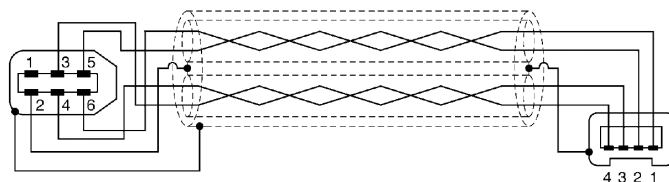
**Figure 4-11I — Cable material construction example (for reference only)**

#### 4.2.1A.2.2 Cable assemblies

Cable assemblies consist of two plug connectors, either the 6-pin connector or the 4-pin connector, joined by a length of cable material. Subclause 4.2.1A.3 describes the performance requirements for the cable assemblies.

The suggested maximum length is 4.5 m. This is to assure that a maximally configured cable environment does not exceed the length over which the end-to-end signal propagation delay would exceed the allowed time. Longer cable lengths are possible if special consideration is given to the actual Serial Bus system topology to be used, as discussed in greater detail in annex M.

Both cable configurations, 6-pin connector to 4-pin connector and 4-pin connector to 4-pin connector, are illustrated in figure 4-11J and figure 4-11K. The connector pins are terminated as shown by figure 4-11J and figure 4-11K. The two signal pairs “cross” in the cable to effect a transmit-to-receive interconnection.



Note: Connectors are viewed as looking at the front plug face.

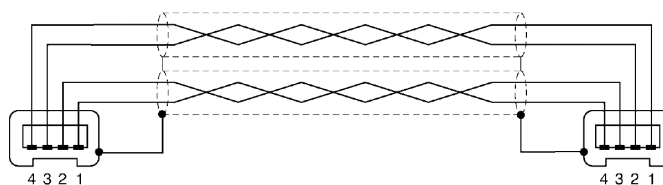
Signal Names  
for reference only

| Pin No. | Signal |
|---------|--------|
| 1       | VP     |
| 2       | VG     |
| 3       | TPB*   |
| 4       | TPB    |
| 5       | TPA*   |
| 6       | TPA    |

Signal Names  
for reference only

| Pin No. | Signal |
|---------|--------|
| 1       | TPB*   |
| 2       | TPB    |
| 3       | TPA*   |
| 4       | TPA    |
| Shell   | VG     |

Figure 4-11J — Cable assembly and schematic (6-pin to 4-pin connector)



Note: Connectors are viewed as looking at the front plug face.

Signal Names  
Both ends identical;  
for reference only

| Pin No. | Signal |
|---------|--------|
| 1       | TPB*   |
| 2       | TPB    |
| 3       | TPA*   |
| 4       | TPA    |
| Shell   | VG     |

Figure 4-11K — Cable assembly and schematic (4-pin connectors)

#### 4.2.1A.3 Connector and cable assembly performance criteria

To verify the performance requirements, performance testing is specified according to the recommendations, test sequences, and test procedures of ANSI/EIA 364-C-94; table 1 in that standard shows operating class definitions for different end-use applications. For Serial Bus, the test specifications follow the recommendations for environmental class 1.3, which is defined as “no air conditioning or humidity control with normal heating and ventilation.” The Equipment Operating Environmental Conditions shown for class 1.3 in table 2 are

- Temperature: +15 °C to +85 °C
- Humidity: 95% maximum

Class 1.3 is further described as operating in a “harsh environmental” state, but with no marine atmosphere.

Accordingly, the performance groupings, sequences within each group, and the test procedures shall follow the recommendations of ANSI/EIA 364-C-94, except where the unique requirements of the Serial Bus connector and cable assembly may call for tests which are not covered in ANSI/EIA 364-C-94, or where the requirements deviate substantially from those in that document. In those cases, test procedures of other recognized authorities or specific procedures described in the annexes are cited.

Sockets, plugs, and cable assemblies shall perform to the requirements and pass all the following tests in the groups and sequences shown.

Testing may be done as follows:

- a) *Plug and socket only.* In this case, for those performance groups that require it, the plugs may be assembled to the cable, to provide a cable assembly, by the connector manufacturer or by a cable assembly supplier.
- b) *Cable assembly (with a plug on each end) and socket.* In this case, a single supplier may do performance testing for both elements or a connector supplier may team up with a cable assembly supplier to do performance testing as a team.
- c) *Cable assembly only (with a plug on each end).* In this case, the cable assembly supplier should use a plug connector source that has successfully passed performance testing, according to this standard.
- d) *Plug only or socket only.* In this case, the other half shall be procured from a source that has successfully passed performance testing, according to this standard. For those performance groups that require it, the plugs may be assembled to the cable, to provide a cable assembly, by the connector manufacturer or by a cable assembly supplier.

#### NOTES

1—All performance testing is to be done with cable material that conforms to this standard. In order to test to these performance groups, ANSI/EIA 364-C-94 requires that the test results specify the cable construction used.

2—All resistance values shown in the performance groups in 4.2.1A.3.1 through 4.2.1A.3.7 are for connectors only, including their terminations to the wire and/or PC board, but excluding the resistance of the wire. Resistance measurements shall be performed in an environment of temperature, pressure, and humidity specified by ANSI/EIA 364-C-94.

3—The number of units to be tested is a recommended minimum; the actual sample size is to be determined by requirements of users. This is not a qualification program.

#### **4.2.1A.3.1 Performance group A: Basic mechanical dimensional conformance and electrical functionality when subjected to mechanical shock and vibration**

Number of samples

- [2] Sockets, not assembled to printed circuit board used for Phase 1, A1, and A2 (one each)
- [2] Sockets, assembled to printed circuit board
- [2] Plugs, not assembled to cable used for Phase 1, A1, and A2 (one each)
- [2] Cable assemblies with a plug assembled to one end, 25.4 cm long

See table 4-11B for testing of performance group A.

**Table 4-11A — Performance group A**

| Phase | Test                               |                     |                                        | Measurements to be performed |                                       | Requirements                                                                              |
|-------|------------------------------------|---------------------|----------------------------------------|------------------------------|---------------------------------------|-------------------------------------------------------------------------------------------|
|       | Title                              | ID No.              | Severity or conditions                 | Title                        | ID No.                                | Performance Level                                                                         |
| A1    | Visual and dimensional inspection  | ANSI/EIA 364-18A-84 | Unmated connectors                     | Dimensional inspection       | Per figure 4-11A through figure 4-11E | No defects that would impair normal operations. No deviation from dimensional tolerances. |
| A2    | Plating thickness measurement      | —                   | —                                      | —                            | —                                     | Record thickness; see 4.2.1A.1.4                                                          |
| A3    | None                               | —                   | —                                      | Low-level contact resistance | ANSI/EIA 364-23A-85                   | 50 mΩ maximum initial per mated pair.                                                     |
| A4    | Vibration                          | ANSI/EIA 364-28C-97 | Condition II (See following paragraph) | Continuity                   | ANSI/EIA 364-46A-98                   | No discontinuity at 1 μs or longer. (Each contact)                                        |
| A5    | None                               | —                   | —                                      | Low-level contact resistance | ANSI/EIA 364-23A-85                   | 30 mΩ maximum change from initial per mated contact.                                      |
| A6    | Mechanical shock (specified pulse) | ANSI/EIA 364-27B-96 | Condition G (See following paragraph)  | Continuity                   | ANSI/EIA 364-46A-98                   | No discontinuity at 1 μs or longer. (Each contact)                                        |
| A7    | None                               | —                   | —                                      | Low-level contact resistance | ANSI/EIA 364-23A-85                   | 30 mΩ maximum change from initial per mated contact.                                      |

Connectors are to be mounted on a fixture that simulates typical usage. The socket shall be mounted to a panel that is permanently affixed to the fixture. The mounting means shall include typical accessories such as

- a) An insulating member to prevent grounding of the shell to the panel.
- b) A printed circuit board in accordance with the pattern shown in figure 4-11G or figure 4-11H for the socket being tested. The printed circuit board shall also be permanently affixed to the fixture.

The plug shall be mated with the socket and the other end of the cable shall be permanently clamped to the fixture. Refer to figure 4-10 for details.

#### 4.2.1A.3.2 Performance group B: Low-level contact resistance when subjected to thermal shock and humidity stress

Number of samples

- [0] Sockets, not assembled to printed circuit board
- [2] Sockets, assembled to printed circuit board
- [0] Plugs, not assembled to cable
- [2] Cable assemblies with a plug assembled to one end, 25.4 cm long

See table 4-11C for testing of performance group B.

**Table 4-11B — Performance group B**

| Phase | Test          |                     |                                                                                                            | Measurements to be performed |                     | Requirements                                         |
|-------|---------------|---------------------|------------------------------------------------------------------------------------------------------------|------------------------------|---------------------|------------------------------------------------------|
|       | Title         | ID No.              | Severity or conditions                                                                                     | Title                        | ID No.              | Performance level                                    |
| B1    | None          | —                   | —                                                                                                          | Low-level contact resistance | ANSI/EIA 364-23A-85 | 50 mΩ maximum initial per mated contact.             |
| B2    | Thermal shock | ANSI/EIA 364-32B-92 | Condition I<br>10 cycles<br>(mated)                                                                        | Low-level contact resistance | ANSI/EIA 364-23A-85 | 30 mΩ maximum change from initial per mated contact. |
| B3    | Humidity      | ANSI/EIA 364-31A-83 | Condition A<br>(96 hours)<br>Method III<br>(cycling)<br>nonenergized<br>Omit steps 7a<br>and 7b<br>(mated) | Low-level contact resistance | ANSI/EIA 364-23A-85 | 30 mΩ maximum change from initial per mated contact. |

#### 4.2.1A.3.3 Performance group C: Insulator integrity when subjected to thermal shock and humidity stress

Number of samples

- [2] Sockets, not assembled to printed circuit board
- [0] Sockets, assembled to printed circuit board
- [2] Plugs, not assembled to cable used for Phase 1, A1, and A2 (one)
- [0] Cable assemblies with a plug assembled to one end, 2 m long

See table 4-11D for testing of performance group C.

**Table 4-11C — Performance group C**

| Phase | Test                 |                     |                                                                              | Measurements to be performed                 |                     | Requirements                                                          |
|-------|----------------------|---------------------|------------------------------------------------------------------------------|----------------------------------------------|---------------------|-----------------------------------------------------------------------|
|       | Title                | ID No.              | Severity or conditions                                                       | Title                                        | ID No.              | Performance level                                                     |
| C1    | Withstanding voltage | ANSI/EIA 364-20A-83 | Test voltage<br>100 V dc ±<br>10 V dc<br>Method C<br>(unmated and unmounted) | Withstanding voltage                         | ANSI/EIA 364-20A-83 | No flashover.<br>No sparkover.<br>No excess leakage.<br>No breakdown. |
| C2    | Thermal shock        | ANSI/EIA 364-32B-92 | Condition I<br>10 cycles<br>(unmated)                                        | Withstanding voltage (same conditions as C1) | ANSI/EIA 364-20A-83 | No flashover.<br>No sparkover.<br>No excess leakage.<br>No breakdown. |

**Table 4-11C — Performance group C (continued)**

| Phase | Test                  |                     |                                                                           | Measurements to be performed                  |                     | Requirements                                                                |
|-------|-----------------------|---------------------|---------------------------------------------------------------------------|-----------------------------------------------|---------------------|-----------------------------------------------------------------------------|
|       | Title                 | ID No.              | Severity or conditions                                                    | Title                                         | ID No.              | Performance level                                                           |
| C3    | Insulation resistance | ANSI/EIA 364-21B-95 | Test voltage<br>100 V dc $\pm$<br>10 V dc<br>(unmated and unmounted)      | Insulation resistance                         | ANSI/EIA 364-21B-95 | 100 M $\Omega$ , minimum, between adjacent contacts and contacts and shell. |
| C4    | Humidity (cyclic)     | ANSI/EIA 364-31A-83 | Condition A (96 hours)<br>Method III nonenergized<br>Omit steps 7a and 7b | Insulation resistance (same conditions as C3) | ANSI/EIA 364-21B-95 | 100 M $\Omega$ , minimum.                                                   |

**4.2.1A.3.4 Performance group D: Contact life and durability when subjected to mechanical cycling and corrosive gas exposure**

Number of samples

- [0] Sockets, not assembled to printed circuit board
- [4] Sockets, assembled to printed circuit board
- [0] Plugs, not assembled to cable used for Phase 1, A1, and A2 (one)
- [4] Cable assemblies with a plug assembled to one end, 25.4 cm long

See table 4-11E for testing of performance group D.

**Table 4-11D — Performance group D**

| Phase | Test                       |                     |                                                                                                                                              | Measurements to be performed              |                     | Requirements                                                                                        |
|-------|----------------------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|---------------------|-----------------------------------------------------------------------------------------------------|
|       | Title                      | ID No.              | Severity or conditions                                                                                                                       | Title                                     | ID No.              | Performance level                                                                                   |
| D1    | None                       | —                   | —                                                                                                                                            | Low-level contact resistance              | ANSI/EIA 364-23A-85 | 50 m $\Omega$ maximum initial per mated contact.                                                    |
| D2    | Continuity-housing (shell) | —                   | See figure 4-11L for measurement points                                                                                                      | Contact resistance, braid to socket shell | ANSI/EIA 364-06A-83 | 50 m $\Omega$ , maximum, initial from braid to socket shell at 100 mA, 5 V dc open circuit maximum. |
| D3    | Durability                 | ANSI/EIA 364-09B-91 | Class II Exposures:<br>(a) 2 mated pairs, 5 cycles<br>(b) 2 mated pairs, automatic cycling to 500 cycles, rate 500 cycles/h $\pm$ 50 cycles. | —                                         | —                   | —                                                                                                   |
| D4    | None                       |                     |                                                                                                                                              | Low-level contact resistance              | ANSI/EIA 364-23A-85 | 30 m $\Omega$ maximum change from initial per mated contact.                                        |

**Table 4-11D — Performance group D (continued)**

| Phase | Test                       |                     |                                                                                                                                         | Measurements to be performed                    |                     | Requirements                                                                                         |
|-------|----------------------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------|---------------------|------------------------------------------------------------------------------------------------------|
|       | Title                      | ID No.              | Severity or conditions                                                                                                                  | Title                                           | ID No.              | Performance level                                                                                    |
| D5    | Continuity-housing (shell) |                     | See figure 4-11L for measurement points                                                                                                 | Contact resistance                              | ANSI/EIA 364-06A-83 | 50 mΩ maximum change from initial from braid to socket shell at 100 mA, 5 V dc open circuit maximum. |
| D6    | Mixed flowing gas          | ANSI/EIA 364-65A-97 | Class II Exposures:<br>(a) 2 mated pairs; unmated for 1 day<br>(b) 2 mated pairs; mated 10 days                                         | Low-level contact resistance                    | ANSI/EIA 364-23A-85 | 30 mΩ maximum change from initial per mated contact.                                                 |
| D7    | Durability                 | ANSI/EIA 364-09B-91 | Class II Exposures:<br>(a) 2 mated pairs, 5 cycles<br>(b) 2 mated pairs, automatic cycling to 500 cycles, rate 500 cycles/h ± 50 cycles | —                                               | —                   | —                                                                                                    |
| D8    | Mixed flowing gas          | ANSI/EIA 364-65A-97 | Class II Exposures:<br>Expose mated for 10 days                                                                                         | Low-level contact resistance at end of exposure | ANSI/EIA 364-23A-85 | 30 mΩ maximum change from initial per mated contact.                                                 |
| D9    | Continuity-housing (shell) |                     | See figure 4-11L for measurement points                                                                                                 | Contact resistance                              | ANSI/EIA 364-06A-83 | 50 mΩ maximum change from initial from braid to socket shell at 100 mA, 5 V dc open circuit maximum. |

**4.2.1A.3.5 Performance group E: Contact resistance and unmating force when subjected to temperature life stress**

Number of samples

- [0] Sockets, not assembled to printed circuit board
- [2] Sockets, assembled to printed circuit board
- [0] Plugs, not assembled to cable used for Phase 1, A1, and A2 (one)
- [2] Cable assemblies with a plug assembled to one end, 2 m long

See table 4-11F for testing of performance group E.

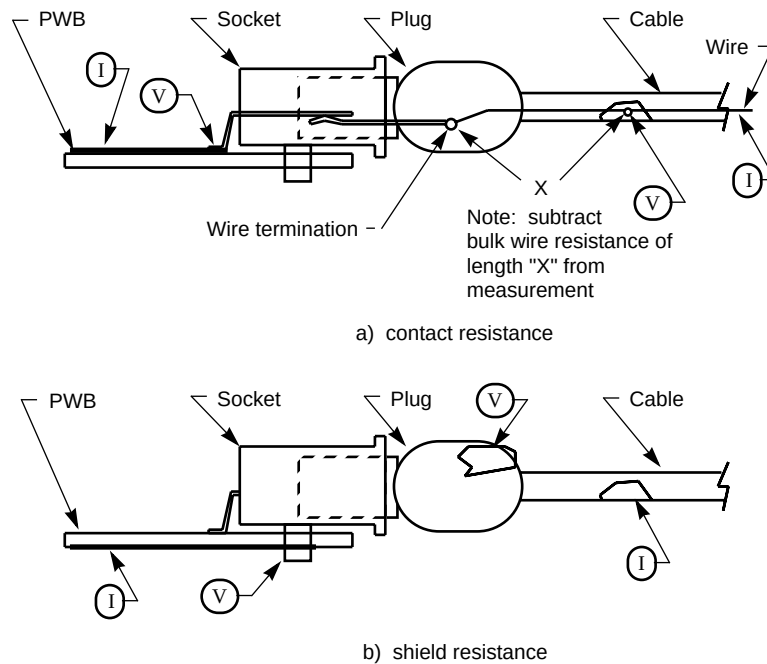


Figure 4-11L — Shield and contact resistance measuring points

Table 4-11A — Performance group E

| Phase | Test                       |                     |                                                 | Measurements to be performed |                     | Requirements                                                                             |
|-------|----------------------------|---------------------|-------------------------------------------------|------------------------------|---------------------|------------------------------------------------------------------------------------------|
|       | Title                      | ID No.              | Severity or conditions                          | Title                        | ID No.              | Performance level                                                                        |
| E1    | Mating and unmating forces | ANSI/EIA 364-13A-83 | Mount socket rigidly; insert receptacle by hand | Mating only                  | —                   | —                                                                                        |
|       |                            |                     | Auto Rate: 25 mm/min                            | Unmating only                | ANSI/EIA 364-13A-83 | Unmating force: 4.9 N minimum 39.0 N maximum                                             |
| E2    | None                       | —                   | —                                               | Low-level contact resistance | ANSI/EIA 364-23A-85 | 50 mΩ maximum initial per mated contact.                                                 |
| E3    | Continuity-housing (shell) |                     | See figure 4-11L                                | Contact resistance           | ANSI/EIA 364-06A-83 | 50 mΩ maximum initial from braid to socket shell at 100 mA, 5 V dc open circuit maximum. |
| E4    | Temperature life           | ANSI/EIA 364-17A-87 | Condition 2 (79° C) 96 hours Method A (mated)   | Low-level contact resistance | ANSI/EIA 364-23A-85 | 30 mΩ maximum change from initial per mated contact.                                     |

**Table 4-11A — Performance group E (continued)**

| Phase | Test                       |                     |                                            | Measurements to be performed |                     | Requirements                                                                                         |
|-------|----------------------------|---------------------|--------------------------------------------|------------------------------|---------------------|------------------------------------------------------------------------------------------------------|
|       | Title                      | ID No.              | Severity or conditions                     | Title                        | ID No.              | Performance level                                                                                    |
| E5    | Continuity-housing (shell) | —                   | —                                          | Contact resistance           | ANSI/EIA 364-06A-83 | 50 mΩ maximum change from initial from braid to socket shell at 100 mA, 5 V dc open circuit maximum. |
| E6    | Mating and unmating forces | ANSI/EIA 364-13A-83 | Mount socket rigidly; insert plug by hand. | Mating only                  | —                   | —                                                                                                    |
|       |                            |                     | Auto Rate: 25 mm/min                       | Unmating only                | ANSI/EIA 364-13A-83 | Unmating force: 4.9 N minimum 39.0 N maximum                                                         |

**4.2.1A.3.6 Performance group F: Mechanical retention and durability**

Number of samples

[0] Sockets, not assembled to printed circuit board

[2] Sockets, assembled to printed circuit board

[0] Plugs, not assembled to cable

[2] Plugs, assembled to cable, one end only, 25 cm long

See table 4-11G for testing of performance group F.

**Table 4-11B — Performance group F**

| Phase | Test                       |                     |                                                                | Measurements to be performed |                     | Requirements                                                             |
|-------|----------------------------|---------------------|----------------------------------------------------------------|------------------------------|---------------------|--------------------------------------------------------------------------|
|       | Title                      | ID No.              | Severity or conditions                                         | Title                        | ID No.              | Performance level                                                        |
| F1    | Mating and unmating forces | ANSI/EIA 364-13A-83 | Mount socket rigidly; insert plug by hand.                     | Mating only                  | —                   | —                                                                        |
| F2    | Mating and unmating forces | ANSI/EIA 364-13A-83 | Auto rate: 25 mm/min                                           | Unmating only                | ANSI/EIA 364-13A-83 | Unmating force: 4.9 N minimum 39.0 N maximum                             |
| F3    | Durability                 | ANSI/EIA 364-09B-91 | Automatic cycling to 1000 cycles. 500 cycles/h $\pm$ 50 cycles | Unmating only                | ANSI/EIA 364-13A-83 | Unmating force at end of durability cycles: 4.9 N minimum 39.0 N maximum |

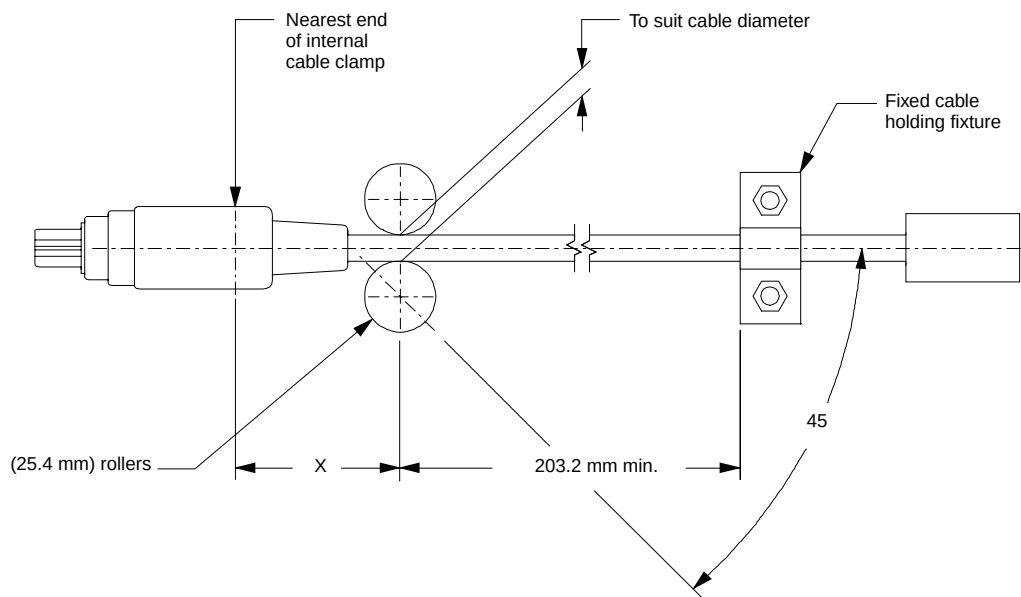
**4.2.1A.3.7 Performance group G: General tests**

Suggested procedures to test miscellaneous but important aspects of the interconnect.

Since the tests listed in table 4-11H may be destructive, separate samples must be used for each test. The number of samples to be used is listed under the test title.

**Table 4-11C — Performance group G**

| Phase | Test                                                  |                         |                                                                                                              | Measurements to be performed |                     | Requirements                                                                                                                                                                     |
|-------|-------------------------------------------------------|-------------------------|--------------------------------------------------------------------------------------------------------------|------------------------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       | Title                                                 | ID No.                  | Severity or conditions                                                                                       | Title                        | ID No.              | Performance level                                                                                                                                                                |
| G1    | Electrostatic Discharge<br><br>[1 plug]<br>[1 socket] | IEC 61000-4-2 (1999-05) | 1–8 kV in 1 kV steps. Use 8 mm ball probe. Test unmated.                                                     | Evidence of discharge        | —                   | No evidence of discharge to any of the 4 contacts; discharge to shield is acceptable.                                                                                            |
| G2    | Cable axial pull test<br><br>[2 cable assemblies]     | —                       | Fix plug housing and apply a 49.0 N load for 1 min on cable axis                                             | Continuity, visual           | ANSI/EIA 364-46A-98 | No discontinuity on contacts or shield greater than 1 $\mu$ s under load. No jacket tears or visual exposure of shield. No jacket movement greater than 1.5 mm at point of exit. |
| G3    | Cable flexing<br><br>[2 cable assemblies]             | ANSI/EIA 364-41B-89     | Condition I, dimension $X = 5.5 \times$ cable diameter; 100 cycles in each of two planes (see figure 4-11M). | (a) Withstanding voltage     | Per C1              | Per C1                                                                                                                                                                           |
|       |                                                       |                         |                                                                                                              | (b) Insulation resistance    | Per C3              | Per C3                                                                                                                                                                           |
|       |                                                       |                         |                                                                                                              | (c) Continuity               | ANSI/EIA 364-46A-98 | No discontinuity on contacts or shield greater than 1 $\mu$ s during flexing.                                                                                                    |
|       |                                                       |                         |                                                                                                              | (d) Visual                   | —                   | No jacket tears or visual exposure of shield. No jacket movement greater than 1.5 mm at point of exit.                                                                           |

**Figure 4-11M — Fixture for cable flex test**

#### 4.2.1A.4 Signal propagation performance criteria

The test procedures for all parameters listed in this clause are described in annex K.

##### 4.2.1A.4.1 Signal impedance

The differential mode characteristic impedance of the signal pairs within the cable section shall be measured by time domain reflectometry at less than 100 ps rise time; the recommended procedure is described in K.3.

$$Z_{TPA} = (110 \pm 6) \, \Omega \text{ (differential)}$$

$$Z_{TPB} = (110 \pm 6) \, \Omega \text{ (differential)}$$

The common-mode characteristic impedance of the signal pairs within the cable section shall be measured by time domain reflectometry at less than 100 ps rise time; the recommended procedure is described in K.3.

$$Z_{TPACM} = (33 \pm 6) \, \Omega \text{ (common mode)}$$

$$Z_{TPBCM} = (33 \pm 6) \, \Omega \text{ (common mode)}$$

The differential mode discrete impedance of the signal pairs within the mated connector section shall be measured by time domain reflectometry at less than 500 ps rise time; the recommended procedure is described in K.3.

$$Z_{TPACONN} = (110 \pm 25) \, \Omega \text{ (differential)}$$

$$Z_{TPBCONN} = (110 \pm 25) \, \Omega \text{ (differential)}$$

##### 4.2.1A.4.2 Signal pairs attenuation

A signal pairs attenuation requirement applies only to the two signal pairs, for any given cable assembly. Attenuation is measured using the procedure described in K.4.

| Frequency | Attenuation      |
|-----------|------------------|
| 100 MHz   | Less than 2.3 dB |
| 200 MHz   | Less than 3.2 dB |
| 400 MHz   | Less than 5.8 dB |

##### 4.2.1A.4.3 Signal pairs propagation delay

The differential propagation delay of the signal pairs through the cable shall be measured in the frequency domain; the recommended procedure is described in K.5.

$$V_{TPA} \leq 5.05 \text{ ns/m}$$

$$V_{TPB} \leq 5.05 \text{ ns/m}$$

The common-mode propagation delay of the signal pairs shall be less than or equal to the differential propagation delay. For typical cable constructions this is correct by design; consequently no test procedure is described for this in K.5.

$$V_{TPACM} \leq 5.05 \text{ ns/m}$$

$$V_{TPBCM} \leq 5.05 \text{ ns/m}$$

#### 4.2.1A.4.4 Signal pairs relative propagation skew

The difference between the differential mode propagation delay of the two signal twisted pairs shall be measured in the frequency domain; the recommended procedure is described in K.6.1.

$$S \leq 400 \text{ ps}$$

#### 4.2.1A.4.5 Crosstalk

The TPA-TPB and signal-power crosstalk shall be measured in the frequency domain using a network analyzer in the frequency range of 1–75 MHz; the recommended procedures are described in K.8.

$$X \leq -26 \text{ dB}$$

### 4.2.2 Media signal interface

#### General Background

**Cable physical layer performance enhancement specifications.** The following amendments to clause 4 specify a set of related enhancements to the physical layer of Serial Bus. When implemented as a group they can significantly increase both the efficiency and robustness of Serial Bus. The enhancements address the following:

- *Connection hysteresis (debounce).* When a connector is inserted or removed from a socket, electrical contact is made and broken countless times in a short interval. The existing standard does not take this into account and, as a consequence, a storm of bus resets occurs when a connection is made or broken. These resets are highly disruptive to isochronous traffic on the bus. IEEE Std 1394a-2000 specifies a connection time-out to avoid the problem.
- *Arbitrated (short) bus reset.* The current definition of bus reset assumes that the state of the bus is not known when a reset is initiated. The minimum reset assertion time must be long enough to complete any packet transmission that may have been in progress. However, if reset is asserted after first arbitrating for the bus, the minimum reset time can be significantly reduced.
- *Multiple-speed packet concatenation.* There is a defect in IEEE Std 1394-1995 in that PHYs are required to transmit a speed-signal only for the first packet of a multiple packet sequence, yet they are expected to receive a separate speed-signal for each packet. Faced with this contradiction, different vendors have attempted sensible interpretations; the interpretations have not been uniform and this has already resulted in observed interoperability problems with PHYs from different vendors. New requirements for PHYs in IEEE Std 1394a-2000 correct the defect and promote interoperability between existing PHYs and those that conform to IEEE Std 1394a-2000.
- *Arbitration improvements.* There are two circumstances identified in which a node may arbitrate for the bus without first observing a subaction gap. One occurs when an isochronous or acknowledge packet is received from a child port—fly-by concatenation. The other occurs subsequent to the observation of an acknowledge packet—ack-accelerated arbitration.
- *Transmission delay calculation (PHY ping).* The ability to transmit a “ping” packet to a PHY and time its return permits the inclusion of cables longer than 4.5 m or PHYs with delays longer than 144 ns into Serial Bus topologies.
- *Remote PHY register read.* The ability to interrogate another PHY’s registers; the response to a remote register read may be used to time round-trip delay in the same fashion as a “ping” packet.
- *Extended speed encoding.* Although speeds in excess of S400 are not specified by IEEE Std 1394a-2000, the coding infrastructure in the PHY/link interface, PHY registers, and self-ID packets is established for future use.