

Information technology— Microprocessor systems— Futurebus+™, Profile M (Military)

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**Bus Architecture Standards Committee
of the
IEEE Computer Society**

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International Organization for Standardization
and by the
International Electrotechnical Commission
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Abstract: This International Standard provides a set of tools with which to implement a Futurebus+™ architecture. This high-performance bus-based system architecture provides a wide range of performance and cost scalability over time for multiple generations of single- and multiple-bus multiprocessor systems. This document, a companion standard to ISO/IEC 10875 : 1994 [ANSI/IEEE Std 896.1, 1994 Edition], builds on the logical layer by adding requirements for three military profiles. It is to these profiles that products will claim conformance. Other specifications that may be required in conjunction with this International Standard are [ISO/IEC Std 10857: 1994 [ANSI/IEEE Std 896.1, 1994 Edition], IEEE Std 896.2-1991, IEEE Std 896.2a-1994, IEEE Std 896.3-1993, IEEE Std 896.4-1993, IEEE P896.4a, IEEE Std 896.9-1994, IEEE Std 1101.3-1993, IEEE Std 1101.4-1993, IEEE Std 1212-1991, IEEE Std 1194.1-1991, IEEE Std P1394, IEEE Std 1301-1991, and IEEE Std 1301.1-1991.

Keywords: bus architecture, error logging, fault logging, Futurebus+, live insertion, military profiles, multiprocessor systems, node management, open architecture, Serial Bus, software debug

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In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75% of the national bodies casting a vote.

In 1995, ANSI/IEEE Std 896.5-1993, together with IEEE Std 896.5a-1994, *Errata, Corrections, and Clarifications*, was adopted by ISO/IEC JTC 1, as draft International Standard ISO/IEC DIS 14536:1995. This edition incorporates IEEE Std 896.5a-1994 into the text of ANSI/IEEE Std 896.5-1993.

Introduction

[This introduction is not a normative part of ISO/IEC 14536: 1995, but is included for information only.]

IEEE Std 896.5-1993, IEEE Standard for Futurebus+,™ Profile M (Military) culminates a several year effort to define a standard for military use of Futurebus+. It is the result of the combined efforts of a large number of people in industry and in government who felt that the military should adapt commercial standards rather than invent its own. In the adaptation process, special consideration was given to military needs in the following areas: a) harsh environments, b) real time usage, c) security, d) reliability and fault tolerance, e) testing and maintenance, f) software debugging and system integration, and g) analog/RF components. This standard intends to meet these needs.

At the time this standard was completed, the P896.5 Working Group had the following membership:

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IEEE Std 896.5-1993 was approved by the American National Standards Institute on November 24, 1993.

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1. Overview

1.1 Scope

The initial work in development of the Futurebus+™ specification was done under the auspices of the IEEE Computer Society Microprocessor Standards Committee. In 1988, both the United States Navy's Next Generation Computer Resources (NGCR) Backplane Standards Committee and the VFEA International Trade Association (VITA), a trade association of both VME64 manufacturers and users, agreed to join the IEEE in revising ISO/IEC 10857 :1994 [ANSI/IEEE Std 896.1, 1994 Edition].¹ In early 1989, the Multibus Manufacturers Group (MMG), a trade association of both Multibus I and Multibus II manufacturers and users, also agreed to join this effort.

The primary goal of all four groups (IEEE, U.S. Navy, VITA, and MMG) was to provide a new microprocessor bus standard that would be commercially viable and that would be acceptable to the two manufacturer groups and the three user communities.

This work resulted in the IEEE 896 family of standards, of which two have become International Standards. ISO/IEC 10857 :1994 defines the logical functionality of the set of signals that make up the bus. IEEE Std 896.2-1991 describes and specifies the physical layer (i.e., electrical characteristics, pinouts, connector locations, module sizes, etc.) required. It also contains the first three application environment profiles. IEEE Std 896.3-1993 describes Futurebus+ recommended practices and specifies system-level concerns when using a Futurebus+ backplane in the design of a system. IEEE Std 896.4-1993 describes conformance test requirements for Futurebus+. IEEE Std 896.9-1994 [B3]² defines extensions to the base Futurebus+ standards that are used in extremely fault-tolerant systems. This International Standard describes and specifies the physical layer required for harsh environments that require rugged, fault-tolerant, survivable systems, as in military applications. The three profiles in this International Standard describe functional requirements with pointers to existing standards that select and bind options within those standards. It is these profiles, not the component standards, to which manufacturers may claim conformance. An end user who then purchases modules complying to a given profile from a range of suppliers has a higher assurance of interoperability.

¹Information on references can be found in clause 2.

²The numbers in brackets preceded by the letter B correspond to those of the bibliography in annex E.

Three physical form factors are incorporated into the military profiles included in this International Standard at the time of publication. Additional profiles that address other aspects of the Futurebus+ computer spectrum are being developed by the working group. These will appear in companion standards. As new physical or electrical layer requirements (e.g., a different connector type or driver technology) emerge, new profiles will be developed to address the enhanced capabilities available from newer technologies; this is part of the reason for layering the Futurebus+ standards.

The scope of this International Standard has been restricted to exclude some of the higher level system requirements associated with bus-based computer systems. These are addressed in companion standards such as IEEE Std 896.3-1993, IEEE Std 896.4-1993, and IEEE Std 896.9-1994 [B3]. The software interface to common-node capabilities as shared by Futurebus+ and Serial Bus (IEEE P1394) is defined by ISO/IEC 13213 :1994. This interface provides the framework for defining processor, memory, and I/O nodes on the Futurebus+, as well as bridges to other buses (see IEEE P1014.1 [B4]).

1.2 Applicability

This interface International Standard establishes a modular open architecture for military mission critical systems that employ digital computers, processors, and other electronic modules. This International Standard provides for integration and interoperability of diverse sets of electronic and computer modules for the purpose of configuring various types of computer systems, command/control systems, communications systems and/or weapon systems. This International Standard specifies the electrical, protocol, mechanical, thermal, and input/output interfaces necessary to allow modules, developed to this International Standard, to operate together in an integrated system or subsystem. Where necessary for module interoperability, portions of cabinet or rack interfaces dealing with the mounting of modules and their thermal interfaces are also specified. This common interface International Standard allows development of cost effective, reliable, maintainable, and highly available systems and subsystems. Because the various military systems have differing requirements, multiple form factors for different “lines” of modules are specified herein.

2. Normative references

The following standards contain provisions that, through references in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below. Members of IEC and ISO maintain registers of currently valid International Standards.

IEEE Std 896.2-1991, IEEE Standard for Futurebus+™—Physical Layer and Profile Specification (ANSI).³

IEEE Std 896.2a-1994, IEEE Standard for Futurebus+™—Physical Layer and Profile Specification: Errata, Corrections, and Clarifications.

IEEE Std 896.3-1993, IEEE Recommended Practices for Futurebus+™ (ANSI).

IEEE Std 896.4-1993, IEEE Standard for Conformance Test Requirements for Futurebus+™ (ANSI).

IEEE P896.4a, Draft Standard Supplement to IEEE Standard for Conformance Test Requirements for Futurebus+™—Errata, Corrections, and Clarifications. D1.0/June 20, 1995.⁴

³IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.

⁴Authorized standards projects, indicated by a P, were not approved by the IEEE Standards Board at the time this standard went to press. They are available from the IEEE.

IEEE Std 1101.3-1993, IEEE Mechanical Standard for Conduction-Cooled and Air-Cooled 10SU Modules (ANSI).

IEEE Std 1101.4-1993, IEEE Standard for Military Modules, Format E Form Factor (ANSI).

IEEE P1101.5, Draft Standard Mechanical Interface for a Military Module, Air-Flow-Through-Cooled, Format E Form Factor, D1.2/Mar. 2, 1995.

IEEE P1101.6, Draft Standard Mechanical Interface for an Air-Flow-Through-Cooled Module, 10SU Form Factor, D1.0/Oct. 20, 1993.

IEEE P1101.8, Draft Standard for Information Technology—Mechanical Interface for Liquid-Flow-Through-Cooled Electronic Printed Wiring Assemblies, 10SU, D1.0/Oct. 1993.

IEEE P1101.9., Draft Standard for Information Technology—Mechanical Interface for Liquid-Flow-Through-Cooled Electronic Printed Wiring Assemblies, Format E (396-pin connector only), D2.0/Dec. 7, 1994.

IEEE Std 1156.1-1993, IEEE Standard for Microcomputer Environmental Specifications for Computer Modules (ANSI).

IEEE Std 1194.1-1991, IEEE Standard Electrical Characteristics of Backplane Transceiver Logic (BTL) Interface Circuits (ANSI).

IEEE Std 1212.1-1993, IEEE Standard for Communicating Among Processors and Peripherals Using Shared Memory (Direct Memory Access —DMA) (ANSI).

IEEE Std 1275-1994, IEEE Standard for Boot (Initialization Configuration) Firmware: Core Requirements and Practices (ANSI).

IEEE Std 1275.4-1995, IEEE Standard for Boot (Initialization Configuration) Firmware: Bus Supplement for IEEE 896 (Futurebus+™).

IEEE Std 1301-1991, IEEE Standard for a Metric Equipment Practice for Microcomputers—Coordination Document (ANSI).

IEEE Std 1301.1-1991, IEEE Standard for a Metric Equipment Practice for Microcomputers—Convection-Cooled with 2 nun Connectors (ANSI).

IEEE P1394, Draft Standard for a High Performance Serial Bus. D7.1/Aug. 1994.

ISO/IEC 10857: 1994 [ANSI/IEEE Std 896.1, 1994 Edition], Information technology—Microprocessor systems—Futurebus+—Logical protocol specification.⁵

ISO/IEC 13213: 1994 [ANSI/IEEE Std 1212, 1994 Edition], Information technology—Microprocessor systems—Control and Status Register (CSR) Architecture for microcomputer buses.

MIL-HNBK-217, Reliability of Electronic Equipment.⁶

NAVSEA TE000-AB-GTP-010, Parts Application and Reliability Information Manual for Navy Electronic Equipment.⁷

⁵ISO/IEC publications are available from ISO, Case Postale 56, 1 rue de Varembe, CH-1211, Genève 20, Switzerland/Suisse. ISO/IEC [ANSI/IEEE] publications are also available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.

⁶MIL and NAVSEA publications are available from the Director, U.S. Navy Publications and Printing Service, Eastern Division, 700 Robbins Avenue, Philadelphia, PA 19111, USA.

⁷See footnote 6.

3. Definitions

For the purposes of this International Standard, the following definitions apply.

3.1 Special word usage

3.1.1 shall: A keyword that indicates a mandatory requirement. Designers must implement all such mandatory requirements to comply with this International Standard.

3.1.2 should: A keyword that indicates flexibility of choice with a strongly preferred implementation. The phrase *recommended* is used interchangeably with the keyword *should*.

3.1.3 may: A keyword that indicates flexibility of choice with no implied preference.

3.2 General definitions

3.2.1 *: When appended to a signal's name, the suffix “*” (asterisk) indicates that the logic one state of the signal is such that it will override the logic zero state applied by any other module on the line.

3.2.2 ~: Negation

3.2.3 &: Logical AND

3.2.4 |: Logical OR

3.2.5 A32 module: A module whose address space is limited to a 32-bit width.

3.2.6 A64 module: A module whose address space is limited to a 64-bit width.

3.2.7 analog/RF modules: Modules whose electronics are primarily analog or radio frequency (RF) rather than digital. These modules often utilize some digital logic for control and test, and may interface to digital buses and interconnects. Analog modules often require shielding from EMI produced by digital modules.

3.2.8 auxiliary bus: A relatively low capacity narrow bus used for miscellaneous functions for which the primary bus is not suited, or for which an alternate module access is needed.

3.2.9 backplane: An electronic and/or fiber optic interconnected set of connectors used to connect modules together electrically and/or optically. (The backplane connects selected pins of the connectors, thus providing the medium for the transfer of signals needed for the operation of the bus. Note that a backplane may contain zero or more backplane buses as well as other communications and power interconnects.)

3.2.10 backplane bus: A means in a backplane to connect corresponding signals of circuit modules using a standard set of electrical, timing, and logical rules.

3.2.11 backplane interface standard: A set of specifications that define physical and electrical attributes, and some functional and protocol properties, of electronic modules for interconnection to a common backplane interface.

3.2.12 backplane slot: The backplane connections devoted to a single module.

3.2.13 box (electronic): A protective enclosure to house modules, backplane(s), I/O connector assemblies, internal cables, and other electronic, mechanical, and thermal devices. *Syn: box; cabinet; rack*

3.2.14 cabinet: A protective enclosure to house modules, backplane(s), I/O connector assemblies, internal cables, and other electronic, mechanical, and thermal devices. *Syn: box; cabinet; rack*

3.2.15 cabinet interface: The cabinet interface provides within a cabinet the standardized mechanisms for mounting modules, backplane(s), and I/O connector assemblies, and for mounting other electronic, mechanical and thermal devices. The cabinet interface provides heat exchanging facilities, with standardized capabilities for transferring heat from modules and other heat sources within the cabinet, to external heat sink(s).

3.2.16 concurrent bus operation: In dual bus systems, “concurrent bus operation capable” describes buses capable of conducting simultaneous unrelated bus transactions. “Non-concurrent bus operation capable” describes buses capable of conducting a transaction on only one bus at a time.

3.2.17 control and status register (CSR): A register, storage location, or address that is used to control buses, interconnects, and multiple processor systems.

3.2.18 CPU: Central processing unit of a computer.

3.2.19 CSR: Control and status register.

3.2.20 critical component temperature: The temperature of semiconductor components that are most susceptible to malfunction from high temperature.

3.2.21 D32 module: A module whose data space is limited to a 32-bit width.

3.2.22 D64 module: A module whose data space is limited to a 64-bit width.

3.2.23 double-sided board: A board with components on both sides.

3.2.24 EEPROM: Electrically erasable PROM. A variety of PROM whose contents can be erased by special means, so that new contents can be supplied.

3.2.25 electrical pitch: The distance between two adjacent connections to the electrical backplane.

3.2.26 FB+: Futurebus+.

3.2.27 flexcircuit: Flexible printed wiring board. A patterned arrangement of printed circuit and components utilizing flexible base materials with or without flexible cover layers.

3.2.28 folded backplane: A backplane in which the electrical bus runs the length of the backplane twice, connecting to alternating modules on each pass.

3.2.29 Futurebus+ 1 (FB+ 1): Primary Futurebus+.

3.2.30 Futurebus+ 2 (FB+ 2): Primary Futurebus+ 2.

3.2.31 functional element: A set of one or more modules that perform a particular function.

3.2.32 ISA: instruction set architecture.

3.2.33 Institute of Electrical and Electronics Engineers (IEEE): An organization that, among other functions, sponsors standards development.

3.2.34 intermateability: The capability for units of equipment to fit together mechanically but not necessarily work together electrically.

3.2.35 interoperability: The capability for units of equipment to work together to do useful functions.

3.2.36 interoperable modules: A set of modules that have the properties necessary to allow them to work together in a system to do useful functions. The necessary parameters include items such as electrical, protocol, mechanical, thermal, and I/O interfaces.

3.2.37 interworkability: The capability for units of equipment to coexist in the same system, or on the same backplane, and accomplish useful work. (However, units that are interworkable only are not required to work together to accomplish a task. They should only not interfere with one another.)

3.2.38 local interconnect: A special interconnect among a few boards. This interconnect might be used to create a multi-board functional element.

3.2.39 module: A board or board set that comprises a single physical unit. It provides mechanical mounting and protection of electronic components, thermal transfer of heat away from the components to an external heat sink, and electrical and fiber-optic connections. A module is removable and replaceable.

3.2.40 module interface: All aspects of the electrical, fiber optic, protocol, mechanical, and thermal interfaces of a module to associated modules, the backplane, I/O connections, module cage and cabinet mounting, conduction and/or convection cooling, and power and ground.

3.2.41 multi-port module: A module that has a special pin assignment to connect to multiple other modules. Examples of multi-port modules are switch modules and multi-port memory modules.

3.2.42 node: The software visible station on a bus. (Each node is allocated a set of control register addresses [including identification-ROM and reset command registers], which are initially defined in a 4 kbyte [minimum] initial node address space. Although multiple nodes may share one bus interface, each node can be reset independently [a reset of one node has no effect on any other node]. Each module consists of one or two nodes that are independently initialized and configured by operating system software.)

3.2.43 nonconcurrent bus operation: In dual bus systems “concurrent bus operation capable” describes buses capable of conducting simultaneous unrelated bus transactions. “Nonconcurrent bus operation capable” describes buses capable of conducting a transaction on only one bus at a time.

3.2.44 nonvolatile memory: Memory whose contents are retained after power has been shut off.

3.2.45 open system hardware architecture: An electronic system design that allows components, which are developed or built by multiple parties, to work together.

3.2.46 pitch: The centerline to centerline spacing of modules or boards in a card cage or on a backplane.

3.2.47 primary backplane bus: A backplane bus that provides the main communications path among a cluster of modules.

3.2.48 PROM: Programmable read-only memory. A form of nonvolatile memory that is supplied with null contents and is loaded with its contents in the laboratory or in the field. Once programmed, its contents cannot be changed.

3.2.49 rack: A protective enclosure to house modules, backplane(s), I/O connector assemblies, internal cables, and other electronic, mechanical, and thermal devices. *Syn:* **box; cabinet; rack**

3.2.50 read-only memory (ROM): A form of nonvolatile memory whose contents are generally supplied during manufacture and cannot be altered.

3.2.51 ROM: Read-only memory.

3.2.52 single-sided board: A board with components on one side only. Often single-sided boards are used with right-angle connectors.

3.2.53 stub length: Stub length is measured from the point at which the connector assembly connects to the PC board to the pad where the transceiver lead is soldered to the PC board.

3.2.54 switched network: A computer interconnect that uses switches to allow intermodule communications.

3.2.55 transient critical component temperatures: The temperature that a semiconductor critical component may reach for a short (transient) period of time.

3.2.56 unit: The subcomponent of the node that provides a processing, memory, or I/O functionality. (After the node has been initialized [typically, by generic software], the unit provides the register interface, which is accessed by I/O driver software. The units normally operate independently of each other, and do not affect the operation of the node upon which they reside. Note that one node could have multiple units [i.e., processor, memory, and SCSI controller].)

3.2.57 utility signals: A set of discrete lines in the backplane that provide communications among modules for which a bus is not adequate because of latency or other reasons.

4. Military Profile MIL-12SU

4.1 Reference specification

4.1.1 Introduction

This subclause specifies the aspects of class of board, backplane, and chassis interfaces required to guarantee interoperability at the physical and logical layers. Boards that fully conform to mandatory requirements of this subclause may claim conformance to Futurebus+/MIL-12SU. This is verbally stated as “Futurebus+, Profile MIL-12SU.” Profile MIL-12SU is defined to assure interoperability among modules at the physical and logical layers.

The MIL-12SU is a “mil spec” convection-cooled module patterned after the IEEE Std 896.2-1991 Profile A module.

Profile MIL-12SU modules may have either one or two Futurebus+ interconnects. When used, the second Futurebus+ may provide a fault tolerant dual bus configuration or allow a cluster interconnect (e.g., each as a bus among a few modules). Various requirements are placed on dual bus modules to avoid possible incompatibilities.

4.1.2 Target usage

This profile is intended for surface ship, submarine, and limited aircraft cabin usage where the environment is suitable. Because the MIL-12SU module is convection-cooled, it must be used in applications where the direct impingement of air on board components does not cause excessive condensation nor contamination of components.

Profile MIL-12SU of this International Standard is generally compatible with commercial products designed to meet IEEE Std 896.2-1991 Profile A. It is intended that most Profile A compliant modules can be plugged into a MIL-12SU system and that many MIL-12SU profile modules can be plugged into a Profile A system.

Although the module is designed with the Profile A mechanical form factor, it is not limited for use with Futurebus+ and Serial Bus only. It may have additional module interconnects, such as dual buses and switched networks, to meet military requirements. In addition, modules that comply with this International Standard may be used with other backplane fabrics.

4.1.3 Reference tables

Table 4.1 lists the main features of the Profile MIL-12SU logical layer. The table lists specifications for each feature and indicates whether it is required or optional. Table 4.2 lists the main physical features of Profile MIL-12SU in a similar manner.

Table 4.1—Military Profile—MIL-12SU logical layer requirements

Functional requirement	Standard	Mandate	Comments
Arbitration Central Distributed	ISO/IEC 10857 :1994	Required Optional	Arbitration shall not be required for slave-only modules. While support for central arbitration is required, the system does not need to have a central arbiter.
Arbitration messages Power fail All other messages	ISO/IEC 10857 :1994	Optional Optional	See 4.4.1.2.8.
Module address width 32 bits (FB+ 1) 64 bits (FB+ 1) 32 bits (FB+ 2)	ISO/IEC 10857 :1994	Required Optional Optional	In dual bus configurations, both FB+ 1 and FB+ 2 are limited to 32 bits wide . Futurebus+ 2 is 32 bits wide
Module data path width 32 bits (FB+ 1) 64 bits (FB+ 1) 32 bits (FB+ 2)	ISO/IEC 10857 :1994	Required Optional Optional	In dual bus configurations, both FB+ 1 and FB+ 2 are limited to 32 bits wide. Futurebus+ 2 is 32 bits wide
Parity	ISO/IEC 10857 :1994	Required	
Transaction types Read unlocked Write unlocked Address only unlocked Read locked Write locked Address only locked Read partial locked Write partial locked Read partial Write partial Write response Read response Write no acknowledge Read invalid Write invalid Copyback Read shared Read modified Invalidate Shared response Modified response	ISO/IEC 10857 :1994	Required Required Required Optional Optional Optional Optional Optional Optional Optional Optional Optional Optional Optional Optional Optional Optional Optional Optional Optional Optional	CSRs must be accessible while waiting for a split response Required for splits Required for splits with cache Required for splits with cache
Split transactions	ISO/IEC 10857 :1994	Optional	
Locked operation	ISO/IEC 10857 :1994	Optional	
Lock commands Mask and swap Compare and swap Fetch and add (big) Fetch and add (little)	ISO/IEC 10857 :1994	optional optional optional optional	If locks are implemented, they must be in accordance with ISO/IEC 10857 :1994

Table 4.1—Military Profile—MIL-12SU logical layer requirements (Continued)

Functional requirement	Standard	Mandate	Comments
Broadcast Masters Slaves	ISO/IEC 10857 :1994	Optional Optional	Broadcast can be done with node 63 addressing or a broadcast message mailbox
Broadcast Masters Slaves	ISO/IEC 10857 :1994	Optional Optional	
Packet mode	ISO/IEC 10857 :1994	Optional	
CSR	ISO/IEC 10857 :1994 IEEE Std 896.2-1991 ISO/IEC 13213 :1994	Required	See 4.3.3
Tag bits and tag parity	ISO/IEC 10857 :1994	Optional	
Serial Bus	IEEE P1394	Required	One Serial Bus required. Second Serial Bus optional. Backplane version.
Cache coherence	ISO/IEC 10857 :1994	Optional	
Message passing	ISO/IEC 10857 :1994	Optional	
Utility signals		Optional	
Monarch selection	IEEE Std 896.2-1991 Profile F	Optional	Required for monarch capable modules. See 4.3.6.

Table 4.2—Military Profile—MIL-12SU physical layer requirements

Functional requirement	Standard	Mandate	Comments
Board	IEEE Std 1301.1-1991	Required	Height: ~ 265 mm Depth: ~ 287.85 mm
Board pitch: 30 mm	IEEE Std 1301.1-1991	Required	
Connector type: Power: 4 · 8 blades Signal: 2 · 192 pins Keying	Future IEC 1076-4-104 [B2]	Required Required Optional	2 mm pin-pin spacing 2A max per blade Analog power on signal pins 1 A max per pin

Table 4.2—Military Profile—MIL-12SU physical layer requirements (Continued)

Functional requirement	Standard	Mandate	Comments
Module connector pinout: 32-bit bus (FB+ 1) 64-bit bus (FB+ 1) 32-bit bus (FB+ 2) Digital power Analog power User defined clock Local interconnect Other interconnects I/O		Required Optional Optional Required Optional Optional Optional Optional	FB+ 2 data lines overlay part of FB+ 1 for dual buses. Futurebus+ 2 is 32 bits wide Pins reserved Address/data pins reserved Pins reserved Pins reserved e.g., switched network templates recommended
Backplane connector pinout: 32-bit bus (FB+ 1) 64-bit bus (FB+ 1) 32-bit bus (FB+ 2) Digital power Analog power User defined clock Local interconnect Other interconnects I/O		Required Optional Optional Required Optional Optional Optional Optional	In cluster bus applications, not all slots must be bused. Pins reserved Address/data pins reserved Pins reserved Pins reserved e.g., switched network templates recommended
Front panel	IEEE Std 896.2-1991	Required	
Injector/ejector handles	IEEE Std 896.2-1991 Profile A	Required	
Shielding on front panel: EMI/RFI		Optional	
Backplane: Connector B: 32-bit bus (FB+ 1) 64-bit bus (FB+ 1) Connector X: Central arbitration lines Connector E: Analog power User-defined clock Local interconnect 32-bit bus (FB+ 2) Switch network I/O	IEEE Std 896.2-1991	Required Required Required Required Optional Optional Optional Optional	In cluster bus applications, not all slots must be bused Pins reserved
Backplane electrical: Signal impedance Z_o Signal impedance Z_o'	IEEE Std 896.2-1991	62-76 Ω 52-62 Ω	Unloaded, no connector Without connector, no modules
Signal transceivers	IEEE Std 1194.1-1991	Required	BTL signaling levels
Board loading: Stub impedance Z_{stub} Stub length L_{stub}	IEEE Std 896.2-1991	45-75 Ω 25 mm max	

Table 4.2—Military Profile—MIL-12SU physical layer requirements (Continued)

Functional requirement	Standard	Mandate	Comments
Environment performance level	IEEE Std 1156.1-1993		Designed for performance level 3. Other performance levels are optional. See 4.5.
Cooling: Convection	IEEE Std 896.2-1991	Required	
I/O			Connector E
Backplane voltages and power: 5 V 3.3 V ± V VBP +15 V −15 V +28 V −5 V		Required Required Required Required Optional Required Required Optional Optional	Current system dependent. Backplane must be wired for these, although they need not have power supplied. 5 V @ power up 2.1 V to 5 V @ power down Template provided Template provided
Module voltages and power: 5 V 3.3 V ± V VBP +15 V −15 V +28 V −5 V		Optional Optional Optional Optional Optional Optional Optional Optional Optional	Template provided Template provided
Power sequence: Power up Power down Power fail		Any sequence Any sequence Any sequence	
Live insertion: Level 0 Level 1 Level 2 Level 3	IEEE Std 896.2-1991	Optional Optional Optional Optional	
Backplane tag bits and tag parity		Required	TG[0..7] and TP for both FB+ 1 and FB+ 2
Module tag bits and tag parity		Optional	Pins reserved
Backplane utility signals		Optional	Pins reserved
Module utility signals		Optional	Pins reserved

4.1.4 Applicable standards and profile terminology

4.1.4.1 Standards referenced

The following standards are referenced for Profile MIL-12SU. Should any specific feature defined in the following standards be implemented, but not identified in this profile, the feature shall be implemented as specified in that standard.

- Future IEC 1076-4-104 [B2]
- IEEE Std 896.2-1991
- IEEE Std 896.4-1993
- IEEE Std 1156.1-1993
- IEEE Std 1194.1-1991
- IEEE Std 1212.1-1993
- IEEE Std 1275-1994
- IEEE Std 1301-1991
- IEEE Std 1301.1-1991
- ISO/IEC 10857 :1994
- ISO/IEC 13213 :1994

4.1.4.2 Profile terminology

- **Profile MIL-12SU system:** The assembly of hardware elements made up of, at a minimum, the Profile MIL-12SU compliant backplane and card cage, power supply, air mover, etc. Modules complying with other profiles generally may operate compatibly with Profile MIL-12SU systems and modules if they meet Profile MIL-12SU mechanical requirements, and if they properly implement an identity, superset, or subset of those mandated in this profile.
- **Profile MIL-12SU module:** The assembled unit, containing one or two Futurebus+ interfaces and complying with Profile MIL-12SU, which is inserted into a compatible backplane slot. Profile MIL-12SU modules may operate compatibly in systems complying with other profiles if the system meets Profile MIL-12SU mechanical requirements, if the pin usage is compatible, and if non-Profile MIL-12SU nodes properly implement a subset or superset of their transaction set when addressing Profile MIL-12SU modules, as specified in this profile.
- **Futurebus+ 1:** The Futurebus+ on connector B. Futurebus+1 may be either 32 bits or 64 bits wide. Futurebus+ 1 is limited to a 32-bit width in dual Futurebus+ configurations.
- **Futurebus+ 2:** In dual Futurebus+ configurations, the Futurebus+ on connector E. Futurebus+2 is limited to a 32-bit width.
- **Serial Bus 1:** The Serial Bus on connector B.
- **Serial Bus 2:** The Serial Bus on connector E.

4.2 Logical layer detailed specifications

The following text specifies the logical layer for modules and systems conforming to this profile. Where two Futurebus+ or two Serial Buses are used, logical layer specifications apply to both, unless specifically stated otherwise.

4.2.1 Arbitration protocol

The central arbitration protocol shall be implemented as defined in clause 4 of ISO/IEC 10857 :1994. Modules may implement up to 256 different priority levels.

The distributed arbitration protocol, if implemented, shall be implemented as defined in clause 5 of ISO/IEC 10857 :1994.

If a central arbiter is present in the system, modules shall come up in central arbitration mode. Refer to 4.2.2.4 of ISO/IEC 10857 :1994 for the method of determining whether a central arbiter is present in the system. If no central arbiter is present, modules capable of supporting distributed arbitration shall come up in distributed mode.

Arbitration shall not be required for slave-only modules.

4.2.1.1 Arbitration messages

Power fail and other arbitration messages are optional. If implemented, arbitration messages shall be in accordance with ISO/IEC 10857 :1994.

4.2.2 Parallel protocol

Clause 6 of ISO/IEC 10857 :1994 specifies the Futurebus+ parallel protocol. The protocol supports 32 bits or 64 bits of address and 32 bits, 64 bits, 128 bits, or 256 bits of data. Futurebus+ 1 shall implement 32-bit address and 32-bit data capability. It may implement optionally 64-bit address and data capability. Prohibited are 128 bits and 256 bits. In dual Futurebus+ configurations, Futurebus+ 1 is limited to a 32-bit width. Futurebus+ 2 shall be limited to 32-bit address and 32-bit data capability. Modules shall declare their supported bus widths in the module logical capability register as defined in 7.2.4.1.1 of ISO/IEC 10857 :1994. All modules shall be able to default to a single 32-bit primary bus.

Backplanes shall be bused and terminated for address and data path widths of 64 bits on Futurebus+ 1. Busing for Futurebus+ 2 is optional. However, in dual Futurebus+ configurations, Futurebus+ 1 address/data lines 32 through 63 shall be used as Futurebus+ 2 address/data lines 0 through 31.

All modules shall generate and check parity in normal operation. See ISO/IEC 10857 :1994, IEEE Std 896.2-1991, and in particular clause 3 of IEEE Std 896.3-1993 for a complete description of error registers for parity errors.

Support for split transactions is optional. Support for split transactions is necessary to support the use of bridges. If the split transactions feature is implemented, split transactions shall contain bus master ID which may be used by slaves to validate the bus master for secure applications.

Support for packet mode is optional.

4.2.2.1 Transaction types

Modules shall support transactions in accordance with table 4.1. In the event that a module is addressed by an optional transaction that it has not implemented, it shall respond with Beat Error (**BE**^{*}) and record a capability error in the PROTOCOL_ERROR bit of the ERROR_HI_CSR as specified in 3.2.2.14.1 of IEEE Std 896.2-1991.

Use of busy. Modules should minimize use of *busy*. Modules should use busy status to avoid a deadlock condition. For example, a bridge should respond with *busy* if it is being addressed, but is unable to accept new commands until it becomes bus master to issue a read response.

Broadcast or broadcast is implemented using the BC^{*} signal. BC^{*} is induced by referencing node 63 of the control and status registers (CSRs).

Modules used in systems that include bridges should expect to accept splits.

4.2.2.1.1 Lock commands and locked operations

Lock commands are optional.

The following types of modules should support the lock commands, and if necessary, the supporting write locked transaction:

- a) Modules that contain uncached memory. These modules should be capable of receiving and carrying out the lock commands.
- b) CPU modules that drive cached or uncached memory. In cached systems, the requirement to support the lock commands should only apply to CPU modules, because the lock is implemented only on the CPU module. No write locked transaction is necessary. CPU modules that support uncached memory should support the locked commands and the supporting write locked transaction.

For modules that support CSRs only (the only addressable locations are CSRs), locks may be needed if individual bits in a CSR are updated and if multiple modules may be simultaneously trying to write to the same CSR.

Modules that support only message passing need not support lock commands.

If locks are implemented, they shall be in accordance with the ISO/IEC 10857 :1994 lock commands.

Locked operations (different from lock commands) are optional. See 6.1.9 of ISO/IEC 10857 :1994 for a description of locked operations. Locked operations may result in deadlock when used across bridges, and thus are discouraged. Lock commands should be used to perform the locking function across any splitting interface, such as is likely to be implemented by bridges.

4.2.2.1.2 Partial read/write transactions

Partial transactions are optional.

Read partial transactions are not required, because the unused portion of a word can be masked out in the CPU. However, partial reads may be needed when bridging to other buses, such as VME. Some VME I/O modules may have side effects resulting from reading an entire 32 bits or 64 bits when only a 1 byte read was intended.

The following types of modules should support the write partial transaction:

- a) Modules that contain uncached memory;
- b) CPU modules that drive uncached memory. The requirement to support the write partial transaction should not apply to CPU modules driving cached memory, because the write partial is performed in the cache, not over the Futurebus+.

Modules that support CSRs only (the only addressable locations are CSRs) need not support the write partial transaction, because CSRs are read and written in quadlets.

There shall be no block partial operations. Partial operations shall only have one data beat. The bytes selected in a partial operation shall be contiguous.

4.2.3 Caching and cache coherence

Caching functions are not required. Modules designed for cache coherency on Futurebus+ 1 may operate in D32 or D64 data width. Modules may also implement cache coherency on Futurebus+ 2 (D32). Cachecoherent modules may establish a cache-coherent domain on the bus. All modules within the cache coherent domain shall fully implement the cache-coherence protocols and transaction types. Non-caching modules shall lie outside the cache-coherent domain of the system and take no part in transactions involving cachecoherence protocols. System implementers shall take responsibility for correct interoperability between the modules within and outside the cache-coherence domain. Because of the limitations of Futurebus+, D32 and D64 modules shall operate in different cache-coherent domains.

4.2.4 Message passing

Message passing is optional. When implementing message passing, modules shall, as a minimum, implement the frame level message-passing protocols according to clause 9 in ISO/IEC 10857 :1994.

4.2.5 Tag bits

Tag bits are optional on the module. **TG[0..7]** and **TP** are required in the backplane for both Futurebus+ 1 and Futurebus+ 2.

Modules are not required to implement, use, or respond to tag bits or tag parity. Although tag bit use is undefined, it may be used for vendor-specific intermodule communication.

If tag bits are used, their function may be incompatible with that of the same signals from another module that is still compliant with this profile. A module using tag bits should be able to confirm whether another module also using them does so in a compatible way.

4.2.6 Serial Bus

Use of at least one serial bus is required. The IEEE P1394 Serial Bus backplane version shall be used. A second Serial Bus may also be implemented on the pins provided. If dual Serial Buses are used, the module shall be configurable to operate on either Serial Bus 1 or Serial Bus 2. When Futurebus+ 1 is used as a cluster bus (see 4.2.8.1), either Serial Bus 1 or Serial Bus 2 may be used as a system level Serial Bus.

Operational uses for Serial Bus shall include functional element testing, fault management, logging of errors, software debug support, and low band-width communication among boards.

Software support functions managed on the Serial Bus include both intrusive functions (i.e., setting and servicing module breakpoints, loading and dumping memory contents, examining registers, stimulating fault conditions for error detection tests, etc.) and reporting out real-time non-intrusive data collected, such as history stacks.

The Serial Bus shall share CSRs with Futurebus+ (or other interconnects) as defined in alternate access unit (see A.3 in annex A).

Modules (such as analog/RF modules) that have no need to connect to Futurebus+ may connect only to the Serial Bus(es).

4.2.6.1 Power down imminent (Serial Bus)

Modules connected to the Serial Bus may be able to accept a power fail imminent transaction from the Serial Bus. If implemented, this transaction shall be in the form of a CSR write (see 4.3.3.5).

4.2.7 Utility signals

Utility signals are discrete lines used to distribute information where there is a unique requirement that cannot be satisfied by use of the Futurebus+ or the Serial Bus. Examples include low latency requirements or support for special radiation hardened hardware. The utility signals are optional. If they are implemented, they shall be implemented in accordance with this International Standard.

Refer to 4.4.2.4 for electrical specifications for utility signals.

When both Futurebus+ 1 and Futurebus+ 2 are implemented, some utility signals may also be duplicated. The utility signals are specified below.

4.2.7.1 User console interface (UCIF) master present

UCIF master present (UMP^{*}). When asserted, **UMP^{*}** shall indicate that the UCIF is operating within the backplane. When asserted, the breakpoint discretes and other debug functions within modules may operate. The **UMP^{*}** signal may be activated at any time. When present, it enables the trigger 1 “halt” function. The full software development unit is available upon activation (as described in A.1 in annex A) by a Serial Bus message following the activation of **UMP^{*}**.

UMP^{*} shall be an active low signal that shall be asserted only by the UCIF.

To preclude the possibility that **UMP^{*}** could be falsely asserted (e.g., by noise), a transaction or message on the Serial Bus is required, in addition to the assertion of **UMP^{*}**, to enable breakpoint discretes and other debug functions within the module.

UMP^{*} is not duplicated when Futurebus+ 2 is implemented.

4.2.7.2 Trigger 1

Trigger 1 (TR1^{*}). This discrete is a trigger signal that may be programmed to be driven by any module(s). Each module can monitor this trigger. The action that a module takes upon receipt of this signal is also programmed via the Futurebus+ or the Serial Bus (see A.1 and A.3 in annex A). Typical functions accomplished with a trace trigger are stopping or starting a collection of processors in a precisely time synchronized fashion, and relating events in different modules by triggering the trace stack resources. As a minimum, if trigger 1 is implemented, it shall be able to perform a stop function.

In the presence of the **UMP^{*}** signal and provided that the software development unit has not been activated as described in A.1 in annex A, the activation of trigger 1 shall be interpreted as a processor HALT command for any module incorporating a processor.

TR1^{*} signals shall be active low for a minimum of 50 ns.

TR1^{*} is not duplicated when Futurebus+ 2 is implemented.

4.2.7.3 Trigger 2

Trigger 2 (TR2^{*}). This discrete is a trigger signal that may be programmed to be driven by any module(s). Each module can monitor this trigger. The action that a module takes upon receipt of this signal is also programmed via the Serial Bus. A typical function accomplished with a trace trigger is to relate events in different modules by triggering the trace stack resources.

TR2^{*} signals shall be active low for a minimum of 50 ns.

TR2^{*} is not duplicated when Futurebus+ 2 is implemented.

4.2.7.4 Nuclear event detect

Nuclear event detect (NED^{*}). The assertion of **NED^{*}** indicates that a nuclear event has occurred and that circumvention of transient radiation and its effects on electronics (TREE) should be initiated. It is intended that the circumvention be accomplished by a) draining all power supply modules, and other modules, if necessary; b) having the nuclear event detection module initiate hardened timers and set hardened CSRs for the purpose of restarting power, restarting the system hardware, restarting the system software, and distinguishing between power and input/output glitches that are associated with the nuclear event. In systems implementing **NED^{*}** shutdown, system start-up software should poll a hardened standard unit address to determine if the start-up is due to recovery from an **NED^{*}** or for other reasons. It is assumed that systems implementing **NED^{*}** will periodically checkpoint critical data to radiation

hardened memory prior to a nuclear shutdown, as there will be insufficient time for checkpointing after nuclear event has been detected and before non-radiation hardened memory is erased.

NED* shall be an active low signal that shall be asserted only by the nuclear event detection module.

All logic associated with this signal must be hardened against radiation upset.

NED* signals shall be active low for a minimum of 50 ns.

NED* is not duplicated when Futurebus+ 2 is implemented.

4.2.7.5 Power failure imminent

Power fail imminent (PFI)*. The assertion of **PFI*** indicates that input power to the power supply or to the power conditioning unit is not within acceptable ranges; and that consequently, the power supply output may fall out of regulation. Regulated power supply output voltage at rated current shall be available for at least 100 µs after the assertion of **PFI***. **PFI*** shall be released upon recovery of power supply input power, provided that **PFI** has been asserted for a minimum of 100 µs. In no case shall **PFI*** be asserted for less than 100 µs.

PFI* shall be an active low signal that may be asserted by either the power supply or the UCIF.

PFI* is not duplicated when Futurebus+ 2 is implemented.

Designs shall implement a power fail emergency method using at least one of the methods described in 4.4.1.2.8.

4.2.7.6 Run

Run (RUN)*. This discrete signal will cause the processor to go to a run state only when it transitions from a high level to a low level. Holding the run signal at a low level will not keep the processor in run mode if a stop is generated during this time. The run signal will be ignored if the UCIF master present (**UMP***) is not active. The run discrete has the same effect as a write to the continue bit in the UCIF_CONTROL register.

The run signal is used in conjunction with the **UMP*** and trigger signals to provide synchronous debug capability. The trigger discretizes can be used to halt processors on breakpoints or other events. The run discrete is used to restart processing. These signals can be wired between crates to provide debug capability in multi-crate systems.

RUN* shall be active low for a minimum of 50 ns.

RUN* is not duplicated when Futurebus+ 2 is implemented.

4.2.7.7 Power normal

Power normal (PN). This discrete is an active high signal when dc power has stabilized and stays within the voltage tolerances. The intent of power normal is to provide a means for protecting circuitry (such as EEPROMS) from being driven when the power level is not up to normal, and the results may be indeterminate. The power normal is defined as a low-level signal while dc power is coming up and until dc power has stabilized for 10 ms. At that time, the power normal signal will go to its high-level state. The power normal signal will remain at the high-level state until a voltage out of tolerance condition occurs, and that causes the power normal to go to a low level. The power normal discrete provides the Futurebus+ modules with a constant reset while power is coming up and holds a constant reset while power is going down. The reset provided by power normal may be ignored by modules. The reset is needed by some modules to hold off writes to EEPROM.

The power normal discrete is active high and is normally generated by the power supply that monitors the dc regulators and the input power.

Because the functions of power normal can be performed with an on-board power monitor, **PN** is not duplicated when Futurebus+ 2 is implemented.

4.2.7.8 Warmstart

Warmstart (WS^{*}). The warmstart condition is needed immediately at power-up to determine if built-in self-test is to be run. If warmstart is desired, **WS^{*}** will be at an active low level before the power normal (**PN**) goes active and will remain low for 100 ms after power normal (**PN**) goes active.

Warmstart shall be active low.

4.2.8 Local interconnects

4.2.8.1 Cluster bus

A cluster bus is used to interconnect a small number of modules into an independent cluster (e.g., a local memory bus among a few modules). When a cluster bus is required, either Futurebus+ 1 or Futurebus+ 2 shall perform that function. The module Futurebus+ 1 or Futurebus+ 2 interface, when used as a cluster bus, shall be identical to the Futurebus+ 1 interface used for a single Futurebus+ application.

Alternatively, another interconnect or bridges may be used to connect Futurebus+ 1 clusters.

4.2.8.2 Custom local interconnects

Custom local interconnects may be used if the interconnect need cannot be satisfied with Futurebus+. Custom local interconnects shall use the pins defined for local interconnects in 4.4.6.2.2.1. Custom local interconnects should be accomplished by using movable flexcircuit, a movable secondary backplane, or wire-wrap, rather than customizing the main backplane. This allows the modules requiring the custom interconnect to be moved from slot to slot.

4.2.9 Input/output

Input/output modules may couple with other modules (typically CPU modules) using either a message-passing paradigm or a shared-memory paradigm. If a shared-memory paradigm is followed, the interface to the I/O module through Futurebus+ shall be as specified by a standard unit as defined by ISO/IEC 13213 :1994, if one is available. Clause A.4 in annex A contains standard units developed as part of this International Standard. Commercial standard units should be used if available. If a message-passing paradigm is used, I/O modules shall receive requests/data from other modules, and pass requests/data to other modules using the Futurebus+ standard message-passing feature. Pin usage for I/O shall conform to 4.4.6.2.2.2.

4.2.10 User-defined clock

The clock lines (CLK1 and CLK2) reserve pins for a user-defined clock. Use of a clock is optional, but if one is used, it shall utilize the pins specified in figure .

4.3 Bus and node management

4.3.1 Addressing

Modules may implement either 32-bit or 64-bit (single Futurebus+ only) addressing. Those that implement 32-bit addressing shall never assert **AW^{*}**. They access CSRs via the top 256 Mbyte of their 4 Gbyte address space. Those that implement 64-bit addressing shall release **AW^{*}** when addressing the lower 3.75 Gbyte of memory or CSR space.

When a 32-bit equivalent of a 64-bit address exists, a module shall use the 32-bit address. This restriction allows interoperability of A32 and A64 modules.

4.3.2 Byte-lane mapping

Modules shall implement the “little addressian” byte labeling convention specified in 3.1.1.4 of IEEE Std 896.2-1991.

4.3.3 CSRs

The CSR address space shall be allocated as shown in table 4.3.

Table 4.3—CSR address space

Area name	Register offset address range
CSR core registers	0–508
Futurebus+ reserved CSRs	512–1020
ROM entries	1024–2044
Initial unit space	2048–4092

CSRs are defined by ISO/IEC 13213 :1994, ISO/IEC 10857 :1994, and IEEE Std 896.2-1991. These standards specify a set of optional registers, fields, and bits. It is intended that each Futurebus+ profile will specify a minimum implementation subset of required registers. A complete list of the minimum required military profile register set, with field and bit assignments, is shown in tables 4.4 through 4.9. Registers, field, or bits not listed are considered optional. Actual CSR and ROM entry locations are defined by clause 3 in IEEE Std 896.2-1991.

A mandate of *required* also means that the register, field, or bit shall be readable, whatever its value. Some bits, like capability bits, are additionally required to be set to 1, meaning that the capability is required. All non-implemented bits, fields, and registers shall return zero when read.

4.3.3.1 Core CSRs

All implemented registers, optional or required, shall be in accordance with the requirements specified in clause 3 of IEEE Std 896.2-1991 and ISO/IEC 13213 :1994. Tables 4.4 and 4.5 contain the optional and all required military profile core CSRs.

Table 4.4—Military Profile core CSRs

Register name	Bit/field name	Mandate	Comments
STATE_CLEAR	Unit-specific	Optional	See note 1.
	ELOG	Optional	
	ATN	Optional	See note 2.
	OFF	Required	
	STATE	Required	
STATE_SET	Unit-specific	Optional	See note 1.
	ELOG	Optional	
	ATN	Optional	See note 2.
	OFF	Required	
	STATE	Required	
NODE_IDS	BUS_ADDRESS	Required	
	GEOGRAPHICAL_ADDRESSES	Required	
	NODE_SIDE	Required	
	PRIORITY	Optional	
RESET_START		Required	
INDIRECT_ADDRESS		Optional	See note 3.
INDIRECT_DATA		Optional	See note 3.
SPLIT_TIMEOUT	all fields	Optional	See note 4.
ARGUMENT		Optional	See note 5.
TEST_START	CAT[0]	Required	CAT[0] = Initialize category See note 6.
	TEST_STEP	Required	
TEST_STATUS	TEST_STATE	Required	
UNITS_BASE	all fields	Optional	See note 7.
UNITS_BOUND	all fields	Optional	See note 7.
MEMORY_BASE	all fields	Optional	See note 8.
MEMORY_BOUND	all fields	Optional	See note 8.

Table 4.4—Military Profile core CSRs (Continued)

Register name	Bit/field name	Mandate	Comments
INTERRUPT_TARGET		Optional	
INTERRUPT_MASK		Optional	
CLOCK_VALUE	all fields	Optional	See note 9.
CLOCK_TICK_PERIOD	all fields	Optional	See note 9.
CLOCK_STROBE_ARRIVED	all fields	Optional	See note 9.
CLOCK_STROBE	all fields	Optional	See note 9.
CLOCK_REFERENCE	all fields	Optional	See note 9.
MESSAGE_REQUEST		Optional	
MESSAGE_RESPONSE		Optional	
NOTES: 1 — May be used by single unit or shared by multiple units. If shared, this field shall be used only for interrupt status reporting. 2 — Required if live insertion is implemented. 3 — Required if indirect address space is implemented or if any alternate access units are implemented. 4 — Required if split transaction capable. Modules that do not implement this register shall implement a fixed 18–36 ms timeout. 5 — Required if CAT[1] (extended diagnostics) in the TEST_START CSR is implemented. 6 — CAT[0] indicates bit 0 of CAT field is set (CAT=0001₂). 7 — Required if the module implements any units in extended address space. 8 — Required if the module implements any bus addressable memory. 9 — Required if the module implements clock synchronization. See 3.2.2.12 of IEEE Std 896.2-1991 for details.			

Table 4.5—ERROR_LOG_BUFFER CSRs

Register name	Bit/field name	Mandate	Comments
ERROR_HI	ERROR_SUMMARY MASTER NONEXISTENT_ADDR COMMAND_PAR_ERROR DATA/ADDR_PAR_ERROR PROTOCOL_ERROR TRANSACTION_TIMEOUT SPLIT_TIMEOUT CAPABILITY_LINES STATUS_FIELD COMMAND_FIELD	Required Required Required—Master Required Required Required Required—Master Required—Master Required Required Required Required	
ERROR_LO	BUSY_RETRY_THRESHOLD_EXCEEDED LENGTH_ERROR ARB_ERROR ARB_COMPARISON_OR_PARITY_ERROR ARB_TIMEOUT_ERROR NONEXISTENT_TRANSACTION_ID	Required—Master Required Optional Optional Optional Required	See note. See note. See note.
NOTE — Required for systems that use distributed arbitration and/or arbitrated messages.			

4.3.3.2 Futurebus+ specific CSRs

All implemented registers, optional or required, shall be in accordance with the requirements specified in clause 3 of IEEE Std 896.2-1991 and ISO/IEC 13213 :1994. Table 4.6 contains the bus specific CSRs required by the MIL profiles.

Table 4.6—Military Profile Futurebus+ bus specific CSRs

Register name	Bit/field name	Mandate	Comments
LOGICAL_COMMON_CONTROL	DISTRIBUTED_	Required	
	MESSAGE_ENABLE		
	SPLIT_ENABLE	Required	
LOGICAL_MODULE_CONTROL	NON_CACHE_DW	Required	See note 1.
	COMPELLED_DATA_LENGTH	Required	
	64_BIT_ADDRESS	Required	
	PARITY_REPORT_ENABLE	Required	
	MASTER_ENABLE	Required	
BUS_PROPAGATION_DELAY		Required	
COMPETITION_SETTLING_TIME		Required	See note 2.
TRANSACTION_TIMEOUT		Required	See note 3.
BUSY_RETRY_COUNTER	RETRY_THRESHOLD	Required	See note 4.
	RETRY_COUNTER	Required	
BUSY_RETRY_DELAY	RETRY_DELAY	Required	See note 5.
ERROR_RETRY_COUNTER	RETRY_THRESHOLD	Required	
	RETRY_COUNTER	Required	
ERROR_RETRY_DELAY	RETRY_DELAY	Required	
NOTES: 1 — Only data width of 32 bits allowed to Core, ROM, and Futurebus+ specific CSRs for profile MIL 12SU, 10SU and Format E. 2 — This field is optional on profile MIL 12SU modules that do not support distributed arbitration. 3 — Transaction timeout as defined in ISO/IEC 10857 :1994. There are 32 bits with a value of 233 ps per bit. Nodes shall implement at least a timeout range of 30.5 μ s to 457.7 μ s with a tolerance of $\pm 10\%$ of the value set. 4 — Nodes shall implement the full 16-bit counter for a threshold. 5 — Nodes shall implement at least a delay range of 7.6 μ s to 62.4 ms with a tolerance of $\pm 10\%$ of the value set.			

4.3.3.3 ROM entries

ROM entries are specified in clause 3 of IEEE Std 896.2-1991 and ISO/IEC 13213 :1994. The ROM entries consist of the bus info block, root directory, and optional unit directories and leafs. ROM entries start at offset 1024 of the CSR address space with the bus info block. Annex D provides an example of ROM entries for a MIL profile module.

4.3.3.3.1 BUS_INFO_BLOCK ROM entries

The bus info block contains the Futurebus+ specific ROM entries. Table 4.7 contains the bus info block ROM entries required by the MIL profiles.

Table 4.7—Military Profile ROM bus info block entries

ROM entry name	Mandate	Comments
Bus identifier	Required	The Bus Identifier is 0x30383936 (ASCII “0896”).
Profile ID	Required	2 Quadlets. The Profile ID ROM Entries are as follows: 0x4D494C2D31325355 (ASCII “MIL-12SU”) 0x4D494C2D31305355 (ASCII “MIL-10SU”) 0x4D494C2D53454D45 (ASCII “MIL-SEME”)
MODULE_LOGICAL_CAPABILITY	Required	All bits describing the module's implemented capability shall be set to 1. Non-implemented features shall have the corresponding capability bits set to 0.
NODE_CAPABILITIES_EXT	Required	All bits describing the node's implemented capability shall be set to 1. Non-implemented features shall have the corresponding capability bits set to 0. See notes 1 and 2.
COMPETITION_INTERNAL_DELAY	Required	
PACKET_SPEED	Required	All fields set to 0 if packet mode is not supported.
MESSAGE_FRAME_SIZE	Required	Set to 0 if message passing is not supported.
BUSY_RETRY_COUNTER_CAPABILITY	Required	
BUSY_RETRY_DELAY_CAPABILITY	Required	
ERROR_RETRY_COUNTER_CAPABILITY	Required	
ERROR_RETRY_DELAY_CAPABILITY	Required	
NOTES: 1 — “Live insertion” field specifies the module level of live insertion support. 2 — Profile MIL 12SU, 10SU, and Format E protocols require the module to declare its data_length capability.		

4.3.3.3.2 directory ROM entries

The root directory contains entries that describe the module and node and may provide pointers to unit directories. The order in which the entry appears in the directory, with the exception of textual descriptors, is unconstrained. Textual descriptor leaves, which contain vendor-specific information, shall immediately follow the entry that is being described. A textual descriptor may be provided for each entry in the root directory with the exception of another textual descriptor. Table 4.8 contains the optional and required root directory ROM entries.

Table 4.8—Military Profile ROM root directory entries

ROM entry name	Mandate	Comments
MODULE_VENDOR_ID	Required	IEEE assigned vendor ID#
TEXTUAL_DESCRIPTOR	Required	Offset to leaf containing vendor ID in ASCII format. Must immediately follow the MODULE_VENDOR_ID entry in ROOT_DIRECTORY. See notes 1 and 2.
MODULE_HW_VERSION	Optional	A number used in conjunction with MODULE_VENDOR_ID, to identify diagnostic software for the module.
MODULE_SPEC_ID	Optional	IEEE assigned vendor ID # of the vendor that defined the architectural interface of the module. Required if MODULE_SW_VERSION is implemented.
MODULE_SW_VERSION	Optional	A number used in conjunction with MODULE_SPEC_ID, to identify driver software for the module. Supplied by the vendor defining the architectural interface of the module. See note 3.
MODULE_DEPENDENT_INFO	Optional	An offset to a leaf containing additional information about the module. The format and meaning of this leaf shall be described by the specification of the module. See note 1.
NODE_VENDOR_ID	Optional	IEEE assigned vendor ID # of the vendor that defined the architectural interface of the node. Required if NODE_HW_VERSION is implemented.
NODE_HW_VERSION	Optional	A number used in conjunction with NODE_VENDOR_ID to identify diagnostic software for the node.
NODE_SPEC_ID	Optional	IEEE assigned vendor ID # of the vendor that defined the architectural interface of the node. Required if NODE_SW_VERSION is implemented.
NODE_SW_VERSION	Optional	A number used in conjunction with NODE_SPEC_ID, to identify driver software for the node. Supplied by the vendor defining the architectural interface of the node. See note 3.
NODE_CAPABILITIES	Required	
NODE_UNIQUE_ID	Required	Offset to leaf containing vendor assigned 64 bit binary serial #. See note 1.
NODE_UNITS_EXTENT	Optional	Required if module contains units in extended space. See note 4.
NODE_MEMORY_EXTENT	Optional	Required if module contains memory in extended space. See note 4.
NOTES: 1 — The leaf may reside in the first 1024 bytes of ROM, or in indirect address space if offset is greater than 1024 bytes. 2 — See figure 8-14 of ISO/IEC 13213 :1994 for actual ASCII textual descriptor leaf format. 3 — Either MODULE_SW_VERSION, NODE_SW_VERSION, or UNITS_SW_VERSION(s) shall be implemented. 4 — May be immediate or an offset to a CSR in initial unit space, which contains the size and alignment. See table 8-11, 12 of ISO/IEC 13213 :1994.		

4.3.3.3 Unit directory ROM entries

Unit directories shall be implemented when the module contains more than one unit. The unit directory may be implemented if only one unit is contained on the module. One unit directory is required for each unit on the module. MODULE_SW_VERSION and NODE_SW_VERSION entries shall not be implemented when a unit directory or

directories are implemented. All required fields shall be implemented when the unit directory is implemented. Table 4.9 contains the optional and required unit directory ROM entries.

Table 4.9—Military Profile ROM unit directory entries

ROM entry name	Mandate	Comments
UNIT_SPEC_ID	Required	IEEE assigned vendor ID # of vendor defining architectural interface of unit. The Navy will supply its IEEE assigned vendor ID for units defined by the Navy.
UNIT_SW_VERSION	Required	A number used in conjunction with UNIT_SPEC_ID, to identify driver software for the unit. Supplied by the vendor defining the architectural interface of the unit. See note 1.
UNIT_DEPENDENT_INFO	Optional	An offset to a leaf containing additional information about the unit. The format and meaning of this leaf shall be described by the specification of the unit. See note 2.
UNIT_LOCATION	Required	Contains an offset to a Unit_Locate leaf. See notes 3 and 4.
UNIT_POLL_MASK	Optional	Required if the unit affects one or more of the bits in the STATE_CLEAR.unit_depend field.
UNIT_DIRECTORY	Optional	Required if more than one unit is implemented.
NOTES: 1 — Either MODULE_SW_VERSION, NODE_SW_VERSION, or UNIT_SW_VERSION shall be implemented. 2 — See figure 8-20 of ISO/IEC 13213 :1994 for actual unit_locate leaf format. 3 — The leaf may reside in the first 1024 bytes of ROM, or in indirect address space if offset is greater than 1024 bytes. 4 — Immediate or an offset to a CSR that contains the size and alignment. See tables 8-11 and 8-12 of ISO/IEC 13213 :1994.		

4.3.3.4 Initial and extended units space

The initial units space (node offset 2084-4096) and the extended units space are defined by ISO/IEC 13213 :1994 and IEEE Std 896.2-1991. These spaces shall be used for the military specified unit architectures defined herein, industry standard unit architectures, and vendor defined unit architectures.

All unit architectures, if implemented, shall be in accordance with ISO/IEC 13213 :1994 and IEEE Std 1212.1-1993. Existing standard industry and military unit architectures shall be implemented where applicable. If no standard exists, the common industry practice shall be used.

4.3.3.4.1 Military specific unit architectures (shared-memory paradigm)

The military specific unit architectures are units unique to the military environment that were developed for use in the military profiles. These units were developed assuming a shared-memory paradigm.

4.3.3.4.1.1 Software development unit

A node should provide CSRs to implement several aspects of system development that involve modules after application software is installed. These functions are used throughout the system life cycle. Some functions are oriented to initial development of system software; others emphasize system verification, validation, and software maintenance. Identified functional areas are termed non-real time functions and real time functions. Real time functions are further subdivided into areas that use cooperative code to instrument functions and non-intrusive instrumentation (RTNI) of software that is invisible to on-module code. Clause A.1 in annex A defines the military-specific standard software development unit.

4.3.3.4.1.2 History units

Modules should implement the history units. Clause A.2 defines the military-specific standard history units for stress/errors, module revision, and module usage.

4.3.3.4.1.3 Federal stock number unit

The federal stock number unit shall be implemented as shown in clause A.2.

4.3.3.4.1.4 Alternate access unit

An alternate access unit shall be implemented to allow Serial Bus access to Futurebus+ CSRs to perform test maintenance functions. Clause A.3 defines the military-specific standard alternate access unit.

4.3.3.5 Serial Bus CSRs

IEEE P1394 specifies that ISO/IEC 13213 :1994 is the standard to use when implementing control and status registers. That relationship is reiterated here, and the requirements of ISO/IEC 13213 :1994 are to be used without modification, except as authorized within IEEE P1394 and/or herein.

All modules shall implement INDIRECT_ADDRESS and INDIRECT_DATA CSRs, as specified in ISO/IEC 13213 :1994, in Serial Bus CSR space in addition to those CSRs required in IEEE P1394 .

All modules may implement the power fail imminent CSRs in Serial Bus CSR space as shown in clause A.5. Designs shall implement a power fail emergency method using at least one of the methods described in 4.4.1.2.8.

4.3.3.6 Conflicting standards

Should any of the above standards conflict as to the implementation of CSRs, the precedence shall be resolved with the following priority: this standard, ISO/IEC 10857 :1994, IEEE Std 896.2-1991, IEEE P1394, and ISO/IEC 13213 :1994.

4.3.3.7 Fault tolerance extensions CSRs

4.3.3.7.1 Introduction

IEEE Std 896.9-1994 [B3] contains additional fault-detection mechanisms and CSRs to improve the fault tolerance of a Futurebus+ system. Use of the extensions in IEEE Std 896.9-1994 is optional. However, if the fault tolerance extensions are implemented, they shall be implemented as mandated in tables 4.10 through 4.22.

4.3.3.7.2 Fault-detection mechanisms

Table 4.10 lists fault-detection mechanisms specified in IEEE Std 896.9-1994 [B3] , and their mandates specified in MIL profiles.

Table 4.10—Fault-detection mechanisms

Mechanism	Mandate	Comments
Geographic address parity	Required	GAP*
Reflection	Required	RF*, use of command/status signals
Duplication	Required	TED*, SLD*, RED*
Protocol monitoring	Required	

4.3.3.7.3 FTE CSRs

Tables 4.11 through 4.22 list additional CSRs and/or bits/fields in existing CSRs that are included in the fault tolerance extensions in IEEE Std 896.9-1994 [B3] .

Table 4.11—NODE_CAPABILITIES_EXT CSR

Register name	Bit/field name	Mandate	Comments
NODE_CAPABILITIES_EXT	FTE_CAP	Required	

Table 4.12—FTE_HOLD CSR

Register name	Bit field name	Mandate	Comments
FTE_HOLD	All bits	Optional	

Table 4.13—ERROR_HI CSR

Register name	Bit field name	Mandate	Comments
ERROR_HI	ERROR_SUMMARY_INVERSE	Required	

4.3.4 Private space

The private space and the equivalent Futurebus+ address mapping is defined by ISO/IEC 13213 :1994 for vendor-dependent node-local uses.

Some nodes may need to allocate a portion of their address space for internal uses, in a way that makes the equivalent Futurebus+ address space inaccessible to these nodes. Such nodes shall allocate this internal address space in the equivalent Futurebus+ address space known as private space. These nodes are said to implement private space.

Table 4.14—ERROR_LO_CSR

Register name	Bit/field name	Mandate	Comments
ERROR_LO	TRANSACTION_ERROR	Required	See note 1.
	ARB_MESSAGE_SYNCH_ERROR	Required	
	SEQUENC_ERROR	Required	
	GA_PAR_ERROR	Required	
	WRITE_VIOLATION	Required	See note 2.
	REQ/GRANT//PE_ERROR	Required	
	REQUEST_TENURE_TIMEOUT	Required	See note 2.
	RETRY_NOT_ALLOWED	Required	See note 1.
	ARB_MSG_TIMEOUT	Required	
	STATUS/CAPABILITY_ERROR	Required	
	RESET_TIMEOUT	Required	
	RESET_ERROR	Required	
NOTES: 1 — Required for modules that support Distributed Arbitration and/or Arbitrated Messages. 2 — Required if Master.			

Table 4.15—WRITE_PROTECT_CSR

Register name	Bit/field name	Mandate	Comments
WRITE_PROTECT	PROT_CODE	Required	
	CSR_GROUP_A	Required	
	CSR_GROUP_B	Required	

Table 4.16—REQ_TENURE_TIMEOUT_CSR

Register name	Bit/field name	Mandate	Comments
REQ_TENURE_TIMEOUT		Required	See note.
NOTE — Transaction Timeout: Nodes shall at least implement at timeout range of 30.5-457.7 μ s with a tolerance of $\pm 10\%$ of the value set.			

Table 4.17—ARB_MSG_TIMEOUT_CSR

Register name	Bit/field name	Mandate	Comments
ARB_MSG_TIMEOUT		Required	See note.
NOTE — Required for modules that support Distributed Arbitration and/or Arbitrated Messages.			

Nodes that do not implement private space (nodes that can access all of the Futurebus+ address space) may access these addresses on the bus. However, software is expected not to assign the extended spaces within the private space, since these bus addresses cannot be accessed by those nodes that implement the private space option.

4.3.5 Interrupts

If modules use event mechanisms, they should support the soft interrupt mechanism defined in clause 3 of IEEE Std 896.2-1991 . All nodes generate an interrupt by writing a 32-bit (4-byte) datum to an assigned

Table 4.18—MAINT_CONTROL CSR

Register name	Bit/field name	Mandate	Comments
MAINT_CONTROL	RETRY_STATUS/CAPABILITY	Required	
	RETRY_LENGTH	Required	
	RETRY_NON_EXISTENT_ADDR	Required	See note.
	RETRY_DATA/ADDR_PAR	Required	See note.
	RETRY_TE/BE	Required	See note.
	RETRY_SEQUENCE	Required	See note.
	RETRY_REQ/GRANT/PE	Required	See note.
	RETRY_TENURE	Required	See note.
	DISABLE_ON_ERROR	Required	See note.
	DISABLE_PAA	Required	
	MAINT_MONITOR_ENABLE	Required	
	ERROR_RPT_ENABLE	Required	
	FTE_ENABLE	Required	
NOTE — Required if Master.			

Table 4.19—MAINT_MONITOR_SYNCH CSR

Register name	Bit/field name	Mandate	Comments
MAINT_MONITOR_SYNCH	AS	Required	
	AK	Required	
	AI	Required	
	DS	Required	
	DK	Required	
	DI	Required	
	ET	Required	

Table 4.20—MAINT_MONITOR_INFO CSR

Register name	Bit/field name	Mandate	Comments
MAINT_MONITOR_INFO	CM[7..0]*	Required	
	CP*	Required	
	ST[7..0]*	Required	
	CA[2..0]*	Required	
	RF*	Required	
	TED*	Required	
	SLD*	Required	

32-bit CSR address; the CSR address and interrupt datum (perhaps a vector) are assigned at system configuration time. Write to the interrupt address may return a *busy* status if there is a short-term condition (such as a queue of interrupts that is temporarily full) that prevents the responding node from logging the interrupt.

4.3.6 Monarch selection

Not all modules (although at least one) need be monarch-capable, but all monarch-capable modules shall support a standard monarch selection method so that they may be used in systems that may implement this process. The monarch is responsible for the initialization of low level bus parameters as required to facilitate system boot. Once system software is operating, that software may choose to select a new monarch; however, system software operation is beyond the scope of this standard.

Table 4.21—Other MAINT_MONITOR CSRs

Register name	Bit/field name	Mandate	Comments
MAINT_MONITOR_BP	Bits [3..0]	Required	
MAINT_MONITOR_AD_32	All bits	Required	
MAINT_MONITOR_ARB	RQ0, RQ1, GR, PE	Required	
MAINT_MONITOR_AB	All bits	Required	See note.
NOTE — Required for modules that support Distributed Arbitration and/or Arbitrated Messages.			

Table 4.22—MAINT_UTILITY CSRs

Register name	Bit/field name	Mandate	Comments
MAINT_UTILITY	Supports FB+ data bus width	Required	

The Profile F monarch selection process shall be used by all monarch-capable modules.

4.3.6.1 Monarch duties during system initialization

Once the monarch for a bus segment has been selected, the monarch is expected to perform a minimum set of duties to initialize the local bus segment. These duties shall include the following:

- a) Initialize and configure physical memory (extended memory);

- b) Initiate boot firmware process or bypass boot firmware and initiate a custom bootstrap program (for time-critical applications);
- c) Probe modules to determine the minimum interoperable set of Futurebus+ parameters and configure each node on the local bus segment (i.e., bus arbitration settling time).

4.3.7 System initialization

All modules that are monarch-capable shall implement system initialization in accordance with IEEE Std 1275-1994. In addition, all modules shall provide Fcode drivers in nonvolatile memory according to IEEE Std 1275-1994. Modules may bypass open boot during initialization in extremely time-critical systems. IEEE Std 1275-1994 defines a standard method for system initialization that will promote multi-vendor interoperability. For Futurebus+ specific aspects of boot firmware, refer to IEEE Std 1275.4-1995.

4.3.8 Direct memory access (DMA)

When direct memory access (DMA) transactions are conducted across the backplane, they should be implemented in accordance with IEEE Std 1212.1-1993 DMA framework. All unit architectures that are developed for, or implemented on, the backplane should be in accordance with IEEE Std 1212.1-1993. In addition, existing unit architectures should be utilized wherever possible. If no unit architecture exists, a new unit architecture should be developed in accordance with ISO/IEC 13213 :1994 CSR architecture and IEEE Std 1212.1-1993 DMA framework.

4.3.9 Diagnostics and test

All modules should have built-in self test. Test coverage shall be stated in the product literature. The interface to built-in tests shall be through the Serial Bus(es). In addition, testing may be initiated through the Futurebus+. In dual bus systems, either Serial Bus 1 or Serial Bus 2 shall be capable of providing the test interface.

4.3.9.1 Module built-in-test (BIT) control

The module should provide on-module test support (module BIT). Each module should provide BIT and the capability to report results for fault detection, fault isolation, and fault reporting. Module test architecture, if implemented, shall include the necessary functional and physical partitioning, functional and parametric tests, test control, and test access (e.g., design for test, scan path, level sensitive scan design, boundary scan, etc.) to meet the module test requirements.

Built-in testing for three categories of operational tests may be implemented. These are defined as start-up BIT (SBIT), initiated BIT (IBIT), and on-line BIT (OBIT).

Module start-up BIT (SBIT) should include test sequences required during module power-up cycles to meet the platform requirements for power-up testing. This should include, but not be limited to, tests of all functional module resources. These tests are generally not exhaustive to reduce warm-up time and with the expectation that modules nearly always test satisfactorily on start-up. SBIT does not incorporate exhaustive memory function testing.

Module initiated BIT (IBIT) should include test sequences required when the module is commanded to run BIT, and generally implies that the module has been isolated from backplane transactions to determine the health of the module. IBIT is invoked by the system diagnostic control functions (platform-dependent), typically by the backplane serial bus. IBIT tests should include diagnostic testing extensive enough to meet the required fault isolation and identification requirements of the platform. IBIT should be assumed to alter module state and memory contents so that a normal “cold start” will be required following completion of tests and a healthy report.

Module on-line BIT (OBIT) should include test sequences required for normal background operation while the module is in service. OBIT should include tests that may be carded out while allowing the module to carry out normal operation for the target use. OBIT activities should include test sequences required to determine normal and correct module functionality. OBIT tests may require extensive time to complete, and so must be interruptible.

4.3.10 Live insertion and withdrawal

Provisions for live insertion are made at several levels in the Futurebus+ standard and this standard. At the Futurebus+ signaling level, procedures for aligning modules with the bus when inserting or withdrawing modules are specified in ISO/IEC 10857 :1994. Mechanisms to support live insertion at the physical level are specified in the power and electrical clauses of this standard and in clause 4 of IEEE Std 896.2-1991.

This standard allows any of the levels 0, 1, 2, and 3 of live insertion, which differ in reliability and impact on system operation. All levels of live insertion are optional. See 4.4.1.1.3 and 4.4.2.3.5.

4.4 Physical layer detailed specification

4.4.1 Profile power

This subclause specifies power distribution and behavior for modules and systems. Requirements for modules and for the systems they plug into are specified in separate clauses.

Performance requirements impose constraints on module and backplane design in order to satisfy the following requirements:

- a) Distribute power-return and power blades to equalize current concentrations;
- b) Maintain power supply voltages within required tolerances for a wide range of module power requirements;
- c) Align power and power return blades to satisfy connector mechanical requirements.

All voltage measurements of the power rails or power distribution system shall be made relative to the nearest 0 Vdc power supply return blade of the same or nearest connector on the backplane for all but the ± 15 Vdc analog power rails or the 48 V supply. The reference for the ± 15 V power shall be the nearest available GNDA pin. The 48 V supply is measured between +V and -V. All measurements of signal voltages shall be made relative to the closest signal ground (GND) return pin for digital signals, and power return (GNDA) for analog signals.

4.4.1.1 Module power

4.4.1.1.1 Pin current limits

The current passing through any power supply blade, power return blade, or ground pin, except for the ± 15 Vdc (or any optional voltage) supplied to signal pins, shall not exceed 2 A (averaged across all blades for each supply voltage). The ± 15 Vdc power sources supply power to pins on block E connector that have less current-carrying capacity. The current passing through any ± 15 Vdc power supply pin, any other optional (e.g., +28 V) voltage supply on a signal pin, or GNDA pin shall not exceed 1 A.

For purposes of system configuration, maximum current per pin is defined as the following:

- a) For ± 15 Vdc supplies (or any other optional voltage), no block E connector shall conduct steady-state current in excess of the 1 A current limit.
- b) For all other supplies, measure current on a sample of five modules at nominal voltage under maximum-power operating conditions. For each voltage, take the average current for the five modules and add 10%.

The above current per pin ratings are an absolute maximum based on the physical limitations of the connector pins. System-dependent voltage levels and noise considerations may further limit this maximum current rating. Refer to annex C for current per connector pin guidelines.

Maximum current for all voltages used by the module type shall be declared in module product literature and product specifications.

4.4.1.1.2 Module bypass capacitance and di/dt

Each module shall supply the following amount of bypass capacitance on each power bus. The capacitance of the +5 V bus divided by the maximum value of the +5 Vdc current shall be between 10 $\mu\text{F/A}$ and 50 $\mu\text{F/A}$. The capacitance on the +3.3 V bus divided by the maximum value of the +3.3 Vdc current shall be between 30 $\mu\text{F/A}$ and 110 $\mu\text{F/A}$.

Modules with live insertion capabilities need to limit the inrush current at power-up to avoid forcing any voltages it uses out of regulation. Typically, power control circuits under the control of the live-insertion logic are required to limit inrush current.

Module specifications shall state the maximum di/dt (change in module current demand) for each voltage in normal operation (other than power-up). Modules with live insertion capability shall further state the maximum inrush current at each voltage under live-insertion power up conditions.

4.4.1.1.3 Live insertion considerations

Modules with live insertion capability shall limit their power-on inrush current to a maximum of 1 mA/ μs at +3.3 V, 1 mA/ μs at +5.0 V, 0.8 mA/ μs at +15 V and -15 V , and 0.2 mA/ μs at $\pm\text{Vdc}$. This figure shall include the combined effects of on-module capacitance and circuitry. Typically, some form of active power control will be required to constrain inrush current, managed by on-board live-insertion logic, which itself draws little current.

Live insertion is optional. Designs intending to use level 2 live insertion may use the VBP voltage available at two blades of row b of the power connectors (see 4.4.6.3). This voltage is available on the longer blades of row b for precharging Futurebus+ transceivers that have the special precharge pin. Through this pin, the transceiver bus driver output circuits are charged to a voltage less likely to cause signal disruption when the module pins make contact with active bus lines. VBP may be current-limited through a resistor on the module to reduce instantaneous current drawn when the connector pins first make contact.

Module designers, who intend to use the live insertion option, should note that the mechanical design of the power connector forces a random “power-up sequence.” The longer power blades in row of the power connectors will cause the +5 V precharge and supply return (0 V) blades to make contact first. Following in an unpredictable sequence will be +3.3 V, +V and $-V$, +15 V, -15 V , and the main VBP. Module designs that intend to use live insertion, and require special power sequencing, shall control that sequencing on the module.

4.4.1.2 System power supplies

Different power supply types may be employed depending on the configuration requirements. These could include

- a) *Chassis mounted supply.* A supply mounted adjacent to the bus that is connected to the bus via cabling.
- b) *Plugged-in bused supplies.* One or more supplies for the same voltage rail(s) may reside on the bus. Multiple supplies are used for redundancy or load distribution reasons, provided appropriate protection networks and load-balancing circuitry are employed. The advantage of this method is that the power supplies can be plug-in like any other board.

Refer to annex C for a discussion on how power supply quality and baseline voltage may effect the maximum current per signal pin rating.

4.4.1.2.1 Supply voltages

Backplane power blade assignments provide for five voltages for powering digital logic: +5 V, +3.3 V, +V, $-V$, VBP, and the associated digital return 0 Vdc. Bus termination requires +2.1 Vdc. The backplane also provides power and return pins for analog circuit power (+15 V, -15 V and GNDA). The backplane shall supply digital power to circuit boards via conducting planes within the backplane. Separate return paths (grounds) for digital and analog circuits may be provided if analog circuitry is employed.

Power connections between detached equipment shall be isolated. Peripheral devices deriving power from a module on the bus shall be driven from an isolated power supply; each external line shall have its own isolated power supply.

The +V and –V supply forms a 48 V nominal supply. It may be preregulated. One use of the +V/–V is as a floating supply. In such applications, it shall not inflict its return current on the system logic ground. Failure to maintain complete isolation will result in ground loops with potentially serious system noise implications. The referencing of this supply to 0 Vdc is flexible. Possible configurations include the following:

- a) Direct referencing the –V terminal to the single point or primary system ground to form a +48 V supply;
- b) Direct referencing the +V terminal to the single point or primary system ground to form a –48 V supply;
- c) Referencing +V and –V through equal value resistors to form a ± 24 V supply (or from a center tapped transformer secondary to two balance regulators to form a ± 24 V supply).

In any case, the referencing of +V and –V to 0 V shall maintain the voltages within the range specified in 4.4.1.2.4. It is recommended that when either +V or –V, or both, are not directly referenced to 0 Vdc, the +V or –V, or both, be referenced to a single point or primary system ground through a resistor of not more than 100 k Ω .

On modules, power shall be drawn from the +V and –V only through galvanically isolated dc-dc converters. Modules using power from +V and –V shall be able to operate with +V and –V within the range specified in 4.4.1.2.4. On any one module, the maximum dc leakage current from the 48 V supply shall be 5 μ A. This is defined as the current sourced from the +V and not returned to the –V, or vice versa. Proper design practices should be followed to ensure that digital or analog signals derived from the +V/–V supply do not capacitively couple to the system logic or backplane ground, and that such signals be separately shielded with a separate return path to the single point or primary system ground.

Only the digital supply voltages specified in the connector blade assignments (see 4.4.6.3) shall be connected to their assigned power blades. For each supply voltage provided, that voltage shall be available at every power blade assigned to it, as indicated in figure 4-33. Systems designed for high reliability using on-module regulation may choose to provide 48 V from two independent sources; if this is done, the two sources shall connect to the 48 V supply blades as described in the power pinout clause of this standard.

If a supply voltage is not provided by a particular system power supply, the blades assigned to that voltage shall be reserved. In addition, 0 Vdc power returns and 0 V signal grounds shall be connected to backplane ground plane(s) at all connector positions. Figure 4.1 depicts power and ground distribution over the backplane.

In a like manner, only the analog voltages (+15 V and –15 V) and the analog ground (GNDA) specified in the connector pin assignments of figure shall be connected to the assigned power pins. For each analog supply voltage provided, the voltage shall be available at each pin assigned to it, as indicated in figure 4.13. Figure 4.2 depicts analog power and ground distribution over the backplane.

4.4.1.2.2 Rise time and power sequencing

Power supply transients at turn-on shall not exceed the limits specified in 4.4.1.2.4. Rise time shall be less than 200 ms from 10% to 90% of the nominal voltage under all specified loading conditions.

Voltages during power-up, power-down, and power-fail can follow any sequence.

Observation: Power-fail can occur on any voltage, therefore boards must be designed to protect against situations where any one of the voltages may not be present if more than one voltage source is used. For systems that are reconfigured in the field, it is difficult to predict system current required for all applications. Adding or deleting boards from a preconfigured system will change the current draw from the power supply. During power-down, the collapse rate will vary from configuration to configuration. Again, boards will experience a variety of power down sequences and should be designed not to cause a failure under a variety of applications.

4.4.1.2.3 Noise and ripple

Noise and ripple on any regulated power blade on the backplane shall remain below 50 mV, peak-peak, measured at all frequencies up to 20 MHz, under all specified loading conditions.

4.4.1.2.4 Voltage variation

The voltage between the +5 V and 0 Vdc blades, at all module connector sites, under all conditions of loading, noise, ripple, and variation of input voltage to the power supply, shall remain within the limits of +4.85 V to +5.25 V.

The voltage between the +3.3 V and 0 Vdc blades, at all module connector sites, under all conditions of loading, noise, ripple, and variation of input voltage to the power supply, shall remain within the limits of +3.20 V to +3.465 V.

The voltage between the VBP and 0 Vdc blades, at all module connector sites, under all conditions of loading, noise, ripple, and variation of input voltage to the power supply, shall remain within the limits of +4.85 V to +5.25 V.

The VBP blade may be used optionally for battery backup when primary power is not available. Under these circumstances, VBP shall remain within the limits of +2.1 V to 5.25 V.

The voltage between the +V and –V blades, at all slot locations, under all conditions of loading, noise, ripple, and variation of input voltage to the power supply, shall remain within the limits of +38 V to +56 V.

The voltage between the +V blades and 0 Vdc blades, at all slot locations, under all conditions of loading, noise, ripple, and variation of input voltage to the power supply, shall always satisfy the relationship $+V \geq 0$ Vdc.

The voltage between the –V blades and 0 Vdc blades, at all slot locations, under all conditions of loading, noise, ripple, and variation of input voltage to the power supply, shall always satisfy the relationship $-V \leq 0$ Vdc.

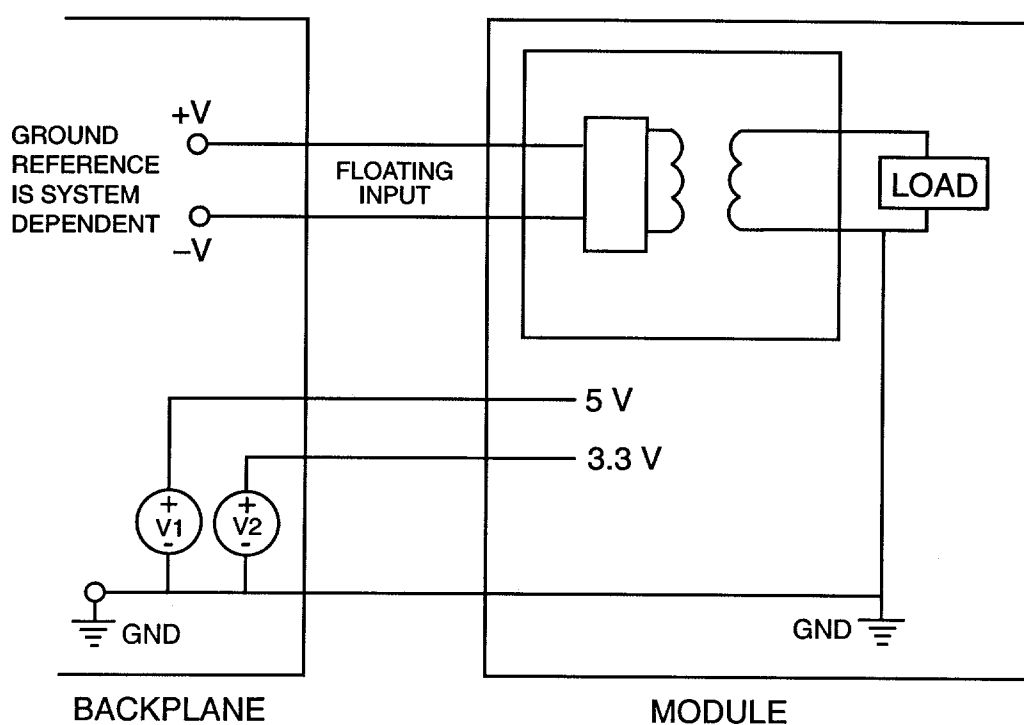


Figure 4.1—Digital power rails

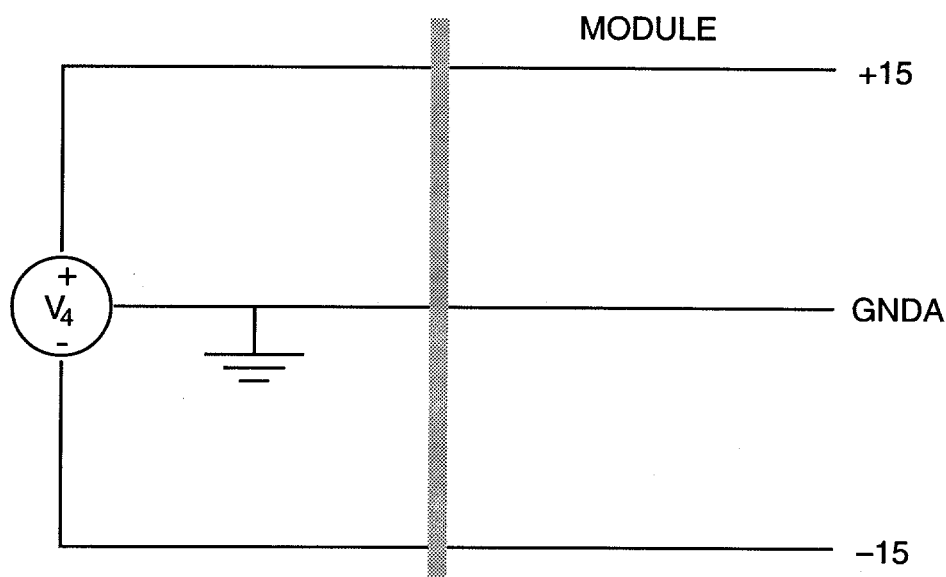


Figure 4.2—Analog power rails

The analog supply (+15 V and -15 V) shall have a separate ground return (GNDA) from the digital return (0 Vdc). The supply capability and specifications shall be adequate for the analog functions supported. In general, a supply with a

5% total noise and bias tolerance will suffice, with precision voltages being developed from this source on each circuit board as needed.

The voltage between the +15 V and GNDA pins, at all module connector sites, under all conditions of loading, noise, ripple, and variation of input voltage to the power supply, shall remain within the limits of +13.5 V to +16.5 V. The voltage between the –15 V and GNDA pins, at all module connector sites, under all conditions of loading, noise, ripple, and variation of input voltage to the power supply, shall remain within the limits of –13.5 V to –16.5 V.

The voltage between the –5 V and 0 Vdc blades, at all slot locations, under all conditions of loading, noise, ripple, and variation of input voltage to the power supply, shall remain within the limits of –4.85 V to –5.25 V.

The voltage between the +28 V and 0 Vdc blades, at all slot locations, under all conditions of loading, noise, ripple, and variation of input voltage to the power supply, shall remain within the limits of +25.2 V to +30.8 V.

4.4.1.2.5 Analog power and ground

± 15 V and a separate ground/power return are optionally provided (for this voltage). These are intended to be used in applications where low noise power and ground are required for analog/RF modules. Analog modules that do not require an isolated low-noise power and ground may use any power available on the backplane, including the optional $\pm V$ for high-current applications. The analog ground (GNDA) should be separated from all other grounds and should be used as a power return for all ± 15 V usage. Analog ground (GNDA) should not be used as a power return for voltages other than ± 15 V.

4.4.1.2.6 Power supply current capability and di/dt tolerance

Minimum current supplied for each voltage, under all environmental conditions, shall be indicated in the system product specification. It remains the responsibility of those configuring systems to ensure that the total worst-case current demand of the chosen module set does not exceed the rated capacity of the system power supplies for any supply voltage, under all specified environmental conditions.

Specifications for system power supplies shall state the maximum di/dt the supply can tolerate for each voltage while remaining in regulation. It is the responsibility of those configuring systems to ensure that the combined (sum) di/dt of all modules in the system does not exceed the di/dt tolerance of the power supply. This calculation should include the sum of normal operating di/dt, as well as maximum specified inrush current for live-inserted modules, if that feature is used.

4.4.1.2.7 Maximum dc voltage drops across backplane

Power return paths of 0 Vdc on the backplane shall present a maximum voltage differential of 50 mV across the backplane, measured between any components or connector pins making contact with the 0 Vdc rail, under conditions of maximum current demand and all conditions of loading and noise expected for that system. Backplane terminator areas are included in this requirement.

4.4.1.2.8 Power fail

Under all operating conditions, the power supply or its agent shall provide a power fail emergency message (via the PFI utility signal, the PFI Serial Bus CSRs, or the PFI arbitrated message) at least 100 μ s prior to the time any dc supply goes out of regulation.

During the 100 μ s power fail period, all dc outputs shall remain within the limits specified in 4.4.1.2.4. See also 4.2.7.5.

4.4.1.3 Power and ground distribution

The power and ground distribution shall be in accordance with the following requirements:

- a) Special precautions shall be taken to ensure that I/O cables do not couple noise into the backplane and the system. To minimize both internally and externally coupled noise for peripheral interfaces (e.g., MIL-STD-1397 [B17] , analog, synchro type links, etc.) external return paths should be isolated from backplane logic ground.
- b) Additional connector pins may be reserved to bring external ground lines to the single point ground within a cabinet (see figure 4.1 and 4.4.4.6).
- c) The backplane shall contain laminated power and ground plane pairs for each digital voltage. For maximum decoupling, the power and return planes should be immediately adjacent. Analog ground plane(s), if incorporated, shall be fabricated separately and isolated from the digital ground plane(s). This does not preclude the opportunity to provide single or multiple points of analog/digital ground connections on either the module or the backplane.
- d) An analysis shall be made to determine the severity of induced noise on an I/O module's power and ground when an external reactive load is being powered by the module. Each module supplying power to an external load that could have its on-board power source corrupted by 50 mV rms or more of induced noise from an external source shall supply power to the external load from an isolated power supply. On-board isolated power can be developed from dc-dc transformer coupled converters with optical or winding feedback for external power regulation. In this manner, the output can be regulated and electrically isolated from the input power source. Where isolated power is called for, the external ground or return line should not be connected directly to the backplane's 0 Vdc ground blades but should be returned to the crate's single point ground through user-defined backplane connector pins or through GNDA pins if noise on GNDA will not disturb other circuits.
- e) Proper grounding, bonding, and shielding practices shall be followed generally. However, for equipment destined to process national security related information, TEMPEST requirements for primary power filtering, shielding of power and signal cables and the positioning of cables to minimize crosstalk, bonding and shielding of units and modules, electromagnetic interference (EMI) elimination, and separation of red and black equipment must be followed (see 4.4.1.4).

Figure 4.3 depicts power and ground distribution over the backplane.

4.4.1.4 Security/TEMPEST considerations

If modules related to red and black data are mixed in the same box, it is presumed that the red and black modules connect to separate Futurebus+ and power buses. If it is necessary to mix black and red data on the same module, additional precautions must be taken.

Documents that provide guidance with regard to TEMPEST considerations are MIL-HDBK-419 [B14] , MIL-HDBK-232 [B13] , NACSEM 5202 [B21] , and MIL-STD-1680B [B19] .

4.4.2 Electrical profile

4.4.2.1 Backplane characteristics and design requirements

Table 4.23 lists conditions under which the electrical specifications were developed. Although modules may operate satisfactorily under other conditions, such as the maximum number of modules, these conditions were not studied or simulated during design.

Table 4.24 summarizes the electrical parameters for the MIL-12SU module. These parameters are described in detail in the following subclauses.

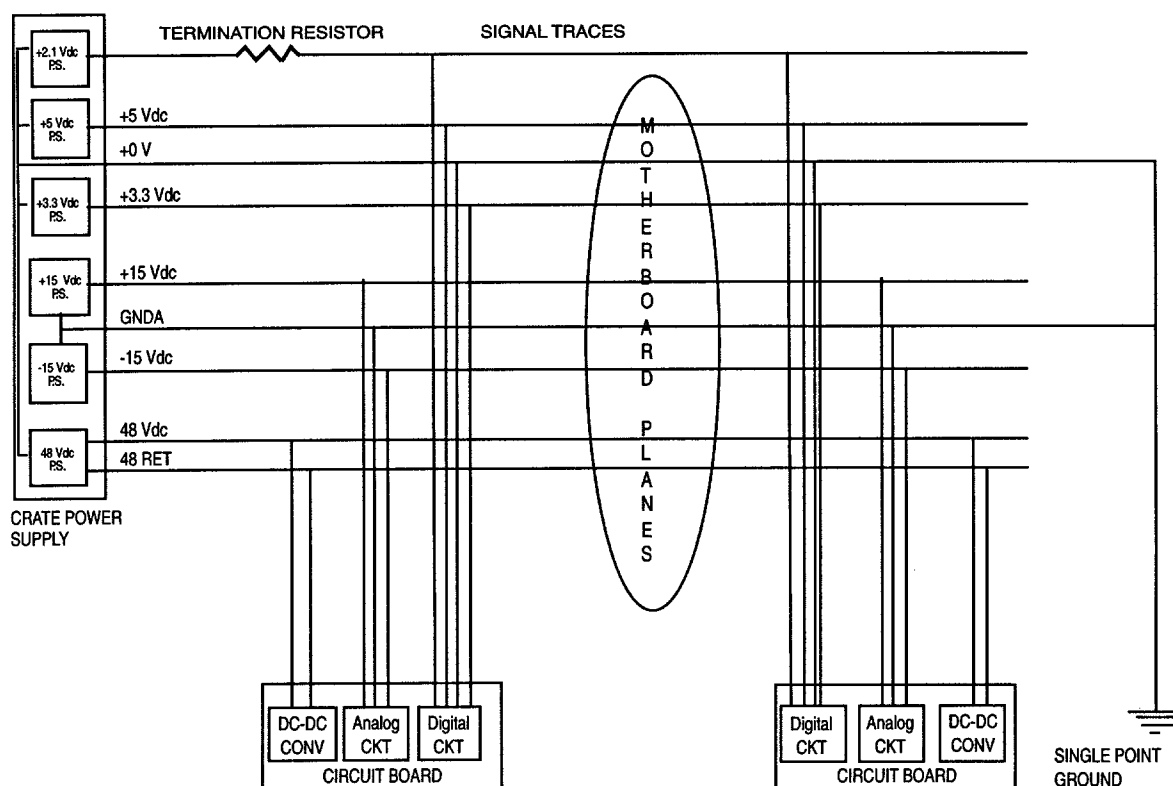


Figure 4.3—Example of logic, analog power, and ground configuration

Table 4.23—MIL-12SU electrical specifications conditions

Number of slots	14 maximum
Electrical pitch	30 mm
Configuration requirement	Partially populated systems should have modules distributed as uniformly as possible—avoid lumping modules in one area of the backplane
Vias per stub	Two vias per stub. One of the vias may be at the transceiver and the other may be at the connector.
Transceiver as specified in IEEE Std 1194.1-1991	One transceiver per bus signal per module

4.4.2.1.1 Geographical address lines

The geographical address pins, **GA[4..0]**^{*}, shall provide a binary-encoded number on the connector representing the slot number in which it is located, with **GA4**^{*} being the most significant bit, and **GA0**^{*} being the least significant bit. The slots shall be numbered in ascending order. The numbering should be contiguous (note that 1F is reserved). The leftmost slot, when viewed from the front of the rack, is slot number 1.

Table 4.24—Summary of MIL-12SU electrical characteristics

Parameter	Value				Comments
	Min	Nominal	Max	Units	
Z_o'	52	57	62	ohms	See 4.4.2.1.2
R_{sig}			1	ohms	See 4.4.2.1.3
R_{term}		$33 \pm 1\%$		ohms	See 4.4.2.1.6
V_{term}		$2.1 \pm 2\%$		volts	See 4.4.2.1.7
Z_{stub}	45	60	75	ohms	Characteristic impedance of signal line stub on the module
L_{stub}			25	mm	See 4.4.2.2.2
Behavioral					
ΔV_{gnd}			± 50	millivolts	Limits ground-plane voltage drop under maximum current load
signal skew			1.5	ns	See 4.4.2.1.5

On the **GA[4..0]*** pins, logic zero is represented by an open circuit on the backplane and logic one by grounding the pin on the backplane.

4.4.2.1.2 Impedance

Backplane signal traces, including the backplane halves of the signal connectors and vias, but not including add-in circuit modules, shall present an effective characteristic impedance Z_o' , where

$$52 \, \Omega \leq Z_o' \leq 62 \, \Omega$$

with a nominal value of $57 \, \Omega$

4.4.2.1.3 Resistance

The maximum signal trace resistance corresponding to the maximum possible signal path length (i.e., from one end of the bus to the other end) shall not exceed $1 \, \Omega$. All 0 V logic pins shall be tied to the 0 Vdc ground plane at their connector pin positions.

4.4.2.1.4 Maximum propagation delay

The maximum one-way propagation delay t_{pd} on a signal line, in a fully loaded system, should be 7.5 ns (15 ns round trip), including connection to termination networks. (This parameter is derived using a 14-slot backplane built with a 5.5 permittivity material and fully populated on a 30 mm pitch).

4.4.2.1.5 Signal skew

Signal line skew on the unloaded backplane (with connectors) shall not exceed 1.5 ns between any two module locations. With the specified tolerance on signal line capacitance, the skew in a fully loaded 30-module backplane is expected to be 6 ns or less.

4.4.2.1.6 Termination

Each bus line shall be terminated in a resistance of $33\ \Omega \pm 1\%$ to a source of the termination voltage at both ends of the backplane. Resistance shall remain within tolerances over the full profile-specified environmental conditions. Surface-mount termination resistors, with individual resistor pins for +2.1 V, are recommended for lowest inductance, lowest cross-coupling, and better matching to the bus line impedance to minimize reflections.

The termination circuit shall be capacitively bypassed so the +2.1 V termination voltage, measured at the termination resistors, stays within the limits specified at all frequencies up to 20 MHz.

4.4.2.1.7 Termination voltage

The termination voltage for all lines on the bus signal paths shall be +2.1 V $\pm 2\%$, measured at the termination resistor. In addition, $-50/+50$ mV of ripple is allowed. This termination voltage may be derived from other voltages available on the backplane, or provided by an external power supply.

4.4.2.2 Module electrical characteristics and design requirements

4.4.2.2.1 Geographical address lines

A module shall attach each of its five **GA[4...0]** pins through a resistor to a voltage that, when received by the appropriate logic on the module, is interpreted as a logic zero by that logic if the backplane does not ground that pin. The resistor shall limit current on any GA line to 2 mA maximum. The module should bypass each of its **GA[4...0]** signals with a low-inductance capacitor (surface-mount type recommended) of 100 pF to module GND.

4.4.2.2.2 Stub lengths

Stub length of conductors from any signal pin on the specified connector to its corresponding transceiver I/O pin shall not exceed 25 mm. Transceivers may be mounted on one or both sides of the module. The stub length is to be measured from the point at which the connector assembly connects to the PC board to the pad where the transceiver lead is soldered to the PC board.

4.4.2.2.3 Stub impedance

The characteristic impedance of the signal line stub on the module shall be $60 \pm 15\ \Omega$.

4.4.2.3 Characteristics of Futurebus+ transceivers

Devices used for driving backplane signals and for receiving signal information from the backplane bus shall be active-low (on Futurebus+ side) transceivers, conforming to IEEE Std 1194.1-1991.

Transceivers shall be capable of wired-OR functions on all bus signal lines, except the **GA[4..0]** lines.

Transceiver devices shall conform to the following specification, operating over the range of card cage-internal environmental conditions required by the class or classes in the environmental clause of this standard, and specified in IEEE Std 1156.1-1993.

4.4.2.3.1 Wired-OR glitch filters

Modules shall have programmable glitch filters on the following Futurebus+ signals:

AI^{*}, AK^{*}, AP^{*}, AQ^{*}, AR^{*}, RE^{*}, DI^{*}, and DK^{*}.