

IEEE Standard for the Common Test Interface Pin Map Configuration for High-Density, Single-Tier Electronics Test Requirements Utilizing IEEE Std 1505™



IEEE Instrumentation and Measurement Society

Developed by the
IEEE Standard Coordinating Committee 20 on Test Diagnostics for Electronic Systems

IEEE
3 Park Avenue
New York, NY 10016-5997
USA

IEEE Std 1505.1™-2019
(Revision of
IEEE Std 1505.1-2008)

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Approved 13 June 2019

IEEE SA Standards Board

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Abstract: An extension to the IEEE 1505™ receiver fixture interface (RFI) standard specification is provided in this standard. Particular emphasis is placed on defining within the IEEE 1505 RFI standard a more specific set of performance requirements that employ a common scalable: 1) pin map configuration; 2) specific connector modules; 3) respective contacts; 4) recommended switching implementation; and 5) legacy automatic test equipment (ATE) transitional devices. This is intentionally done to standardize the footprint and assure mechanical and electrical interoperability between past and future automatic test systems (ATS).

Keywords: automatic test equipment (ATE), automatic test systems (ATS), fixture, IEEE 1505.1™, interconnecting device (ICD), interface, interface test adapter (ITA), mass termination, receiver, scalable, test program set (TPS), unit under test (UUT)

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PDF: ISBN 978-1-5044-5975-4 STD23757
Print: ISBN 978-1-5044-5976-1 STDPD23757

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Participants

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Robert Spinner, *Chair*
Stephen Mann, *Vice Chair*

Larry Adams
Malcolm Brown
David Droste

George Isabella
Ted Ronnenburg

Mike Seavey
Michael Stora
Ronald Taylor

The following members of the individual balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

Demetrio Bucaneg, Jr.
David Droste
Randall C. Groves
Werner Hoelzl
Anand Jain

Osamu Karatsu
Stephen Mann
Leslie Orlidge
Robert Spinner

Joseph Stanco
Michael Stora
Walter Struppler
Ganesh Subramanian
Ronald Taylor

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Masayuki Ariyoshi
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David J. Law
Joseph Levy
Howard Li
Xiaohui Liu
Kevin Lu
Daleep Mohla
Andrew Myles

Annette D. Reilly
Dorothy Stanley
Sha Wei
Phil Wennblom
Philip Winston
Howard Wolfman
Feng Wu
Jingyi Zhou

*Member Emeritus

Introduction

This introduction is not part of IEEE Std 1505.1™-2019, IEEE Standard for the Common Test Interface Pin Map Configuration for High-Density, Single-Tier Electronics Test Requirements Utilizing IEEE Std 1505™.

Developers, users, and buyers of general-purpose rack-and-stack or portable test equipment will benefit by using this modular and scalable IEEE standard for the receiver fixture interface design whether the application is for a manual, semiautomated, or fully automated test system. Previous versions of this standard restricted its adoption by mandating specific pin configurations for the interface and in doing so limited the applicability of the modular and scalable design. By eliminating the pin configuration requirement, the modular and scalable design also lends itself to being reconfigurable for easy reuse of the IEEE primary design.

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IEEE ~~Trial-Use~~ Standard for the Common Test Interface Pin Map Configuration for High-Density, Single-Tier Electronics Test Requirements Utilizing IEEE Std 1505™

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1. Overview

1.1 Scope

The scope of this ~~trial-use~~ standard is the definition of a [physical](#) pin map utilizing the IEEE 1505™[†] receiver fixture interface (RFI). The pin map defined within this ~~trial-use~~ standard shall apply to military and aerospace automatic test equipment (ATE) testing applications.

1.2 Purpose

~~The purpose~~ ~~Standardization~~ of [this standard is to permit](#) ~~a common input/output (I/O) will enable~~ the [physical](#) interoperability of IEEE 1505-compliant interface fixtures (~~{~~also known as interface test adapters (~~ITA~~), interface devices (~~ID~~s), or interconnecting devices (~~ICD~~s)~~}~~) on multiple ATE systems utilizing the IEEE 1505 RFI [by providing a standardized physical pin map with related connector configuration and contact performance characteristics.](#)

1.3 Statement of the problem

~~1.3.1 U.S. Government guidance~~

~~From 1980 to 1992, the U.S. Department of Defense (DoD) investment in field, depot, and factory automatic test systems (ATS) exceeded \$35 billion with an additional \$15 billion for associated support. Most of this test capability was acquired as part of individual weapon system procurements. This led to a proliferation of different custom equipment types with unique interfaces. Recent policy decisions have changed the direction of the purchase of test equipment towards a standards-based approach with both hardware and software critical interface requirements.~~

[†]~~Information on references can be found in Clause 2.~~

The U.S. DoD Instruction 5000.2 R1 ATS Policy states: “ATS capabilities shall be defined through critical hardware and software elements” (see [B2]²). This policy however, did not define these critical elements. The Critical Interfaces Project was created to define critical ATS elements.

1.3.2 Critical Interfaces Project

The Factory to Field Integration of Defense Test Systems Project (commonly referred to as the *Critical Interfaces Project*) was started in the latter part of 1995. The Critical Interfaces Working Group (CIWG) within the Joint Service ATS Research and Development Integrated Product Team (ARI) was established to perform the project. The ATS Executive Agent Office (EAO) has provided project management and coordination among the Air Force, Army, Marine Corps, and Navy participants. In addition, many industry representatives have participated. The CIWG published their findings in the Automatic Test System Critical Interfaces Report [B1] and this report served as the basis for the development of the RFI architecture and subsequent specification.

The objective of the Critical Interfaces Project was to demonstrate the feasibility of reducing the cost to re-host test program sets (TPSs) and increase the interoperability of TPS software among the military services by using standardized interfaces.

Interfaces that offer the potential to achieve this objective are deemed critical. Potential savings will be quantified through demonstration. The Automatic Test System Critical Interfaces Report [B1] is maintained by the ATS EAO and provides guidance to DoD ATE acquisition programs. This document also addressed the requirements of DoD Regulation 5000.2 R1 [B2] and assisted in migrating the DoD designated tester families towards a common solution. The Hardware Interfaces (HI) Subcommittee of the IEEE Standards Coordinating Committee on Test and Diagnosis for Electronic Systems (SCC20) applied the recommendations of the report as it related to the RFI, to the extent that the current RFI standard is in full compliance with the report.

² The numbers in brackets correspond to those of the bibliography in Annex B.

1.3.1 [IEEE 1505.1 working group](#) ~~CTIWG~~ guidance recommendations

During the Common Test ~~Interfaces~~ ~~Interface~~ Working Group (CTIWG) October 2003 meeting, the [working group \(WG\)](#) ~~DeD~~ provided the following recommendations as guidance for the [WG's](#) ~~Working Group's~~ success:

- a) Identify a modular/[scalable](#) ~~scaleable~~ interface
- b) Allow use of different-[sized interface devices \(IDs\)/fixtures](#) ~~size ID/fixture~~ on the same general-purpose interface (GPI)
- c) Ensure [test program set \(TPS\)](#) hardware compatibility as interface grows
- d) Provide legacy system support
- e) Provide a transition path to support legacy TPS hardware
- f) Adhere to an open architecture system
- g) [Build](#) ~~Built~~ to one specification
- h) [Provide](#) multiple sources
- i) [Create](#) nonproprietary design and components
- j) Ensure capabilities that provision for growth and special requirements
- k) Provide room for future expansion and TPS requirements
- l) Support and promote the use of commercial-off-the-shelf (COTS) interconnect components
- m) Use industry standard connector technology

1.3.2 [IEEE 1505.1 working group](#) ~~CTIWG~~-legacy test program set support

In support of these recommendations, the [common test interface \(CTI\)](#) architecture shall assure past legacy and future TPS *plug-and-play* compatibility between defense agencies and defense–aerospace suppliers. Areas addressed by the CTIWG include [the following](#):

- a) [Physical electrical](#) pin mapping
- b) Scalability
- c) TPS legacy support
- d) Connector parametric (dc to light)
- e) Reliability and maintainability
- f) Physical
- g) Switching
- h) Design-to-cost factors

[Historical fact gathering and analysis that resulted in the formation of the original IEEE 1505.1 physical pin map are included in Annex A as informative.](#)

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated [references](#) ~~referenced~~, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1505TM~~-2006~~, IEEE Standard for Receiver Fixture Interface.^{1,2 3,4}

3. Definitions, specification terms, acronyms, and abbreviations

3.1 Definitions

For the purposes of this document, the following terms and definitions apply. The ~~Authoritative Dictionary of IEEE Standards~~ Dictionary Online ~~Terms [B5]~~ should be consulted ~~referenced~~ for terms not defined in this clause.³

physical pin map: The physical electrical data table and explanatory text that provides the assignment of electrical connector/contact characteristics to the receiver–fixture interface input/output (~~or instrument~~ I/O) to specific pins.

3.2 Specification terms

The specification terms used throughout this ~~trial-use~~ standard are described as follows:

observation: These spell out implications of rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules, so that the reader understands why the rule must be followed.

permission: They are included to clarify the areas of the specification that are not specifically prohibited. They reassure the reader that a certain approach is acceptable and will cause no problems. The word *may* is reserved for indicating permissions.

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³ IEEE Standards Dictionary Online is available at: <http://dictionary.ieee.org>.

recommendation: They consist of advice to applicants that will affect the usability of the final device. Discussions of particular hardware to enhance throughput would be included. These should be followed to avoid problems and to obtain optimum performance.

rule: They ~~Rules~~ shall be followed to ensure compatibility with ~~to~~ the ~~trial-use~~ standard. They are ~~A rule is~~ characterized by the use of the words *shall* and *shall not*. These words are not used for any other purpose other than stating rules.

~~**Recommendation:** Recommendations consist of advice to applicants that will affect the usability of the final device. Discussions of particular hardware to enhance throughput would fall under a recommendation. These should be followed to avoid problems and to obtain optimum performance.~~

~~**Suggestion:**~~ **A suggestion:** They contain ~~contains~~ advice that is helpful but not vital. The reader is encouraged to consider the advice before discarding it. They ~~Suggestions~~ are included to help the novice designer with problematic areas of the design.

~~**Permission:** Permissions are included to clarify the areas of the specification that are not specifically prohibited. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. The word *may* is reserved for indicating permissions.~~

~~**Observation:** Observations spell out implications of rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules, so that the reader understands why the rule must be followed.~~

3.3 Acronyms and abbreviations

ACPS	alternating current power supply
ADC	analog-to-digital converter
AI	analog instrument
AM	amplitude modulation
ATE	automatic test equipment

ATS	automatic test system
AWG	arbitrary waveform generator, ~~American wire gauge~~
BW	bandwidth
CAL	calibration
CAN	controller-area network
CASS	Consolidated Automated Support System ^{4 5}
CH	channel
CTIWG	Common Test ~~Critical~~ Interfaces Working Group
CLK	clock
COTS	commercial-off-the-shelf
CSW	coax switch
CTI	common test interface
DAC	digital-to-analog converter
DAS	display analyzer-simulator
DCPS	direct current power supply
DMM	digital multimeter
DPDT	double-pole-double-throw
~~DoD~~	~~U.S. Department of Defense~~
DTC	design-to-cost

^{4 5} U.S. Navy Tester, AN/USM-636 (V).

ECL	emitter ~~emitter~~ -coupled logic
ESTS	Electronic Systems Test Set ^{5 6}
~~ETE~~	~~end-to-end~~
EXT	external
freq	frequency
FM	frequency modulation
FTIC	frequency time interval counter
GND	ground
GPI	general purpose interface
~~HPL~~	~~high-power load~~
IAIS	improved avionics intermediate shop
~~ICD~~	~~interconnecting device~~
ID	interface device
IF	intermediate frequency
IFTE	Integrated Family of Test Equipment ^{6 7}
Instr	instrument
I/O	input/output
ITA	interface test adapter

^{5 6} U.S. Air Force Tester, AN/GSM-397 (V).

^{6 7} U.S. Army Tester, AN/USM-632 (V)3.

JTAG	Joint Testability Action Group
LCC	life-cycle ~~cost~~ costs
~~LFC~~	~~low frequency calibrator~~
LM-STAR®	Lockheed Martin Star ^{Z 8}
<u>low-R</u>	<u>low resistance</u>
~~LPL~~	~~low power load~~
~~LXI~~	~~LAN extensions for instrumentation~~
max	maximum
min	minimum
MOD	modulation
~~MoD~~	~~Ministry of Defense (UK)~~
~~MOD~~	~~SRG modulation source~~
MRK	marker
MTA	microwave transition analyzer
MTBF	mean time between failures
MUX	multiplexer
~~NOM~~	~~nominal~~
OCD	open-collector driver

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ORD	Operational Requirements Document
PAM	phase-angle modulation
~~PCI~~	~~Peripheral Component Interface~~
PECL	positive ~~emitter~~ ~~emmitter~~ -coupled logic
~~PGEN~~	~~pulse generator~~
PH	phase
PM	pulse (or phase) modulation, power meter
~~Prog~~	~~programmable~~
~~PS~~	~~power supply~~
PSW	power switch
~~PXI~~	~~PCI Extensions for Instrumentation (compact PCI format)~~
RAF	Royal Air Force
~~ResLoad~~	~~resistive load~~
RF	radio frequency
RFI	receiver fixture interface
RSIA	raster stroke image acquisition
SAMe	sistema automatico de mantenimiento estandar
Spec	An spectrum analyzer
STA	system trigger assembly
~~Std~~	~~Standard~~

Sync	synchronizer
Sys	system
TETS	Third Echelon Test System ^{8 9}
TPS	test program set
Trig	trigger
TSP	twisted shielded pair
TTL	transistor-transistor logic
UBIC	universal bus interface controller
~~USB~~	~~Universal Serial Bus~~
UUT	unit under test
VSWR	voltage standing wave ratio
WG	Working Group
~~VGA~~	~~Versatile Graphics Adapter~~
~~VME~~	~~versa-module extended~~
~~VXI~~	~~VME extended for instrumentation~~

^{8 9} U.S. Marine Tester, AN/USM-657 (V)1, (V)2, (V)3.

4. Common test interface requirements

4.1 Introduction

The information following subclauses and illustrations provided in 4.2 to 4.11 describe the requirements for this ~~trial-use standard, IEEE Std 1505.1-2008,~~ to support military/aerospace test requirements. This information is supplemental and not stand alone and shall coexist with that presented in the ~~IEEE Std 1505~~ RFI specifications, Clause 1 through Clause 6, of IEEE Std 1505.⁹

This ~~The IEEE 1505.1~~ standard for the use of IEEE 1505 RFI to support military/aerospace test requirements represents a higher order subset of cost/physical/signal performance requirements to meet specific industry and defense agency goals of a common test interface (CTI). These high-order requirements expand on the following previously defined RFI: 1(a) framework and 2-(b) connector modules and respective contacts; to meet objectives for 3-(e) a common scalable pin map configuration; 4(d) switching; and 5(e) legacy automatic test system (ATS) transitional device for third echelon test system ~~Third Echelon Test System~~ (TETS), Consolidated Automated Support System (CASS), Integrated Family of Test Equipment (IFTE), and others as deemed necessary by the cognizant agencies. This is intentionally done to standardize the footprint and assure mechanical and electrical interoperability between past and future ATS.

4.2 Common test interface ~~CTI~~ open-system requirements

4.2.1 Best practice ~~Government~~ “open-systems ~~system~~” policy

Military/aerospace companies prefer ~~On 29 November 1994, the Honorable Paul G. Kaminski, Under Secretary of Defense for Acquisition and Technology, directed acquisition executives in the DoD to~~ use “open-systems” specifications and standards (electrical, mechanical, thermal, etc.); for acquisition of all weapon systems ~~electronics~~ to the greatest extent practical. The use ~~Open-Systems Joint Task Force (OS JTF) was formed in September 1994 to: “Sponsor and accelerate the adoption of~~ open systems accelerates delivery of primary and secondary products reducing in weapons systems and subsystems electronics to reduce life-cycle costs (LCCs ~~LCC~~) and facilitates ~~facilitate~~ effective weapon system intra- and interoperability.”

⁹ Information on references can be found in Clause 2.

4.2.2 Common test interface **CTI** “open” architecture

Rule 4.2.2: An open standard CTI *architecture* shall identify components, the relationship between components, and the rules for the architecture’s composition.

Recommendation 4.2.2: Typical guidelines for addressing the CTI architecture should include the following:

- a) ~~Define and describe~~ A system architecture is defined and described that is traceable to the Operational Requirements Document (ORD).
- b) A preferred architecture is modular, hierarchical, and layered, and it is based on open standards at its interfaces.
- c) The selection of an architecture shall be a cooperative process between government and industry.
- d) ~~Specify~~ Key performance attributes of system building blocks shall be specified, including internal interface standards.
- e) Where a new system is contemplated, consensus among potential contractors and their key suppliers on application of widely accepted standards is desirable.
- f) ~~Identify~~ Aspects of the program shall be identified that might limit the use of an open-systems approach.
- g) ~~Determine~~ The level at which the architecture will be defined shall be determined for the system.
- h) The architecture approach resulting from a system engineering process shall be linked to a business case analysis.
- i) Decisions about the architecture shall be linked to performance, LCC, schedule, and risk.

- j) ~~Identify~~ Opportunities for reuse of hardware and software configuration items and dependence ~~on~~ ~~upon~~ interfaces shall be identified.

4.3 Common test interface ~~CTI~~ cost requirements

Recommendation 4.3a: Fundamental to the implementation of the CTI recommended practice should be the paramount need to address design-to-costs (DTCs ~~DTC~~) and LCCs ~~LCC~~ attributed to test interface and TPS requirements.

Recommendation 4.3b: CTI should improve the test acquisition process by creating a competitive multivendor environment that provisions common module components that can be procured as COTS, at pricing that benefits from industry economics-of-scale production/quality processes, and improved time-to-market availability.

Recommendation 4.3c: CTI should meet advanced functional and technological needs through shared industry research and development, ~~R&D~~, multifunctional/virtual modules that can be replicated, distributed, and reconfigured to meet a broad set of applications without customization. Extend legacy system life through technology insertion of plug-and-play enhancements based ~~on~~ ~~upon~~ standardized infrastructure, and related cost-avoidance of ATS obsolescence.

Recommendation 4.3d: CTI should minimize configuration variations and related software customization and adjustments between unique test assets, integration methods, and signal routing schemes.

Recommendation 4.3e: CTI should promote cooperative design, design reuse, shared design data models, automation in software development, rehostability and portability of TPSs, implementation of lessons learned, and enhanced ~~enhance~~ long-term support between vendors, integrators, and users. Standards also promote common fabrication processes, signal routing schemes, and canned solutions that could reduce TPS engineering integration time and cost.

4.4 Vertical integration test support requirements

Recommendation 4.4: The ~~implementation of the~~ CTI/RFI standard ~~should be implemented as a~~ as common *vertical integrated test support* ~~system building block~~ through the product cycle and various maintenance levels ~~to assure~~ assures the greatest benefits of common system implementation and cost savings. Specific benefits include the shared development/manufacturing of ATS and TPS assets, enhanced TPS verification and refinements, and transitional improvements in lessons learned, hands-on training, and asset management.

4.5 Common test interface ~~CTI~~ configuration/interoperability requirements

Recommendation Rule 4.5a: CTI *pin map requirements*, as defined by Clause 4 ~~general pin map requirements in Annex A~~, and Annex A of IEEE Std 1505, ensure compliant implementations ~~subsequent detailed CTI pin map input/output (I/O) configuration, shall be implemented~~ to assure test interface interoperability between agencies and ATS configurations.

Observation Recommendation 4.5a: A common CTI pin map configuration, described in Annex A of IEEE Std 1505 has been recommended across government multiagencies, to stimulate greater use of common assets, which reduces proliferation and support duplication. ~~By satisfying interoperability requirements between government agencies TPS development, deployment and asset duplication can be eliminated and related weapon system support enhanced.~~

4.6 Maintainability/end-user support requirements

Rule 4.6: ~~The general pin map requirements in Annex A, and subsequent detailed CTI pin map I/O configuration, as part of this IEEE 1505.1 CTI document, shall be maintained/upgraded through IEEE standards revision processes.~~

Recommendation 4.6: ~~The CTI implementation within~~ Industry and ~~the~~ government adopters of this standard should manage the CTI pin map configurations at their respective discretion, utilizing CTI standard product configurations, multivendor interchangeable parts, calibration, and maintenance support as described herein ~~is recommended~~.

Observation 4.6: Applying common CTI products to ATS and CTI fixture deployment would dramatically reduce duplicative requirements for unique system development, validation, production, deployment, configuration product management, and long-term support. This approach would further enhance asset availability/uptime mean time between failures (~~MTBFs~~ ~~MTBF~~), calibration/spares consolidation, and mean-time-to-repair (MTTR) results. Users could also benefit from common maintenance practices, tooling, and training costs. Furthermore, CTI implementation would ~~also~~ focus product management/feedback on a smaller number of unique installed systems, their related failures/lessons learned, and iterative improvements, resulting in improved reliability, less obsolescence, and longer life cycles.

4.7 Scalable ~~Scaleable~~ architecture requirements

4.7.1 Overview

Rule 4.7.1: CTI shall support modular and scalable ~~scaleable~~ concepts as illustrated in Figure 1 of this standard. Based on ~~upon the~~ IEEE Std 1505 ~~RFI standard~~, CTI shall support upward scalable compatibility without modification or added extensions of a low-end (four ~~4~~-slot CTI configuration), midsized ~~and a mid-sized~~ (20-slot CTI configuration), and ~~to a~~ high-end (29-slot CTI configuration) test system capability.

Observation 4.7.1: Scalability—“Serves to minimize or eliminate the costs of fixturing by scaling the requirements to minimum framework and related pin map configuration. This minimizes the size, storage requirements, and complexity of fixturing, as well as the related receiver and fixture(s) costs, to only what is necessary to interface the unit under test (UUT) to the ATS (e.g., a cable assembly can be plugged into the receiver without a fixture box being applied). This also permits an avionics board manufacturer to develop a compatible TPS for factory test and allow for the ~~Government to utilize that~~ same fixture to be utilized on the high-end depot tester without modifications/adapters. Such capabilities demand that the mechanism support engagement actuators at incremental points to pull smaller fixtures into the receiver.”

4.7.2 General building block architecture

Rule 4.7.2: CTI shall support a scalable building block architecture with [a](#) common I/O pin map that remains upwardly compatible with [the](#) matched connector/contact configuration and scalable application levels described in Table 1 [of this standard](#).¹⁰

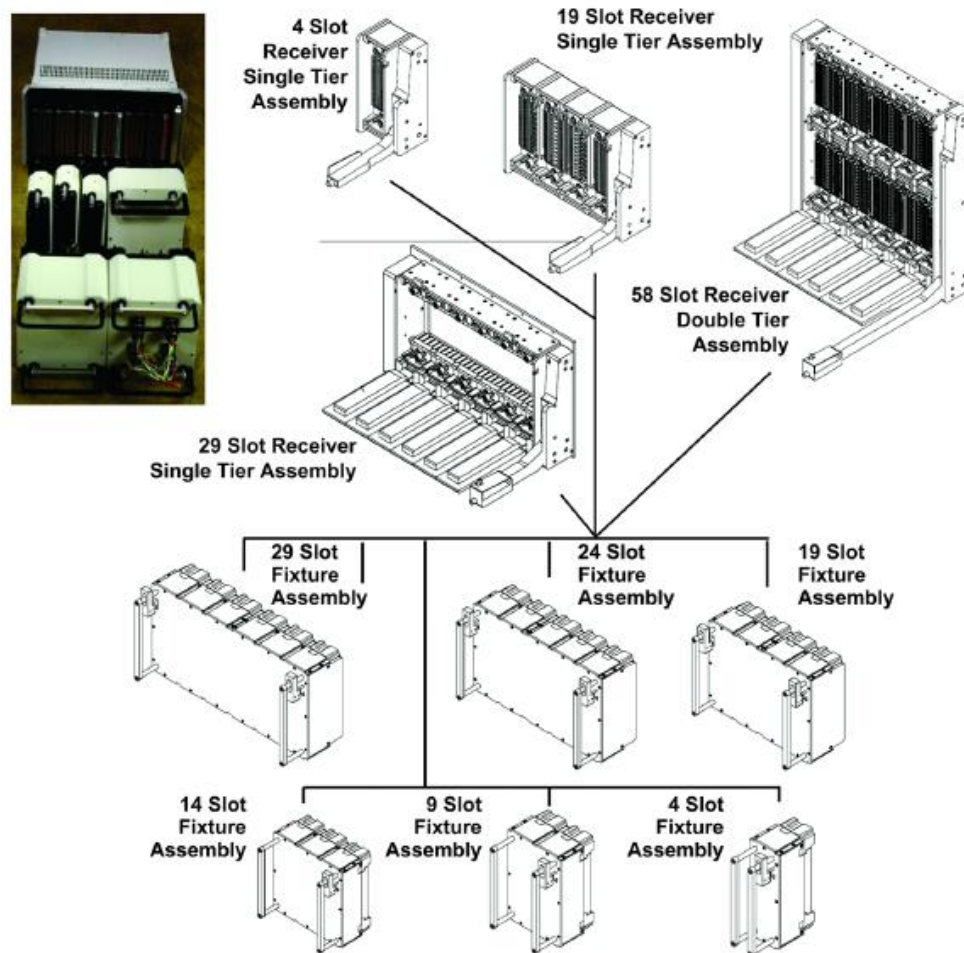


Figure 1—[Common test interface](#) **CTI system receiver modular scalable framework architecture**

¹⁰ Notes in text, tables, and figures of a standard are given for information only and do not contain requirements needed to implement this trial-use standard.

4.8 Physical framework requirements

4.8.1 IEEE 1505 RFI standard compliance

Rule 4.8.1: The CTI shall be fully compliant with IEEE ~~Std~~—1505 RFI standard framework specifications, [as outlined in](#) Clause 5 [of IEEE Std 1505](#), expandable to two tiers, to a maximum of 29 slots per tier (26 slots usable for connector mounting; ~~z~~ see Figure 2 and Figure 3 [of this standard](#)).

Table 1—[Common test interface](#) ~~CTI~~ building block suggested configuration

Worst case: High-end test system application—26 connector slots/3 blanks	
Signal contacts:	3200 pos, 0-3 A/200 pos module
Lo/hi power contacts:	270 pos 23 A/152-59 pos
Lo/hi coax contacts:	363 pos 3 GHz/152-59 pos
Typical: Midrange test system application—18 connector slots/2 blanks	
Signal contacts:	2800 pos, 0-3 A/200 pos module
Lo/hi power contacts:	211 pos 23 A/152-59 pos
Lo/hi coax contacts:	59 pos 3 GHz/152-59 pos
Basic: Low-end test system application—4 connector slots	
Signal contacts:	600 pos, 0-3 A/200 pos module
Lo/hi power contacts:	59 pos 23 A/152-59 pos
Lo/hi coax contacts:	0 pos 3 GHz/152-59 pos
NOTE—pos = position (interchangeable with term <i>contact</i> in this context).	

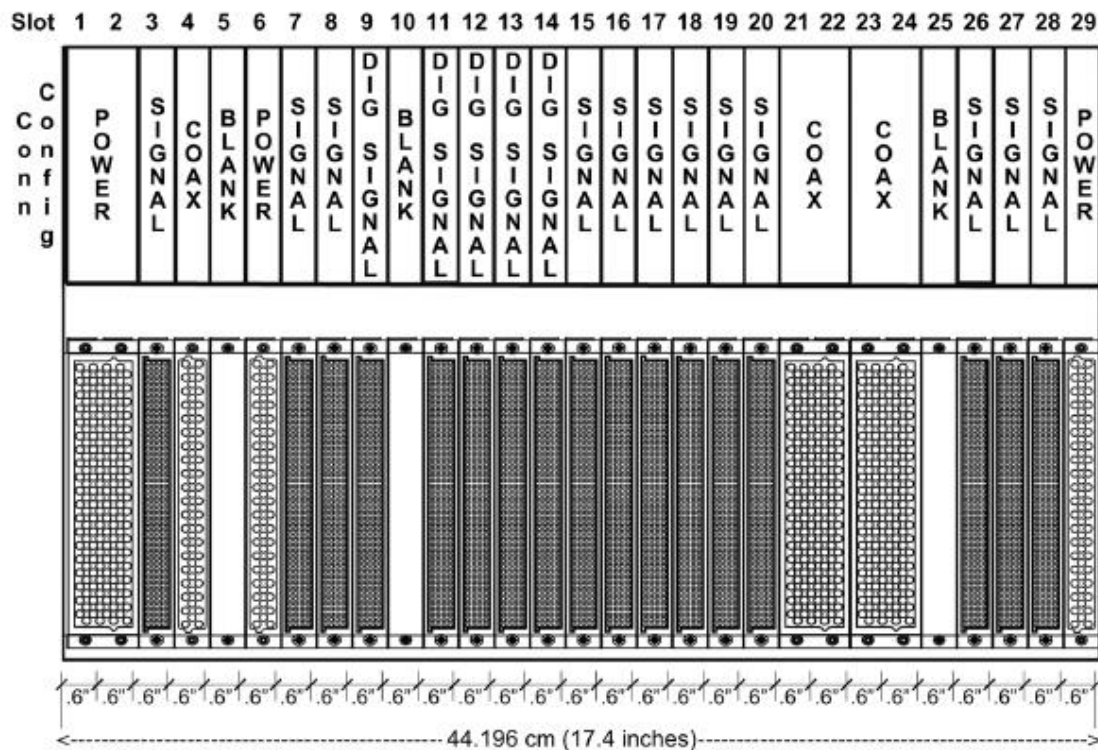


Figure 2—[Common test interface](#) **CTI** system 29-slot receiver connector configuration

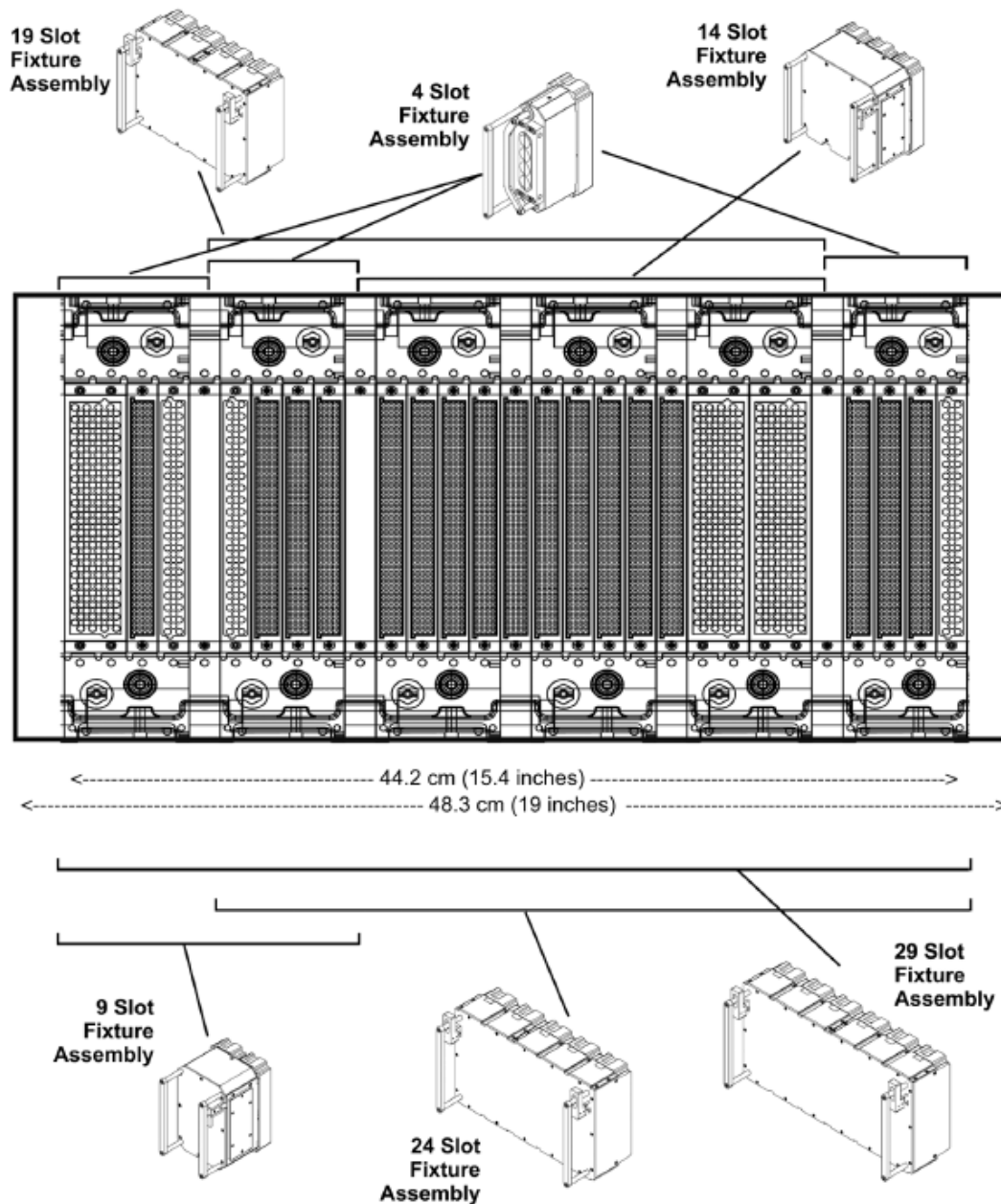


Figure 3—[Common test interface CTH](#) system configuration to fixture options

4.8.2 Common test interface ~~CTI~~ modular combination framework design

Rule 4.8.2: Under IEEE ~~Std~~-1505 *combination framework specification* (detailed in the RFI framework specification, Clause 5 of IEEE Std 1505), the CTI *framework* shall provision three ~~(3)~~ blanks at slots ~~slot~~ 5, 10, and 25 to provision a 1.524-cm (0.6-in) spacing for the protective shrouds of two adjoining fixtures.

Permission 4.8.2: The combinational framework requirement can be implemented in one ~~any~~ of two methods: 1) by ~~(a)~~ combining *segmented and continuous framework* (illustrated in Figure 6 of this standard), to form a 29-slot configuration made up of three ~~(3)~~ segmented 5.6-cm (3-in) wide frames, with four ~~(4)~~ connector slots each, and one ~~(1)~~ continuous 22.9-cm (9-in) wide frame, which that supports ~~fourteen~~ ~~(14)~~ connector slots that support ~~supports~~ frame/blank spacing at slots 5, 10, and 25; or 2) by ~~(b)~~ modifying a 29-slot continuous framework (illustrated in Figure 5 and Figure 6 of this standard); to provision three blanks at slots 5, 10, and 25.

4.8.3 Common test interface ~~CTI~~ receiver footprint/scalable ~~scaleable~~ requirements

Rule 4.8.3a: The CTI receiver framework footprint shall be a scalable ~~scaleable~~ combinational implementation that can be incremented from the smallest footprint of a segmented framework of four ~~(4)~~ connector slots; and expandable to 29 slots by adding segmented and/or continuous framework intervals, while maintaining downward compatibility with any smaller fixture increments (26 slots for connectors and 3 slots for shroud spacings). Either of the framework implementations can be reduced to any interval segmented at slots ~~slot~~ 5, 10, and 25 with combinations that can support 4, 8, 14, 18, or 22 slots usable for connector mounting. All connector configurations shall satisfy the IEEE ~~Std~~-1505 framework/connector specifications, outlined in Clause 5 and Clause 6 of IEEE Std 1505, and CTI pin map I/O configuration and general pin map requirements, outline in Annex A of IEEE Std 1505.

Rule 4.8.3b: [The](#) physical footprint of the CTI *receiver framework* shall be in accordance with framework specification, Clause 5 [of IEEE Std 1505](#), that describes receiver framework under IEEE ~~Std~~ 1505 segmented and continuous framework layouts, as the examples in Figure 4 and Figure 6 [in this standard](#) further illustrate. Although the receiver drive system implementation is supplier dependent, the CTI receiver mechanical drive system shall not extend beyond the dimensional envelope of a standard 48.3-cm (19-in) rack width or height of 35.6 cm (14 in) (including handle height).¹¹

Rule 4.8.3cd: [The](#) overall physical size of each CTI *receiver tier*, including drive assemblies, shall not exceed [the](#) standard 19-in equipment rack width in accordance with EIA/ECA-310-E (2005) [~~B3~~ [B4](#)],¹¹ or 35.56-cm (14-in) height, or protrude from the mounting plate more than 8.89 cm (3.5 in).

Observation Rule 4.8.3ae: The CTI specification permits integrators or users to add [an](#) incremental receiver framework, anytime~~7~~, to satisfy any [mixture](#) ~~mix~~ of fixture requirements, as shown in Figure 1 and Figure 3 [of this standard](#), [which](#) ~~that~~ includes multiple tier increments (two tier shown in Figure 1), in accordance with the CTI pin map I/O configuration and general pin map requirements [outlined in](#)~~7~~, Annex A [of IEEE Std 1505](#).

4.8.4 [Common test interface](#) ~~CTI~~ receiver physical weight requirements

Rule 4.8.4: [The](#) physical weight of the CTI receiver framework shall not exceed a maximum of 5.63 kg (8.0 lb) per 7.62-cm (3-in) frame interval and 21.8 kg (48.0 lb) for each CTI 29-slot tier, including fully populated connector modules and the engagement mechanism.

4.8.5 [Common test interface](#) ~~CTI~~ mechanical engagement requirements

Rule 4.8.5: The CTI *receiver mechanical engagement system* shall be in accordance with framework specification, [Clause 5 of](#) IEEE Std 1505~~, Clause 5~~, and provide sufficient mechanical advantage to overcome the physical mating insertion force of a fully-populated interface and the cantilevered fixture weight requirements, [as well as](#) ~~and~~ apply sufficient mechanical advantage to assure a 15.9 kg (35 lb) of handle force is not exceeded.

¹¹ [The numbers in brackets correspond to those of the bibliography in Annex B.](#)

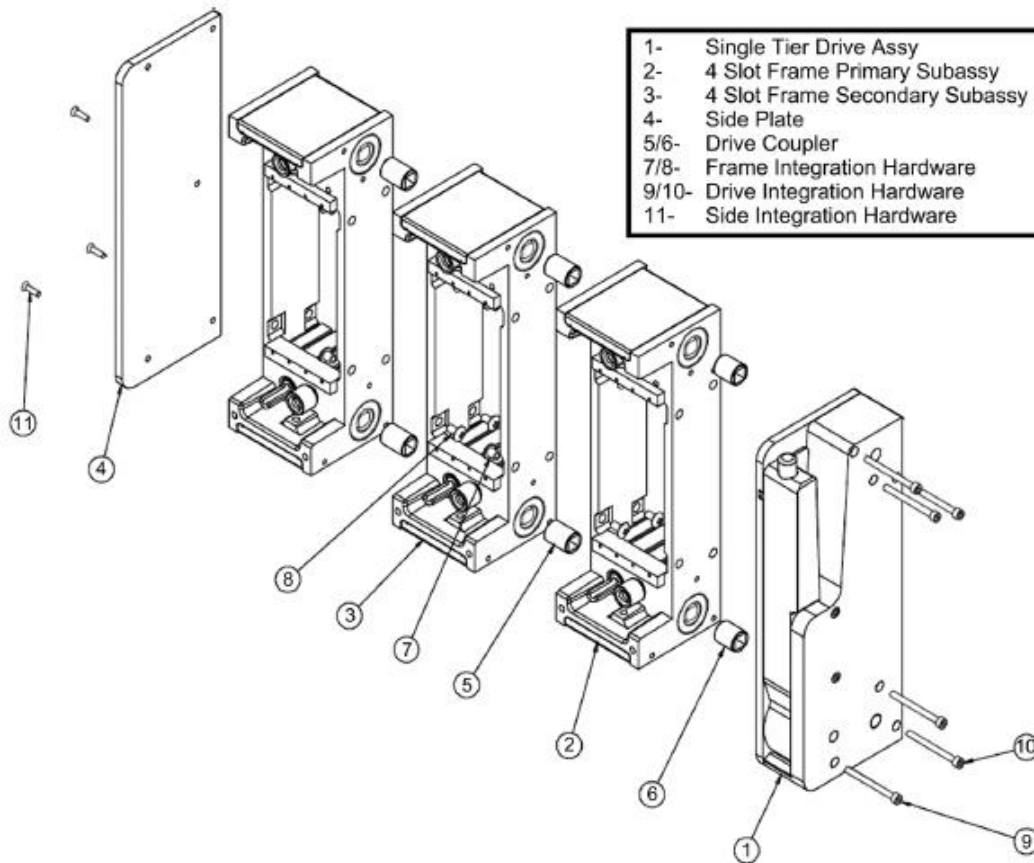


Figure 4—IEEE 1505 receiver segmented framework example

4.8.6 Common test interface ~~CTI~~ fixture weight requirements

Rule 4.8.6: Each CTI receiver 4-slot *frame increment* shall support a maximum static fixture weight (fixture fully engaged to receiver) of 4.54 kg (10 lb) cantilevered at 38.1 cm (15 in) from the receiver mating interface while meeting life-cycle, interface insertion force, and electrical parametric requirements. In increments of 4.54 kg (10 lb) per 7.62-cm (3-in) frame interval, a CTI 29-slot receiver with six frame intervals shall support a maximum of 22.68 kg (50 lb) at 38.1 cm (15 in).

NOTE—Implementers/users are recommended to ~~shall~~ provide additional safety support to assist operators during lift, as well as to ~~and~~ prevent injury or damage to equipment, when engaging/disengaging heavy fixture applications.

4.8.7 Oversized fixture keep-out area

Rule 4.8.7: Fixture manufacturers that offer large (oversize) fixture footprints shall not intrude on the dimensional areas annotated in Figure 5 [of this standard](#).

Observation 4.8.7: The area to the right is reserved for operation of the engaging handle. The area below the fixture is reserved for fixture support facilities.

CAUTION

Manufacturers should be cognizant of cantilevered weight and other surrounding interference factors that may impact implementation when standard footprints are exceeded.

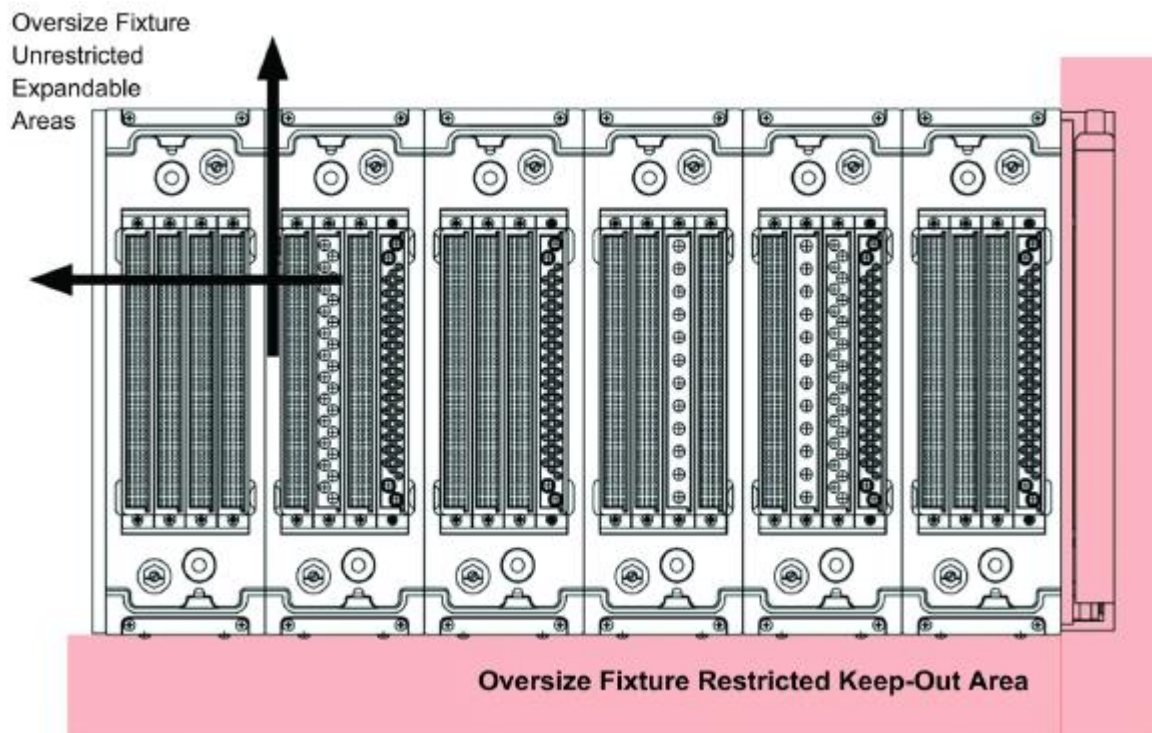


Figure 5—Fixture ([interface test adapter](#) **ITA**) footprint restricted areas

4.8.8 Transportability/mobility requirements

Rule 4.8.8: CTI shall meet transportability/mobility requirements per the IEEE ~~Std~~-1505 RFI environmental/quality specifications, defined in Clause 4 and Clause 5 of [IEEE Std 1505](#) ~~the standard~~. A fully assembled CTI (framework, connector modules, contacts, and engagement mechanism) shall withstand ~~a~~ 5 ms of 49 m/s for shock drop test [force](#).

Observation: 4.8.8: The intent of the drop test is to ensure the assembled interface does not deform or otherwise become unusable if it is “dropped” during assembly or repair. The condition of this test includes the interface as a stand-alone object, impacted on all corners and [facing faces](#) ~~at a~~ 5 ms of 49 m/s for shock drop test force.

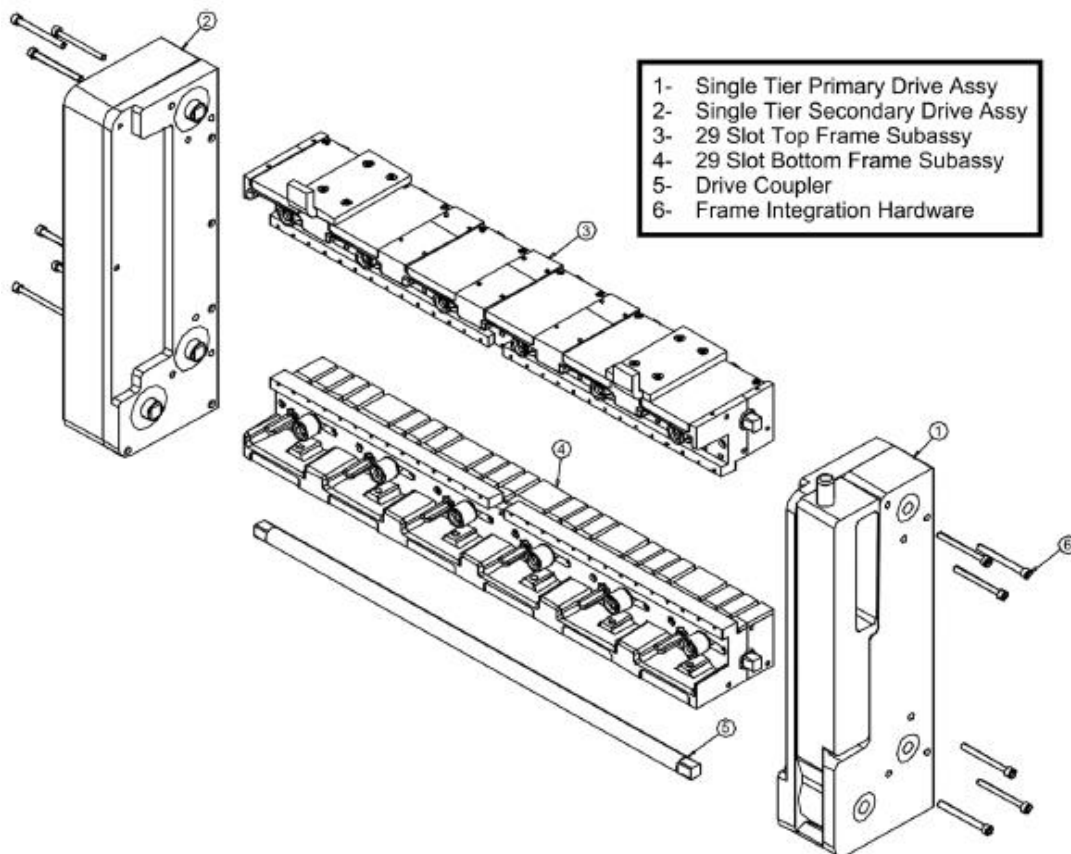


Figure 6—IEEE 1505 receiver continuous framework example

4.9 Reliability requirements

4.9.1 Repeatability/reproducibility/interchangeability

Rule 4.9.1: CTI design shall conform to dimensional and functional requirements defined in IEEE ~~Std~~-1505 RFI environmental/quality specifications, described in Clause 5 and Clause 6 [of IEEE Std 1505](#), ~~in order~~ to assure component part interchangeability/intermateability and interoperability between components from multiple vendors. Component parts shall remain “operational” [throughout the](#) ~~through~~ life of the program. Any part changes that affect form, fit, or function cannot obsolete existing parts.

4.9.2 Mean time between failures requirements

Rule 4.9.2: CTI components shall be designed and produced to perform without failure between established durability/life-cycle requirements. Failures shall be assessed to determine cause and corrective actions. MTBF data for the CTI components shall be calculated in accordance with MIL-HDBK-217 [\(1992\)](#) [\[B20\]](#) ~~[B21]~~.

4.9.3 Durability and [life](#) cycle~~life~~

Rule 4.9.3: Durability and [life](#) cycle~~life~~ for CTI receiver/fixture mechanism shall have a minimum durability rating of 25 000 cycles. Connector module contacts shall have a minimum durability rating of 10 000 cycles. Cycle limits are considered end of life requiring replacement of wearable items. Manufacturers shall validate conformance to this specification in accordance with the IEEE ~~Std~~-1505 RFI qualification requirements, [as outlined in](#) Clause 4, cycle testing, and per framework specifications [in](#) Clause 5 [of IEEE Std 1505](#).

4.10 Common test interface ~~CTI~~ connector footprint/parametric requirements

4.10.1 IEEE 1505 RFI standard compliance

Rule 4.10.1a: CTI shall be compliant with the IEEE ~~Std~~ 1505 RFI standard connector specifications, Clause 6 of IEEE Std 1505, that establishes the Eurocard Deutsches Industrie Normal (DIN) standard connector footprint as the basis of CTI architecture.

~~**Observation 4.10.1:** Both commercial and ruggedized versions (under MIL-C 55302/179-180 [B20]) were available in a 200-pin, 4-row connector by two of the three primary interface suppliers. Signal module meets the highest levels for open-system, low-cost, performance, COTS acceptance, and level of applicability, receiving more than 25% higher grade over any of the other connectors reviewed.~~

Rule 4.10.1b: CTI shall implement three DIN connector types: 1(a) signal; 2(b) power; and 3) radio frequency (e)-RF) coax; as defined in IEEE-~~Std~~ 1505 RFI standard connector specifications, Clause 6, and related connector specifications, Clause 7 through Clause 12, of IEEE Std 1505.

4.10.2 Common test interface ~~CTI~~ requirements for compliance

Rule 4.10.2: Suppliers of systems shall state their degree of compliance to this standard ~~IEEE Std 1505.1~~ using the definitions of compliance in 4.10.2.1 and 4.10.2.2.

4.10.2.1 Mechanical compliance

Rule 4.10.2.1: To meet this criterion ~~criteria~~, a manufacturer shall at the minimum supply an IEEE 1505 RFI compliant interface that conforms to a connector per slot type that matches the configuration shown in Figure 2 of this standard. That is, the power connector is used in slots 1 and 2 ~~slot 1/2~~, the 200-pin signal module in slot 3, and so on ~~etc.~~

Observation 4.10.2.1: This level of compliance only ensures that physical connector damage will not result from installing a fixture (ITA/ID) from one minimum-level compliant system onto a different minimum-level compliant system's receiver. It does *not* ensure that the proper signals will be routed.

4.10.2.2 Full compliance

This is the highest degree of compliance and requires full slot-by-slot mechanical and electrical compatibility for the stated compliance categories defined as follows.

Rule 4.10.2.2a: To state full compliance, a manufacturer shall meet all the requirements for the signals for each slot as identified in Annex A [of this standard](#), except for the columns labeled "Recommended attributes." Non-populated modules should be blank (e.g., if block is "blank," it can be keyed normally; if [a](#) block has [a](#) different pin out, it shall be keyed differently). Both the full compliance and the ~~following~~ category shall be stated.

The ~~following are the~~ defined categories [are as follows](#):

- a) Category 1—This is defined as mechanically and electrically compliant with ~~the Annex A~~ slots 6 through 9 [of Annex A of IEEE Std 1505](#). This is the basic *stimulus-measurement* section of the pin map.
- b) Category 2—This is defined as mechanically and electrically compliant with ~~Annex A~~ slots 1 through 9 [of Annex A of IEEE Std 1505](#). This is the basic stimulus-measurement plus power supplies and switching of the pin map.
- c) Category 3—This is defined as mechanically and electrically compliant with ~~Annex A~~ slots 6 through 24 [of Annex A of IEEE Std 1505](#). This is the basic stimulus-measurement plus digital, switching, and additional analog of the pin map.
- d) Category 4—This is full slot compliance (mechanical and electrical) for slots 1 through 24 of the [pin map in Annex A of IEEE Std 1505](#) ~~pin map~~.
- e) Category 5—This is full slot compliance (mechanical and electrical) for all 29 slots of the [pin map in Annex A of IEEE Std 1505](#) ~~pin map~~.

NOTE—Partially compliant approaches ~~should~~ ~~shall~~ rotate keys 180°-degrees to ~~ensure~~ ~~insure~~ that physical and/or electrical damage ~~does~~ ~~is~~ not ~~occur~~ ~~incur~~.

Observation 4.10.2.2: This level of compliance ensures both mechanical compatibility between systems *and* electrical signal compatibility/interoperability between systems for the slots included in the categories. The categories represent scalable increments based on the segmented architecture and on the electrical signals included in the scalable options.

Permission 4.10.2.2a: Pins may also have lesser or higher capability as identified in the tables in Annex A of IEEE Std 1505 ~~tables~~ as long as the pin mapping of Annex A is met and the capability is of the same/similar functionality. For example, an identified dc power supply (DCPS) capability identified in Annex A of IEEE Std 1505 should be matched with a DCPS, not with an ac supply.

Permission 4.10.2.2b: The designer of a compliant system is allowed to implement the capability identified in Annex A of IEEE Std 1505 with nonclassical instruments.

4.10.3 Standardized keying

A standardized keying arrangement is required to support the compliant interfaces. Each 4-slot section of the IEEE 1505 RFI interface has a top and bottom key as shown in Figure 7 of this standard. Each key is set in a hexagonal socket that allows one of six rotational positions. Therefore, with the top and bottom key being independently variable, the keying of one 4-slot segment can have one of 36 different keying arrangements.

Rule 4.10.3a: Systems (receivers and ITAs) that implement a mechanically or fully compliant interface as defined in 4.10.2 of this standard and subparagraphs shall implement the keying as shown in Figure 7.

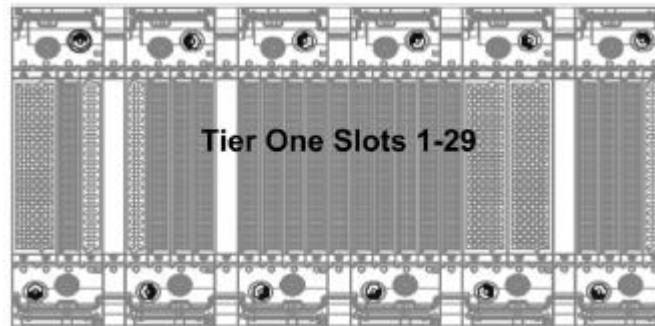


Figure 7—Standardized keying for compliant systems (receiver view)

Rule 4.10.3b: Systems that have segments that are noncompliant per the definition of 4.10.2 [in this standard](#) shall implement a different keying option. The option used shall *not* duplicate any of the keying options shown for a compliant interface for any section. The goal is to *prevent* any ability to mount a compliant ITA on any noncompliant receiver or a noncompliant ITA on [any](#) ~~⌘~~ compliant receiver.

4.10.4 Population policy

[Recommendation](#) **Rule 4.10.4a:** A test system developer shall follow a set order of precedence in the selection of test assets and the associated pins from the pin map. The following process [should](#) ~~shall~~ be followed:

- a) Identify an unused test asset/instrument that meets the *minimum* test requirements.
- b) If the asset/instrument is part of a group of like-capability assets, use the lowest numbered, available (unused) asset for the test.
- c) Proceed in like fashion for the entire group of similar assets
- d) If the *minimum* required capability assets become completely used (implemented) in the TPS, proceed to utilize the next highly capability asset/instrument.

- e) If this asset/instrument is part of a group, follow the same rules in which the lowest numbered is utilized first.

Recommendation Rule 4.10.4b: A TPS developer shall follow a set order of precedence in the selection of test assets and pins from the pin map. The following process ~~should~~ **shall** be followed:

- a) Select an unused test asset/instrument that meets the minimum requirements for the test.
- b) If the asset/instrument is part of a group of like-capability assets, use the lowest numbered, available (unused) asset for the test.
- c) Proceed in like fashion for the entire group of similar assets
- d) If the *minimum* required capability assets become completely used (implemented) in the TPS, proceed to utilize the next highly capability asset/instrument. These should also be implemented from lowest numbered asset to higher numbered asset.
- e) If this asset/instrument is part of a group, follow the same rules in which the lowest numbered is utilized first.

~~**Recommendation 4.10.4:** Refer to Annex A tables for clarification of asset capabilities and how assets are numbered.~~

4.10.5 Common test interface ~~CTI~~ connector parametric requirements

Rule 4.10.5: The CTI connector module with contacts shall comply with the definitions contained in IEEE ~~Std~~ 1505 RFI connector specifications, Clause 6, and related connector specifications, Clause 7 through Clause 12 of IEEE Std 1505, that satisfies the respective parametric requirements defined by Table 2 in this standard.

Table 2—[Common test interface CTH](#) connector module/contact module performance requirements

Signal contact/module	
Operating voltage	300 Vdc max
Operating current	3.0 Adc continuous
Contact resistance	10 m Ω max
Insulation resistance	5.0 $\times$ 10e9 Ω min
Capacitance	10 pF max
Reliability	10 000 engagement cycles min
Footprint	0.025 in square pins on 0.1 in centers arranged in 4 row $\times$ 50 pin multiples
Mating force	2.0 oz/pin max
Module footprint	200 positions in 4 columns
Power module/contact	
Operating voltage	300 Vdc max
Operating current	23 A dc/ac rms continuous/free stdg/ambient air
Contact resistance	5 m Ω max
Characteristic imped	n/a
Insulation resistance	5.0 $\times$ 10e9 Ω min
Capacitance	10 pF max
Reliability	10 000 engagement cycles min
Contact	Size 16 DIN requirements
Mating force	18 oz/pin max
Module footprint	59 positions in 3 columns, or 152 positions in 8 columns

Table 2—[Common test interface CTI](#) connector module/contact module performance requirements (*continued*)

Coax module/contact	
Frequency bandwidth	dc 3 GHz
Operating voltage	150 V ac, rms
Contact resistance	10 mΩ max
Voltage standing wave ratio (VSWR)	1:1.22 + 0.52 f (GHz)
RF insertion loss	0.03√f (GHz)
RF leakage	– 90 dB at 2.5 GHz
Contact resistance	Center contact; straight 6.0 mΩ max
Crosstalk	Less than or equal to – 90 dB to 2 GHz
Characteristic imped	50 ± 2 Ω
Insulation resistance	1000 MΩ min
Capacitance	15 pF max
Reliability	10 000 engagement cycles min
Contact	Size 16 DIN requirements
Mating force	18 oz max
Module footprint	59 positions in 3 columns or 152 positions in 8 columns

4.11 [Common test interface CTI](#) pin map requirements

4.11.1 [Common test interface scalable CTI-sealeable](#)/modular pin map configuration

Rule 4.11.1a: The CTI [scalable sealeable](#) pin map configuration shall support scalability (the use of less than a full tier interface as previously discussed in 4.8.3 [of this standard](#)), through the distribution of station resources as defined in CTI pin map I/O configuration and general pin map requirements, [as outlined in](#) Annex A [of IEEE Std 1505](#).

Rule 4.11.1b: The CTI configuration shall apply the five ~~(5)~~ connector modules: ~~1(a)~~ signal, single slot 200 position; ~~2(b)~~ power, single slot 59 position; ~~3(e)~~ power, double slot 152 position; ~~4(d)~~ RF coax, single slot 59 position; and ~~5(e)~~ RF coax, double slot 152 position; in the configuration shown in Figure 2 of this standard, and in accordance with IEEE 1505 RFI connector specification, connector specifications, Clause 7 through Clause 12 of IEEE Std 1505.

Rule 4.11.1c: The CTI configuration shall be implemented in intervals conforming to framework segmentation in accordance with IEEE 1505 RFI framework specification, Clause 5 of IEEE Std 1505, that supports mounting of connector types in intervals of ~~four (4_L)~~, ~~four (4_L)~~, ~~fourteen (14_L)~~, and ~~four (4)~~ slots, or any reduced footprint, as determined by the specific application.

4.11.2 CTI pin map I/O categories

~~**Rule 4.11.2:** The CTI connector configuration, as illustrated in Figure 2, shall be implemented in accordance with detailed CTI pin map I/O configuration and general pin map requirements, Annex A. These requirements shall be divided into several I/O parametric categories, described as follows, and distributed in scaleable segments, to assure test signal mapping is maintained for all CTI applications.~~

~~The following describes the general pin map categories:~~

- ~~a) Digital I/O~~
- ~~b) Analog instrumentation~~
- ~~c) Programmable ac/dc load~~
- ~~d) Programmable ac/dc power supplies~~
- ~~e) Bus I/O~~
- ~~f) Switching implementation~~

4.11.2.1 Digital I/O

Rule 4.11.2.1a: ~~CTI shall implement a scaleable digital I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A.~~

Rule 4.11.2.1b: ~~CTI digital I/O shall be applied utilizing Eurocard DIN/MIL-DTL-55302/180 4 row 200 position connector design specifications in accordance with IEEE Std 1505 RFI standard connector specifications, Clause 7 through Clause 12.~~

Suggestion 4.11.2.1: ~~Digital I/O signal channel may be implemented with 200 discrete wires, 100 twisted pairs, or two pins per channel of precision point to point 50 Ω matched impedance wiring having a bandwidth from dc to 750 MHz to a maximum of 100 channels increments (200 pins), as necessary to meet selected ATE digital requirements.~~

4.11.2.2 Analog instrumentation

Rule 4.11.2.2a: ~~CTI shall implement a scaleable AI (AI) I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A, and subsequent requirements. CTI AI I/O shall be implemented utilizing either the CTI signal or coax connectors as subsequently described.~~

Rule 4.11.2.2b: ~~If implemented, the CTI AI I/O shall apply Eurocard DIN/MIL-DTL-55302/180 4 row 200 position connector design specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12.~~

Suggestion 4.11.2.2: ~~AI I/O signal channel may be implemented with 200 discrete wires, 100 twisted pairs, or two pins per channel of precision point to point 50 Ω matched impedance wiring having a bandwidth from dc to 750 MHz to a maximum of 100 channels increments (200 pins), or as necessary to meet selected ATE digital requirements.~~

Rule 4.11.2.2c: ~~If implemented, the CTI AI I/O shall apply RF coaxial size 16 contact with RF coax size 16 connector module design and wiring specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12.~~

4.11.2.3 Programmable ac/dc load

~~**Rule 4.11.2.3a:** CTI shall implement a scaleable programmable dc load I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A.~~

~~**Rule 4.11.2.3b:** CTI programmable dc load I/O shall be applied utilizing the CTI power connector using 23 amp contact in a 59 or 152 positions power module connector design in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12. These contacts shall be derated to 18 A, when six or more are clustered adjacent to each other and operating simultaneously and continuously at that current level.~~

~~**Suggestion 4.11.2.3:** Discrete 23 amp pins should be implemented with 14 AWG MIL spec (high temperature and flammable resistant) discrete or twisted pair wiring.~~

~~**Permission 4.11.2.3:** CTI programmable dc load I/O where applicable may utilize low level (current ≤ 3 A) discrete I/O signal pins using Eurocard DIN 41612 and MIL C 179/180 5 row 200 position connector design specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12, and the CTI pin map I/O configuration and general pin map requirements, Annex A. Discrete pins may be implemented with 24 AWG discrete or twisted pair wiring.~~

4.11.2.4 Programmable ac/dc power supply

~~**Rule 4.11.2.4a:** CTI shall implement a scaleable programmable dc/ac power supply I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A.~~

~~**Rule 4.11.2.4b:** CTI programmable dc/ac power supply I/O shall be normally applied utilizing the CTI power connector using 23 amp contact in a 59 or 152 positions power module connector design specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 6 and Clause 8. These contacts shall be derated to 18 A, when six or more are clustered adjacent to each other, and operating simultaneously and continuously at that current level.~~

~~**Suggestion 4.11.2.4:** Discrete 23-amp pins should be implemented with 14 AWG MIL-spec (high temperature and flammable resistant) discrete or twisted pair wiring.~~

~~**Permission 4.11.2.4:** CTI programmable dc/ac power supply I/O where applicable may utilize low-level (current ≤ 3 A) discrete I/O signal pins using Eurocard DIN/MIL-DTL-55302/179/180 4-row 200-position connector design specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12. Discrete pins shall be implemented with 24 AWG discrete or twisted pair wiring.~~

4.11.2.5 Bus I/O

~~**Rule 4.11.2.5a:** CTI shall implement a scaleable bus I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A.~~

~~**Rule 4.11.2.5b:** CTI bus capability shall be applied utilizing Eurocard DIN/MIL-DTL-55302/180 4-row 200-position connector design specifications in accordance with IEEE Std 1505 RFI standard connector specifications, Clause 7 through Clause 12.~~

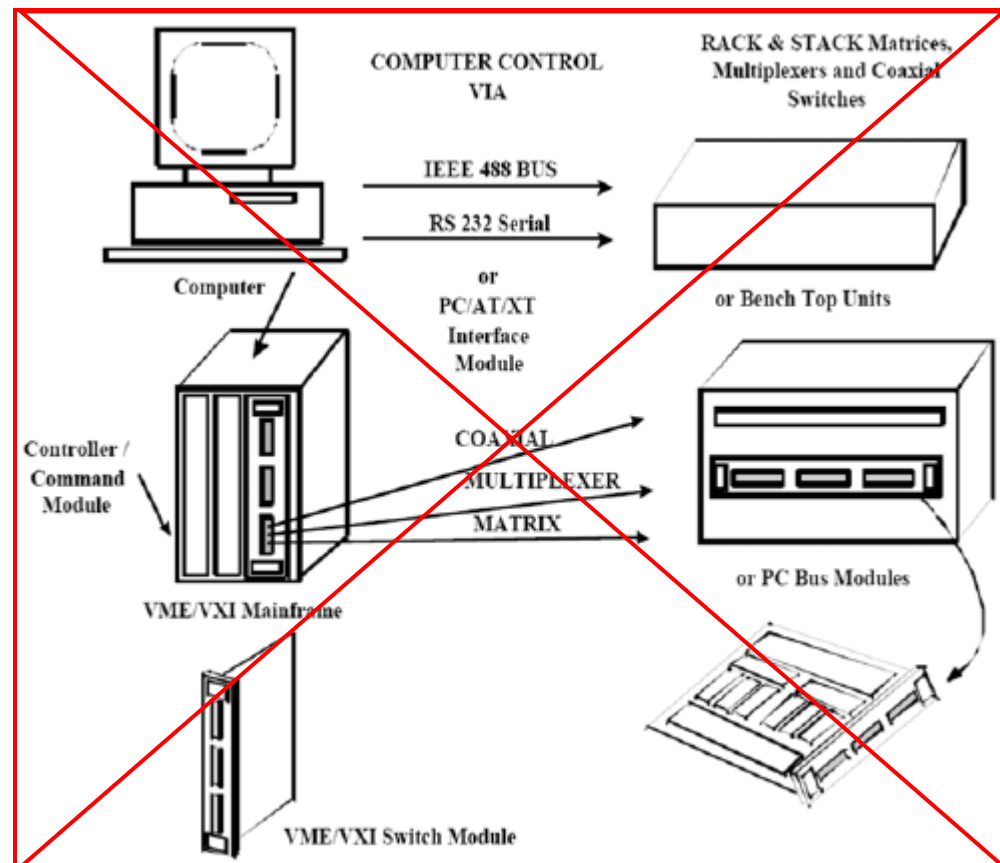
~~**Suggestion 4.11.2.5:** Bus I/O signal channels may be implemented with 200 discrete wires, 100 twisted pairs, or two pins per channel of precision point-to-point 50 Ω matched impedance wiring having a bandwidth from dc to 500 MHz to a maximum of 100 channels increments (200 pins), as necessary to meet selected ATE bus requirements.~~

4.11.2.6 Switching implementation

4.11.2.6.1 General requirements

~~These interfaces describe the hardware requirements necessary to switch stimulus, response, and power signals between the UUT and the test instrumentation. The switching may be implemented in various ways.~~

Observation 4.11.2.6.1: The combination of the switch and CTI I/O provides the ATS developer the ability to select various signal paths between the instrument and UUT. Examples of switch implementations are shown in Figure 8 as: (a) benchtop units; (b) integrated switch cards; (c) rack-mounted units; and (d) switch modules meeting published industry standards such as (but not limited to) LXI, USB, VME, VXI, and PXI.



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Figure 8—Switching product designs