

1532TM

IEEE Standard for In-System Configuration of Programmable Devices

IEEE Computer Society

Sponsored by the
Test Technology Committee



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IEEE Std 1532-2000)

IEEE Standard for In-System Configuration of Programmable Devices

Sponsor

**Test Technology Committee
of the
IEEE Computer Society**

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Abstract: *The communication protocol described by IEEE Std 1149.1 (Standard Test Access Port and Boundary-Scan Architecture) has been adopted by this standard for providing standardized programming access and methodology for programmable integrated circuit devices. Devices that implement this standard shall first be compliant with IEEE Std 1149.1 used for testing purposes. A device, or set of devices implementing this standard may be programmed (written), read back, erased, and verified, singly or concurrently, with a standardized set of resources. Sample implementation and application details (which are not part of this standard) are included for illustrative purposes.*

Keywords: *complex programmable logic device (CPLD), erasable programmable read-only memory (EPROM), field programmable gate array (FPGA), flash ram, in-system (or in-situ) configuration (ISC), programmable device*

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Introduction

(This introduction is not part of IEEE Std 1532-2001, IEEE Standard for In-System Configuration of Programmable Devices.)

The development of this standard began with a preliminary meeting held April 19, 1996. There, a group of Programmable Device vendors and users discussed the possibility of standardizing the programming process for these devices. Subsequent meetings were held regularly and agreement was developed for basing the programming process upon the IEEE Std 1149.1 communication protocol, because many of these devices were expected to support IEEE Std 1149.1 for testing purposes. This group adopted as its mission:

To define, document and promote the use of a standardized process and methodology for implementing programming capabilities within programmable integrated circuit devices, utilizing (and compatible with) the IEEE Std 1149.1 communication protocol. This standard would allow the programming of one or more compliant devices concurrently, while mounted on a board or embedded in a system, known as "In-System Configuration." Concurrent programming may often result in significant programming time efficiencies. The In-System feature would address the need to configure or reconfigure, read back, verify or erase programmable devices after they have been installed by a manufacturing process. This eliminates handling damage and the need for manufacturing steps and inventory management related to preprogrammed devices.

This work received the support of the IEEE Std 1149.1 Working Group which ultimately urged that this effort become its own standard within the Test Technology Technical Committee of the IEEE Computer Society, in July of 1998. The initially approved version of this standard described the necessary hardware elements for compliance. By making this available quickly and early, the development of compliant silicon was facilitated and its availability accelerated. This revision completes the standard by formalizing the ISC algorithm description within the infrastructure of BSDL. This last element is required to enable the proliferation of software capable of universally supporting compliant devices.

Participants

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Rob Eccles	Mark Moyer *	Carmy Yellin
Peter van den Eijnden	Matthew Murphy	Dan Young
Bernardo Elayda	Gary O’Brien	Piotr Zbysinski

The following members of the balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention:

Guy Adam	Rich Hatcher	Mark Moyer
David Bonnett	Jim Heaton	Robert Myers
William Borroz	Alan Herrmann	Benoit Nadeau-Dostie
John Braden	Bradley Ishihara	Bruce Peterson
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IEEE Standard for In-System Configuration of Programmable Devices

1. Overview

1.1 Scope

This standard describes a series of mandatory and optional programming instructions and associated data registers that define a standard methodology for accessing and configuring programmable devices. These additional registers and instructions extend the capabilities of devices that comply with IEEE Std 1149.1-2001 such that the IEEE Std 1149.1 test access port (TAP) may be used for configuration activities. A data description format and extensions to boundary-scan description language (BSDL) are also specified and provide for the development of standardized automation tools for device programming.

1.2 Organization of the standard

This standard is divided into nine clauses and two annexes.

Clause 1 describes the scope, context, objectives, and organization of this standard.

Clause 2 provides references to other IEEE documentation needed to understand this document.

Clause 3 defines terms and acronyms used in this standard.

Clause 4 defines the variations of system state that are unique to programmable logic devices.

Clause 5 describes the general architecture of an in-system configurable (ISC) device.

Clause 6 describes the ISC instruction set.

Clause 7 describes the ISC register set and the operation of each register.

Clause 8 describes conformance and documentation requirements.

Annex A provides a device designer with a rationale for implementing various features in this standard.

Annex B describes programming flows for combinations of devices compliant with this standard.

Annex C gives a coordinated example of a BSDL file and data file for a hypothetical ISC device.

1.3 Context

Figure 1 shows a printed circuit board containing many types of devices. Of these, some could be compliant with IEEE Std 1149.1-2001 for the support of testing activities. Three devices labeled “ISC” are in-system configurable, meaning they are programmable devices that may not have their programming states loaded into them before the board has been assembled. These devices may be programmed *after* they have been attached to the board, via a physical and logical protocol. The physical protocol for programming utilizes the IEEE Std 1149.1-2001 test access port (TAP) pins, which allow a multiplicity of devices (both ISC and conventional) to be accessed serially with four or five wires. The logical protocol is based upon new instructions added to the IEEE Std 1149.1-2001 instruction set and is the subject of this standard.

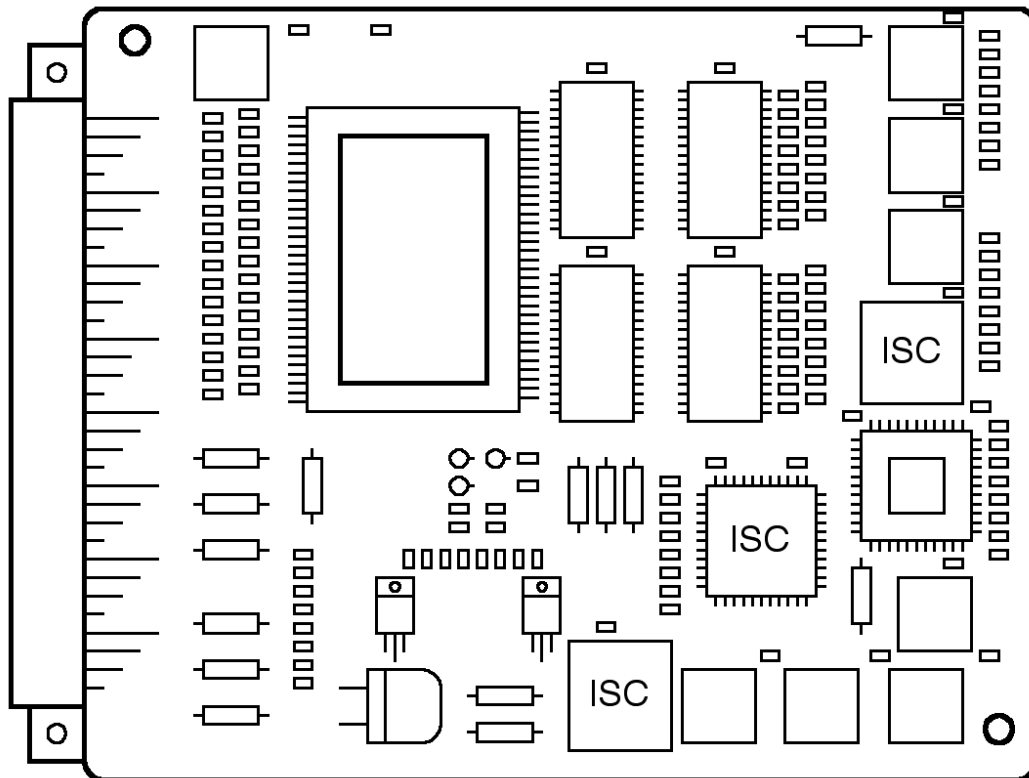


Figure 1—A printed circuit board containing a variety of components, including three in-system configurable (ISC) integrated circuits

The ISC devices also contain testability circuitry compliant with IEEE Std 1149.1-2001. This allows them to participate in manufacturing tests that detect and diagnose faults such as open solder joints and shorts either before or after they are programmed.

1.4 Objectives

The objective of this standard is to enhance user access to IEEE Std 1149.1-2001 based programmable devices. Since such devices are built on the foundation of the IEEE Std 1149.1-2001 TAP and state machine, they shall already comply with that standard.

Devices that adhere to this standard will realize significant savings in software, product development, and manufacturing costs related to ISC. It will not be necessary to develop new tools to support new vendor parts

with ISC features as they arrive in the marketplace. These parts can be integrated immediately into existing systems and tools.

In addition, tools based on this standard may be developed upon the existing IEEE Std 1149.1-2001 based tool sets and knowledge base, rapidly incorporating the features of this standard.

This standard also allows for multiple devices from independent vendors to be programmed concurrently. Development time and manufacturing costs (in terms of programming time) can thereby be significantly reduced, even in the multivendor environment. In the past, one family of devices from a single vendor may have been incompatible with another family from that same vendor, with respect to the programming process.

The standard also serves board and system designers by providing a consistent framework for system initialization, stabilization, and event initiation, which is important for robust system design.

The standard will realize the following additional benefits:

- a) It will serve as the development model for new entrants to the ISC industry and guarantee their immediate access to all the latest tools, development systems, and test and manufacturing flows and processes.
- b) It will facilitate innovations potentially including applications in reconfigurable computing, emulation, diagnostics, and field upgrading that would be usable across vendors.
- c) It will encourage tool vendors targeting the programmable device marketplace that there will be sufficient return on their investment to warrant tool development.

2. References

This standard shall be used in conjunction with the following standards. When the following standards are superseded by an approved revision, the revision shall apply.

IEEE 100, *The Authoritative Dictionary of IEEE Standards Terms*, Seventh Edition.

IEEE Std 1149.1-2001, IEEE Standard Test Access Port and Boundary-Scan Architecture.¹

3. Definitions and acronyms

See also IEEE Std 1149.1-2001² for definitions of terms used in this document.

3.1 Definitions

The following terms are used within this standard.

3.1.1 addressing: Programmable devices usually contain one or several arrays of memory locations. Each memory location has an address, which must be provided when reading or programming memory content.

¹IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA (<http://standards.ieee.org/>).

²Information on references can be found in Clause 2.

3.1.2 asymmetrically writeable device: A device with program memory that can only be written to one state. For example, a “1” may be written into a location containing a “0,” but not vice versa. Such devices must be erased to the blank state before new program data can be written. *Contrast:* **symmetrically writeable device.**

3.1.3 blank: Programmable devices usually contain one or several arrays of memory locations. The data placed in these locations constitute the device program. *See:* **device program.** Many devices are asymmetrical with respect to writing data into these locations. For example, a “1” may be written into a location containing a “0,” but not vice versa. Thus a “blank” device is filled with a field of overwriteable states. For symmetrically writeable devices, the “blank” state is usually defined as a field of states that implement no programmable functionality.

3.1.4 burn time: An interval of time during which a set (or subset) of device programming bits is presented to on-chip programming functions, which become the definition of the logic functions the device will subsequently implement. In some older technologies, tiny on-chip fuses are vaporized (hence the term “burn”), which requires a minimum time to achieve. Burn time is technology-dependent and may be nearly instantaneous in some devices or require many milliseconds in others. *Syn:* **bake time, cook time, and soak time.**

3.1.5 chain: Two or more IEEE Std 1149.1-2001 compliant devices that share common test clock (TCK) and test mode select (TMS) signals and are linked together with the test data out (TDO) signal of one device connected to the test data in (TDI) signal of a subsequent device. The overall chain may be accessed by a 4- or 5-wire TAP port. *See:* **test access port (TAP).**

3.1.6 checksum: An integer created by a mathematical process that operates on a stream of data. The checksum for this data is then published so that it can be compared to subsequently recalculated checksums for that same data. If the data has not been changed or disturbed, the published checksum should match a newly calculated checksum. The mathematical process is often based upon binary addition (to some modulus) or logical Exclusive OR of bytes or words. There are well-known flaws with such processes that can allow damaged data streams to masquerade as good by having the same checksum. *See:* **CRC Cyclic Redundant Codes.**

3.1.7 completion: In the context of an in-system configurable (ISC) instruction, completion occurs when the sequence of activities performed during execution has finished. *See:* **execute.** However, the requirements for execution may not be met or error conditions may be encountered such that successful completion is not possible. These events constitute unsuccessful completion.

3.1.8 complex programmable logic device (CPLD): A high capacity programmable logic device (PLD) usually provided in packages with 40 or more pins, essentially an array of programmable logic blocks interconnected by a routing matrix.

3.1.9 concurrent operation: The ability to conduct programmable device operations in two or more devices *in the same* IEEE Std 1149.1-2001 *chain* concurrently in time. During concurrent operation, all devices in a chain operate continuously in the *Run-Test/Idle* test access port (TAP) controller state. In particular, the burn times of the devices can be made to elapse concurrently.

3.1.10 CRC Cyclic Redundant Codes: This can be used as an improved checksum process. Such a code (properly constructed) is much less prone to aliasing a bad data stream with a good stream because it encodes the positional information of 1s and 0s in a stream as well as their frequency. *See:* **checksum.**

3.1.11 device program: A sequence of bits that, when loaded into a programmable device via a protocol, subsequently defines the functions it will implement. *See:* **volatile program** and **nonvolatile program.**

3.1.12 displaced: An instruction in the test access port (TAP) instruction register is *displaced* when another instruction is shifted in and then a falling edge of test clock (TCK) in the *Update-IR* TAP controller state

occurs. Note that any instruction besides IDCODE (the default instruction jammed into the TAP instruction register) will be displaced immediately if the TAP enters the *Test-Logic-Reset* TAP controller state.

3.1.13 duration: In the context of an in-system configurable (ISC) instruction, a period of time that starts when a TAP controller first enters the *Run-Test/Idle* TAP controller state. A duration is given for each ISC instruction which specifies how much time (typically a minimum) the action(s) performed by that instruction will take to complete.

3.1.14 electrically erasable programmable read-only memory (EEPROM): Programmable read-only memories have evolved from mask-programmable devices to devices that were erasable by exposure to ultraviolet light [erasable programmable read-only memory (EPROM)] to EEPROM devices that can be electrically erased.

3.1.15 enabled protection mechanism: In-system configurable (ISC) devices may be implemented with the ability to protect the memory content from erasure, reading, or writing in various combinations (see 5.1.10). *See: protect.* When any of these mechanisms is available, it can be enabled, thus preventing the action it can protect against.

3.1.16 erasable programmable logic device (EPLD): At first, an EPROM-based programmable logic device, the term now includes flash and electrically erasable programmable read-only memory (EEPROM) based devices as well.

3.1.17 erase: An operation that removes any previously installed device program by changing programmed bits to their unprogrammed state. Erasure may be implemented in several ways. For example, there may be a “bulk erase” function that erases the entire device program in one action. There may be selective, or addressed erasure that only erases a specified “word” of the program. Between these two extremes there may be a “sector” erase feature that erases a group of words. This operation may be inhibited if the device contains a security feature enabled by a protect operation.

3.1.18 execute: In the context of an in-system configurable (ISC) instruction, execution occurs after the test access port (TAP) controller has proceeded to the *Run-Test/Idle* TAP controller state. In this state, the instruction performs a specific function that may contain multiple steps or a set of activities. After a minimum amount of time [or clocking of test clock (TCK)] has occurred, the instruction completes execution. Additional time (or clocking of TCK) beyond this minimum requirement does not affect the results of the instruction’s execution.

3.1.19 explicit addressing: Address information is provided by an external algorithm when operating on memory content.

3.1.20 field-programmable gate array (FPGA): A programmable alternative to a masked gate array using a channeled programmable interconnect matrix to join blocks of configurable logic. Physical characteristics such as line length and number of fuses is not known until routing. This may lead to some timing unpredictability. The advantage comes in logic density and flexibility.

3.1.21 fixed system pin: A system pin with an input/output (I/O) function that is independent of configuration information programmed into the device and has not been designated as an in-system configurable (ISC) system pin by the device designer.

3.1.22 flash random access memory (flash RAM): A memory technology similar to electrically erasable programmable read-only memory (EEPROM) but implemented with a single transistor rather than two.

3.1.23 flow: A logical sequence of in-system configurable (ISC) instructions that performs a basic programming function such as erasing programmable memory, verifying it, or programming it.

3.1.24 generic array logic (GAL): An earlier programmable logic technology still widely used, featuring a fixed OR array and programmable AND array.

3.1.25 implicit addressing: Address information is provided by an internally managed process when operating on memory content. For example, successive memory locations may be sequentially accessed by an “auto-increment” addressing process supported by the device such that an external algorithm does not have to be aware of how memory locations are organized.

3.1.26 in-system configuration (ISC): The ability to load, read back, or erase programming bits in a programmable logic device after it has been attached to a printed circuit board. *See* **device program**.

3.1.27 ISC_Disable_Erase signal: An optional signal (see 5.1.10.3) used to indicate that program data erasure is not allowed.

3.1.28 ISC_Disable_Program signal: An optional signal (see 5.1.10.2) used to indicate that program data writing is not allowed.

3.1.29 ISC_Disable_Read signal: An optional signal (see 5.1.10.1) used to indicate that program data reading is not allowed.

3.1.30 ISC_Done signal: A signal used to indicate that a device program has been successfully written to the satisfaction of an external algorithm. When this signal is cleared, the device is considered to be unprogrammed, even if physically the device does contain programmed bits. When this signal is set, the device is considered to be programmed and ready for operation. In volatile devices, this signal is automatically cleared at power-up. In nonvolatile devices, this signal maintains its state during nonpowered intervals. This signal can be set by programming operations described in this standard and may be protected by a security function implemented within the device.

3.1.31 ISC_Enabled signal: A signal (see Clause 4) used to indicate that a device has been successfully conditioned for programming activity. This signal is cleared during power-up for both volatile and nonvolatile devices.

3.1.32 ISC system pin: A system pin with an input/output (I/O) function that is defined by configuration information programmed into the device or has been designated as an in-system configurable (ISC) system pin by the device designer.

3.1.33 load: In the context of an instruction, an instruction is loaded when opcode bits present in the TAP instruction shift register are updated into the parallel-hold portion of the register by passing through the *Update-IR* TAP controller state. At the time an instruction is loaded, its data register is selected for data shifting. *Contrast:* **execute**.

3.1.34 mission logic: *See:* **system logic**.

3.1.35 mission pin: *See:* **system pin**.

3.1.36 noninvasive instruction: Instructions from IEEE Std 1149.1-2001 (including BYPASS, SAMPLE, PRELOAD, IDCODE, and USERCODE) that maintain the device in system mode rather than in test mode. Thus, these instructions do not interfere with the system behavior of the device. *Contrast:* **pin-permission instruction**.

3.1.37 nonvolatile program: Device programming that is retained by a device even when power is removed and later restored.

3.1.38 nullified: Proper in-system-configurable (ISC) instruction operation is predicated on the device being in the ISC accessed system modal state (see Clause 4) while it is being executed. If this condition is not met, the instruction's operation is nullified. A nullified ISC instruction will still place a defined register in the shift path and shift bits through it as required by IEEE Std 1149.1-2001, but the ISC actions defined for the instruction by this standard will not be completed and the result of its execution is undefined.

3.1.39 Optimize: In-system configurable (ISC) programming activities can be optimized for time efficiency. There are two forms of optimization. First, if a device has a specific instruction loaded, it may be redundant to reload this instruction. This is called "IR optimization." Second, when a register is targeted between TDI and TDO, "DR optimization" can be employed by shifting out captured data while new update data is being shifted in, rather than first shifting out captured data and then shifting in new update data. When a chain of devices is operated, optimization can be performed, but each device in the chain must be considered. For example, if two of three devices in subsequent activities will be executing the same instruction but the third will need a new instruction loaded, then IR optimization is not possible because loading the third device's instruction forces the reload of the first two.

3.1.40 pin-permission instruction: Instructions from IEEE Std 1149.1-2001 (including EXTEST, INTEST, CLAMP, HIGHZ, and RUNBIST) and instructions from this standard, which place the device in test or programming modes. These instructions take over control of the system input/output (I/O) pins. *Contrast:* **noninvasive instruction.**

3.1.41 program: An operation that installs externally supplied device programming bits (or a portion thereof) within a programmable device. This operation may be inhibited if the device contains a security feature enabled by a protect operation.

3.1.42 programmable array logic (PAL): An earlier programmable logic technology still widely used, featuring a fixed OR array and programmable AND array.

3.1.43 programmable logic devices: This family of devices includes the complex programmable logic device (CPLD), electrically erasable programmable read-only memory (EEPROM), the erasable programmable logic device (EPLD), field-programmable gate array (FPGA), flash random access memory (flash RAM), and programmable array logic (PAL).

3.1.44 protect: Traditionally, an operation that prevents a subsequent read operation from being able to read out a device program. This is a security feature used to prevent copying or deciphering of a device program. In some implementations, writing one or more "security" bits located somewhere in the device program enables protection. Once set, these bits block subsequent read operations. Security bits are usually only cleared by erasing the device program. More recently, protect has been expanded to include the prevention of unwanted programming or erasure operations.

3.1.45 read: An operation that allows a device program to be read back out from a programmed device. This operation may be inhibited if the device contains a security feature enabled by a protect operation.

3.1.46 signal: A named signal is used to denote a binary condition used to choose between two outcomes. It is deliberately "implementation-vague" so as not to constrain a designer's freedom. For example, a signal may be implemented as a bit in a register, or derived as a function of several bits, or as a one-hot decode from an instruction decoder, as fits the designer's needs. This should not be confused with input/output (I/O) signals on device pins that may be high, low, or disabled.

3.1.47 simple programmable logic device (SPLD): A family of programmable logic devices including programmable array logic (PAL), generic array logic (GAL), and the erasable programmable logic device (EPLD).

3.1.48 symmetrically writeable device: A device with program memory that can be written to either state. These devices are often static RAM based. *Contrast:* **asymmetrically writeable device.**

3.1.49 system logic: Any item of logic that is dedicated to realizing the nontest function of the component or is at the time of interest configured to achieve some aspect of the nontest function. In the case of programmable devices, the system logic may not be defined until after the device is programmed. *See:* **device program.** *Syn:* **mission logic.**

3.1.50 system modal states: IEEE Std 1149.1-2001 defines two modes, “system” and “test.” Devices that conform to this standard have a system mode that is divided into four modal states, as defined in Clause 4. This reflects the fact that programmable devices, at various times in their operation, may 1) be in “operational” mode containing system logic, 2) be in an “unprogrammed” mode with blank logic configuration memory, 3) be in “ISC accessed” mode for programming or accessing logic configuration memory, or 4) be in “ISC complete” mode when accessing configuration memory is complete before returning to the operational mode.

3.1.51 system pin: A component pin that feeds, or is fed from, the on-chip system logic. In the case of programmable devices, the system logic may not be defined until after the device is programmed. *See:* **device program.** In devices that contain conventional logic in addition to programmable logic, system pins may be classified as in-system configurable (ISC) system pins and fixed system pins. *See:* **ISC system pin** and **fixed system pin.** *Syn:* **mission pin.**

3.1.52 TAP controller: A 16-state finite state machine used to control the activities of the test access port (TAP) and the test logic within the device. *See:* **test access port (TAP).**

3.1.53 test access port (TAP): As defined by IEEE Std 1149.1-2001, this consists of four (optionally five) device pins dedicated for use by IEEE Std 1149.1-2001 and programming usage defined by this standard. TAP pins are *not* system pins.

3.1.54 verify: An operation similar to reading that compares an installed device program (or a portion thereof) to a program supplied externally. If a discrepancy is found, an error indication is given. This operation may be inhibited if the device contains a security feature enabled by a protect operation.

3.1.55 volatile program: Device programming that is lost when a device has power removed from it.

3.1.56 write: *See:* **program.**

3.2 Acronyms

The following acronyms are used within this standard.

BSDL	boundary-scan description language (see IEEE Std 1149.1-2001)
BSR	boundary-scan register
CPLD	complex programmable logic device
EEPROM	electrically erasable programmable read-only memory
EPLD	electrically programmable logic device
EPROM	erasable programmable read-only memory
FPGA	field-programmable gate array
GAL	generic array logic
IC	integrated circuit
I/O	input/output
IOM	input/output module
ISC	in-system configuration, in-system configurable

PAL	programmable array logic
PROM	programmable read-only memory
SRAM	static random access memory
TAP	IEEE Std 1149.1-2001 test access port
TCK	test clock input pin contained in the IEEE Std 1149.1-2001 TAP
TDI	test data input pin contained in the IEEE Std 1149.1-2001 TAP
TDO	test data output pin contained in the IEEE Std 1149.1-2001 TAP
TLR	Test-Logic-Reset, the reset state of the IEEE Std 1149.1-2001 TAP controller state diagram
TMS	test mode select input pin contained in the IEEE Std 1149.1-2001 TAP
TRST*	test reset input pin contained in the IEEE Std 1149.1-2001 TAP (this pin is optional)

NOTE—Following the convention used in IEEE Std 1149.1-2001, pins or signals with a trailing asterisk (“*”) in their names are active low true signals.

4. System modal states

A conventional (i.e., nonprogrammable) device compliant with IEEE Std 1149.1-2001 has a “system” mode and a “test” mode. In system mode, the device performs its intended mission even while executing “noninvasive” nontest instructions from IEEE Std 1149.1-2001. In test mode, these test instructions control the device’s system input/output (I/O) pins for testing purposes. A compliant IEEE Std 1149.1-2001 device passes from system mode to test mode when certain IEEE Std 1149.1-2001 instructions become active, as shown in Figure 2.

Devices that are compliant with IEEE Std 1149.1-2001 power-up in system mode. Noninvasive nontest IEEE Std 1149.1-2001 instructions include BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE. Test instructions include EXTEST, INTEST, CLAMP, HIGHZ, and RUNBIST. Entering the *Test-Logic-Reset* TAP controller state will also force the device into system mode.

NOTES:

1—After a device has been in test mode, it may return to system mode but be unable to resume logical operation in concert with other devices to which it is connected because while in test mode, all communication with these devices was severed. It will likely be necessary to issue a system reset to restore proper system operation.

2—User-defined instructions may create new modes of operation that are not depicted in Figure 2.

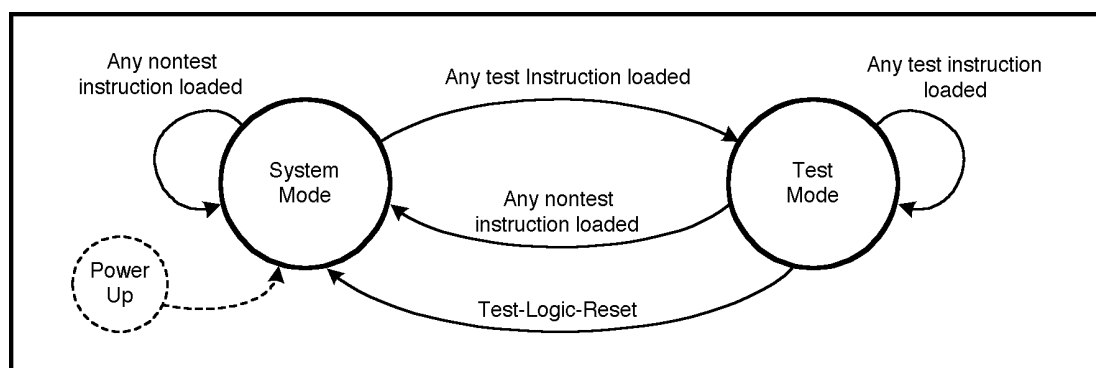


Figure 2—Transitions from system mode to test mode for a conventional device compliant with IEEE Std 1149.1-2001

Unlike conventional integrated circuit (IC) devices, a programmable logic device may have many different user-defined operation behaviors depending on the pattern that is currently programmed into the device. To precisely define device behavior before, during, and after programming, the system mode of an ISC programmable device has four different “system modal states,” all composing the “system” mode of the

device as defined by IEEE Std 1149.1-2001 (see 4.1). The four system modal states define the “system” behavior of system I/O pins when noninvasive instructions from IEEE Std 1149.1-2001 are loaded. (Test instructions already have I/O behavior specified by IEEE Std 1149.1-2001, and ISC instructions defined herein also have prescribed I/O behavior.)

NOTE—See 5.1.1 for a classification of system pins. For the discussion in this clause, assume that all system I/O pins are associated with programmable logic.

Well-defined and predictable I/O behavior is of paramount importance to designers of boards and systems who must ensure that the power-up behavior and system initialization processes of their designs are robust. This is of particular concern where a design is programmable. It must exhibit robust behavior before, during, and after the programming process.

4.1 Definition of system modal states

The four system modal states (see Figure 3) of a programmable device conforming to this standard are as follows:

- *Unprogrammed*: In this system modal state, an ISC programmable logic device may be blank (see 3.1.3) or incompletely programmed. In this system modal state, and while a noninvasive IEEE Std 1149.1-2001 instruction (see 3.1.36) is loaded, the device’s system I/O pins are disabled such that they cannot contend with output drivers that may exist in other devices connected to the ISC device. Any ISC instruction (excepting ISC_ENABLE) will have its ISC operation nullified [see 6.1.1, rule b)] if executed in this state. Upon power-up, volatile device, blank devices, and incompletely programmed nonvolatile devices should reside in this state.
- *ISC accessed*: In this system modal state, ISC instructions may be used (when permitted) to read, write, verify, protect, or erase the device. In this system modal state, and while a noninvasive IEEE Std 1149.1-2001 instruction is loaded, the device’s system I/O pins are either disabled or specifically controlled by the content of the device’s boundary-scan register as determined in 6.1.1, rule c).
- *ISC complete*: This system modal state exists so an external algorithm can control transitions to the unprogrammed or operational system modal state after ISC operations are complete. This system modal state is entered as a result of executing the ISC_DISABLE instruction. This system modal state is temporary; if any instruction other than ISC_DISABLE is loaded into the instruction register (at the falling edge of TCK in the *Update-IR* TAP controller state), this system modal state is exited. Thus, this system modal state cannot exist when a noninvasive IEEE Std 1149.1-2001 instruction is present in the instruction register.
- *Operational*: In this system modal state, the device is ready for its “operational” mode defined by its programming. In this system modal state, and while a noninvasive IEEE Std 1149.1-2001 instruction is loaded, the device’s system I/O pins take on their programmed system nature of inputs, outputs, bidirectionals, or unused. Any ISC instruction (excepting ISC_ENABLE) will have its operation nullified [see 6.1.1, rule b)] if executed in this system modal state. Successfully programmed nonvolatile devices, upon power-up, should reside in this system modal state.

In all system modal states, all public 1149.1 instructions are available and supported per the IEEE Std 1149.1-2001 standard. This means that IEEE Std 1149.1-2001 chain integrity or infrastructure testing can be accomplished at any time regardless of the system modal state of any ISC device.

NOTES:

1—Certain operations conducted in test mode (for example, EXTEST-based interconnection tests) may not be electrically compatible with programming activities (or vice versa) conducted in the ISC accessed modal state due to noise or power supply considerations. However, it may be quite reasonable to read out a device USERCODE from the ISC accessed modal state and later return to an ISC instruction.

2—There may be restrictions that should be observed for a given ISC device regarding the interruption of a programming flow in order to execute a non-ISC instruction.

It is important to realize that a noninvasive 1149.1 instruction such as BYPASS may demonstrate up to three distinct system I/O behaviors depending upon the system modal state of the device:

- a) All pins disabled (unprogrammed system modal state).
- b) All pins either disabled or specifically controlled by the content of the device's boundary-scan register as determined in 6.1.1 rule c) (ISC accessed system modal states).
- c) All pins behaving in their programmed mission mode (operational system modal state).

This modal behavior conforms to IEEE Std 1149.1-2001 because of the definition of system modal states given by this standard. The plurality of system I/O pin behaviors allows a device to move from executing an ISC instruction to executing a noninvasive 1149.1 instruction with seamless and predictable system I/O behavior.

NOTE—It can also lead to a potentially surprising result. For example, when a device is in the ISC accessed system modal state and its pins are controlled by the boundary-scan register, the PRELOAD instruction may be used to change the content of the boundary-scan register. This change, upon the falling edge of TCK in the *Update-DR* TAP controller state, will appear at the device I/O pins, simulating the operation of EXTEST. This is because the *system behavior* of this device in the ISC accessed system modal state is *defined* to have the property of the system I/Os being controlled by the boundary-scan register.

4.2 Description of system modal state transitions

Figure 3 shows the four system modal states for an ISC device and how transitions between these states occur.

NOTE—Figure 3 also shows transitions to test mode. These are further described in Figure 4.

Modal state transitions are governed by three factors:

- The instruction loaded into the 1149.1 instruction register. This instruction becomes effective on the falling edge of TCK in the *Update-IR* TAP controller state. ISC instructions will define system I/O behavior at this time, but they also require some time spent in the *Run-Test/Idle* TAP controller state for their operations to complete.
- The state of an internal “ISC_Done” signal. (In volatile devices, this signal is cleared at power-up. In nonvolatile devices this signal is retained during loss of power.) The ISC_Done signal is set when the device is programmed to the satisfaction of an external ISC programming algorithm. This indicates the device is no longer blank. The ISC_Done signal is set one of three ways: by executing the ISC_DISABLE instruction to completion with a specific data pattern set in the ISC_Config register; by execution of the (optional) ISC_PROGRAM_DONE instruction; or by programming one or more specific bits in the program memory array. The ISC_Done signal also determines the functionality of the device system I/O pins on power-up. If the ISC_Done signal is clear, the device I/O pins are disabled.

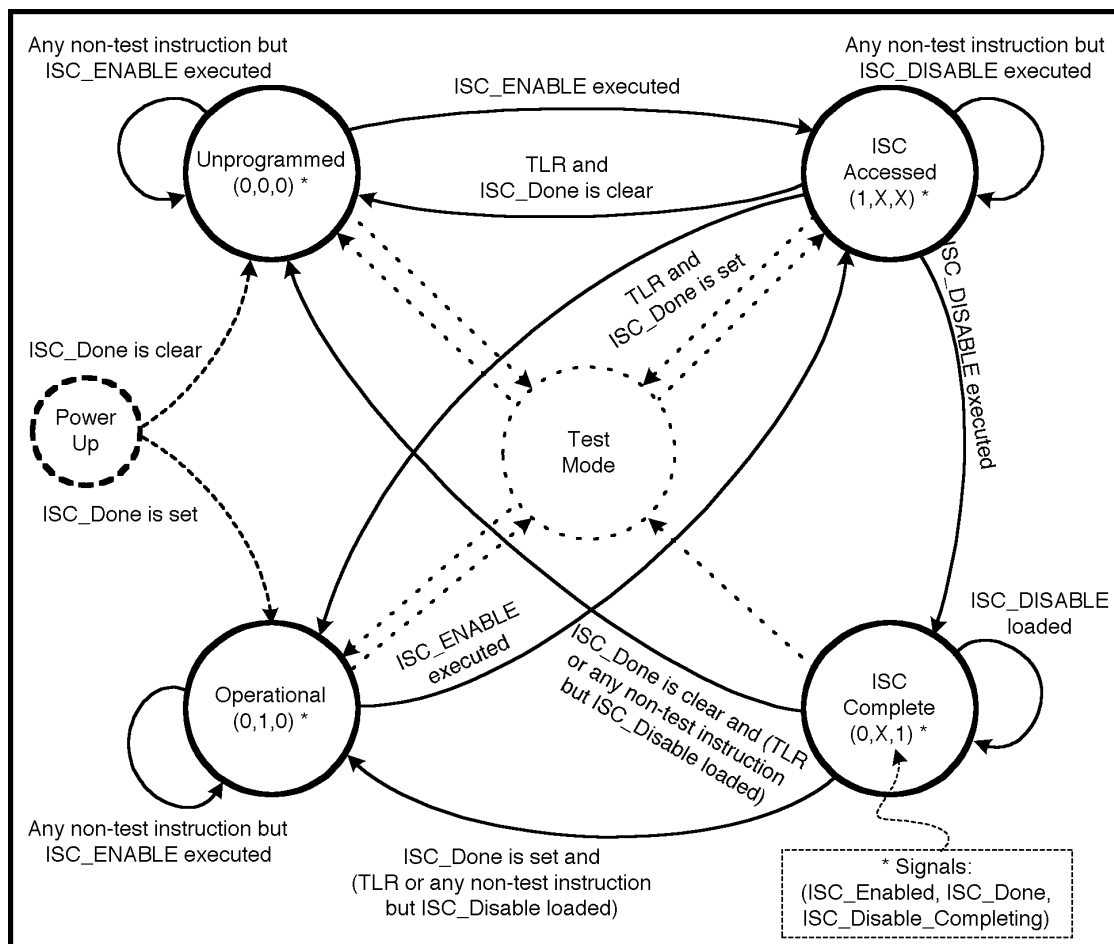


Figure 3—Four modal states that compose the “system mode” of operation for an ISC device and transitions (A description of the transitions to and from test mode appears in Figure 4. The three signals are described in 4.2 and 4.3.)

NOTE—The ISC_Done signal may be subject to protection by a security feature that may prevent changes to its state.

- The state of an internal volatile signal called the “ISC_Enabled” signal. This signal is set by the execution of the ISC_ENABLE instruction and may be cleared by subsequent events. In both volatile and nonvolatile devices, this signal is cleared at power-up.

Two of these factors (the ISC_DISABLE instruction is loaded and ISC_Enabled is set) are utilized to derive a third signal named “ISC_Disable_Completing.” This signal is used to indicate that the ISC complete system modal state has been entered legally, that is, from the ISC accessed system modal state by action of the ISC_DISABLE instruction. The derivation of ISC_Disable_Completing is conceptualized in 4.3, though any number of other derivations are possible.

The unprogrammed modal state is entered upon power-up if the ISC_Done signal is cleared. The only way to exit the unprogrammed modal state is by loading and executing the ISC_ENABLE instruction (see 6.2.1) which sets the ISC_Enabled signal upon successful completion. Setting the ISC_Enabled signal causes a transition to the ISC accessed modal state. If the ISC_ENABLE instruction is not successfully completed, the ISC_Enabled signal is not set and the device stays in the unprogrammed modal state.

NOTE—If while in the unprogrammed or operational modal state an ISC instruction other than ISC_ENABLE is loaded, it will not operate to fulfill its intended mission [see 6.1.1, rule b)], that is, its operation will be nullified.

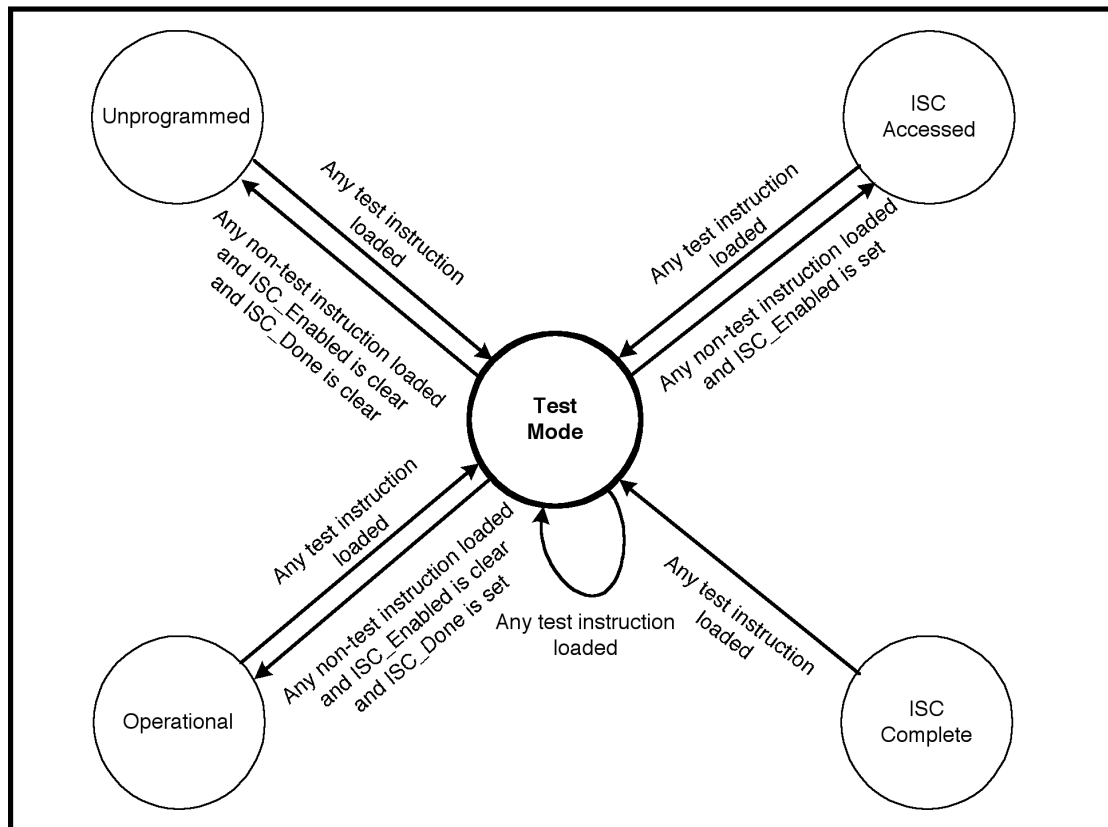


Figure 4—Transitions to and from system modal states and test mode. (A description of the transitions among the four modal states appears in Figure 3.)

Once the ISC accessed modal state is entered (that is, the ISC_Enabled signal is set) all other ISC instructions are enabled to operate as documented in Clause 6. The preferred way to exit the ISC accessed system modal state is by executing the ISC_DISABLE instruction, which clears the ISC_Enabled signal (and potentially sets the ISC_Done signal) and causes a transition to the ISC complete system modal state. If the *Test-Logic-Reset* TAP state is entered while in the ISC accessed system modal state, then the currently loaded instruction is aborted and either the unprogrammed modal state is entered if ISC_Done is clear, or the operational state is entered if ISC_Done is set. In typical ISC programming flows, a sequence of operations such as erasing, writing, reading, and protecting would all be done successively within the ISC accessed modal state.

NOTES:

1—If the ISC accessed system modal state is left abnormally (by traveling to *Test-Logic-Reset*) while the ISC_Done signal is set, it is possible that an improperly programmed device could be set to the operational system modal state. It is the responsibility of external controlling algorithms to avoid this. In some technologies it is possible that the ISC_Done signal can only be cleared by an erase operation. In such devices, it will be important to construct the erase operation to clear the ISC_Done signal early in the erasure process. This reduces the chance that terminating the erasure process before completion will leave the ISC_Done signal set.

2—The ISC_Disable_Completing signal is also generated by the loading of ISC_DISABLE as seen in 4.3.

In the ISC complete modal state, the device is ready to transition to either the operational or unprogrammed system modal states, depending on the state of the ISC_Done signal. The transition from ISC complete is accomplished by loading any instruction other than ISC_DISABLE into the instruction register. One way to

do this is to cause the TAP controller to enter the *Test-Logic-Reset* TAP controller state, which forces the IDCODE instruction into the instruction register which in turn forces a transition to either the unprogrammed or the operational system modal state depending on the state of the ISC_Done signal. However, if several ISC devices in a chain are in the ISC complete system modal state, then it may be desirable to sequence their transition to the operational system modal state in a particular order. Loading one ISC device with BYPASS while reloading the others with ISC_DISABLE, and so progressing until all devices are loaded with BYPASS would accomplish this objective.

Once a device enters the operational system modal state from the ISC complete system modal state, it is fully programmed and capable of performing its mission function. System I/O pins are subject to the instruction that was used to displace the ISC_DISABLE instruction. If it is a test instruction (like EXTEST), then that instruction controls the system I/O pins. If the instruction was an ISC instruction (like ISC_ENABLE), then it will control the system I/O pins per 6.1.1, rule c). If the new instruction was a noninvasive 1149.1 instruction (like BYPASS), the system I/O pins are governed by the programming of the device and take on their intended system function. The only way to leave the operational system modal state (excepting a transition into test mode) is to load and execute the ISC_ENABLE instruction, thus returning to the ISC accessed system modal state. This might be done to reprogram, verify, or erase a device's programming at some future point in time.

NOTES:

1—If while in the operational system modal state an ISC instruction other than ISC_ENABLE is loaded, it will not operate to fulfill its intended mission [(see 6.1.1, rule b)], that is, its operation will be nullified.

2—If the operational system modal state is entered abnormally (in response to *Test-Logic-Reset*) the device may not be capable of performing its mission function. If this abnormal transition is performed, it is the responsibility of the programming algorithm to subsequently erase the ISC_Done signal so that the device no longer appears to be properly programmed.

Transitions to and from test mode in Figure 3 were shown with unlabeled dotted lines to avoid clutter. Figure 4 shows how transitions between the system modal states and test mode occur. From any system modal state, the transition to test mode occurs when a test instruction (EXTEST, INTEST, CLAMP, HIGHZ, or RUNBIST) is loaded.

There are three ways to return to a system modal state from test mode. All of these require that a nontest instruction (BYPASS, PRELOAD, SAMPLE, IDCODE, USERCODE) or an ISC instruction described by this standard be loaded and are qualified by the states of the ISC_Enabled and ISC_Done signals.

The design of a particular ISC device may not be able to support all the transitions shown in Figure 4. For example, depending on implementation technology, when in the ISC accessed system modal state an ISC device may generate high programming voltages internally. While these voltages are present, it may be difficult to ensure correct operation of the device if it also makes transitions on system I/O pins. In all cases, the designer is required to ensure that the 1149.1 instructions operate as specified [see permission r) of 5.2 and related notes] and to document instruction sequences that should be avoided (see 8.2).

4.3 System modal state transition timing

Transitions on output pins and between system modal states occur at prescribed times shown in Figure 5. (This drawing does not show time to scale, but represents the ordering of events.)

NOTE—In Figure 5, the convention is used that “set” is high and “clear” is low.

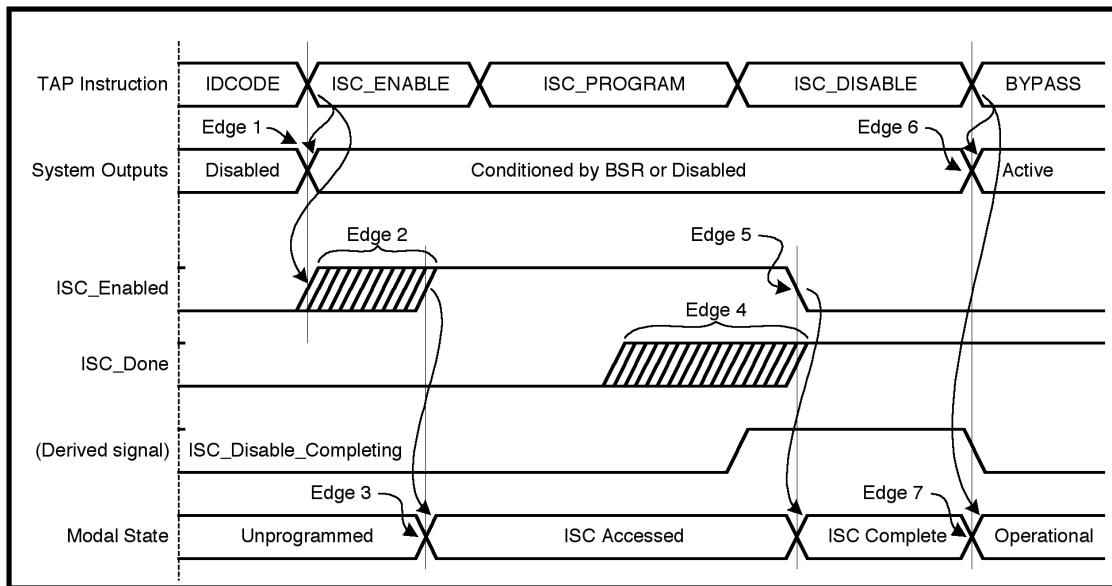


Figure 5—Waveforms (not to scale) for signals that control system outputs and system modal state transitions

There are 7 edges of interest shown in Figure 5:

- *Edge 1:* System I/O pins that were disabled take on the state given by 6.1.1 rule c) when the TAP instruction changes from IDCODE to ISC_ENABLE (triggered by the falling edge of TCK in the *Update-IR* TAP controller state).
- *Edge 2:* The ISC_Enabled signal is asserted somewhere between the time the TAP instruction changes from IDCODE to ISC_ENABLE (triggered by the falling edge of TCK in the *Update-IR* TAP controller state) and the last rising edge of TCK in the *Run-Test/Idle* state that satisfies the minimum duration specification [see 6.1.1, rule i)] for ISC_ENABLE.
- *Edge 3:* The system modal state changes from unprogrammed to ISC accessed when the ISC_Enable signal is asserted.
- *Edge 4:* The ISC_Done signal is set either by programming (with the ISC_PROGRAM instruction) one or more bits in the program data area, by the execution of the ISC_DISABLE instruction, or by the execution of the ISC_PROGRAM_DONE instruction. The ISC_Done signal is set no later than the last rising edge of TCK in the *Run-Test/Idle* state that satisfies the minimum duration specification [see 6.1.1, rule i)] for the instruction setting ISC_Done.
- *Edge 5:* The ISC_Enabled signal is cleared during execution of the ISC_PROGRAM or ISC_DISABLE instructions. This occurs on the last rising edge of TCK in the *Run-Test/Idle* state that satisfies the minimum duration specification [See 6.1.1, rule i)] for ISC_DISABLE. This causes the system modal state to change from ISC accessed to ISC complete.

NOTE—In a preferred embodiment, the ISC_Done and ISC_Enabled signals (at edges 4 and 5) transition at the same time. If ISC_Done should transition before ISC_Enabled, it is possible for a transition to the *Test-Logic-Reset* TAP controller state to occur between them, resulting in possible confusion about what ISC_Done means. (It will be the responsibility of external programming algorithms to avoid this confusion.) Simultaneous transition of these two signals requires that the ISC_Done signal be controlled by the ISC_DISABLE instruction.

- *Edge 6:* When any non-ISC instruction is loaded into the TAP instruction register (upon the falling edge of TCK in the *Update-IR* TAP controller state) the system outputs take on their programmed nature.

- *Edge 7:* When any instruction other than ISC_DISABLE is loaded into the TAP instruction register (upon the falling edge of TCK in the *Update-IR* TAP controller state) the system modal state changes from ISC complete to operational.

The case where ISC_DISABLE is executed and then ISC_ENABLE is immediately executed is shown in Figure 6. When this occurs, the system modal state changes briefly to operational, but because the TAP instruction register still contains an ISC instruction, the system I/O pins remain in the state governed by rule c) of 6.1.1. Once the ISC_ENABLE instruction completes, the device is again in the ISC_Accessed system modal state at edge 8. Thus, if several ISC operations are executed back-to-back (for example, programming followed by readback) the device I/O pins will not leave their quiescent state even when these ISC operations are bounded by ISC_ENABLE and ISC_DISABLE instructions.

The derived signal ISC_Disable_Completing, first referenced as a control signal in Figure 3 and as its waveforms appear in Figure 5 and Figure 6, may at first appear to be a signal from the TAP instruction decoder (call it ISC_Disable_Decoded) that is set whenever the ISC_DISABLE instruction is loaded in the TAP instruction register. However, it must be a function of both ISC_Disable_Decoded and ISC_Enabled as shown in Figure 7. This reflects the fact that ISC_Disable_Completing indicates that the ISC_DISABLE instruction was loaded properly while the device was in the ISC accessed system modal state (that is, the ISC_Enabled signal is set).

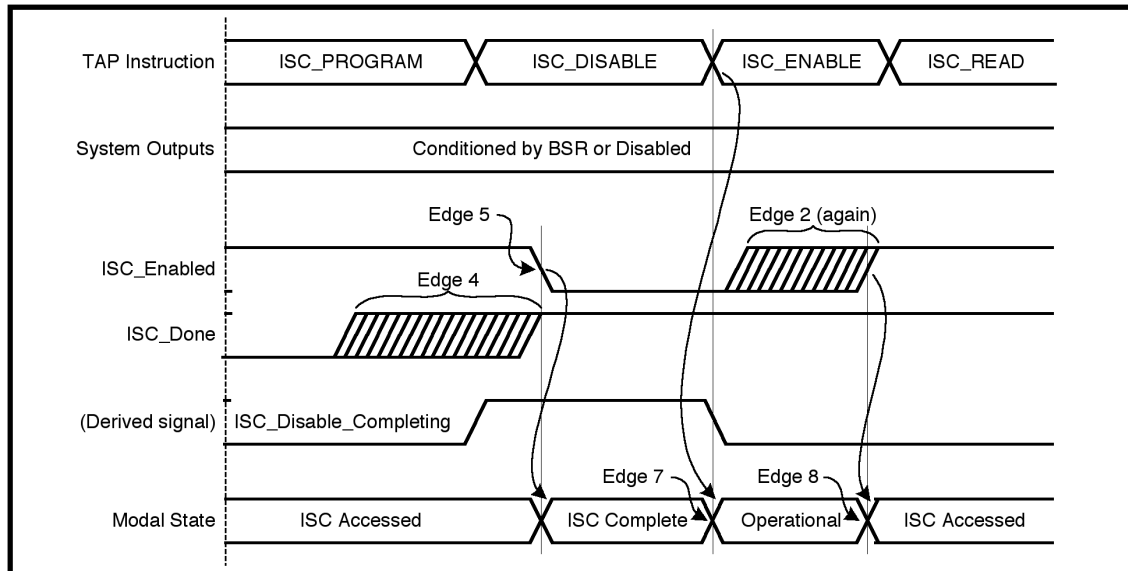


Figure 6—Waveforms observed when ISC_ENABLE is executed upon completion of ISC_DISABLE

The case where the ISC_DISABLE instruction is loaded when the device is *not* in the ISC accessed system modal state is shown in Figure 8. When this occurs, the system modal state does not change.

4.4 System I/O pin behavior

System I/O pins of a device compliant with rules given herein have behavior summarized as follows:

- If an ISC instruction defined by this standard (see Clause 6) is loaded in the instruction register, the system I/O pins are controlled per 6.1.1, rule c), regardless of what system modal state the device may be in.

NOTE—An instruction is loaded in the instruction register on the falling edge of TCK in the *Update-IR* TAP controller state.

- If an IEEE Std 1149.1-2001 test mode instruction (EXTEST, INTEST, RUNBIST, CLAMP, HIGHZ) is loaded in the instruction register, the system I/O pins are controlled as defined by that standard regardless of what system modal state the device may have been in before the test mode instruction was loaded.

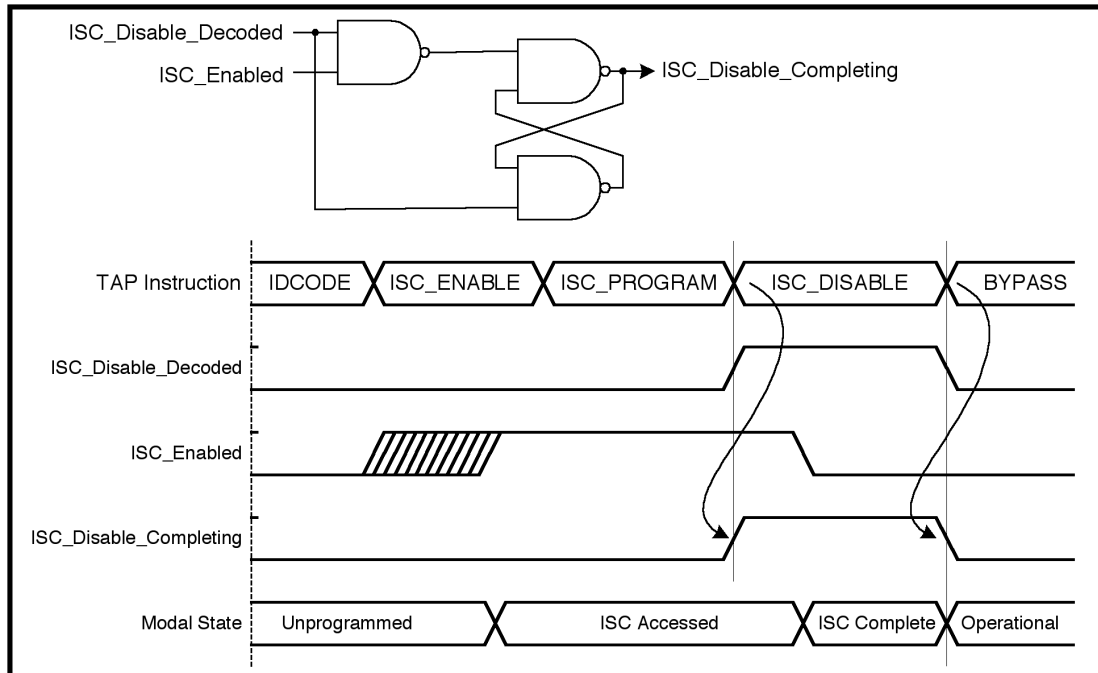


Figure 7—Derivation of the ISC_Disable_Completing signal. The circuit shown is conceptual as there are other implementations with the same result.

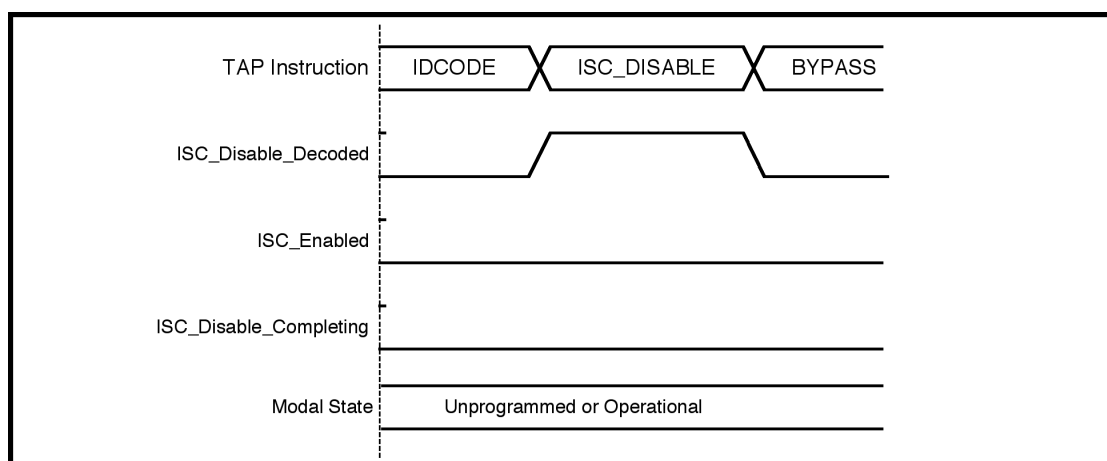


Figure 8—The system modal state remains unchanged and the ISC_Disable_Completing signal remains cleared when the ISC_DISABLE instruction is not properly prefaced with the ISC_ENABLE instruction.

- If an IEEE Std 1149.1-2001 nontest mode instruction (BYPASS, IDCODE, USERCODE, SAMPLE, PRELOAD) is loaded in the instruction register, the system I/O pin behavior is determined by the system modal state of the device when the instruction is loaded.

NOTE—The system modal state of the device cannot be changed by the *execution* of non-ISC instructions. The system modal state may, however, change from ISC complete to operational or unprogrammed upon *loading* any instruction other than ISC_DISABLE. The system modal state of the device can be changed by passing to the *Test-Logic-Reset* TAP controller state, potentially resulting in a change of system I/O pin behavior.

It is when an IEEE Std 1149.1-2001 nontest mode instruction is loaded in an ISC device that there is a choice of behaviors for the system I/O pins. These are summarized as follows:

- If the device is in the unprogrammed system modal state, the system I/O pins are disabled.
- If the device is in the ISC accessed system modal state, the system I/O pins are governed by 6.1.1, rule c).
- If the device is in the operational system modal state, the system I/O pins operate as determined by the programming of the device.

NOTE—If, at the point of time an IEEE Std 1149.1-2001 nontest instruction was loaded into the device, it was in the ISC complete system modal state, the device transitions to the operational or unprogrammed system modal state because the ISC_DISABLE instruction has been displaced.

When a device complying with this standard is in the operational modal state, it behaves as if it were a conventional device that contains both IEEE Std 1149.1-2001 testability circuitry and mission circuitry as shown in Figure 9. The typical programmable device contains a series of input-output modules (IOMs) that contain boundary-scan register cells and a three-state output driver. The boundary-scan register cells shown have the required capture flip-flop (C) and an update latch (U). The IOM depicted is fully bidirectional.

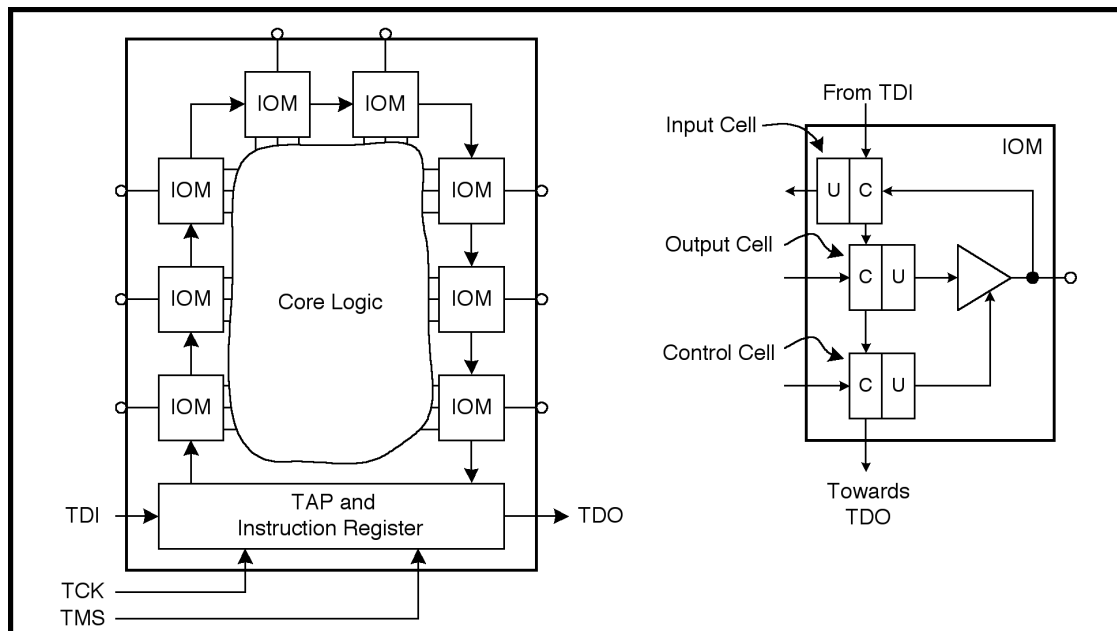


Figure 9—A programmed device and its connection to the boundary-scan register

NOTE—The IOM shown in Figure 9 can be implemented more efficiently with a single bidirectional data cell structure (see IEEE Std 1149.1-2001) rather than the two-cell data structure shown here for the sake of simplicity. This will eliminate 33% of the cells, saving silicon area as well as test data shift time and test program storage space.

When a device is configured, a given system I/O pin may be fully bidirectional, or limited to being an input, output, or unconnected pin. This limiting may be accomplished by tying the control cell input (the lowest cell in the IOM in Figure 9) to a fixed “0” or “1.” When a pin-permission instruction such as EXTEST is loaded into the instruction register, the driver data and control signals are derived from the update latches (U) as IEEE Std 1149.1-2001 requires.

NOTE—If a pin’s programming is “unused,” it should, at the very least, still be monitored by the input boundary-scan register cell of the IOM. The IOM could be treated as fully bidirectional, however, to allow a testing procedure to discover whether shorts exist from “unused” pins to other pins. This would allow the testing procedure to establish an identity (using the IOM driver) for the unused pin that the IOM receiver would verify. Testing even the unused pins for shorts will help discover manufacturing process problems and ensure the integrity of the system in the event the programming is subsequently changed such that unused pins are later used.

When a programmable device is in the unprogrammed system modal state and an IEEE 1149.1 nontest instruction is loaded, then there is, by definition, no core logic as shown in Figure 10. In order to meet the requirement [see 6.1.1, rule e)] that a device in the unprogrammed modal state have all of its drivers inactive, the control cell in the IOM should produce a logic level that will disable the driver, a “0” in this case. When a programmable device is in the ISC accessed or ISC complete modal states, then the device drivers should either be controlled by the boundary-scan register or be inactive as governed by 6.1.1, rule c). Example data cell designs are shown in Figure 11. Two example control cell designs that meet the two options for 6.1.1, rule c), are shown in Figure 12 and Figure 13.

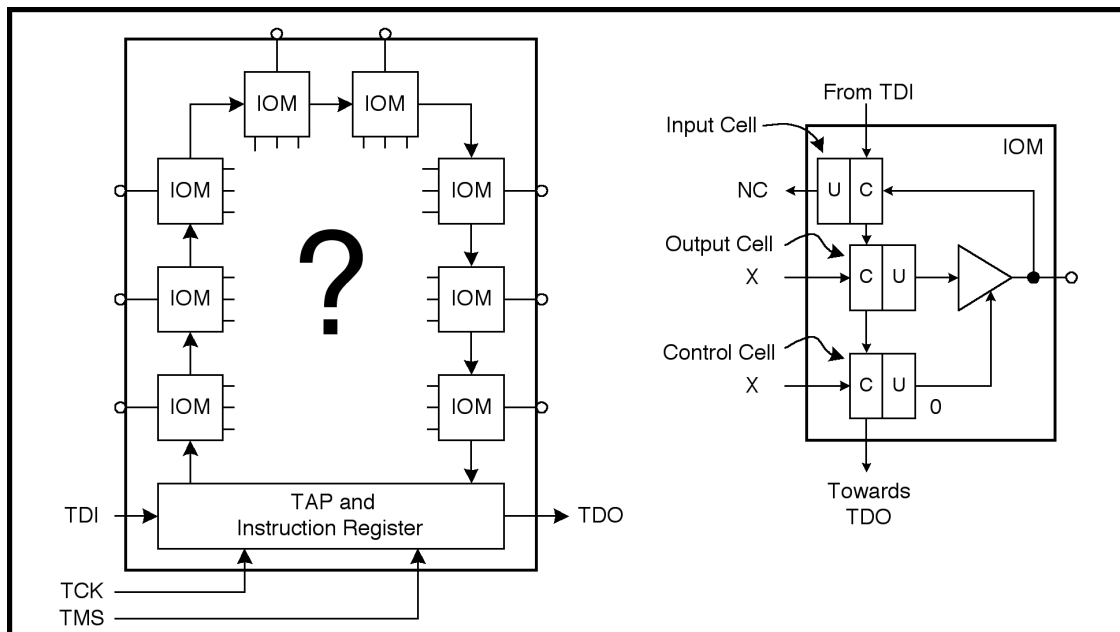


Figure 10—An unprogrammed device and how the unconnected IOM signals should be viewed

The data cell design shown in Figure 11, part A, used when the device is intended to exhibit the HIGHZ-like behavior [see 6.1.1, rule c)] is identical to a “generic” boundary-scan register data cell design from IEEE Std 1149.1-2001, which may be used for inputs or outputs. It does not make use of any of the specialized ISC signals defined by this standard. The “mode” signal is generated by the TAP instruction decoder as described in the table within Figure 11. Note that mode changes on the falling edge of TCK in the *Update-IR* TAP controller state.

NOTE—The cell shown in Figure 11, part A is known as “BC_1” in BSD. (See IEEE Std 1149.1-2001, subclause B.9, the standard VHDL package STD_1149_1_2001, and B.10.2, cell description constants, for information on describing boundary-scan cells.)

The data cell design shown in Figure 11, part B, uses ISC_Enabled to assure that when the device is intended to exhibit the CLAMP-like behavior [see 6.1.1, rule c)] it will pass the boundary-scan register content to the pin.

NOTE—With respect to the BSDL description (see IEEE Std 1149.1-2001) of the data cell design depicted in Figure 11, part B, while materially different in the output multiplexing structure from the cell design called BC_1 in BSDL, this design is still equivalent to BC_1. This is because the BC_1 structure describes the capture behavior of the cell and not the multiplexing structure on its output.

The control cell design incorporates ISC signals in its design to govern when an IOM driver is enabled or disabled, and where its source of control data comes from.

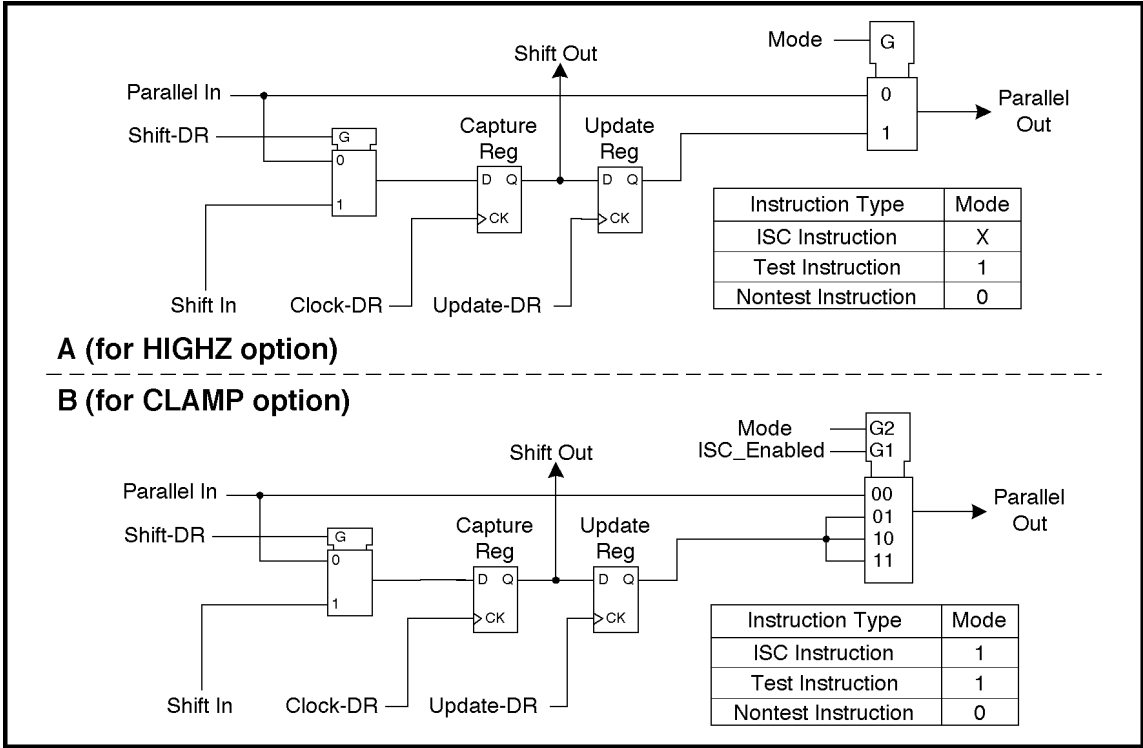


Figure 11—A possible data cell design that meets the requirements of this standard

Figure 12 shows a possible control cell design that will disable the system I/O pins whenever an ISC instruction is loaded or whenever a nontest instruction is loaded and the device is in the ISC accessed system modal state. Loading a test mode instruction will allow the boundary-scan register to control the state of the driver enable. The “Mode1” and “Mode2” signals are generated by the TAP instruction decoder as described in the table within Figure 12. Note that mode signals change on the falling edge of TCK in the *Update-IR* TAP controller state, but that the ISC_Enable and ISC_Done signals change at other times governed by the execution of certain ISC instructions. Thus, these signals cannot change while an ISC instruction is *not* loaded.

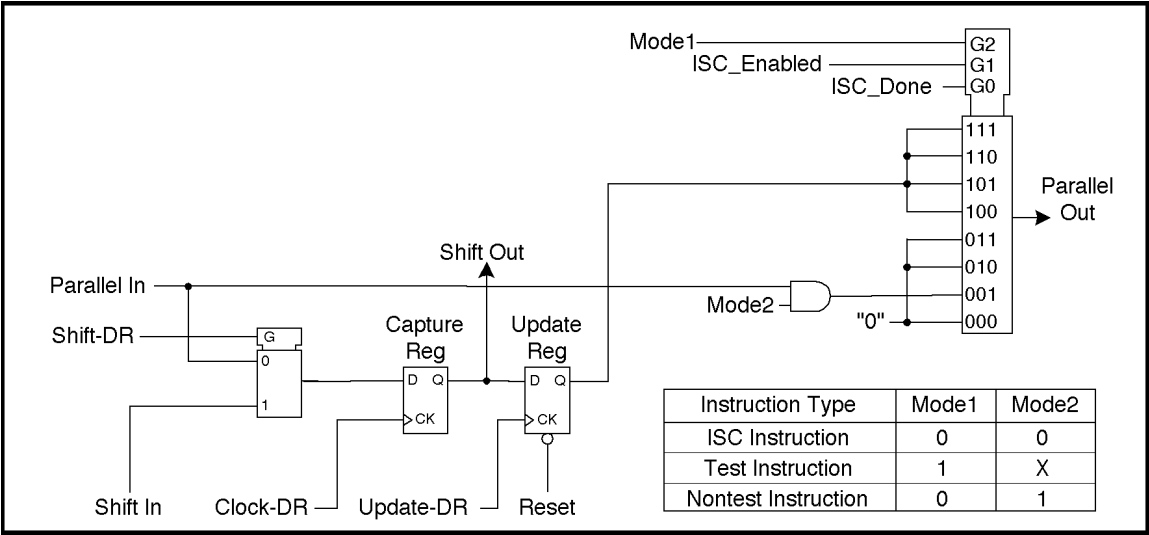


Figure 12—A possible (unoptimized) control cell design that satisfies 6.1.1, rule c), by disabling the system I/O pins

The control cell design in Figure 13 is similar except that it uses the boundary-scan register to control the output driver enable whenever an ISC (or test mode) instruction is loaded, as well as when a nontest instruction is loaded and the device is in the ISC accessed system modal state. This design has only one “mode” signal, which is derived per the table in Figure 13.

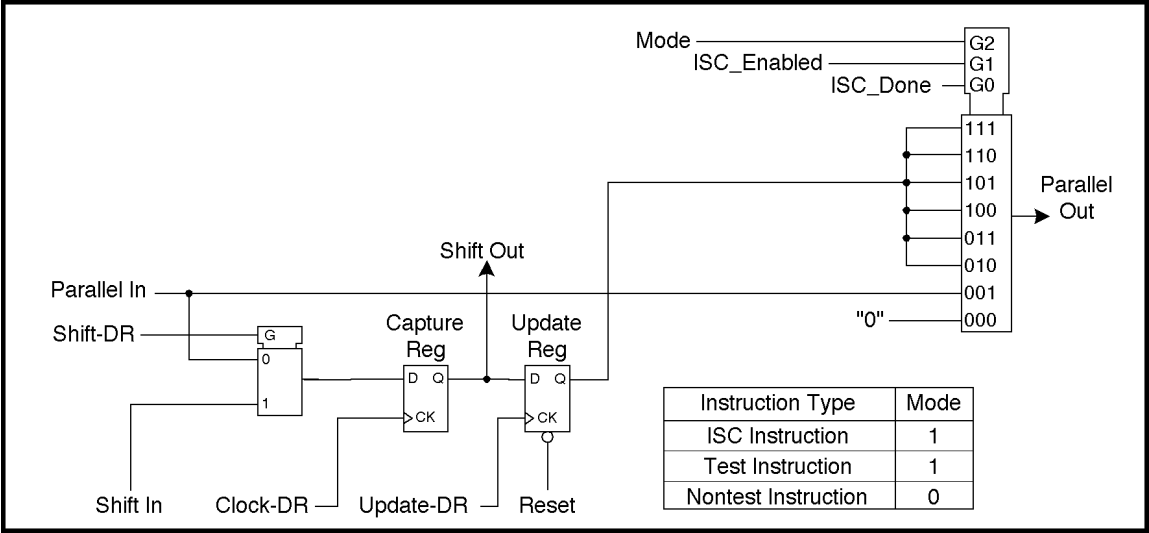


Figure 13—A possible (unoptimized) control cell design that satisfies 6.1.1, rule c) by using the boundary-scan register to control the system I/O pin state

Both of the designs in Figure 12 and Figure 13 have been shown in an unoptimized form for clarity. A designer would probably spend some effort on optimizing the speed of a single path (parallel in to parallel out). All other paths are low speed and may be compromised accordingly.

NOTES:

1—With respect to the BSDL description (see IEEE Std 1149.1-2001) of the control cell designs depicted in Figure 12 and Figure 13, while materially different in the output multiplexing structure from the cell design called BC_1 in BSDL,

these designs are still equivalent to BC_1. This is because the BC_1 structure describes the capture behavior of the cell and not the multiplexing structure on its output.

2—A BC_7 cell design (a single-celled bidirectional data cell structure) can be modified in a similar way.

5. ISC architecture

5.1 Overview

5.1.1 Classification of system pins

This standard recognizes that multiple functions may be placed upon a single integrated circuit die and that some of these may be programmable logic functions addressable by this standard and others may be conventional (nonprogrammable) electronic structures. In some cases, it may be important to differentiate system I/O pins based on the recognition that they are connected to programmable functionality or fixed functionality.

The differentiation of system I/O pins is based on whether their I/O functions (input, output, bidirectional) are programmable by the ISC programming process. This excludes other types of pin configuration capability that could exist for pins that may determine parametric factors such as logic voltage levels, drive currents, pull-up or pull-down functions, etc., that any pin may also possess.

5.1.1.1 ISC system pins

ISC system pins are those pins whose I/O functions (input, output, or bidirectional) are established by configuration information installed by the ISC programming process. Further, additional I/O pins *chosen by the device designer* may also be designated as ISC system pins. All ISC system pin behavior is determined by the system modal state as discussed in 4.4. Except where specifically noted in this document, the term “system pin” will be synonymous with “ISC system pin.”

5.1.1.2 Fixed system pins

Fixed system pins are those whose I/O functions (input, output, or bidirectional) are not determined by configuration information installed by the ISC programming process, *and have not been designated as ISC system pins by the device designer*. Fixed system pin behavior is completely specified by IEEE Std 1149.1-2001. This, along with the fact that ISC instructions operate within system modal states (see 4.1) implies that fixed system pins may be fully operational *while ISC programming activities are in progress*. To reiterate, fixed system pins are in system mode when ISC instructions are being executed.

NOTE—Thus the designation of fixed and ISC system pins may be predicated solely on their relationship with the programmable portion of a device or may be arbitrarily designated as ISC system pins at the discretion of the device designer. This allows the designer to determine the I/O behavior of *any* pin on the device while it is being programmed. This has important consequences as the following example shows.

An example of a device with both fixed and ISC system pins is shown in Figure 14. In this device, a microcontroller and a programmable logic device have been integrated onto the same IC substrate. When first powered up (and with no programming present within the programmable section), the ISC system pins are disabled and the fixed pins are active, allowing the microcontroller to perform its function. Subsequently, through the TAP, the programmable portion of the device can be configured. While this is going on, the ISC system pins are either disabled or fixed by a pattern held in the boundary-scan register. The fixed pins, at the same time, are free to perform system functions. Finally, when the ISC portion of the device is fully configured, the ISC system pins take on their system function when the ISC_DISABLE instruction is displaced. Notice that the controller that actually programmed the ISC portion of the device may have been the microcontroller on the same substrate, along with other external circuitry not shown.

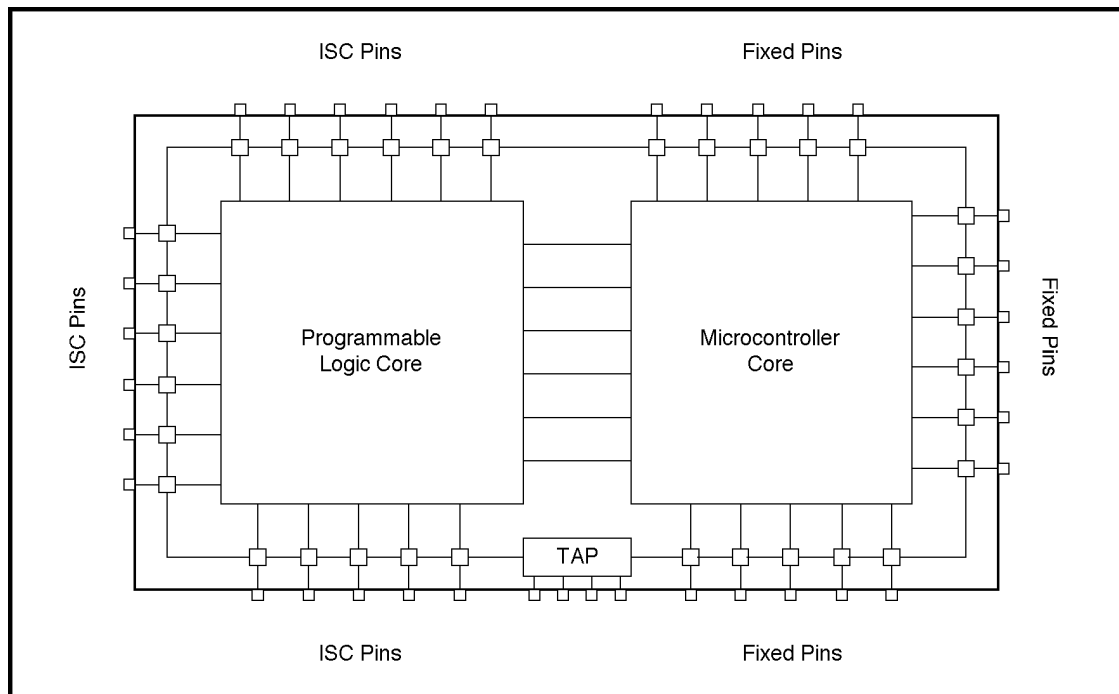


Figure 14—A device containing both programmable and nonprogrammable logic, with associated pins

NOTES:

1—In Figure 14 there are connections between the programmable and nonprogrammable cores. These may or may not have boundary-scan register cells at the discretion of the designer, but in either case, when the programmable core is unprogrammed, the nonprogrammable logic should perform appropriately.

2—The designer of a device containing less intelligent nonprogrammable logic could, if desired, design *all* I/O pins as ISC system pins. Then, all pins would be disabled or fixed at static states during the programming process.

5.1.2 Test access port (TAP)

A device compliant with this standard will possess a TAP containing four (optionally five) pins labeled test clock (TCK), test mode select (TMS), test data input (TDI), and test data output (TDO). The optional fifth pin is test reset (TRST*), which is active low. These pins are dedicated and may not be shared with other functions.

5.1.3 IEEE Std 1149.1 compliance enable pins

IEEE Std 1149.1-2001 contains, in subclause 4.8, “Subordination of this standard within a higher level test strategy,” the concept of compliance enable pins. These are one or more pins that must be statically conditioned with a set of logic states before the 1149.1 facilities within the device are guaranteed to be compliant. Further, these pins must be maintained at those states for the duration of any 1149.1-based activities. Such pins may exist on devices that comply with this standard and are thus required to be conditioned before and during all ISC activities.

NOTE—Signals associated with compliance enable pins are *not* included in the boundary-scan register, per IEEE Std 1149.1-2001.

5.1.4 Programming voltage pins

For systems requiring over-voltage programming, allowance may be made for one or more static programming voltage pins used to supply energy for the physical programming process [see 5.2, rule s)]. ISC devices shall interpret all instructions in the same manner, and the programming voltage pin(s) may not be used to signal additional data or control functions.

5.1.5 TAP controller and instruction unit

The TAP is used to drive a 16-state finite state machine called the TAP controller, completely specified by IEEE Std 1149.1-2001. This state machine controls all aspects of the test logic and the ISC programming process.

Each compliant device contains an instruction register and instruction decoder. This unit, along with signals derived from the TAP, is used to sequence activities within the test and ISC logic.

5.1.6 Mandatory instructions from IEEE Std 1149.1-2001

Mandatory instructions from IEEE Std 1149.1-2001 are required; SAMPLE, PRELOAD, BYPASS, and EXTEST. Programmable devices are also required to implement the IDCODE and USERCODE instructions. See 6.2 for additional mandatory instructions specified by this standard.

5.1.7 Data registers

All devices adhering to this standard are required to implement the bypass register, the boundary-scan register, and the device identification register from IEEE Std 1149.1-2001. In addition, specific registers targeted by ISC instructions documented in this standard are also required. (See Clause 7.)

5.1.8 Modal state control signals

As discussed in Clause 4, the system state of a programmable device conforming to this standard has four identified modal states. Two control signals are required to identify which of these modal states the device currently resides within.

5.1.8.1 ISC_Done

This signal, which is nonvolatile in programmable devices that are nonvolatile, is used to indicate that a device has been programmed to the satisfaction of an external programming algorithm. In volatile devices, this signal is initially clear upon power-up.

5.1.8.2 ISC_Enabled

This volatile signal, initially clear when a programmable device is first powered, is set by the successful execution of the ISC_ENABLE instruction [see 5.2, rule j)]. This signal is cleared by the execution of the ISC_DISABLE instruction or by passage of the TAP controller to the *Test-Logic-Reset* TAP controller state [see 5.2, rule k)]. This signal must be set for other ISC instructions to operate correctly.

5.1.9 Optional status indication

An optional status indication scheme is defined by this standard. If this status indication scheme is implemented in a device, it shall adhere to rules given in 5.2.

NOTE—A designer is free to implement a private status indication scheme if desired, but tools designed to work with this standard will not be able to determine status unless specifically modified to recognize this private functionality.

As described in 6.1, each ISC instruction causes events to occur that are initiated by entering the *Run-Test/Idle* TAP controller state and remain there for some minimum duration. It is possible that errors could be sensed by the circuitry responding to an instruction that would be useful information for an external programming algorithm. This algorithm could branch to appropriate exception handling routines when it observed errors reported by the status indication.

As all ISC instructions place some data register between TDI and TDO, the data register may be loaded with a status indication field in the *Capture-DR* TAP controller state. This field is (at minimum) the least two significant bits of the register and indicates the status of the ISC instruction functionality that was last executed in the *Run-Test/Idle* TAP controller state.

NOTE—If the status indication field is implemented, then all ISC data registers are required to be a minimum of two bits long. As seen in Clause 6 and Clause 7, some ISC registers may be defaulted to the bypass register. This default is not compatible with the implementation of status reporting since the bypass register is only one bit long.

Figure 15 gives a structure for the registers that may at some time appear between TDI and TDO. Status reporting can be added by appending a two-bit (minimum) register onto the ISC data registers as shown in Figure 16.

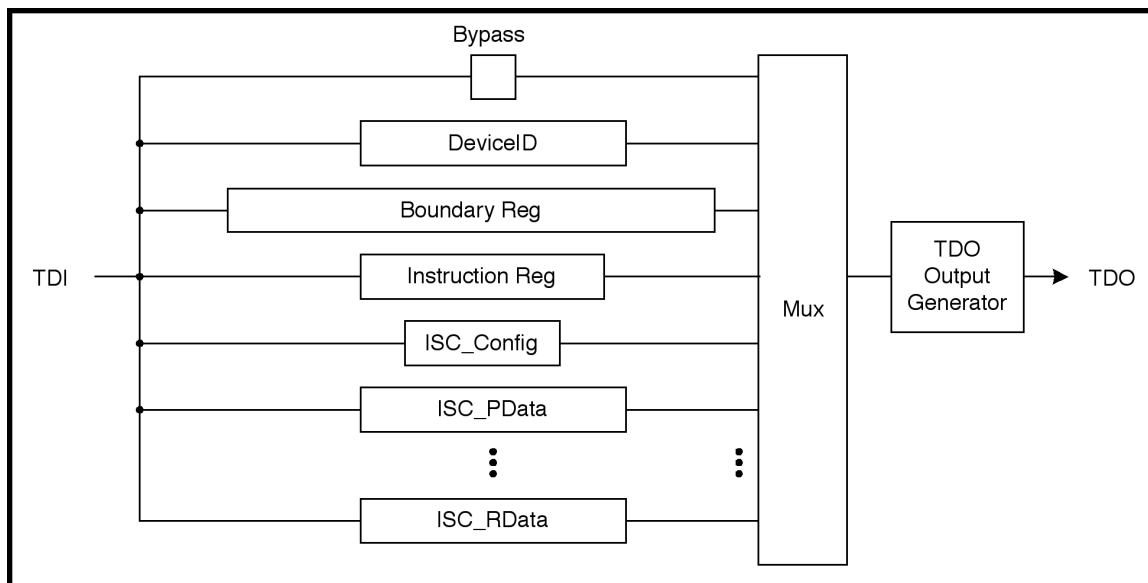


Figure 15—Structure of registers placed between TDI and TDO when there is no status reporting

Simply appending a status field to each register lengthens each by two (or more) bits. This simple model is consistent with the rules in IEEE Std 1149.1-2001 concerning the concatenation of registers: the concatenated register paths (between TDI and TDO) must have a single unique name. Thus, there is no “status” register addressable by some instruction, only the normal ISC register set extended by two (or more) bits. In a more sophisticated implementation, a designer could reuse the least significant bits of most ISC data registers as status bits that are captured in the *Capture-DR* TAP controller state. Note that registers, such as *ISC_RData* (see 7.7), *must* be extended in length to prevent the status bits from overwriting data that is intended to be read back.

The status field indicates the execution status of the current instruction if the *Capture-DR* TAP controller state is entered after *Run-Test/Idle*. The status of the previously executed ISC instruction can be observed by entering *Capture-DR* after loading a new ISC instruction, but before entering the *Run-Test/Idle* TAP controller state.

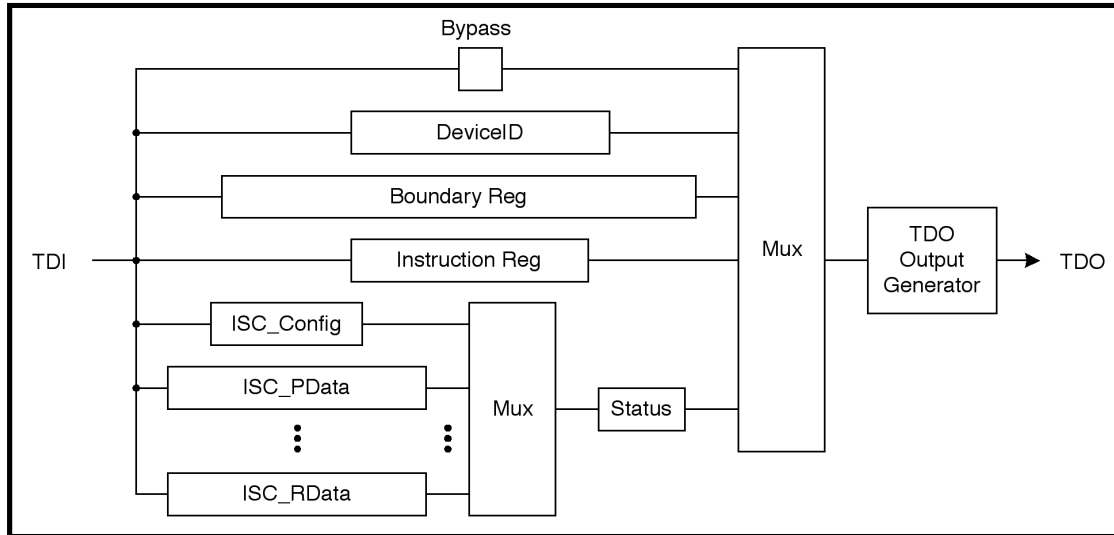


Figure 16—Insertion of a status reporting register at the least significant two bits of the ISC data registers

NOTE—The ISC_NOOP instruction may be used as a status query instruction. However, it will return status of the last executed ISC instruction. If ISC_NOOP is executed a second time, then the status shifted out will be that of the previous ISC_NOOP execution.

Status bits may be manipulated at other times by instructions during their execution. For example, upon first entry into the *Run-Test/Idle* TAP controller state, instructions may load the status register with an error code that indicates the required duration in the *Run-Test/Idle* TAP controller state has not expired. After the duration has expired (but before leaving the *Run-Test/Idle* TAP controller state), the status code may be updated to a nonerror state. If the instruction is not allowed to complete its required duration (by leaving the *Run-Test/Idle* TAP controller state early), the content of the status field subsequently captured will indicate an error.

The ability to observe instruction execution status allows external programming algorithms to respond to errors more closely to the time when they occur. This can allow a programming process to immediately abort or take some remedial action. If status indication is not implemented, an algorithm can still make basic checks, but a substantial amount of time and activity may pass between the occurrence of the error and when it is detected. For example, an ISC_PROGRAM instruction may sense the failure of a data packet to be programmed and present this to an algorithm via the status field. If status is unavailable (or not checked) the algorithm may continue programming all subsequent locations (which may also be failing) and not see any error until a verification process is then executed. Notice that if verification has been made impossible by the activation of a read-protection security mechanism, then the error(s) could not be detected.

The status register may be constructed as shown in Figure 17. At a minimum, it contains a 2-bit error code that is used to indicate the status of an executed instruction (see 5.2 and 6.1.1). Optionally, it may also contain an N-bit field containing additional information subcodes defined by the device designer to convey the cause of an error. Two examples are 1) the minimum duration for time spent in the *Run-Test/Idle* TAP controller state was not met [see 6.1.1, rule i)], and 2) a security violation prevented the instruction from operating [e.g., read-security has blocked ISC_READ instruction execution (see 5.1.10.1 and 6.3.1)].

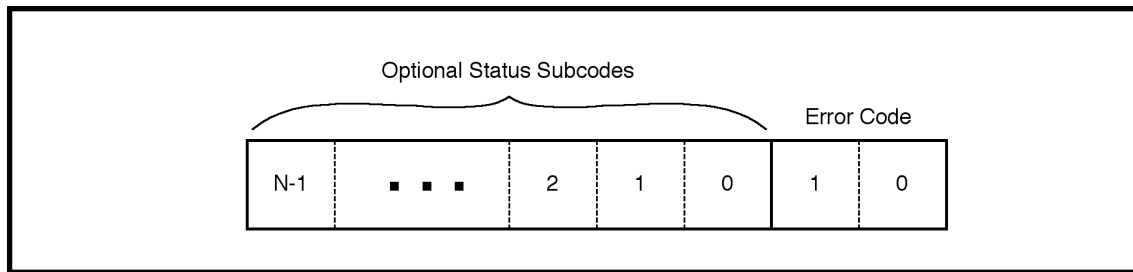


Figure 17—Status register with optional subcode bits

5.1.10 Optional security provisions

An optional security mechanism is provided by this standard. Security features, when activated, prevent unwanted activities such as reading out programming data, changing programming data, or unauthorized erasure. This security mechanism is intended to work in conjunction with the optional `ISC_PROGRAM_SECURITY` instruction (see 6.4.3) or with `ISC_PROGRAM`. This security mechanism is very flexible and contains several options that allow it to implement all security features known to be in use as well as a richer set of capabilities.

The main features of the security mechanism defined herein are:

- a) It allows up to three discrete forms of protection: read-protection, program-protection, and erasure-protection.
- b) It provides for the implementation of a “key” that will allow a user to “unlock” protection. A user can generate the key rather than it being hardwired by the IC vendor.
- c) A “permanent” lock feature may be added that, when activated, will prevent any subsequent modification of security.
- d) The key may be encrypted by an on-chip function before it is stored, such that knowledge of the original key is not sufficient to unlock security.
- e) The architecture of this security mechanism may be reduced in complexity to offer only the most basic read-protection at very low cost, emulating those capabilities used in past devices.

The security mechanism is based upon an internal protection control (IPC) register that is nonvolatile in programmable devices that are nonvolatile. This register contains one, two, or three discrete bits used to control the form(s) of security, an additional (optional) N-bit key field, and optional space for other functions (such as optional sector selection), as needed by the designer.

Figure 18 shows a general architecture of this security mechanism with all three forms of security implemented independently. The IPC register is divided into a 3-bit field for function disable signals and an N-bit key field. This register is programmed by `ISC_PROGRAM_SECURITY` (see 6.4.3), which transfers the contents of the `ISC_PData` register (see 7.6) into the IPC register. This transfer occurs upon the successful completion of the instruction and may be conditioned by some additional factors. In Figure 18, the transfer is allowed when the key bits in the IPC register are all-zero or match those in `ISC_Pdata`, and the key bits in IPC are not all-ones. The “all-ones” key is used as a permanent lock; once the all-ones key is installed (and erasure has been disabled) there is no way to update the IPC register in the future. This permanently establishes the states of the three security signals. (Note it is assumed that the initial state of the IPC for a blank device is all-zero.) The all-zero code may be thought of as “no security.” The all-zero code is the only code that can be directly overwritten. Once a key (containing both 1s and 0s) has been entered, it cannot be changed directly to another key. Note that `ISC_ERASE` (if not disabled) may be used to zero out the IPC register. Thus, erasure is the only means for changing a nonzero security key.

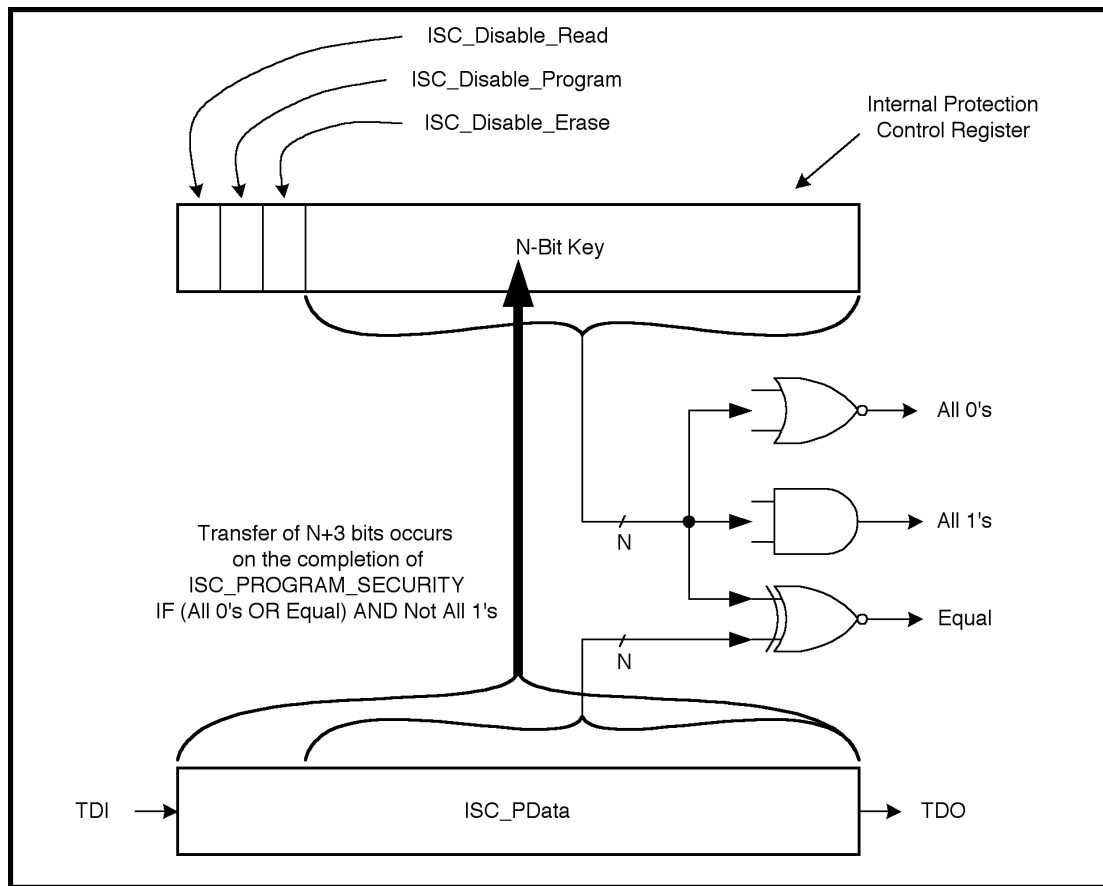


Figure 18—Architecture of the optional security mechanism

This architecture may be simplified by removing one or two of the security signals if they are not desired, by sharing any combination of security signals, by removing the all-ones permanent lock feature, or by removing the key field altogether. The architecture may implement stronger security by encoding the key while it is being transferred such that the original key will not match the stored key. This encoding may be made entirely general by making it a function of other bits previously stored elsewhere in program memory. This range of implementation options allows any level of security, from none to arbitrarily strong keyed security to permanent locking. Further, all known security systems previously developed are subsets of this general capability.

5.1.10.1 ISC_Disable_Read

This optional signal, which is nonvolatile in programmable devices that are nonvolatile, is used to indicate to the ISC_READ instruction (see 6.3.1) that the device programming data is secured and should not be read out. This signal may be controlled by an independent bit of memory, or it may share a bit with one or both of the other disable signals. If the optional status indication capability (see 5.1.9) is implemented, then the fact that read back has been inhibited can be indicated. Read-protection is often used to inhibit malicious or inadvertent exposure of system design details.

5.1.10.2 ISC_Disable_Program

This optional signal, which is nonvolatile in programmable devices that are nonvolatile, is used to indicate to the ISC_PROGRAM instruction (see 6.2.3) that the device programming data is secured and should not be

overwritten. This signal may be controlled by an independent bit of memory, or it may share a bit with one or both of the other disable signals. If the optional status indication capability (see 5.1.9) is implemented, then the fact that programming has been inhibited can be indicated. Program-protection may be used to inhibit malicious or inadvertent overwriting of existing program data.

5.1.10.3 ISC_Disable_Erase

This optional signal, which is nonvolatile in programmable devices that are nonvolatile, is used to indicate to the ISC_ERASE instruction (see 6.3.2) that the device programming data is secured and should not be erased. This signal may be controlled by an independent bit of memory, or it may share a bit with one or both of the other disable signals. If the optional status indication capability (see 5.1.9) is implemented, then the fact that erasure has been inhibited can be indicated. Erase-protection may be used to inhibit malicious or inadvertent erasure of existing program data.

5.1.11 Programmable memory array access

A programmable logic device (PLD) contains a memory array that holds the configuration data that determines the programmed function of the device. A basic model is shown in Figure 19. Note that it is composed of a number of rows of data, some of which may contain blank or unused bits. An address and data register are used to access the array. The data register must be wide enough to accommodate the longest row of data. When rows containing unused locations are accessed, corresponding locations in the data register are “don’t care” locations.

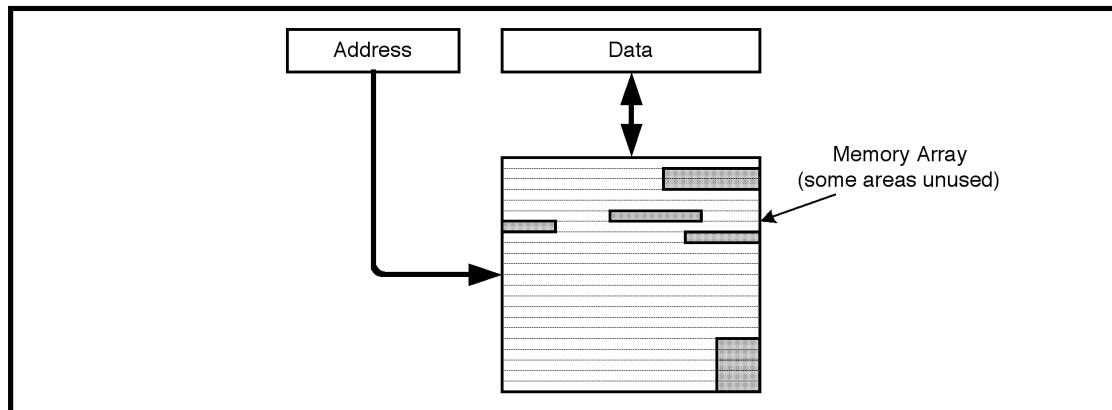


Figure 19—Basic model of a PLD configuration memory

The rules in this standard are designed to precisely and unambiguously define an access methodology for in-system configuration of programmable logic devices, but at the same time, offer designers a high degree of freedom in the design of the internal programmable structures. Thus, a device designer has many options for delivering address and data information to the internal memory array(s). Figure 20 shows a very basic access concept, where the address and data registers are linked together as one shiftable ISC register. Address and data can be shifted in or out of these two registers via the TDI/TDO shift path, thus setting up a program or read cycle to be executed by ISC instructions. The combination of address and data registers can be labeled the ISC_PData and ISC_RData registers as is allowed by IEEE Std 1149.1-2001. (See Clause 7 for a discussion of ISC data registers.) Whenever an operation on the memory array is done, a full scan of address and data is required.

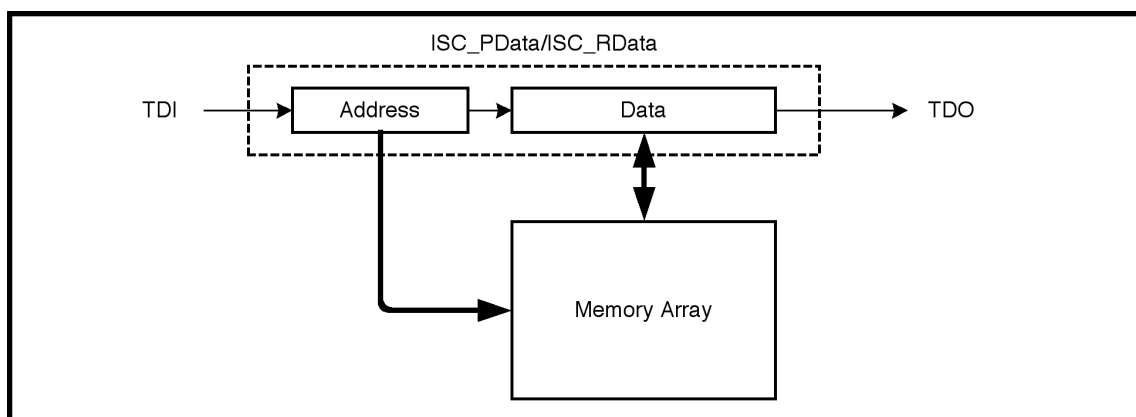


Figure 20—Basic programmable memory array access

A different memory access scheme is shown in Figure 21. Here, the address register can be independently accessed (see the ISC_ADDRESS_SHIFT instruction, 6.5.4) to initialize an address. The data register can be accessed directly by the ISC_PROGRAM instruction (6.2.3) or ISC_READ instruction (6.3.1). This scheme still requires that address and data both be shifted into the device to program a single location.

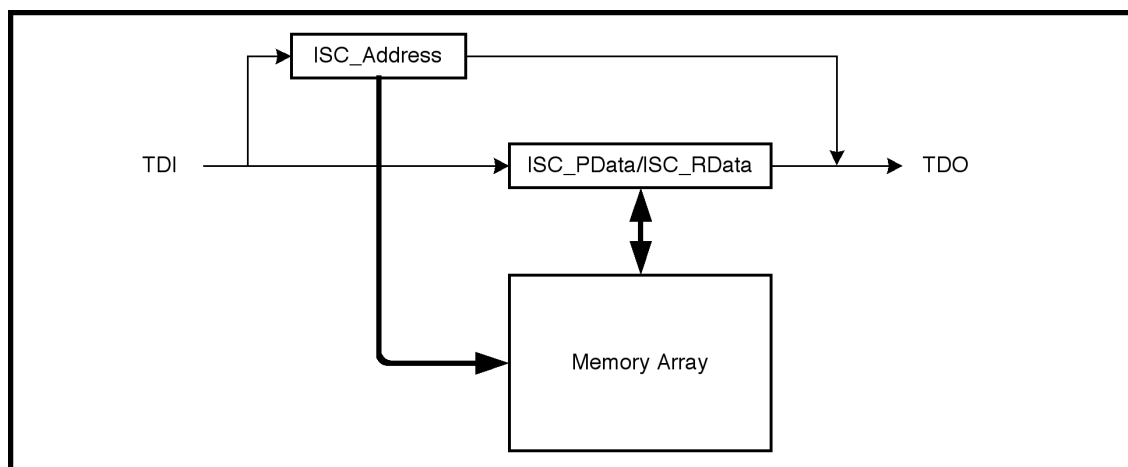


Figure 21—A structure with individual access to address and data

A more sophisticated approach simply adds address generation logic (see Figure 22). This logic may perform an auto-increment function, even skipping unused addresses in a fragmented address space. The triggering of this function may be tied to the programming and reading instructions to coordinate the programming of successive memory locations without the need for loading the address register for each. This may greatly reduce the time and amount of data shifting (and storage) needed for linearly accessing long memories.

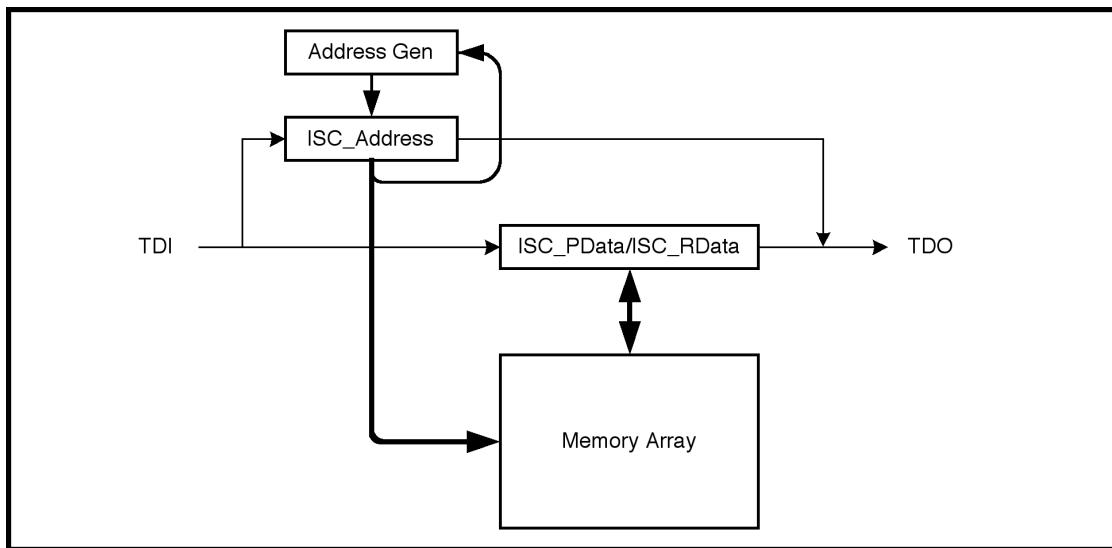


Figure 22—Memory array access with independently controlled address and data registers

It is also possible that the memory data for a programmable device is stored in more than one array, as shown in Figure 23. In this situation, there are two memory arrays with different lengths, widths, and even different burn times. By selecting an address scheme, such as having the high order address line select between the two arrays, it is possible to use the same structure seen earlier for accessing memory. Memory can be accessed linearly as one block, although a change in duration in the *Run-Test/Idle* TAP controller state may be needed when the array boundary is crossed.

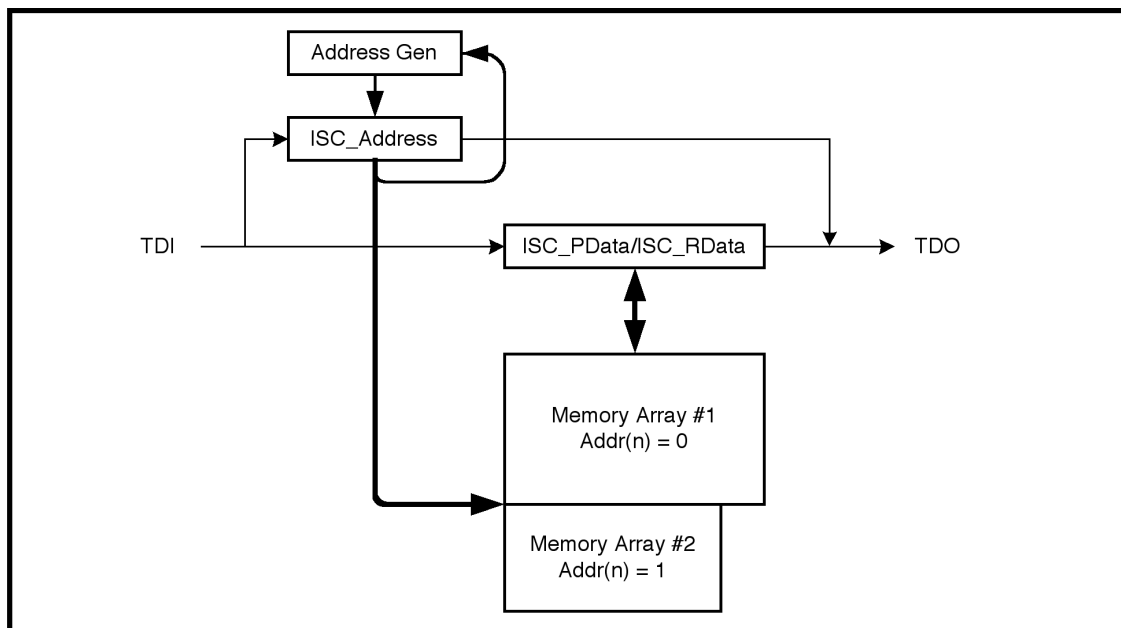


Figure 23—Accessing two memory arrays with different dimensions

A similar situation is shown in Figure 24 where a device contains two quite different arrays of memory, one being volatile and the other nonvolatile. The selection between them is controlled by a bit in the *ISC_Config*

register, which may control other important parameters as well. In this case, the ISC_ENABLE instruction effectively chooses which array will be accessed. Such a device on a board may have its nonvolatile content supplied once during board manufacture, and the volatile content refreshed while on-line in the field. Proper execution of ISC_ENABLE will prevent programming of the volatile content from interfering with the nonvolatile content.

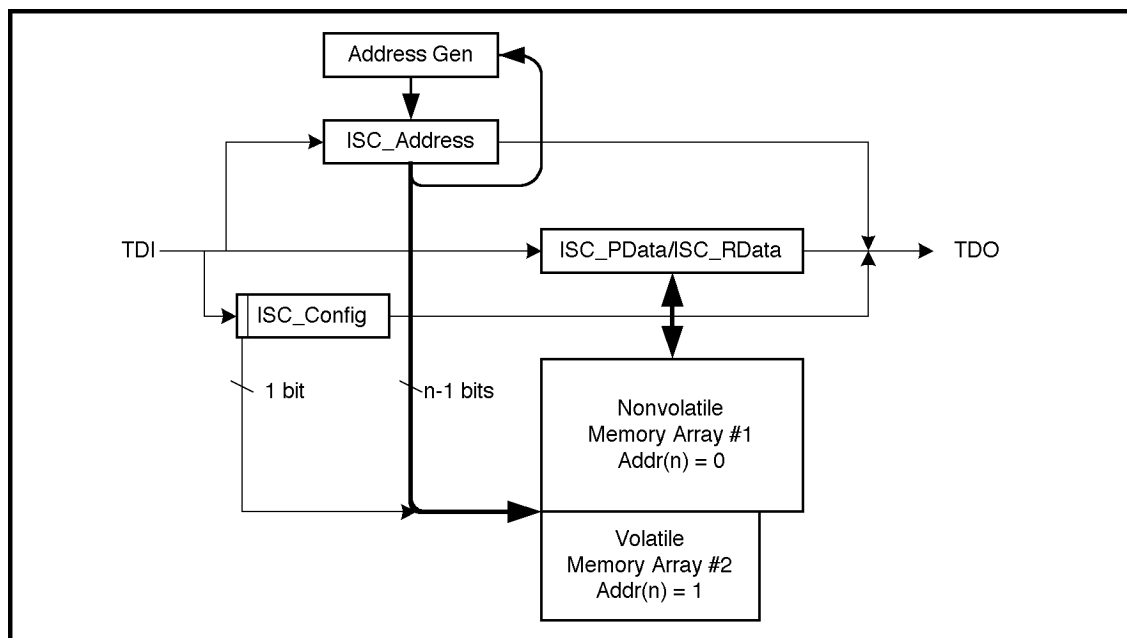


Figure 24—A programmable device with two embedded technologies

Figure 25 shows a scheme where the address register is not directly accessible from the outside, but is controlled by a short (perhaps 1-bit) command field appended to the data register. One command could initialize the address register and a second could increment it. While this again shortens the volume of data that must be scanned into the device, it has less addressing flexibility in that the start of a memory operation cannot be set to an arbitrary location.

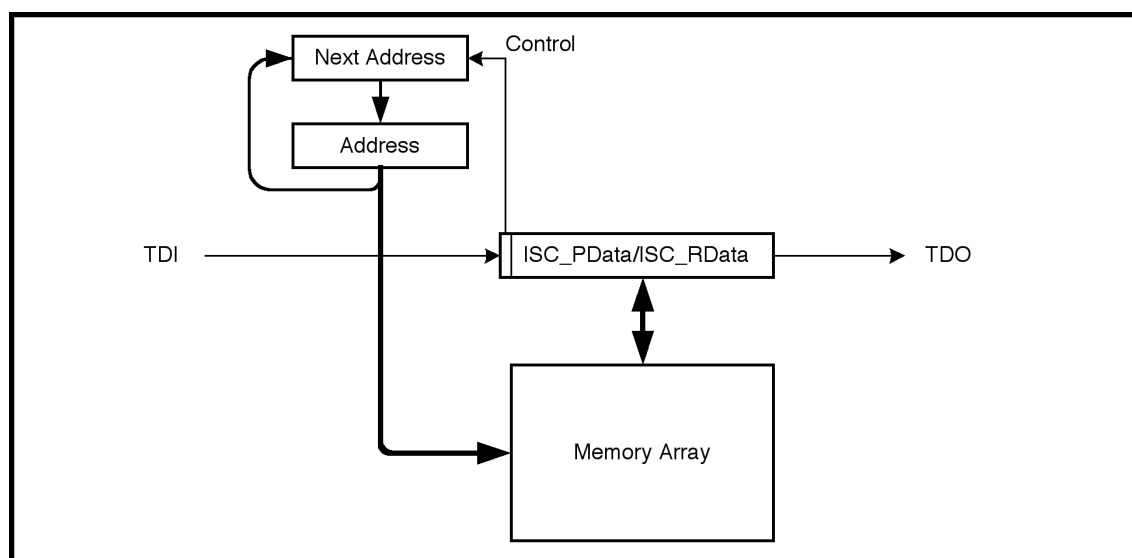


Figure 25—An approach where there is no direct access to the addressing structure

The inventiveness of a device designer has few constraints imposed by this standard. At least five access approaches may be utilized:

- a) The address may be directly loaded into the ISC_Address register (see 7.11) by previous use of the ISC_ADDRESS_SHIFT instruction (see 6.5.4). This is called explicit addressing.
- b) The address may be auto-initialized to the start of the array by the act of loading an ISC instruction destined to access memory. Subsequent accesses may automatically increment the addressing mechanism to the next valid entry. This is called implicit addressing.
- c) An address may be shifted into the ISC_RData or ISC_PData registers in the *Shift-DR* TAP controller state where, upon passing the *Update-DR* TAP controller state, it is then loaded into an addressing register [for example, see permissions 6.3.1.1, rule e) and 6.3.1.1 rule f)].
- d) Address control commands may be shifted into the ISC_RData register in the *Shift-DR* TAP controller state where, upon passing the *Update-DR* TAP controller state, the commands control an addressing register [for example, see permissions 6.3.1.1, rule e) and 6.3.1.1, rule f)]. These commands may cause actions, such as initializing the address, incrementing it, decrementing it, shifting it, adding an offset, etc.
- e) A combination of these methods may be implemented.

The actual technology of the addressing method is not specified by this standard, again allowing the designer freedom to use binary addressing, one-hot addressing, address encoding, etc.

5.2 Specification

Rules

- a) A component conforming to this standard shall first conform to all mandatory provisions of IEEE Std 1149.1-2001.
- b) The component shall conform to all rules within IEEE Std 1149.1-2001 that are specified for programmable devices.

NOTE—Rule b) assures that the normally optional IDCODE and USERCODE instructions are understood to be mandatory for devices conforming to this standard.

- c) The system mode (described by IEEE Std 1149.1-2001) of a component conforming to this standard shall be organized as four system modal states—*unprogrammed*, *operational*, *ISC accessed*, and *ISC complete*—as given in Clause 4.

NOTE—System modal states are determined by the ISC_Done and ISC_Enabled signals (along with a derived signal ISC_Disable_Completing) as shown in Figure 3. The following rules govern the derivation and timing of these signals.

- d) The component shall contain an ISC_Done signal that is nonvolatile in nonvolatile programmable devices and that is cleared during power-up in volatile programmable devices.
- e) When the ISC_Done signal is not protected by an enabled protection mechanism, the ISC_Done signal shall be set by exactly one of three choices of implementation:
 - 1) By successful completion of the ISC_DISABLE instruction when a specified data pattern is in place in the ISC_Config register (see 6.2.2).
 - 2) By successful completion of the (optional) ISC_PROGRAM_DONE instruction (see 6.4.1).
 - 3) By successfully writing a specified bit or set of bits to the program memory using the ISC_PROGRAM instruction (see 6.2.3).