

IEEE Standard for Static Component Interconnection Test Protocol and Architecture

IEEE Computer Society

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IEEE Standard for Static Component Interconnection Test Protocol and Architecture

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Abstract: IEEE Std 1581 defines a low-cost method for testing the interconnection of discrete, complex memory integrated circuits (ICs) where additional pins for testing are not available and implementing boundary scan (IEEE Std 1149.1™) is not feasible. This standard describes the implementation rules for the test logic and test mode access/exit methods in compliant ICs. The standard is limited to the behavioral description of the implementation and will not include the technical design for the test logic or test mode control circuitry.

Keywords: board test, connectivity test, IEEE 1581, integrated circuit, interconnect test, interconnection test, memory device, test logic, test mode, transparent test mode

The Institute of Electrical and Electronics Engineers, Inc.
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Introduction

This introduction is not part of IEEE Std 1581-2011, IEEE Standard for Static Component Interconnection Test Protocol and Architecture.

In 1999, an idea was presented, at the International Test Conference (ITC), on testing the interconnections between certain complex memory devices that do not comply with IEEE Std 1149.1 and other IEEE 1149.1 devices on a printed circuit board (PCB). The process of testing for interconnections is also referred to as *interconnect testing* and *connectivity testing*. The complex memories at which this technique is directed are those that cannot be conveniently tested using static test techniques, such as boundary scan, because they involve high frequencies. Another reason is that those devices often contain a state machine that can be exercised only using data and address lines that are yet to be tested. The idea presented was a test method comprising a combinational function designed into the memory. The combinational function replaced the memory function when the test mode was activated and did not otherwise interfere with memory operation of the memory. Thus, the complexity of the memory may be bypassed during test by the combinational function. The idea was described in two papers. One paper described the theoretical background of the combinational function in relation to detection and diagnosis of defects (Biewenga et al. [B1]).^a The other paper described a practical approach: an implementation in synchronous dynamic random access memory (SDRAM) (de Jong et al. [B2]).

The novel idea attracted much attention from the test community. A fringe meeting at ITC was held and resulted in a plan to have this idea captured within a test standard. Since implementation would be within the silicon of memory devices, standardization was planned to start within JEDEC Solid State Technology Association (JEDEC). It was later decided to first develop an IEEE standard, as this approach would lead to a more extensive and unambiguous description of the implementation. The continued need for JEDEC involvement was, however, clearly recognized.

In 2000, first attempts were made to form a study group of people enthusiastic about this novel test concept. This group was the precursor of the IEEE working group. At the beginning of 2001, the P1581 Working Group was officially formed after having had two preliminary telephone conferences. Shortly after formation of the working group, one member found an alternative to the method first introduced in 1999. This method, a simple extension of traditional connectivity tests such as NAND trees, etc., was brought to the attention of the working group in 2001. In addition, the original proposal for standardization was extended with a number of test mode entry/exit methods as well as a set of general rules for test logic implementations. This standard is the result of the work performed to date by the P1581 Working Group.

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^a Numbers in brackets correspond to the numbers in the bibliography in Annex A.

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Participants

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Heiko Ehrenberg, *Chair*
Bob Russell, *Vice Chair*
Adam Ley, *Secretary*
Frans de Jong, *Chair Emeritus*
Leon van de Logt, *Editor Emeritus*

Steve Butkovich
Jeff Halnon
Joseph Kadaras

Shuichi Kameyama
Mike Laisne
Kenneth P. Parker

Rob Raaijmakers
Bambang Suparjo
Bradford van Treuren

In the development of this standard, the working group was supported by many other individuals from many other organizations. The working group wishes to acknowledge the following people:

Henrik Andersson
Dave Bonnett
Ben Bennetts
Ian Burgess
C. J. Clark
Luis Cordova
Adam Cron

Ray Dellecker
Ted Eaton
Peter van den Eijnden
Bill Eklow
David Ford
Bill Hovis
James Huang

Dennis Lia
Patrick McHugh
Gordon Robinson
Pralhadrao Vasantbhatt
Shantagiri
Donald Smith
Bernard Sutton

The following members of the individual balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

Keith Chow
Frans G. De Jong
Thomas Dineen
Heiko Ehrenberg
Timothy Ehrler
Ron Greenthaler
Randall Groves
Jeff Halnon
P. Harrod

Werner Hoelzl
Robert Holibaugh
Paul Lambert
Adam Ley
Edward McCall
Ian McIntosh
Jeffrey Moore
Michael S. Newman
Kenneth P. Parker
Ulrich Pohl

Mike Ricchetti
Gordon Robinson
Robert Robinson
Bartien Sayogo
Gil Shultz
Walter Struppler
Bambang Suparjo
Srinivasa Vemuru
Oren Yuen

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Masayuki Ariyoshi
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Alexander Gelman
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Jim Hughes
Joseph Koepfinger*
David J. Law
Thomas Lee
Hung Ling
Oleg Logvinov
Ted Olsen

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Don Messina
IEEE Standards Program Manager, Document Development

Mike Kipness
IEEE Standards Program Manager, Technical Program Development

Contents

1. Overview	1
1.1 Scope	1
1.2 Purpose	1
1.3 Organization of the standard.....	2
1.4 Context	2
1.5 IEEE 1581 defect model, detection, and diagnosis.....	4
1.6 Objectives	7
2. Normative references.....	7
3. Definitions, acronyms, and abbreviations	7
3.1 Definitions	7
3.2 Acronyms and abbreviations	10
4. Test architecture	11
4.1 Overview	11
4.2 Combinational test logic architecture	13
4.3 Test mode architecture.....	13
5. Classification of device pins.....	14
5.1 Specification	14
5.2 Description	15
6. Test mode behavior	16
6.1 Specification	16
6.2 Description	16
7. Test mode control	20
7.1 Specification	20
7.2 Description	20
7.3 Test pin (TPN).....	20
7.4 Transparent test mode (TTM).....	22
7.5 Test pattern partitioning (TPP)	33
8. Test logic	42
8.1 Specification	43
8.2 Example implementation 1: XOR test logic	44
8.3 Example implementation 2: IAX test logic	45
8.4 Example implementation 3: XOR-2 test logic	47
9. Conformance and documentation	49
9.1 Conformance	49
9.2 Documentation.....	49
Annex A (informative) Bibliography	51

IEEE Standard for Static Component Interconnection Test Protocol and Architecture

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1. Overview

1.1 Scope

This standard defines a low-cost method for testing the interconnection of discrete, complex memory integrated circuits (ICs) where additional pins for testing are not available and implementing boundary scan (IEEE Std 1149.1™)¹ is not feasible. This standard describes the implementation rules for the test logic and test mode access/exit methods in compliant ICs. The standard is limited to the behavioral description of the implementation and will not include the technical design for the test logic or test mode control circuitry.

1.2 Purpose

There is currently no defined, independent standard for test technology in memory devices. Each vendor is free in the way of implementing test hardware functionality in their ICs to support connectivity tests. Without an independent standard, testability is reduced, and test coverage may not be complete — making the test technology less useful for others.

This standard will improve interconnect testing for discrete memory devices by specifying implementation rules for test logic and test mode entry/exit methods included in memory ICs as guidance both to IC vendors implementing the standard and to test equipment manufacturers supporting this standard. The standard is aimed at ICs that are otherwise not provisioned with design for testability (DFT) for any reason, targeting primarily memory devices but also allowing for implementation in other devices, while supporting the highest fault coverage and pin-level diagnostics of board-level connectivity faults on such devices.

¹ Information on normative references can be found in Clause 2.

1.3 Organization of the standard

This standard is divided into the following clauses:

- Clause 1 provides an overview and context for this standard.
- Clause 2 provides references necessary to understand this standard.
- Clause 3 describes the terms, definitions, and acronyms used in this standard.
- Clause 4 describes the test technology as applied for this standard and provides the motivation for using this standard.
- Clause 5 describes the classification of pins for an IEEE 1581 device.
- Clause 6 describes the behavior of an IEEE 1581 device while it is in test mode (versus functional mode).
- Clause 7 describes the test mode control protocol. It defines methods for test mode control of the device.
- Clause 8 describes the test architecture and test circuitry. This clause includes the specification of combinational logic functions for the test circuitry and provides examples of implementation and use.
- Clause 9 provides rules for conformance and documentation of devices designed to this standard.

1.4 Context

This standard is intended to operate within the context of a printed circuit board (PCB) on which electronic components are placed and electrically connected with each other (the interconnections). The protocols in this standard are focused on digital parts of such PCBs. This standard is intended to be used for, but not limited to, testing the interconnections of memory devices on those PCBs. Figure 1 shows such a PCB. Typically for memory devices (components IC4 and IC5 in the figure), at least one adjacent component is connected to this component. This neighboring device is in many cases a memory controller. In Figure 1, the two IEEE 1581 devices (target devices) are controlled by three IEEE 1149.1 devices (IC1, IC2, and IC3). Some of those connections between the controlling device and the target device may be indirect, as indicated with the buffer devices IC6 and IC7 (other examples would be in-line resistors).

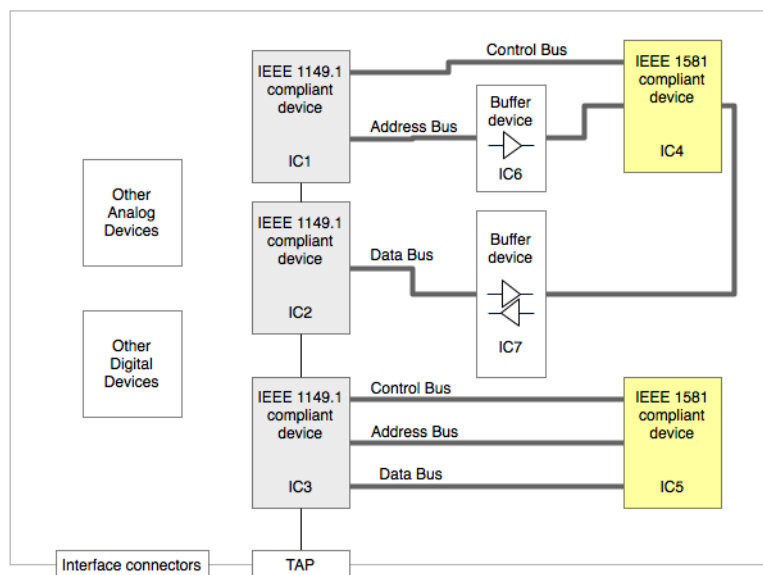


Figure 1 — A PCB with boundary-scan devices and complex memories

Modern designs have increasing functionality resulting in increasingly complex designs. The high component density of the designs and the use of package types like ball grid arrays (BGAs) for the ICs make verification of first prototypes difficult. During production, it is important to know the quality of the interconnections by testing them to prevent shipment of incorrectly assembled products to the market.

The electrical connections can be tested using this standard preferably in conjunction with IEEE Std 1149.1 since IEEE Std 1581 is complementary to it. Many other test methods are hampered by the lack of access for static signal measurements. Therefore, electronic access, as provided by boundary scan, is an increasingly popular method.

The currently available and widely accepted IEEE Std 1149.1 provides an efficient method for testing interconnections on a PCB populated with digital components. Memories often do not include circuitry conformant to IEEE Std 1149.1. Testing of interconnections to these memories using other devices that include IEEE 1149.1 circuitry is, if at all possible due to boundary scan cell implementation and test tools used, limited to basic bridging and stuck-at faults. In other words, when a boundary scan cell is implemented in a device with a write and read capability, it is possible to directly read back the value driven. If a defect is present on this pin, it can be detected for simple stuck-at fault behavior. However, open circuit defects on this interconnection can still not be detected. Additionally, from manufacturing, it is shown that these open circuit defects form the majority of soldering defects. The primary objective of IEEE Std 1581 is to allow simple but complete testing of such memory interconnections.

This standard does not provide an independent mechanism for testing interconnections on the PCB. Compatibility with IEEE Std 1149.1 of devices connected to the memory to be tested is preferred for obtaining test access. IEEE Std 1149.1 provides an efficient mechanism for reading and writing test patterns to a memory conformant to IEEE Std 1581. However, this standard does not forbid other means of access.

Figure 2 illustrates the range of defects and associated faults that can be covered when applying this standard to a device in conjunction with IEEE Std 1149.1. The standard is not limited to wires but is also applicable if interconnections are occupied with inverters/buffers, resistors, and pull-up/down resistors.

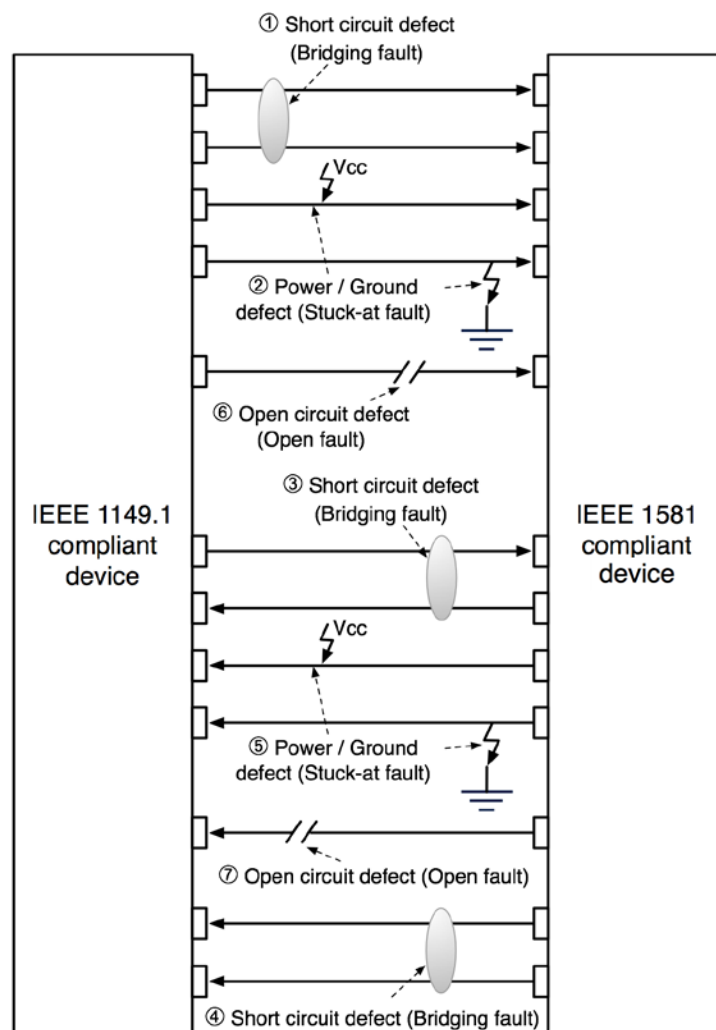


Figure 2 — Defects covered when applying IEEE Std 1581

1.5 IEEE 1581 defect model, detection, and diagnosis

1.5.1 Categories of defects

This standard focuses on board-level manufacturing defects. These principally include device attachment defects. Using the “PCOLA/SOQ” model (see Hird et al. [B3]¹), the following categories of manufacturing problems can occur:

- a) For devices themselves:
 - 1) Presence – Is a device actually present?
 - 2) Correct – Is the correct device present?
 - 3) Orientation – Is the device oriented correctly? (This question is for gross orientation errors, such as multiples of 90° rotations.)

¹ Numbers in brackets correspond to the numbers in the bibliography in Annex A.

- 4) Live – Is the device basically alive? (The device responds to inputs, and its outputs move appropriately. This response does not imply the device may not have subtle defects deep inside of it.)
 - 5) Alignment – Is the device aligned properly? (This question is for subtle alignment problems such as a small rotation error or a lateral shift off center.)
- b) For device pin connections (typically soldered):
- 1) Shorts – Is a device pin shorted to another nearby conductor? (This question includes neighboring pins on the same device that may conduct signals or power and includes shorts to other board signal connections close enough to be spanned by a solder bridge.)
 - 2) Opens – Is a device pin properly connected to a board-level signal?
 - 3) Quality – Is the connection properly formed? (This question addresses issues of solder volume sufficiency or insufficiency, cold or cracked joints, etc.)

1.5.2 Defects as addressed by IEEE Std 1581

Given the classification of manufacturing defects given by the PCOLA/SOQ model, IEEE Std 1581 addresses some defects well, others partially, and the rest not at all:

- a) For devices themselves:
- 1) Presence – An IEEE 1581 test will fail if a tested device is not present.
 - 2) Correct – It is expected that, if the wrong device is mounted in a position and an IEEE 1581 test is executed, it will fail; but this failure cannot be guaranteed if the improperly mounted device has an identical IEEE 1581 implementation within it. (IEEE Std 1581 provides the concept of an identification (ID) code by which the IEEE 1581 device could be identified if it features an ID code.)
 - 3) Orientation – An IEEE 1581 test will fail if a device is improperly oriented. If such a device is connected in parallel with other devices, it is likely the test will not yield much useful diagnostic data, and the device may interfere with the testing of other devices in parallel with it.
 - 4) Live – An IEEE 1581 test will determine whether a device is basically “alive.”
 - 5) Alignment – An IEEE 1581 test cannot determine any information about device alignment.
- b) For device pin connections (typically soldered):
- 1) Shorts – An IEEE 1581 test is expected to detect the presence of most shorts, as in the following cases:
 - i) For tested device inputs:
 - Shorted to another neighboring signal input pin (label ① in Figure 2) – Depending on device technology of the upstream device providing inputs to the tested device, the tested device may interpret shorted inputs as being both at the same state when the upstream device is producing different states. The combinational test circuitry of IEEE Std 1581 produces an error when this condition occurs.
 - Shorted to a neighboring power/ground pin (label ② in Figure 2) – Depending on the device technology of the tested device, this condition will be interpreted by the input as a “stuck 1” or “stuck 0.” If the upstream device providing data to this input produces both states, the combinational test circuitry of IEEE Std 1581 produces an error when this condition occurs.
 - Shorted to a neighboring signal output pin (label ③ in Figure 2) – Depending on the tested device’s technology and the technology of the device feeding signals to

the input, when those two states are not similar, the input may interpret the state in the opposite sense as intended by the upstream driver. The combinational test circuitry of IEEE Std 1581 produces an error when this condition occurs. Or, if the upstream driver is able to overcome the value of the tested device output that is coupled by the short, then the downstream device monitoring this output will perceive an error.

- Shorted to another signal from some other device on the board – This condition may or may not be detectable depending on the signal strength of the other signal. For example, if it is strongly driven to a state opposite to the tested signal, the combinational test circuitry of IEEE Std 1581 produces an error when this condition occurs. If the other signal is weakly driven or disabled, then the tested input may not see a difference, and the short will not be detected.
- ii) For tested device outputs (conditions not included above):
- Shorted to a neighboring signal output pin (label ④ in Figure 2) – Depending on the tested device's technology, the shorted pins will attain a single state when the two affected pins are expected to produce different states. The expected outputs during an IEEE 1581 test produce different outputs between all output pin pairs at least once during testing.
 - Shorted to a neighboring power/ground pin (label ⑤ in Figure 2) – All outputs produce both logic states during an IEEE 1581 test. Such a short will be detected by the downstream logic receiver because one or both states will not be achievable.
 - Shorted to another signal from some other device on the board – This condition may or may not be detectable depending on the signal strength of the other signal. For example, if it is strongly driven to a state opposite to the tested signal, the combinational test circuitry of IEEE Std 1581 produces an error when this condition occurs. If the other signal is weakly driven or disabled, then the tested output will be able to achieve its expected states, and the short will not be detected.
- 2) Opens – An IEEE 1581 test is expected to detect the presence of most opens, as in the following cases:
- i) For device signal inputs and control signals (label ⑥ in Figure 2):
- An open on a signal or control pin (excepting a designated test pin) – Depending on the device's technology, the input may float to either logic state or appear to have random behavior. If a stable state is achieved, then the IEEE 1581 test can detect the open since both states are used for testing. If the input has randomly variable behavior, there is a small chance that the random behavior matches the expected behavior and the defect will not be detected.
 - An open on the (optional) test pin – Depending on the device's technology, the test pin (test enable input) may float to either logic state or appear to have randomly variable behavior. If it floats to the state that enables testing, then the open cannot be detected. If it floats to the state that disables testing, then the test will fail, with results that may be difficult to diagnose. If it floats with randomly variable behavior, it is unpredictable whether the test will fail.
- ii) For device signal outputs (label ⑦ in Figure 2): An IEEE 1581 test produces both output states; therefore, the pass-failing of the test will be determined by the behavior of the monitoring pin downstream of the output. If that pin floats to a stable value, then the test will fail. If it floats to randomly variable states, there is a chance the test could pass.
- 3) Quality – An IEEE 1581 test cannot determine anything about connection quality.

1.6 Objectives

This standard defines test features to be included in memory devices together with associated test protocols. The standard aims to realize standardized methods for the following tests:

- Interconnection test capability, i.e., testing for open faults and shorts on a PCB (static and IEEE 1149.1 compatible): The aim is to detect and localize defects on the manufactured boards in the interconnection to memory components. This standard typically applies to memory devices of which the interconnections are otherwise not tested (for example, with IEEE Std 1149.1).
- Test architecture and test circuitry: The circuitry and architecture described in this standard are based on the application of combinational logic functions in silicon. This logic function adheres to mandatory rules as described in this standard to make full detection and diagnosis of open faults and shorts possible.
- Test mode control, i.e., protocols for safe, unambiguous access to and exit of the test mode of the device: This control is a description of rules to be met and shall be implemented in the silicon of the memory to which this standard applies.

This standard does not describe implementation details of the test circuitry, although implementation examples are given for illustration.

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used; therefore, each referenced document is cited in text, and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1149.1, IEEE Standard Test Access Port and Boundary-Scan Architecture.²

3. Definitions, acronyms, and abbreviations

For the purposes of this document, the following terms and definitions apply. *The IEEE Standards Dictionary: Glossary of Terms & Definitions* should be referenced for terms not defined in this clause.³

3.1 Definitions

address bus: A set of pins on a memory device used to address the memory cell locations for data read and write actions.

address/data pin: A pin on a memory device that can be used either for address functionality or data functionality. When used for data functionality, the pin operates as an input/output (I/O) pin or bidirectional pin, and the widest possible data bus on the memory device is selected for operation.

bidirectional pin: A pin on a component with the capability of transferring logical data in both directions. In IEEE Std 1581, bidirectional pins are also identified as input/output (I/O) pins.

² IEEE publications are available from the Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, Piscataway, NJ 08854-1441, USA (<http://standards.ieee.org/>).

³ *The IEEE Standards Dictionary: Glossary of Terms & Definitions* is available at <http://shop.ieee.org/>.

chip select (CS): A pin on a component that is capable of making the component accessible for reading and writing data over its pins. Conversely, the CS can also deselect a device so that it completely ignores read/write commands and does not affect any of its connected signals.

clock pin: A pin of a component that is used as a reference for data transfer (the clock of a component). For example, data transfer on a memory device is synchronized to this clock.

combinational logic: Memoryless (acyclicly connected) logic composed of simple gates like AND, OR, NOT, XOR, etc., between multiple inputs and driving one or more outputs.

complex memories: Electronic memory devices that require an initialization procedure using one or more memory pins before these memories can perform operational functions.

data bus: A set of pins on a memory device used as a transfer path for reading and writing data from/to the memory cells.

defect: An unacceptable deviation from a norm. An example of a defect is an open solder joint that disconnects a device pin from the board circuitry.

fault: A physical manifestation of a defect. For example, an open solder joint (a defect) on the input pin to an integrated circuit (IC) may cause one or more of its outputs to produce incorrect data (a physical manifestation).

fault detection: The ability to detect the presence of a defect by observing one of its physical manifestations. However, detection may not yield enough information to identify the precise location of a defect.

fault diagnosis: The ability to both detect and locate a defect. This process may require correlating several different manifestations of the defect.

functional mode: The standard mode of operation of a component as described by the manufacturer's datasheet.

interconnection: A connection path consisting of only a net between one or more components of where the resistance of the path is not significantly different from zero.

master device: A device that is capable of controlling another device. The master device applies a sequence of signals to a slave device that, in turn, causes the slave device to carry out an action or set of actions. In IEEE Std 1581, a master device (such as a memory controller) uses boundary scan-based signaling to cause a slave device (like a memory device) to perform some test-related action.

memory device: An integrated circuit device that preserves data for a certain amount of time for retrieval.

nonsequential logic: *See: combinational logic.*

nonvolatile memory: A memory device that will retain the stored information even if it is not constantly supplied with electric power.

output enable (OE): A pin on a component that is capable of enabling or disabling data transfer on other pins. For example, an OE pin on a memory device can enable or disable a data bus for data transfer.

partial diagnosis: The ability to partially localize a defect on a manufactured board based on a specifically found fault. In IEEE Std 1581, partial diagnosis indicates that *not all* detected defects can be diagnosed to component pin level. *Contrast: full diagnosis.*

pin test coverage: The complete set of pins that are included in the test logic. These pins are then tested by the test logic and thus are covered for analysis.

power-up: The sequence of applying power to a component after which the component can be used in functional mode or test mode as defined by IEEE Std 1581.

reset pin: A pin of a component that is capable of forcing some portion of its functionality into a prescribed reset state. This state may be entered asynchronously upon assertion of reset or may be entered in conjunction with a specific clocking event when asserted.

slave device: A device that is controlled by another device to perform an action or set of actions. For example, a memory, as a slave to a master device, may be sent into a test mode where the master device sends test data to the slave and collects the slave's responses.

static test: Test in which the values on the nets do not decay in time.

test control pin: A memory device input pin that needs to be held in a specific state *while the device is in IEEE 1581 test mode*. Examples for test control pins are chip select (CS) and output enable (OE) pins used to determine whether the output pins are active.

test function: While in test mode, an IEEE 1581 device may provide access to various optional test functions (such as reading identification (ID) code or executing a built-in self-test (BIST)) in addition to the mandatory interconnection test.

test logic: The complete set of logic functions inserted between input pins and output pins during test mode and used for testing the device interconnections on a printed circuit board (PCB).

test logic function: The behavioral logic function between the specified input pins and output pins of the device used for testing the interconnections on a printed circuit board (PCB).

test mode: The state of the device in which it behaves according to the rules in IEEE Std 1581. In test mode, the device is a slave device.

test mode entry: The entering into IEEE 1581 test mode by applying a specific test mode protocol.

test mode exit: The exit from the specific IEEE 1581 test mode by applying a specific test mode protocol.

test pattern partitioning (TPP): A method to reserve certain test patterns for interconnection tests through the IEEE 1581 test logic, while other test patterns are used to select certain test functions implemented in the IEEE 1581 device.

test patterns: Data driven in sequences to the device under test (DUT) to verify the integrity of the interconnections. These patterns together with the test logic allow a test algorithm to locate interconnection defects in the manufactured printed circuit board (PCB).

test pin: A dedicated input pin on a component (in IEEE Std 1581, a memory device) used to control switching between test mode and functional mode.

transparent test mode (TTM): A mechanism to enter and exit test mode in an IEEE 1581 device without the need of a dedicated test pin.

volatile memory: A memory device that requires constant power to maintain stored information. Stored information will be lost if the device is not constantly supplied with electric power.

write enable (WE): A control signal of a memory device that enables write access to that memory device.