

IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)

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**Microprocessor and Microcomputer Standards Committee
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IEEE Computer Society**

Approved 21 March 1996

IEEE Standards Board

Abstract: Scalable Coherent Interface (SCI), specified in IEEE Std 1596-1992, provides computer-bus-like services but uses a collection of fast point-to-point links instead of a physical bus in order to reach far higher speeds. The base specification defines differential ECL signals, which provide a high transfer rate (16 bits are transferred every 2 ns), but are inconvenient for some applications. IEEE Std 1596.3-1996, an extension to IEEE Std 1596-1992, defines a lower-voltage differential signal (as low as 250 mV swing) that is compatible with low-voltage CMOS, BiCMOS, and GaAs circuitry. The power dissipation of the transceivers is low, since only 2.5 mA is needed to generate this differential voltage across a 100 Ω termination resistance. Signal encoding is defined that allows transfer of SCI packets over data paths that are 4-, 8-, 32-, 64-, and 128-bits wide. Narrow data paths (4 to 8 bits) transferring data every 2 ns can provide sufficient bandwidth for many applications while reducing the physical size and cost of the interface. The wider paths may be needed for very-high-performance systems.

Keywords: backplane, bus, cable, differential, low-power, point-to-point, scalable, signal

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ISBN 1-55937-746-1

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Introduction

[This introduction is not a part of IEEE Std 1596.3-1996, IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI).]

The demand for more processing power continues to increase, and apparently has no limit. One can usefully saturate the resources of any computer by merely specifying a finer mesh or higher resolution for the solution to a physical problem such as hydrodynamics or 3-D graphics. This demand leads engineers and scientists in a desperate search for more powerful and faster computers.

To economically obtain this kind of computing power, it seems necessary to use a large number of processors cooperatively. This cooperation is provided by the Scalable Coherent Interface (SCI), a high-speed packet transmission protocol that efficiently provides the functionality of bus-like transactions (read, write, lock, etc.). However, the initial physical implementations are based on emitter coupled logic (ECL) signal levels, which consume more power than is practical in the low-cost workstation environment. The initial specification's 1 Gbyte/s bandwidth (16-bit data path) may be overly expensive in the workstation environment. It may be more cost effective to use a narrower data path of sufficient bandwidth. The combination of a high-speed transmission environment and efficient protocols can provide the link for multiple processors to cooperate in a low-cost workstation environment.

The initial developers of this standard came from the Working Group that developed the SCI protocol (IEEE Std 1596-1992). The ECL signal levels defined for the SCI were effective in getting the standard implemented quickly and are practical for high-performance applications. They are less well suited, however, to using SCI in low-cost workstations. The obvious low-cost solution is to integrate the transceivers into the controller and implement both in CMOS. This integration will satisfy the space and power requirements of the workstation and personal computing market.

Eventually, a lower voltage swing will be needed in order to get higher speeds than ECL signal levels can provide. This standard can provide the basis for increasing parallel signal switching frequency into the gigahertz range.

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IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)

1. Overview

1.1 Scope

This standard specifies a process-technology-independent low-voltage (less than 1 V swing) point-to-point signal interface as optimized for IEEE Std 1596-1992 [B1],¹ which uses a differential driver connected to a terminated receiver through a constant-impedance transmission line. The interface will be optimized for CMOS processes, while being compatible with other IC processes, including GaAs and BiCMOS. The specification should support a transfer rate of at least 200 mega-transfers/second.

In addition, the specification will define encodings for transporting SCI packets over narrow and wide data paths (4-, 8-, 32-, 64-, and 128-bits, rather than the 16 bits defined by IEEE Std 1596-1992) using these signals.

1.2 Objectives

The primary goal of this standard is to create a physical layer specification for drivers and receivers and signal encoding suitable for use with the SCI as specified by IEEE Std 1596-1992 in low-cost workstation and personal computer applications. Other objectives include the following:

- *Technology independence.* Specifications should allow designs to be implemented in a variety of integrated-circuit technologies.
- *CMOS compatible.* Signal voltage levels and other specifications should be compatible with digital CMOS processes operating from 2 V through 5 V power supply levels.
- *Backplane and cable applications.* Specifications should be optimized for connections between boards contained within one chassis and short (less than 5 m) chassis-to-chassis interconnects. Longer connections are not prohibited, provided they meet specified signal loss and ground shift criteria for proper receiver operation. Connector and cable specifications are beyond the scope of this standard.
- *Scalable.* The original 16-bit-wide SCI data path should be supplemented by 4- and 8-bit-wide data paths to support a variety of cost/performance ratios. Support for 32-, 64-, and 128-bit-wide data paths will also be addressed.

¹ The numbers in brackets preceded by the letter B correspond to those of the bibliography in annex A.

1.3 Strategies

The basic design strategies selected by this standard include the following:

- *Low-voltage swing.* To minimize power dissipation and enable operation at very high-speed, low-swing (400 mV maximum) signals are specified.
- *Differential signals.* Small signal swings require differential signaling for adequate noise margin in practical systems.
- *Self-terminated.* To minimize board real estate and costs, and to maximize clock rates, each receiver is assumed to provide its own termination resistors.
- *Uniform ground.* The standard assumes that the ground potential difference between driver and receiver is kept small by the system design. The mechanism for constraining the ground potential difference is beyond the scope of this standard.

The most controversial decision was to use differential signals, which at first appears to double the number of signal lines. The pin-count overhead is actually much less than this, since reliable single-ended schemes require many more ground signals (many high-speed chips and/or backplanes provide one ground for every two signal pins) and run significantly slower. Other design benefits associated with differential signals include the following:

- *Constant driver current.* The transmitter consumes a (near) constant current when driving the links; the current remains the same, but is routed in the opposite direction when the signal value changes. This simplifies the design of power-distribution wiring.
- *Constant link current.* The net signaling current in a differential link is (nearly) constant, which greatly simplifies system design. The links are unidirectional and transmitters always drive a differential signal per table 2–1 or table 2–2. Reversing or stopping links would cause the net common-mode signaling current to change, creating system noise.
- *Low power.* A low signal current can be used, since much of the induced noise and ground-bounce appears as a common-mode signal.
- *Simple board design.* Although differential signals must be carefully routed on adjacent matched tracks, they are usually less sensitive to imperfections in the transmission line environment.
- *Low EMI.* Differential signals minimize the area between the signal and the return path. In addition, the equal and opposite currents create canceling electromagnetic fields. This dramatically reduces the electromagnetic emissions.
- *Low susceptibility to externally generated noise.* Though these links generate little noise, other parts of the system may. Differential signals are relatively immune to this noise.

1.4 Design models

1.4.1 Source-synchronous data

The SCI-LVDS link model assumes unidirectional operation (the driver always at one end of the link, the receiver at the other), and that a clock signal is sent along with the data as though it is just another data bit.

Both edges of the clock are used to delimit data, so the maximum transition rate of the clock is the same as the maximum transition rate of the data signals. This clock flows through the link at the same velocity as the data, and is to be used as the time reference for sampling the data.

In most applications, the received sampled data will need to be synchronized to the receiver's local clock. If the transmitter's clock and the receiver's clock are independent, and thus perhaps at slightly different frequencies, occasional symbols will need to be inserted or removed from time to time in an elasticity buffer in order to maintain synchronization.

The transmission system shall ensure that the setup and hold requirements of the receiving latches are met, in order to avoid incorrect data sampling and triggering metastable states. The receiver can observe the timing of the received clock relative to its own clock in order to choose an appropriate sampling time.

By carefully adhering to these assumptions, the SCI signaling protocol becomes independent of distance or delay. The maximum distance is limited by signal skew, caused by slight differences in propagation velocity from one signal to another, and by attenuation and distortion of the signals.

Because these signals are unidirectional, it is relatively easy to reshape and time-align them in order to transmit them greater distances. However, this may introduce timing jitter, which can make it impossible for the receiver to anticipate clock transitions with sufficient accuracy for reliable operation.

1.4.2 Terminated transmission lines

In addition to extending the signal encoding to parallel widths not included in IEEE Std 1596-1992, this standard specifies driver and receiver parameters only. However, a system must interconnect these components to be useful. The interconnect termination is specified in the receiver portion of this standard. The interconnect is beyond the scope of this standard because of the many options possible. The interconnect could include bond wires, packages and pins, printed circuit board, cables, connectors, multi-chip modules, wafer scale integration, or any combination of the previous options in one driver-to-receiver signal path. This signal path is important to the correct operation of a system implementing LVDS signals and is therefore discussed in general terms in this standard.

At the high data rates this standard supports, it is important to consider the transmission line aspects of the signal path. The high-frequency components of the 300 ps transition times make the parasitic reactive signal path components important. Familiar concepts, such as the receiver input capacitance, are overshadowed by the parasitic inductance of signal path elements that shape the waveform. If the signal delay through a signal path section is greater than the allowed minimum transition time, 300 ps, that section must be analyzed as a transmission line with associated characteristic impedance and delay. Impedance discontinuities through connectors, pins, solder pads, and bond wires to the IC itself cause reflections that degrade the signal integrity.

The receiver and its package input impedance need to match the signal transmission line impedance. This serves to minimize noise-causing reflections that create data errors. Given typical CMOS process tolerances, this generally implies the use of active devices to adjust the terminating resistance until it matches an external reference. Integrating the terminating impedance onto the receiver chip complicates the design and manufacturing, but the trade-off is simplified board layout and better signal integrity.

2. Document notation

2.1 Conformance levels

Several key words are used to differentiate between different levels of requirements and options, as follows:

2.1.1 expected: A key word used to describe the behavior of the hardware or software in the design models *assumed* by this specification. Other hardware and software design models may also be implemented.

2.1.2 may: A key word that indicates flexibility of choice with *no implied preference*.

2.1.3 shall: A key word indicating a mandatory requirement. Designers are *required* to implement all such mandatory requirements to ensure interoperability.

2.1.4 should: A key word indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase *is recommended*.

2.2 Technical glossary

Many bus and interconnect-related technical terms are used in this document. These terms are defined below:

2.2.1 backplane: A board that holds the connectors into which SCI modules can be plugged. In ring-based SCI systems, the backplane may contain wiring that connects the output link of one module to the input link of the next. Usually the backplane provides power connections, power status information, and physical position information to the module.

2.2.2 board: The physical component that is inserted into one of the backplane slots. Note that a board may contain multiple nodes.

2.2.3 byte: Eight bits of data. *Syn:* **octet**.

2.2.4 differential voltage signal: The voltage difference between the true and complementary signals from a driver with two single-ended outputs whose signals always complement each other. Differential signals are also referred to as “balanced signals.”

2.2.5 driver: An electrical circuit whose purpose is to signal a binary state for transmitting information. Also referred to as a “generator” in international standards.

2.2.6 flag: A signal used to delimit packets in parallel-signal-transmission implementations.

2.2.7 ground potential difference voltage: The voltage that results from current flow through the finite resistance and inductance between the receiver and driver circuit ground voltages.

2.2.8 idle symbol: A symbol that is not inside a packet and is therefore not protected by a CRC. Idle symbols serve to keep links running and synchronized when no other data are being transmitted. The idle symbol also contains flow-control information.

2.2.9 jitter: Refers to the time-uncertainty of a transitioning edge recurring in a repetitive signal. This uncertainty is only with respect to other edges in that signal. Jitter is commonly measured using random bit patterns and accumulating an eye pattern to show the worst-case difference in transitions.

2.2.10 LVDS: An abbreviation for low-voltage differential signal.

2.2.11 offset voltage: The driver offset voltage is the average dc voltage generated by the differential driver; $V_{os} = (V_{oa} + V_{ob}) / 2$.

2.2.12 packet: A collection of symbols that contains addressing information and is protected by a CRC. A subaction consists of two packets: a send packet and an echo packet.

2.2.13 physical interface: The circuitry that interfaces a module’s nodes to the input link, output link, and miscellaneous signals.

2.2.14 receiver common-mode voltage: The combination of three components: 1) the driver-receiver ground potential difference (V_{gpd}); 2) the longitudinally coupled peak noise voltage measured between the receiver circuit ground and the signal transmission media with the driver end shorted to ground (V_{noise}); 3) the driver offset voltage.

2.2.15 receiver differential noise margin high: The tolerable signal voltage variation from any source that still results in the receiver producing a logic high output state when the driver is stimulated by a logic high input. Differential noise margin high is calculated by subtracting the receiver’s minimum differential high input voltage from the driver’s minimum high differential output voltage; $V_{odh}(\min) - V_{idh}(\min)$.

2.2.16 receiver differential noise margin low: Tolerable voltage variation to guarantee that the receiver produces a logic low output when the driver is stimulated by a logic low input; $V_{idl}(\max) - V_{odl}(\max)$.

2.2.17 SCI: *See:* **Scalable Coherent Interface**

2.2.18 Scalable Coherent Interface (SCI): An abbreviation for the Scalable Coherent Interface standard, IEEE Std 1596-1992.

2.2.19 signal line: An electrical or optical information-carrying facility, such as a differential pair of wires or an optical fiber, with associated driver and receiver, carrying binary true/false logic values.

2.2.20 skew: The difference in time that is unintentionally introduced between changing signal levels (incident edges) that occur on parallel signal lines. This difference results in an uncertain position with respect to time among parallel signals.

2.2.21 symbol: Refers to data within an SCI packet. A 16-bit unit of data accompanied by flag information. The flag information may be explicitly present as a 17th bit, or implied by the context. Symbols are transmitted one after another to form SCI packets or idles. The particular physical layer used to transmit these symbols is not visible to the logical layer.

2.2.22 sync packet: A special packet that is used heavily during initialization and occasionally during normal operation for the purpose of checking and adjusting receiver circuit timing.

3. Electrical specifications

3.1 Description and configuration

A LVDS interface, (figure 3-1), has a low-voltage swing (400 mV single-ended maximum), is connected point-to-point, and achieves a very high data rate (500 Mbits per second per signal pair) and reduced power dissipation. Power is low because signal swings are small: a minimum of 2.5 mA are sent through a 100 Ω termination resistor. This sharply reduced power dissipation enables an important advance: integrating the line termination resistors, interface drivers and receivers, and the processing logic in the same integrated circuit.

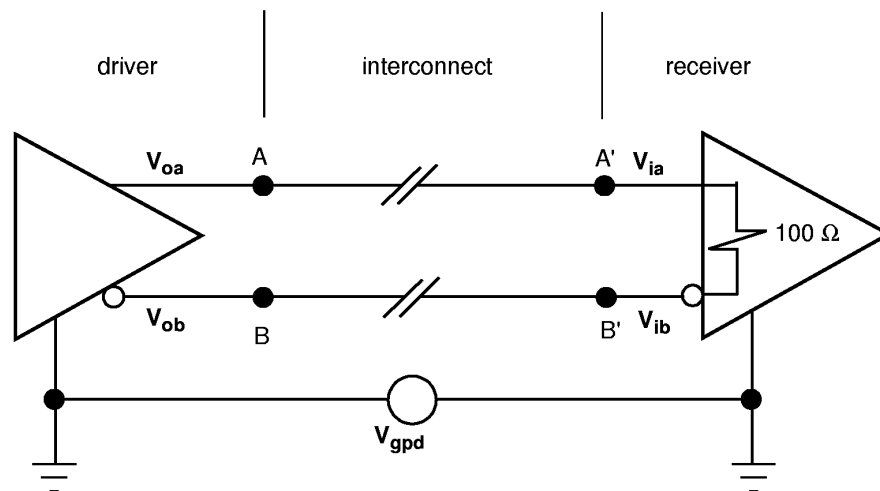


Figure 3-1 —LVDS interface

Switching speed is high because the driver load is an uncomplicated point-to-point 100 Ω transmission line environment. Switching speed is also high because interface devices are all on the same piece of semiconductor material, reducing the skew due to process, temperature, and supply variations between signal pairs. Connected in serial or parallel pairs, the LVDS interface forms a link used to transfer packets between integrated circuits, such as SCI nodes. For example, figure 3-2 shows circuit boards with LVDS links connected in a ring. The ring is implemented on a printed circuit board (PCB) similar in mechanical function to a multidrop bus backplane. The difference is that fewer PCB layers are needed to make the point-to-point connections. The PCB is simplified by eliminating the multidrop bus lines, as there is no need to route around interlayer vias used to make mechanical and electrical connections.

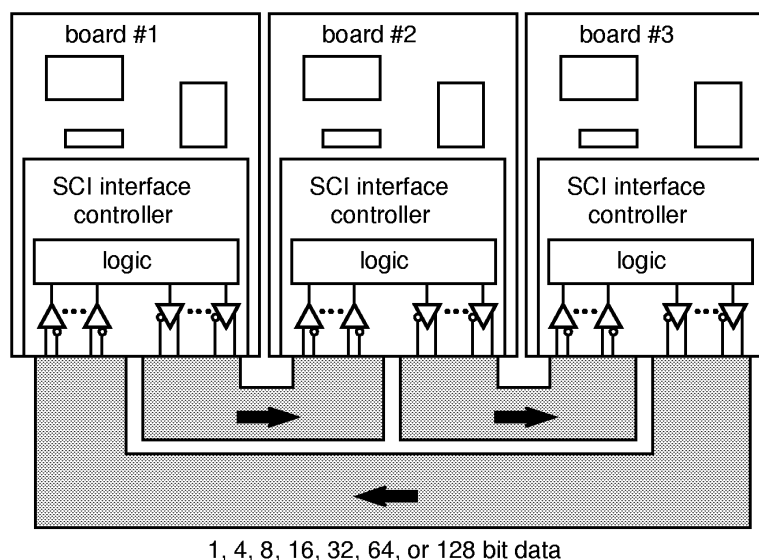


Figure 3-2 —Links in SCI application (ring connection)

LVDS is independent of the physical layer transmission media. As long as the media deliver the signals to the receiver with adequate noise margin and within the skew tolerance range, the interface will be reliable. This is a great advantage when using cables to carry LVDS signals. Since all connections are point-to-point, physical links between nodes are independent of other node connections in the same system. This allows for freedom in developing a useful interconnect that fits the needs of the application.

The data path can be serial or parallel with 1-, 4-, 8-, 16-, 32-, 64-, or 128-bits, depending on the needs of the user (see annex A, Signal encoding, for all widths except 1 and 16, which are defined in IEEE Std 1596-1992, clause 6, Physical layer).

Electrical specifications and skew specifications are optimized for 2–5 V supply voltages. The full range of semiconductor process technologies can be used to implement LVDS. It is intended that the specification be interoperable for all these technologies. The rapid trend toward reduced power supply voltage was considered in providing for signals that can be compatible with future system requirements.

The physical environment of point-to-point connections between circuit boards is further divided into two categories. The first (a general purpose link) is for circuit boards that need to operate with tolerance for V_{gpd} (table 3-1). This tolerance (approximately ± 1 V for a 2.5V powered system) is for a general purpose system. The second (a reduced-range link) is for boards mounted on a PCB or similar environment that will guarantee less than 50 mV V_{gpd} (table 3-2). In this environment, the differential signal is reduced by reducing the driver current. This reduces the power at both driver and receiver. This is a special consideration for subsystem implementations such as IEEE Std 1596.4-1994 RamLink.

The backplane environment implies short interconnects with controlled V_{gpd} . The use of cables implies that all the skew and signal quality requirements will be met by the cables, and the system designer will account for the worst-case V_{gpd} and provide appropriate safeguards. The scope of the electrical specification is the differential interface of drivers and receivers. The transmission media specification, whether cables or printed circuits, is beyond the scope of this standard.

3.2 Electrical specifications

The specification for driver and receiver parameters is given in table 3-1 and table 3-2. Descriptions of these parameters are contained in the following subclauses. These specifications shall be satisfied over the product's stated power supply voltage and temperature operating range.