

IEEE Standard for Terminology and Test Methods of Digital-to-Analog Converter Devices

IEEE Instrumentation and Measurement Society

Sponsored by the
Waveform Generation, Measurement, and Analysis Technical Committee (TC-10)

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IEEE Standard for Terminology and Test Methods of Digital-to-Analog Converter Devices

Sponsor

Waveform Generation, Measurement, and Analysis Technical Committee (TC-10)
of the
IEEE Instrumentation and Measurement Society

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Abstract: Terminology and test methods to clearly document prevalent world-wide terms used to describe and test digital-to-analog converters (DACs) are provided. It is restricted to monolithic, hybrid, and module DACs and does not cover systems encompassing DACs.

Keywords: DAC, digital-to-analog converter, IEEE 1658, SFDR, SNR, spectrum, test terminology, test methods

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Introduction

This introduction is not part of IEEE Std 1658-2011, IEEE Standard for Terminology and Test Methods of Digital-to-Analog Converter Devices.

This standard defines the terms, definitions, and test methods used to specify, characterize, and test digital-to-analog converters (DACs). It is intended for the following:

- Individuals and organizations who specify DACs to be purchased
- Individuals and organizations who purchase DACs to be applied in their products
- Individuals and organizations whose responsibility is to characterize and write reports on DACs available for use in specific applications
- Suppliers interested in providing high-quality and high-performance DACs to acquirers

This standard is designed to help organizations and individuals:

- Incorporate quality considerations during the definition, evaluation, selection, and acceptance of supplier DACs for operational use in their equipment
- Determine how supplier DACs should be evaluated, tested, and accepted for delivery to end users

This standard is intended to satisfy the following objectives:

- Promote consistency within organizations in acquiring third-party DACs from component suppliers
- Provide useful practices on including quality considerations during acquisition planning
- Provide useful practices on evaluating and qualifying supplier capabilities to meet user requirements
- Provide useful practices on evaluating and qualifying supplier DACs
- Assist individuals and organizations judging the quality and suitability of supplier DACs for referral to end users

Several standards have previously been written that address the testing of DACs either directly or indirectly. These include the following:

- IEEE Std 1057, which describes the testing of waveform recorders.
- IEEE Std 1241, which addresses the testing of Analog-to-Digital Converters.
- IEEE Std 746, which addresses the testing of Analog-to-Digital and Digital-to-Analog Converters, used for PCM television video signal processing.
- JEDEC Standard 99, addendum number 1, which deals with the terms and definitions used to describe Analog-to-Digital and Digital-to-Analog Converters. This standard does not include test methods.
- IEC 60748-4 Semiconductor Devices—Integrated Circuits—Part 4: Interface integrated circuits—Sec. 2: Blank detail specification for linear analogue-to-digital converters.

IEEE Std 1658 for digital-to-analog converters is intended to focus specifically on terms and definitions as well as test methods for DACs for a wide range of applications.

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1. Overview

This standard is divided into eighteen clauses plus annexes. Clause 1 is a basic orientation. For further investigation, users of this standard can consult Clause 2, which contains references to other IEEE standards on waveform measurement and relevant International Standardization Organization (ISO) documents. The definitions of technical terms and symbols used in this standard are presented in Clause 3. Clause 4 through Clause 17 present a wide range of tests that measure the performance of a digital-to-analog converter. Annexes, containing the bibliography and informative comments on the tests presented in Clause 4 through Clause 17, augment the standard.

1.1 Scope

This standard defines terminology and test methods to clearly document prevalent world-wide terms used to describe and test digital-to-analog converters (DACs). It is restricted to monolithic, hybrid, and module DACs and does not cover systems encompassing DACs.

1.2 Purpose

This standard is written to clear up confusion relating to the terms and definitions concerning DACs. Test methods are defined with expected output and analysis of the data generated from these test methods. Product specifications are defined in clear terms that will be understandable by all international users and manufacturers.

1.3 Discussion of scope and purpose

A digital-to-analog converter (DAC) receives digital input data and converts it to an analog output. The material presented in this standard is intended to provide common terminology and test methods for the testing and evaluation of DACs. The standard graphic symbol for DAC is given in Figure 1, where N represents the width of the data word (in bits).



Figure 1—DAC graphic symbol

The information in this standard is useful both to manufacturers and users of DACs in that it provides a basis for evaluating and comparing existing devices, as well as providing a template for writing specifications for the procurement of new ones. This standard identifies DAC error sources and provides test methods to measure them. In some applications, the information provided by the tests described in this standard could be used to correct DAC errors, e.g., correction for gain and offset errors.

The reader should note that this standard has many similarities to IEEE Std 1057 [B1]¹ and IEEE Std 1241 [B2].

1.4 Digital-to-analog converter and analog-to-digital converter differences and similarities

DACs and analog-to-digital converters (ADCs) perform complementary functions. DACs receive a digital signal and generate an analog equivalent, while ADCs receive an analog signal and generate a digital equivalent. Some of the subtleties are summarized in the following list:

- a) Transfer function differences (see Figure 2)
 - 1) For a DAC, each digital input corresponds to single average analog output amplitude.
 - 2) For an ADC, each digital output corresponds to an interval of analog input values. The analog quantity defined in the transfer function of an ADC, the code edge, is usually defined to occur at the point where 50% of the output codes are greater than a specified digital output.

¹ The numbers in brackets correspond to those of the bibliography in Annex F.

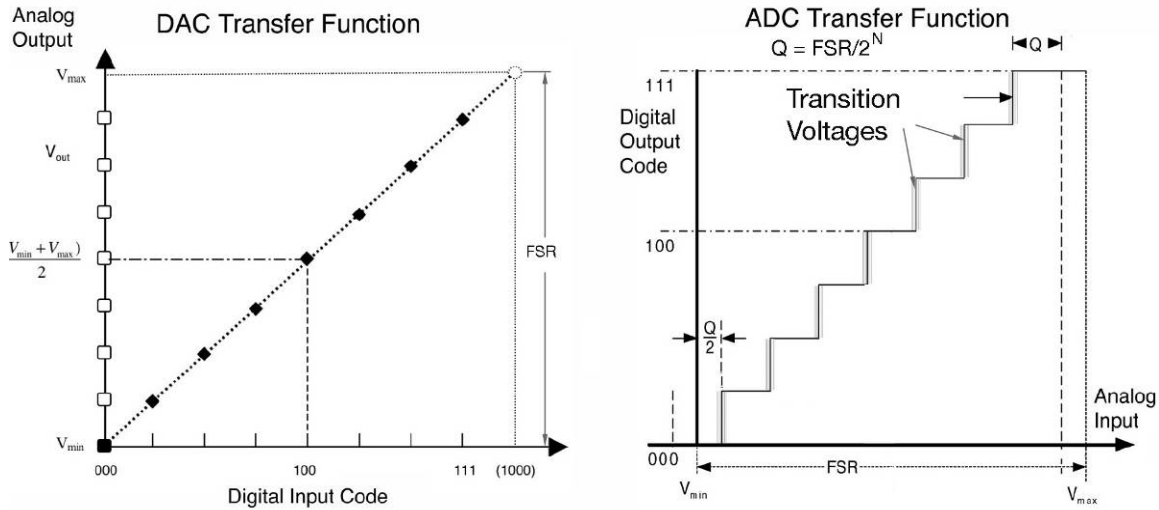


Figure 2—Transfer functions of ideal 3-bit unipolar DAC and ADC

- b) Quantization differences
 - 1) In a DAC, the input is a digital input code and the output is an analog representation of the input.
 - 2) In an ADC the input is analog and the output is the quantized representation of the input.
- c) Time-domain differences
 - 1) A DAC with a constant input code produces a continuous nominally fixed analog output that may contain additive noise.
 - 2) An ADC with a constant input may generate a distribution of quantized outputs because of the presence of noise.
- d) Frequency-domain differences
 - 1) A DAC driven by a single-frequency digital sine wave at its input will produce at its output a single frequency between dc and $\frac{1}{2}$ the data rate. Additionally, other frequencies will be produced that are sums and differences of the input frequency and multiples of the data rate.
 - 2) An ADC with any fixed frequency analog input will produce a data record that will appear to contain frequencies only up to one half the sampling rate.
- e) Both a DAC and an ADC require an internal or external reference current or voltage that will cause the DAC to have an output that can be in some way traced to standard units of voltage or current

There are also some subtle differences between ADCs and DACs in the area of aliasing and image frequency generation. Aliasing is a phenomenon usually associated with ADCs while the generation of image frequencies is usually associated with DACs. The two phenomena are very closely related. In both cases there is a sampling frequency, f_s . For an ADC this is the clock rate, the rate at which samples are taken. For a DAC this is the data rate, the rate at which data words are supplied to the DAC. Two positive frequencies, f_1 and f_2 , are said to be aliases of one another if they satisfy Equation (1).

$$f_2 - f_1 = kf_s, \text{ or } f_2 + f_1 = kf_s, \text{ where } k \text{ is any integer.} \quad (1)$$

Note that the integer k can be positive, negative or zero. Recall that the n^{th} Nyquist band consists of all frequencies, f , satisfying $(n-1)f_s/2 \leq f < nf_s/2$. It is fairly easy to show that any frequency, f , has exactly one alias in each Nyquist band.

When an input signal of frequency, f , is supplied to an ADC the resulting samples will be a signal whose frequency is the alias of f in the first Nyquist band. Thus, many different frequencies get mapped into a single frequency. This phenomenon is called aliasing. Conversely, when an input sequence with a frequency in the first Nyquist band is supplied to a DAC the output signal will generally contain components at all of the aliases of the input signal frequency. These spurious output frequencies are called images of the input frequency. Note that a sine-wave input sequence to a DAC can always be considered to be in the first Nyquist band, because the sampled values of a sine wave in a higher Nyquist band are exactly equal to the sampled values of the signals alias in the first Nyquist band.

The aliasing phenomenon has complementary implications for the measurement of frequency response using sine-wave inputs for ADCs and DACs. For a DAC, inputs only need to be generated in the first Nyquist band, but the outputs need to be measured at the images of the input frequency in all bands of interest. For an ADC, the input signals must be in all Nyquist bands of interest, but the outputs always appear at the alias in the first Nyquist band of the input signal.

1.5 Digital-to-analog converter background

This standard considers only those DACs whose output values have discrete values for discrete input words. Although different methods exist for representing a discrete sequence of binary words as a continuous analog signal, an underlying model implicit in many of the tests in this standard assumes that the relationship between the input code and the output value (transfer function) approximates a straight line as depicted in Figure 3 and Figure 4. Applying this model to a code-input DAC, the full-scale output range (FSR) at the DAC is divided into uniform intervals, with nominal separation of Q . The number of code levels in the discrete transfer function is equal to 2^N where N is the number of bits of the DAC. The number of intervals is $2^N - 1$. The Full scale outputs are generally defined as physical quantities (voltage or current) and are usually given as the values with code 0 applied, and code 2^N applied. The code for 2^N is generally a virtual code that does not exist, but serves as a good definition of the DAC. Thus, a 0 V to 10 V 10-bit DAC will theoretically never actually generate 10.0 V. If the code $2^N - 1$ is applied (the last physically realizable code) the ideal output will be approximately 9.9902 V. The 3-bit DAC modelled in Figure 3 could be described as an 8 V FS unipolar DAC, where each binary least significant bit would correspond to a 1 V increment in the output. Note that the DAC could not actually generate a +8 V output.

In addition to unsigned binary shown in Figure 3, DACs may use twos complement, ones complement, sign-magnitude, Gray, Binary-Coded-Decimal (BCD), or other digital coding schemes. The 3-bit DAC modelled in Figure 4 could be described as a ± 4 V bipolar twos complement DAC, where each binary least significant bit would correspond to a 1 V increment in the output. Note that the DAC could not actually generate a +4 V output.

DAC errors can be divided into the categories of static and dynamic. The static errors are usually caused by mismatch of the components and limit the accuracy at low speed. The static performance is often described by measures of differential and integral nonlinearities (DNL[k] and INL[k], where the DNL and INL are defined for each input word k). The dynamic errors, such as settling errors, glitches, etc., are important and they become more significant with higher update rates and when higher frequency waveforms are being synthesized by the DAC. To analyze the effect of errors, it is usually easier to consider the DAC's behavior in frequency domain using measures, such as the spurious free dynamic range (SFDR) and signal-to-noise and distortion (SINAD) ratio.

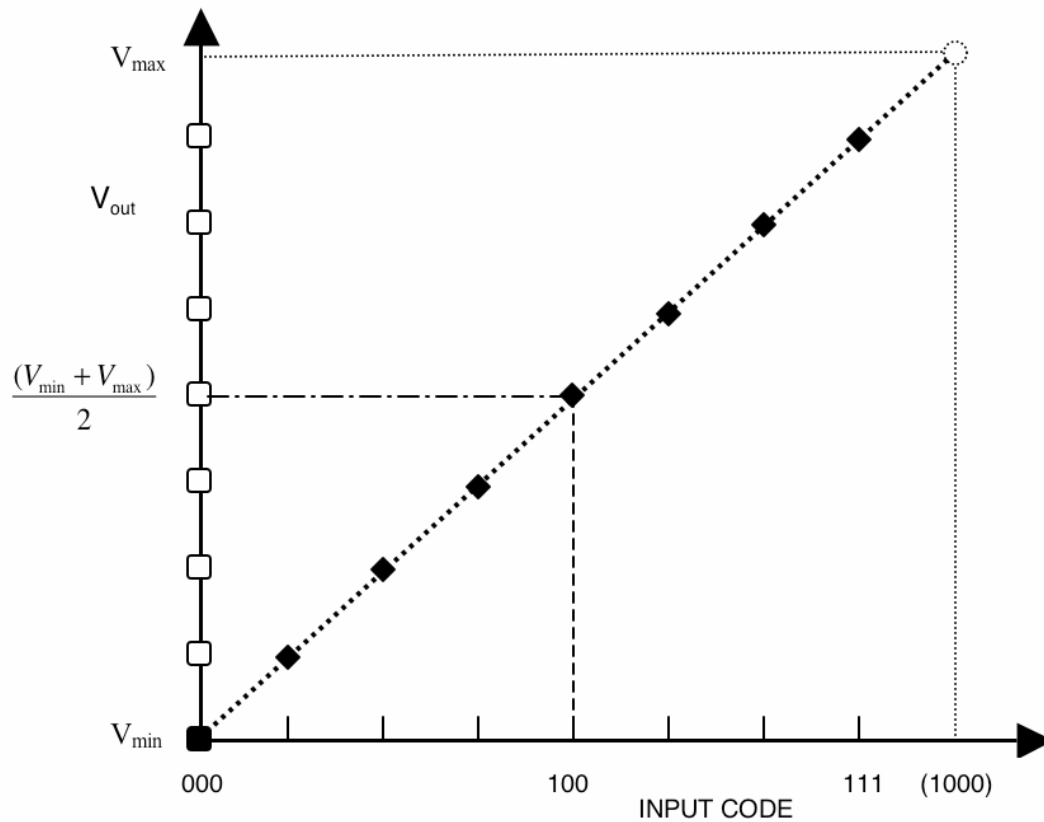


Figure 3—Elements of an ideal linear DAC transfer function (unipolar)

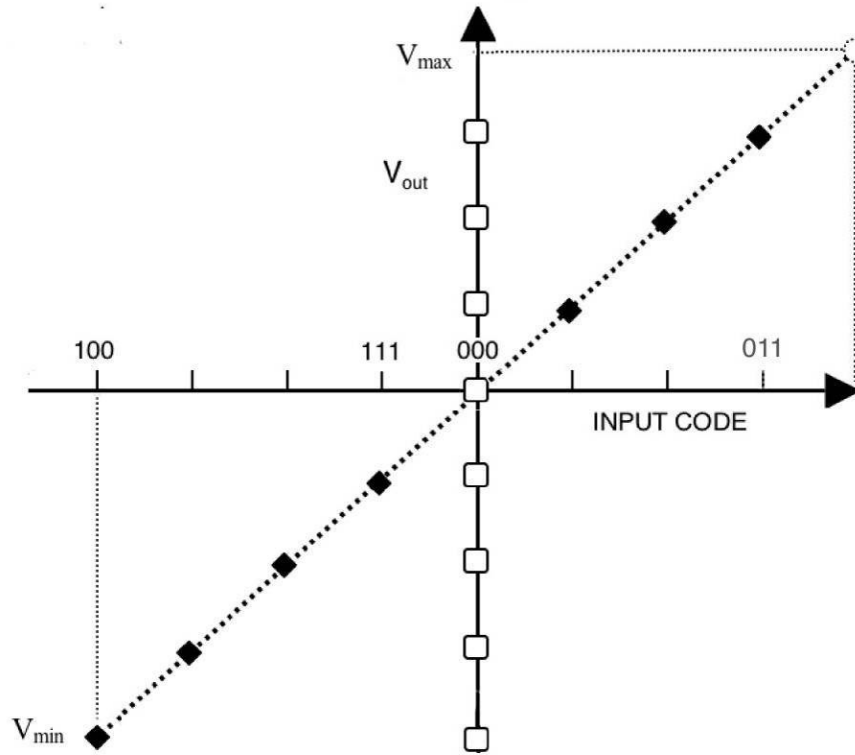


Figure 4—Elements of an ideal two's complement DAC transfer function (bipolar)

DAC input architectures can be divided into parallel and serial. Parallel input converters receive parallel input codes that simultaneously control internal DAC switches that select a number of weights that are summed. Serial converters receive a serial input that is internally converted to a parallel word after a defined number of clocking cycles. The internal parallel word then functions in the same manner as a parallel input converter.

The typical DAC consists of the following four major elements:

- The logic circuitry
- Some type of resistor or capacitor network
- A means of switching either a reference voltage or current to the proper input terminals of the network as a function of the digital value of each digital input bit
- A reference voltage or current

The following mathematical model is useful for discussing and analyzing the dynamic performance of a DAC. However, it should be kept in mind that this is an equivalent approximate mathematical model and does not necessarily reflect the physical operation of the DAC. This model constructs the output signal of the DAC by Equation (2).

$$V_{out}(t) = \left[\sum_{k=-\infty}^{\infty} w_k \delta(t - k\Delta t) \right] * f_R(t) = \sum_{k=-\infty}^{\infty} w_k f_R(t - k\Delta t) \quad (2)$$

where

- w_k = the input word to the DAC at time $k\Delta t$
- Δt = $1/f_{DATA}$ = the time between input words

$\delta(t)$ = the Dirac delta function
 $f_R(t)$ = the reconstruction filter
 $*$ is the convolution of the two functions

For the special case of the zero-order-hold DAC, the impulse response is represented by Equation (3).

$$f_R(t) = f_{ZH}(t) = \begin{cases} 1 & \text{for } 0 \leq t < \Delta t \\ 0 & \text{otherwise} \end{cases} \quad (3)$$

A return-to-zero (RZ) DAC has an impulse response represented by Equation (4).

$$f_R(t) = f_{RZ}(t) = \begin{cases} a & \text{for } 0 \leq t < \tau \\ 0 & \text{otherwise} \end{cases} \quad (4)$$

where a is a constant and τ is the duration of the output pulse from the DAC, which is assumed to be less than Δt . The purpose for a return-to-zero DAC is to generate images of the applied sequence in higher Nyquist bands.

The zero-order-hold DAC is illustrated in Figure 7, where a complex analog waveform is loaded into a DAC as a sequence of digital words. The DAC output is retained at its initial value until the next word is loaded.

The return-to-zero DAC is illustrated in Figure 9, where the complex waveform is loaded into a DAC as a sequence of digital words. The DAC output is retained at its initial value for a time τ , and then returns to 0 until the next word is loaded.

A DAC with a zero-order hold may be followed by an analog filter in order to make the reconstruction process more accurate. In this case the impulse response of the reconstruction filter is the convolution of that of the analog filter and that of the zero-order hold.

In many cases it is desirable to consider the input words, w_k , to be the sampled values of a function, $V_{in}(t)$, of continuous time. In that case, Equation (2) can be written as shown in Equation (5).

$$V_{out}(t) = \left[V_{in}(t) \sum_{k=-\infty}^{\infty} \delta(t - k\Delta t) \right] * f_R(t) \quad (5)$$

The asterisk in Equation (5) denotes the convolution integral. From this it follows that the Fourier transforms of the input and output signals are related by Equation (6).

$$\hat{V}_{out}(\omega) = \left[\sum_{l=-\infty}^{\infty} \hat{V}_{in}(\omega - l\omega_{DATA}) \right] \hat{f}_R(\omega), \quad (6)$$

where

$$\omega = 2\pi f,$$

$$\omega_X = 2\pi f_X$$

for any subscript, X . The situation of $V_{in}(t) = \cos(\omega_{in}t)$, or $\hat{V}_{in}(\omega) = \frac{1}{2}(\delta(\omega - \omega_{in}) + \delta(\omega + \omega_{in}))$, is of particular interest. In this case, Equation (6) yields Equation (7).

$$\hat{V}_{out}(\omega) = \left[\frac{1}{2} \sum_{l=-\infty}^{\infty} (\delta(l\omega_{DATA} - \omega_{in}) + \delta(l\omega_{DATA} + \omega_{in})) \right] \hat{f}_R(\omega) \quad (7)$$

The frequencies $lf_{DATA} \pm f_{in}$, for $|l| \geq 1$, are called the image frequencies of f_{in} . Note that both positive and negative values of l and f_{in} are required to generate all of the image frequencies. This is discussed in more

detail with examples in Annex E. In most cases it is desired for the reconstruction filter to remove the image frequencies while retaining the input frequency. As the input frequency approaches one-half of f_{DATA} , the input frequency and the lowest image frequency become very close, placing stringent requirements on the reconstruction filter.

The requirements on the analog filter are reduced with an interpolating DAC (also called an over-sampling DAC), which updates the DAC at a rate that is a multiple of the input data rate. A block diagram of an interpolating DAC follows in Figure 5.

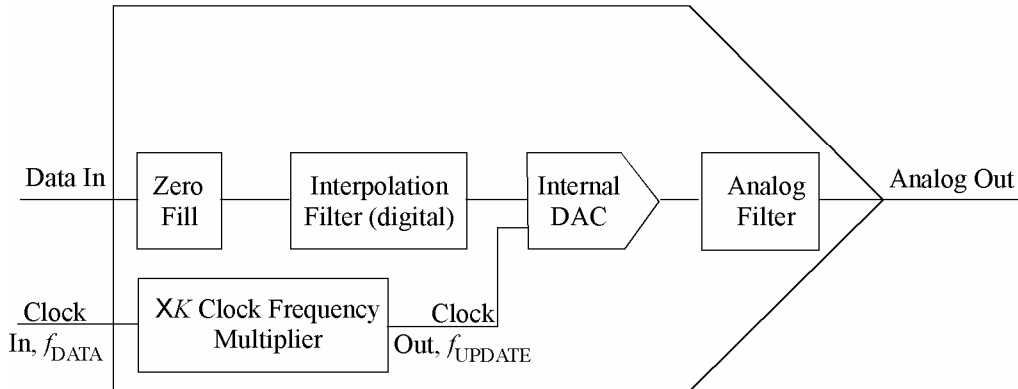


Figure 5—Block diagram interpolating DAC. If $K = 1$, the DAC is a noninterpolating DAC

The figure is a representation of a typical figure from a manufacturer for an interpolating, or oversampling, DAC. The zero-fill box places $K - 1$ zeros after every input word, where K is the oversampling factor. If $K = 1$ then the DAC is a noninterpolating DAC where the internal DAC inputs are identical to Data in. When the term DAC is used without additional specification, it refers to the complete diagram, not to the internal DAC. A DAC will usually have additional inputs to select the oversampling rate, the interpolation filter, and perhaps other parameters.

The interpolation filter is a digital filter that normally converts the zero-filled data into a more accurate representation of the continuous input signal. The interpolation filter has an impulse response of the form shown in Equation (8).

$$f_I(t) = \sum_{k=-\infty}^{\infty} a_k \delta(t - k\Delta t / K) \quad (8)$$

A frequency response that is periodic in frequency with period $f_{UPDATE} = Kf_{DATA}$. The effective reconstruction filter of the interpolating DAC has the frequency response shown in Equation (9).

$$\hat{f}_R(\omega) = \hat{f}_I(\omega) \hat{f}_{R_0}(\omega), \quad (9)$$

where

$\hat{f}_{R_0}(\omega)$ is the reconstruction filter of the internal DAC

Note that the analog filter may be nonlinear. In that case, Equation (9) is only approximate. In some sources it is stated that the image frequencies for an interpolating DAC are separated by f_{UPDATE} rather than by f_{DATA} , but this is incorrect. The zero-fill and interpolation-filter blocks produce image frequencies at the same locations as those for a non-interpolating DAC with the same input data rate. However, a digital filter can be designed to more effectively reduce these image frequencies.

This process can be better understood with frequency domain and time domain plots. Consider a PCM audio DAC with an update rate of 44 kHz. The “Data in” data stream is set to generate 10 tones starting at 2 kHz and ending at 20 kHz. The desired spectrum of the waveform generated by the “Data in” sequence is shown plotted in Figure 5.

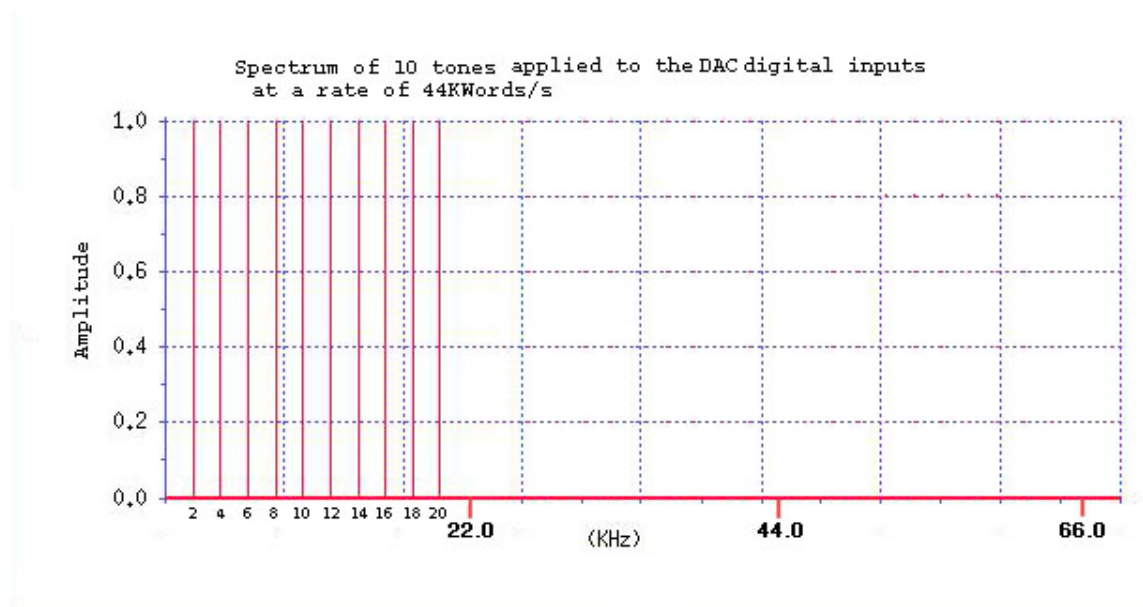


Figure 6—Spectrum of 10 tones of an audio signal that is applied to the circuit shown in Figure 5

If the parameter K is set to 1, the zero-order-hold DAC output will resemble the waveform shown in Figure 7 that is identified as “Unfiltered DAC Output.” The desired output is also shown (without the time delay that is associated with the filtering process).

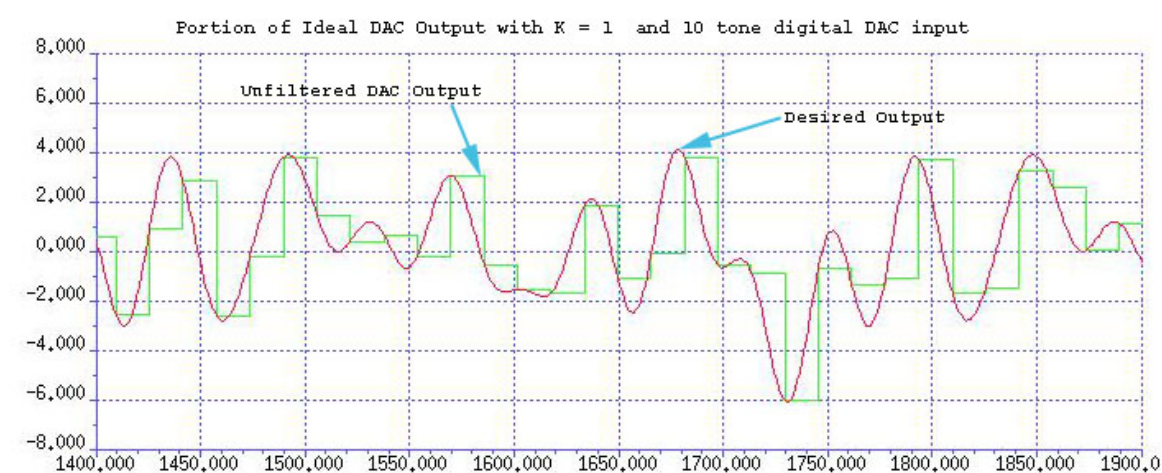


Figure 7—Plots of desired continuous signal and unfiltered DAC output when $K = 1$ (exclusive of time delays) for the circuit shown in Figure 5

The spectrum of the analog waveform observed at the input of the Analog Filter will resemble that shown in Figure 8.

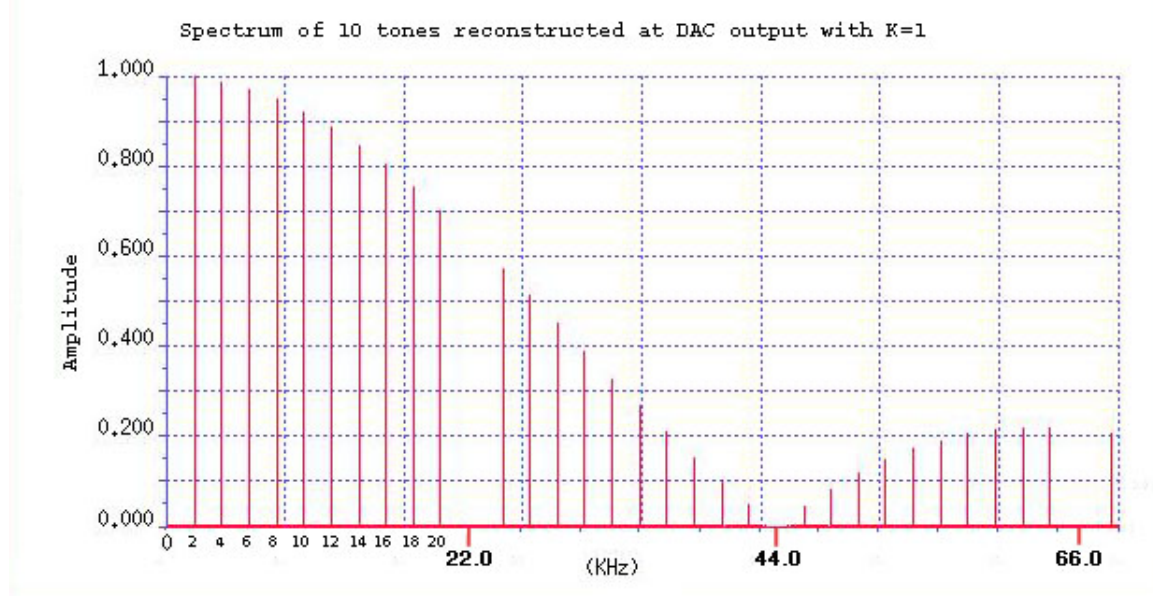


Figure 8—Spectrum of signal at the input to the analog filter for the circuit shown in Figure 5 when $K = 1$

The ideal Analog Output should have the same spectrum as that shown in Figure 6. In order to accomplish this, the Analog Filter must boost the gain appropriately for frequencies less than or equal to 20 kHz, and attenuate the unwanted image frequencies appropriately. It is very difficult to design an Analog Filter which will perform to the standards demanded by PCM audio users.

If $K = 16$, the signal that would be generated at the DAC output if the interpolation filter were bypassed would resemble that shown in Figure 9. The desired output after filtering is also shown in the plot. The time delays that are inherent in the reconstruction process are removed in order to clarify the description.

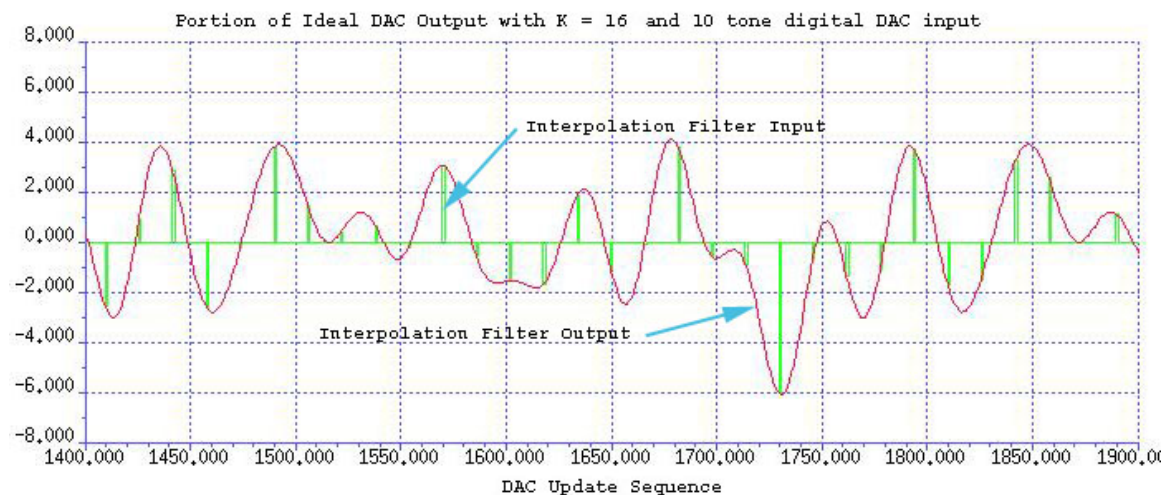


Figure 9—Plot of time domain signal for $K = 16$, and the desired output signal for the circuit shown in Figure 5 (time delays removed for clarity)

The spectrum of the signal that would be generated at the input to the interpolation filter input is ideally that shown in Figure 10. Note that the illustrated spectrum is truncated for clarity. Components continue at higher frequencies. Note also that $K = 16$ implies that the DAC update rate, f_{UPDATE} , is 16 times the input data rate of ~44 kHz or ~704 kHz.

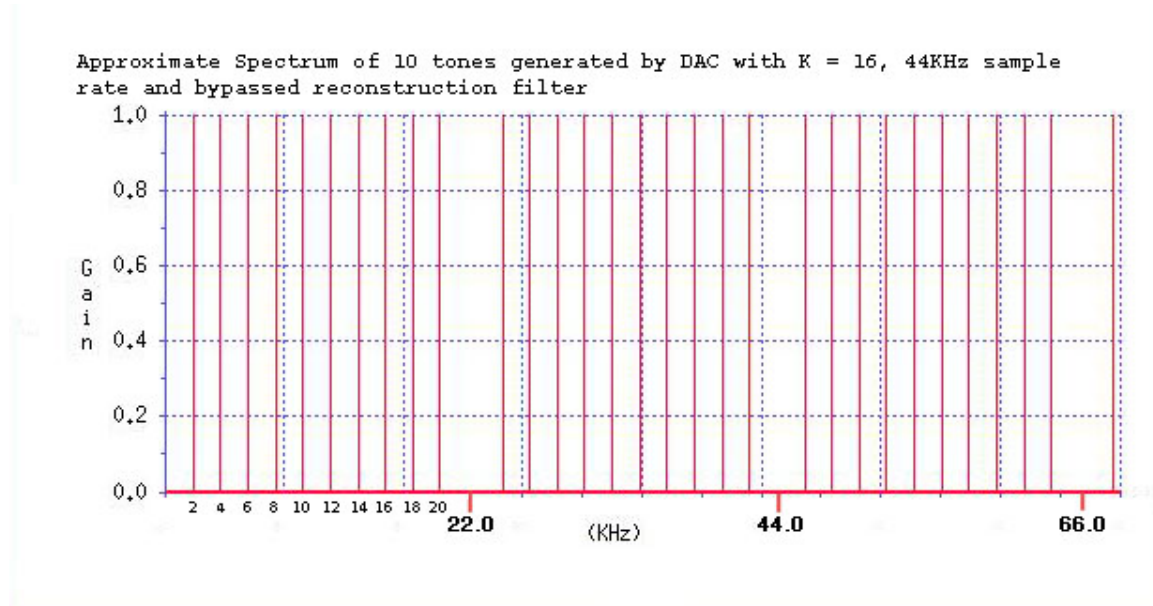


Figure 10—Spectrum of signal before interpolation filter for the circuit shown in Figure 5

The spectrum is flat, but the image frequencies are not attenuated. It is feasible to design a digital interpolation filter that will attenuate all the image frequencies (frequencies above 20 kHz) and not appreciably affect the desired frequencies (dc to 20 kHz). This will generate internal-DAC inputs that correspond to a time delayed version of the “Interpolation Filter Output” shown in Figure 9. The interpolation filter also passes image frequencies at multiples of f_{UPDATE} , ~704 kHz in this example. The analog filter is designed to attenuate those frequencies.

1.6 Guidance to the user

1.6.1 Interfacing

DACs present unique interfacing challenges, and without careful attention users can experience substandard results. As with all mixed-signal devices, DACs perform as expected only when the analog and digital domains are brought together in a well-controlled fashion. The user should fully understand the manufacturer’s recommendations with regard to proper signal buffering and loading, input signal connections, transmission line matching, circuit layout patterns, power supply decoupling, reference decoupling, and operating conditions. Edge characteristics for load-data pulse(s) and clock(s) must be carefully chosen to ensure that input signal purity is maintained with sufficient margin up to the digital input pin(s). Most manufacturers now provide excellent DAC evaluation boards, which demonstrate recommended layout techniques, signal conditioning, and interfacing for their DACs. If the characteristics of a new DAC are not well understood, then these boards should be analyzed or used before starting a new layout.

1.6.2 Coding

Some commonly used input data formats for digital-to-analog conversion are described in the paragraphs that follow.

Binary codes are most familiar in representing integers. In a natural binary integer code having N bits, the least significant bit (LSB) has weight of 2^0 , the next bit has a weight of 2^1 , and so on up to the most significant bit (MSB), which has a weight of 2^{N-1} . The value of a binary number is obtained by adding up the weights of all non-zero bits. When the weighted bits are added up, they form a unique number having any value from 0 to 2^{N-1} . Each additional trailing zero bit, if present, essentially doubles the size of the number.

In converter technology, because full scale is independent of the number of bits resolution, a more useful coding is fractional binary, which is always normalized to full scale. Integer binary can be interpreted as fractional binary if all integer values are divided by 2^N . The MSB has a weight of $1/2$, the next bit has a weight of $1/4$, and so forth down to the LSB, which has a weight of $1/2^N$. When the weighted bits are added up, they form a number with any of 2^N values, from 0 to $(1-2^{-N})$, of the full scale.

With BCD, each decimal digit is represented by a group of 4 binary-coded digits (or “quad”).

In fractional BCD, the LSB of the most significant quad has a weight of 0.1, the LSB of the next has weight of 0.01, the LSB of the next has a weight of 0.001, etc. Each quad has 10 permissible levels with weights 0 to 9. Group values in excess of 9 are not permitted.

In Gray code each bit represents a binary-weighted segment of the range and each code corresponds to a unique location in the range; but the bit weights do not readily combine to form a binary magnitude. In Gray code, as the number value changes, the transitions from one code to the adjacent code involve transitions of only one bit.

In complementary codes all bits are represented by their complements. Complementary binary (or inverted binary) is the negative true binary system. It is identical to the binary code except that all binary bits are inverted. Thus, zero scale is all ones while full scale is all zeros. Complementary BCD, for each quad of a BCD coded converter, is the code obtained by representing all bits by their complements. In complementary BCD, 0 is represented by 1111, and 9 is represented by 0110.

For bipolar DAC, the most often used binary codes are as follows:

- Twos complement
- Sign-magnitude
- Offset binary
- Ones complement

Twos complement code consists of a binary code for positive magnitudes (0 sign bit), and the twos complement of each positive number to represent its negative. The twos complement is formed arithmetically by complementing the code for the positive number and adding 1.

Ones complement code consists of a binary code for positive magnitudes (0 sign bit), and the ones complement of each positive number to represent its negative. The ones complement code for negative numbers is formed arithmetically by complementing the code for the positive number.

A sign-magnitude code determines the code appropriate for the magnitude of signed analog quantities and adds a polarity bit. The polarity bit can be either 0 or 1 for positive values. Table 1 assumes a 1 for positive values.

In offset binary code the weights are given by Equation (10).

$$w_m = 2^{m-1} \quad \text{for } m = 1, \dots, N-1 \quad (10)$$

$$w_N = -2^{N-1}$$

The offset binary code is widely used.

Note that the +FS output is represented by a virtual code that is 1 LSB greater than the maximum number that can be applied to the DAC. A similar phenomenon occurs at the –FS values for ones complement and sign-magnitude coding.

The parameter k represents the index of the input code. The total number of actual physical codes is 2^N for all the tabulated coding methods.

Table 1—Bipolar DAC input codes

SCALE	k	OFFSET BINARY (and BINARY)	TWOS COMPLEMENT	ONES COMPLEMENT	SIGN MAGNITUDE
+Full Scale	2^N	(1111....1111)+1	(01111....1111)+1	(01111....1111)+1	(1111....1111)+1
+Full Scale-1 LSB	2^N-1	1111....1111	0111....1111	0111....1111	1111....1111
+0.75 Full Scale		1110....0000	0110....0000	0110....0000	1110....0000
+0.5 Full Scale		1100....0000	0100....0000	0100....0000	1100....0000
+0.25 Full Scale		1010....0000	0010....0000	0010....0000	1010....0000
+1 LSB		1000....0001	0000....0001	0000....0001	1000....0001
+0		1000....0000	0000....0000	0000....0000	1000....0000
-0		----....----	----....----	1111....1111	0000....0000
-1 LSB		0111....1111	1111....1111	1111....1110	0000....0001
-0.25 Full Scale		0110....0000	1110....0000	1101....1111	0010....0000
-0.5 Full Scale	2^{N-2}	0100....0000	1100....0000	1011....1111	0100....0000
-0.75 Full Scale		0010....0000	1010....0000	1001....1111	0110....0000
-Full Scale+ 1LSB	1	0000....0001	1000....0001	1000....0000	0111....1111
-Full Scale	0	0000....0000	1000....0000	----....----	----....----

1.6.2.1 Adjustment range

Many converter types require no adjustment as purchased to meet specified accuracy. However, there are cases where (1) adjustments are called for in the specifications, (2) cost-savings can be effected by trimming inexpensive devices, with modest specs, for use over narrow ranges for better than specified accuracy, or (3) long-term corrections are necessary after long periods of operation.

The adjustment range is defined by many DAC manufacturers, as the range that a recommended adjustment mechanism can be used to change the full scale range and the offset of a DAC. The adjustment mechanism can be used to correct for the gain and offset deviations from the nominal, or to compensate for other gain and offset errors in the system, or it can be used to change slightly the range of a DAC. A typical case of such a change would involve converting a ± 5 volt DAC to a ± 5.12 volt DAC. Adjustment of a DAC beyond the specified adjustment range may compromise the linearity and stability obtainable from the DAC.

The adjustment can be implemented through many mechanisms, including the following:

- Internal registers and DACs that can be programmed to adjust the gain and the offset.
- Nodes that can be connected to potentiometers to adjust the gain and the offset. The use of potentiometers is generally not recommended, since the reliability of a potentiometer setting is reduced when many adjustments of parameters are made near the same region of a potentiometer setting.

- c) A node that can be connected to an external DAC to perform the functions described in mechanism a).

Proper adjustment of zero and full scale output in DACs is a procedure that requires great care and high-quality instruments. The meter used to read the output of a DAC must have enough resolution so that the test instrument does not limit the adjustment value at both ends of the range of the converter, (at zero and full scale or minus full scale and plus full scale).

Bipolar converters require knowledge of the DAC architecture to be properly adjusted. Some adjustment mechanisms will adjust the offset at the negative full scale of the converter without affecting the range. Other adjustment mechanisms will have interaction between the gain and the offset adjustments.

Many bipolar binary converters that use offset binary or twos complement coding employ analog offsetting to convert a unipolar design into bipolar. For example, a 0 to + 10 V DAC may have its output amplifier offset by –5 V, resulting in an output of –5 V corresponding to 00...0 input and +5 V (minus 1 LSB) corresponding to a 11...1 input. Such a converter should have its “zero” adjusted at –5 V (100...0 in twos complement).

The user should follow the specific instructions published in product datasheets.

It is not simple to calibrate a DAC based on the best-fit-straight-line algorithm. The best-fit approach is usually used to determine the worst-case INL error, where gains and offsets are not a factor. It is recommended that the adjustment of gain and offset be done at two specific codes in the range of the DAC.

Typically these are minus Full Scale (–FS) and plus Full Scale (+FS). In some applications the two points may be 20% of the FSR and 80% of the FSR.

1.6.3 Test conditions

DAC test specifications can be split into two groups: test conditions and test results. Typical examples of the former are: temperature, power supply voltages, clock frequency and reference voltages. Examples of the latter are: power dissipation, effective number of bits, spurious free dynamic range (SFDR), and integral nonlinearity (INL). The test methods defined in this standard describe the measurement of test results for given test conditions.

DAC specification sheets will often give allowed ranges for some test conditions (e.g., power supply ranges). This implies that the DAC will function properly and that the test results will fall within their specified ranges for all test conditions within their specified ranges.

Since the test condition ranges are generally specified in continuous intervals, they describe an infinite number of possible test conditions, which obviously cannot be exhaustively tested. It is up to the manufacturer or tester of a DAC to determine from design knowledge and/or testing the effect of the test conditions on the test result, and from there to determine the appropriate set of test conditions needed to accurately characterize the range of test results. For example, knowledge of the design may be sufficient to know that the highest power dissipation (test result) will occur at the highest power supply voltage (test condition), so the power dissipation test need be run only at the high end of the supply voltage range to check that the dissipation is within the maximum of its specified range. It is very important that relevant test conditions be stated when presenting test results.

1.6.4 Test equipment

One must ensure that the performance of the test equipment used for these tests significantly exceeds the desired performance of the DAC under evaluation. Users may need to include additional signal conditioning in the form of filters and pulse shapers. Accessories such as terminators, attenuators, delay lines, and other such devices are usually needed to match signal levels and to provide signal isolation to avoid corrupting the output signal.

Quality testing requires following established procedures, most notably those specified in standard ISO 9001. In particular, traceability of instrumental calibration to a known standard is important. Commonly used test setups are described in 4.2.

1.6.5 Test selection

When choosing which parameters to measure, one should follow the outline and hints in this clause to develop a procedure that logically and efficiently performs all needed tests on each unique setup. The standard has been designed to facilitate the development of these test procedures. For example, most users require that the DAC meets or exceeds a minimum SINAD limit for their application and that the nonlinearity of the DAC be specified. Certainly, the extent to which this standard is applied will depend upon the application; hence, the procedure should be tailored for each unique characterization plan.

1.7 Manufacturer supplied information

1.7.1 General information

Manufacturers shall supply the following general information:

- a) Device part number
- b) Physical characteristics: dimensions, packaging, pin outs
- c) Power requirements
- d) Environmental conditions: safe operating, non-operating, and specified performance temperature range; altitude limitations; humidity limits, operating and storage temperature ranges; vibration tolerance; and compliance with applicable electromagnetic interference specifications
- e) Any special or peculiar characteristics
- f) Compliance with other specifications
- g) Control signal characteristics
- h) Output signal characteristics
- i) Pipeline delay (if any)
- j) Exceptions to the above parameters where applicable

1.7.2 Minimum specifications

The manufacturer shall provide the following specifications. See appropriate clauses for definitions.

- a) Number of bits
- b) Sample rate (minimum, maximum, typical)
- c) Analog bandwidth (minimum, maximum, typical)
- d) Output signal full-scale range with nominal reference signal levels
- e) Output impedance
- f) Reference signal levels to be applied (minimum, maximum, typical)
- g) Supply voltages (minimum, maximum, typical)
- h) Supply currents (minimum, maximum, typical)
- i) Power dissipation (minimum, maximum, typical)
- j) Logic levels at digital inputs

1.7.3 Additional specifications

- a) Gain error (minimum, maximum, typical)
- b) Offset error (minimum, maximum, typical)
- c) Differential nonlinearity (DNL) (minimum, maximum, typical)
- d) Harmonic distortion and spurious response (minimum, maximum, typical)
- e) Integral nonlinearity (INL) (minimum, maximum, typical)
- f) Unadjusted static error (minimum, maximum, typical)
- g) Signal-to-noise ratio (minimum, typical)
- h) Signal-to-noise and distortion ratio (SINAD) (minimum, typical)
- i) Total harmonic distortion (THD) (maximum, typical)
- j) Spurious free dynamic range (SFDR) (minimum, typical)
- k) Effective number of bits (minimum, typical)
- l) Random noise and associated measurement bandwidth (maximum, typical)
- m) Frequency response
- n) Settling time (maximum, typical)
- o) Transition duration of step response (rise time) (maximum, typical)
- p) Slew rate limit (minimum, maximum, typical)
- q) Timing uncertainty (short-term instability)
- r) Crosstalk (channel-to-channel, input-to-output, etc.)
- s) Monotonicity
- t) Intermodulation distortion (maximum, typical)
- u) Noise power ratio (minimum, typical)
- v) Differential gain and phase (maximum, typical)

1.7.4 Critical DAC parameters

Table 2 is presented as a guide for a few common DAC applications. The wide range of DAC applications makes a comprehensive listing impossible. This table is intended to be a helpful starting point for users to apply this standard to their particular applications.

Table 2—Critical DAC parameters

Typical applications	Critical DAC parameters	Performance issues
Audio	SNR, THD, SINAD (THD+N)	Audio quality
Video/RAMDAC	GE, DNL, INL, DG, DP, OV, SFDR, TR, CM, ST	Picture quality
Control	DNL, T _s , GE	DNL monotonicity is often critical
Communications	IMD, MTPR, ACLR	Communications quality of service

ACLR = adjacent channel leakage power ratio
CM = channel matching
DG = differential gain
DNL = differential nonlinearity
DP = differential phase
ENOB = effective number of bits
GE = gain error
IMD = intermodulation distortion
INL = integral nonlinearity

OV = output voltage compliance range
MTPR = Missing Tone Power Ratio
SINAD = signal-to-noise and distortion ratio
SFDR = spurious free dynamic range
SNR = signal-to-noise ratio
T_s = settling time
THD = total harmonic distortion
THD+N = THD plus noise
TR = transient response

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1057™ - 2007, IEEE Standard for Digitizing Waveform Recorders.^{2, 3}

IEEE Std 1241™-2000, IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters.

IEEE Std 181™-2003, IEEE Standard on Transition, Pulses, and Related Waveforms.

ISO 9001:2008, Quality management systems—Requirements.⁴

MIL Std 810F-2000, Environmental Engineering Considerations and Laboratory Tests.⁵

² IEEE publications are available from the Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, Piscataway, NJ 08854, USA (<http://standards.ieee.org/>).

³ The IEEE standards or products referred to in this clause are trademarks of the Institute of Electrical and Electronics Engineers, Inc.

⁴ ISO publications are available from the ISO Central Secretariat, 1, ch. de la Voie-Creuse, Case postale 56, CH-1211 Geneva 20, Switzerland (<http://www.iso.ch/>). ISO publications are also available in the United States from the Sales Department, American National Standards Institute, 25 West 43rd Street, 4th Floor, New York, NY 10036, USA (<http://www.ansi.org/>).

⁵ MIL publications are available from Customer Service, Defense Printing Service, 700 Robbins Ave., Bldg. 4D, Philadelphia, PA 19111-5094.

3. Definitions, symbols, acronyms, and abbreviations

3.1 Definitions

For the purposes of this document, the following terms and definitions apply. *The IEEE Standards Dictionary: Glossary of Terms & Definitions* should be referenced for terms not defined in this clause.⁶

NOTE—The linearity specifications to follow (gain, offset, INL, DNL) depend on which transfer curve is used as a reference. One can have either “end-point” linearity or “best-fit” linearity. The first takes as reference curve a straight line between the minimum and maximum measured points. The second uses as reference a best-fit regression line through all measured points. Since “best-fit” linearity seems to be the most widely used, that definition is used as the standard. The main advantage of “best-fit” linearity is that it minimizes the linearity error (INL) and thus in general will result in higher parametric yield. End-point linearity is relevant when post-processing does not allow a linear regression.⁷

3.1.1 absolute accuracy (total) error: For a device that uses an internal reference, or a specified external reference, the absolute value of the worst-case difference between the actual output value and the nominal output value for any input code, without gain and offset correction (see figure).

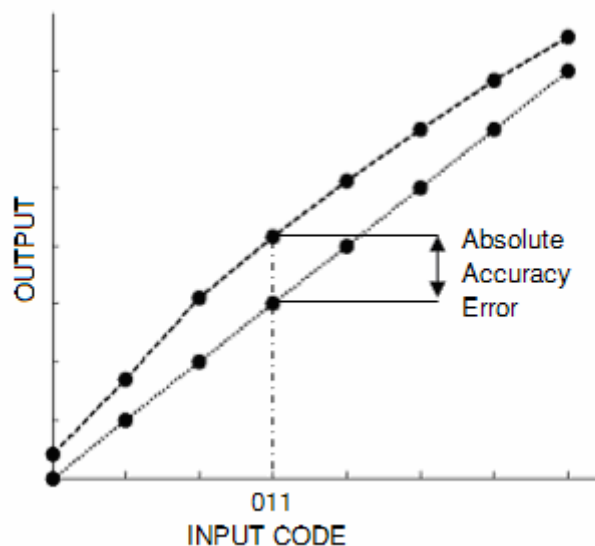


Figure 11—Absolute accuracy error of a DAC

3.1.2 adjacent channel leakage ratio (ACLR): A ratio in dB between the measured power within frequency channel relative to adjacent frequency channels.

⁶ The *IEEE Standards Dictionary: Glossary of Terms & Definitions* is available at <http://shop.ieee.org/>.

⁷ Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

3.1.3 bandwidth: The frequency at which the magnitude of the Fourier transform of the digital-to-analog converter's (DAC's) impulse response computed from the time derivative of its full-scale step response, is attenuated by $1/\sqrt{2}$ from its dc value. This definition of bandwidth is sample-rate independent and does not account for the $\sin(\pi fT)/(\pi fT)$ response arising from zero-order-hold waveform reconstruction.

3.1.4 channel matching (when applicable): Specifies the degree of matching between two or more digital-to-analog converters (DACs) in a single package.

3.1.5 clock and data feedthrough: Specifies the amount of energy in the digital-to-analog converter (DAC) output originating from clock and/or data signals respectively.

3.1.6 clock jitter: The standard deviation of variation in time of the active edge of the clock signal.

3.1.7 clock pulse width (latch pulse width): The minimum amount of time that the clock pulse should be left in the logic "1" state to achieve rated performance.

3.1.8 clock signal duty cycle: The fraction of the time the clock signal spends in excess of the logic threshold.

3.1.9 clock signal slew rate: The time derivative of the clock signal at the point where it crosses the logic threshold.

3.1.10 crosstalk: Undesired energy appearing in a digital-to-analog converter (DAC) channel as a result of coupling with another DAC channel in the same package that is generating a full-scale signal.

3.1.11 cumulative distribution function (cdf): The integral of the probability density function defined in the definition for **output propagation delay**. This function is positive and monotonic.

3.1.12 data rate (f_{DATA}): The rate at which input words are supplied to the digital-to-analog converter (DAC).

3.1.13 differential gain and phase: These tests that were historically performed for video and television applications where a chroma subcarrier was used. Differential gain is defined as the percentage difference between the output amplitudes of a small chroma sine wave superimposed on two defined voltage levels. Differential phase is defined as the difference in the output phase of a small chroma sine wave superimposed on two defined voltage levels.

3.1.14 differential gain: The ratio of the maximum gain and the minimum gain of a small-amplitude sine wave that is superimposed on multiple static levels, divided by the average gain. This test was historically performed for video and television applications where a chroma subcarrier was used.

3.1.15 differential phase: The difference in the output phase of a small high-frequency sine wave for two stated levels of a low frequency signal on which it is superimposed. This test was historically performed for video and television applications where a chroma subcarrier was used.

3.1.16 differential nonlinearity (DNL): The differences between the output at adjacent input codes, divided by the measured average step width of the digital-to-analog converter (DAC) under test minus 1.

3.1.17 differential-output impedance: For a differential-output digital-to-analog converter (DAC), the impedance between the positive output and the negative output.

3.1.18 digital feedthrough: This is the glitch transferred to the output of a digital-to-analog converter (DAC) channel in response to a change in an input. It includes data feedthrough and clock feedthrough.

3.1.19 digital-to-analog converter (DAC): A converter that translates digital input codes into analog output values.

3.1.20 dynamic range: *See: spurious free dynamic range (SFDR).*

3.1.21 effective number of bits (ENOB): A measure of the signal-to-noise and distortion ratio used to compare actual digital-to-analog converter (DAC) performance to the expected performance of an ideal DAC.

3.1.22 full-scale (FS) errors: The difference between the actual digital-to-analog converter (DAC) output and the expected nominal output when a digital code is applied, which should generate the maximum and the minimum outputs. Unlike gain error, offset error is included in the FS error measurement.

3.1.23 full-scale range (FSR): The difference between the most positive and most negative analog outputs of a converter's operating range. Generally FSR includes the virtual codes at the minimum and the maximum outputs. Thus, a -10 V to $+10\text{ V}$ digital-to-analog converter (DAC) will have FSR equal to 20.000 V .

3.1.24 gain and offset: Gain and offset are the values by which the ideal output values are multiplied and then to which the ideal output values are added, respectively, to cause the output values to satisfy specified conditions. Two conditions are commonly used: "independently based" where the sum of the squared deviations from the ideal output values is minimized, and "terminal-based" where the ideal outputs are matched at the first and the last code.

3.1.25 gain matching: In a multichannel converter, the difference between the largest gain and the smallest gain, expressed in % FSR or dB.

3.1.26 glitch: A short, undesirable transient in the analog output.

3.1.27 glitch area (GA): The time integral of the analog value of the glitch transient.

3.1.28 glitch energy (GE): The time integral of the electrical power of the glitch transient.

3.1.29 harmonic: A frequency that is an integer multiple of the fundamental.

3.1.30 hold time (t_{H}): The amount of time required for the digital inputs to remain deterministic after a trigger clock edge.

3.1.31 ideal code bin width (Q): The ideal full-scale output range (FSR) divided by the total number of codes.

3.1.32 impulse: A time signal that approximates a Dirac delta function.

3.1.33 impulse DAC: An idealized digital-to-analog converter (DAC) for which the output is a sequence of impulses proportional to the input word at the update rate.

3.1.34 impulse response: Response of a device with a discrete time input to an impulse sequence applied at the input. The output of the device may be either discrete time or continuous time.

3.1.35 input data rate (f_{DATA}): The rate at which input words are supplied to the digital-to-analog converter (DAC) from an external source.

3.1.36 integral nonlinearity (INL): The maximum difference between the ideal and actual analog output values after correcting for gain and offset.

3.1.37 Intermodulation Distortion (IMD): The ratio of amplitude of the intermodulation product with the largest amplitude to the largest amplitude generated test tone.

3.1.38 interpolation filter: The filter in an interpolating digital-to-analog converter (DAC) that converts the digital data at the input data rate to digital data at the update rate.

3.1.39 interpolation ratio: The ratio of the update rate to the input data rate in an interpolating digital-to-analog converter (DAC).

3.1.40 jitter: Variations in the timing of a signal transition.

3.1.41 least significant bit (LSB): The input bit that has the smallest mathematical weight.

3.1.42 major carry transition: The midscale point where the MSB changes from low to high and all other bits change from high to low, or where the MSB changes from high to low and all other bits change from low to high. This point is often where the worst switching noise occurs.

3.1.43 monotonic digital-to-analog converter (DAC): A DAC that has output values that do not decrease (increase) for a uniformly increasing (decreasing) input codes, disregarding random noise. *See: monotonicity.*

3.1.44 monotonicity: A property of the transfer function that ensures the consistent increase or decrease of the analog output in response to a consistent increase or decrease of the digital input. (The following figure illustrates non monotonic conversion). There are some data converter architectures that are monotonic by design, e.g., thermometer-coded digital-to-analog converters (DACs).

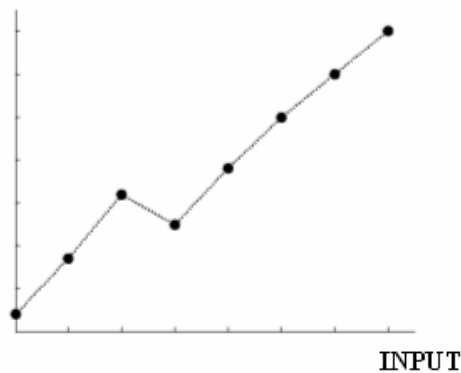


Figure 12—Transfer function of a non monotonic DAC

3.1.45 most significant bit (MSB): The digital input bit in a data converter code that has the greatest weight, equal to 2^{N-1} , where N is the number of bits.

3.1.46 multiplying DAC: A digital-to-analog converter (DAC) that allows a signal to be applied to the reference input pin to scale the DAC output.

3.1.47 multiplying DAC: A digital-to-analog converter (DAC) that allows a signal to be applied to the reference input pin to scale the DAC output.

3.1.48 multitone power ratio (MTPR): The spurious free dynamic range containing multiple carrier tones of equal amplitude. It is measured as the difference between the rms amplitude of the largest carrier tone to the peak spurious signal in the region of a removed tone.

3.1.49 noise: Noise has historically been an ambiguous term. In this standard, noise is any deviation between the desired nominal output signal and the actual output signal except deviations caused by linear time invariant system response (gain and phase shift), a dc level shift, total harmonic distortion, or an error in the applied update rate. For example, noise includes the effects of random errors, nonlinearities producing harmonics at frequencies greater than those used in measuring total harmonic distortion, apparent quantization error, and spurious signals.

3.1.50 noise and distortion (NAD): The sum of the effects of noise and total harmonic distortion.

3.1.51 noise power ratio (NPR): It is the measure of the spectral power of all contributed errors, such as intermodulation and harmonic distortion, in a narrow frequency-slot within the baseband of the composite signal being processed.

3.1.52 noise spectral density: The digital-to-analog converter (DAC) output noise normalized to a 1 Hz bandwidth.

3.1.53 Nyquist frequency: One-half of the data rate of a digital-to-analog converter (DAC).

3.1.54 Nyquist band: The n^{th} Nyquist band is the band of frequencies between $n-1$ times the Nyquist frequency and n times the Nyquist frequency.

3.1.55 offset: *See: gain and offset.*

3.1.56 offset binary coding: For bipolar signals; Offset binary is a digital coding scheme in which the most negative value is represented by all zeros (00000000) and the most positive value is represented by all ones (11111111).

3.1.57 output compliance range: The range of allowable voltage at the output of a current output digital-to-analog converter (DAC). Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

3.1.58 output propagation delay (t_{PD}): The delay between the 50% point of the clock edge and the time when the DAC output traverses 50% of the output transition. The propagation delay includes the effect of digital pipelines, and analog filtering.

3.1.59 pass band: Frequency band in which a sine wave waveform generated by a digital-to-analog converter (DAC) is not significantly attenuated.

3.1.60 phase noise: Random fluctuations in the phase of a periodic signal.

3.1.61 phase nonlinearity: to be completed when the test method is finished.

3.1.62 pipeline delay: A measure of the latency in terms of digital-to-analog converter (DAC) clock cycles between the clock transition that initiates sampling of the digital input and the presentation of the output value of that sample.

3.1.63 power-supply rejection (PSR): The amount of change in the converter's output (often measured at full scale), as the power-supply voltage is changed from its nominal value.

3.1.64 power-supply rejection ratio (PSRR): The ratio of the amount of change in the converter's output (often measured at full scale), relative to the change of the power-supply voltage.

3.1.65 power-supply sensitivity (PSS): Synonymous with power-supply rejection (PSR).

3.1.66 probability density function (pdf): For a continuous random variable, the function $f_X(x)$, which has the interpretation that $f_X(x)dx$ is the probability that the random variable, X , lies in the interval $(x, x + dx)$.

3.1.67 quantization: The mathematical operation of truncating or rounding a value of arbitrary precision to a lower fixed resolution.

3.1.68 quantization error: The error caused by conversion of a variable having a continuous range of values to a quantized form having only discrete values, as in analog-to-digital conversion. The error is the difference between the original value and its quantized representation translated into input units. A digital-to-analog converter (DAC) does not generate quantization error. The error that is caused by the resolution limitation of a DAC is called the truncation error.

3.1.69 quantization noise: Equivalent noise produced during the quantization of a continuous range variable. A quantization process of step size Q produces an rms quantization noise of $Q/\sqrt{12}$ when the continuous variable range is much larger than Q .

3.1.70 random noise: A non-deterministic fluctuation in the output of a digital-to-analog converter.

3.1.71 reconstruction filter: The conceptual filter that relates the input data sequence of a digital-to-analog converter (DAC) to its output signal.

3.1.72 record of data: A sequential collection of samples.

3.1.73 relatively prime: Describes integers whose greatest common divisor is 1.

3.1.74 residuals: In curve fitting, the differences between the recorded data and the fitted function.

3.1.75 resolution: The number of output levels the digital-to-analog converter (DAC) is designed to produce. Usually stated as the number of bits used (the base two logarithm of the number of levels). A 1-bit DAC is designed to produce 2 (2^1) levels while an 8 bit DAC is designed to produce 256 (2^8) levels.

3.1.76 root-mean-square (rms): For a given set of data, the square root of the arithmetic mean of the squared values of each of the data.

3.1.77 root-sum-square (rss): For a given set of data, the square root of the sum of the squared values of each of the data.

3.1.78 sampling: The process of assigning discrete time values to a continuous time signal.

3.1.79 settling time interval: The time at which the step response enters and subsequently remains within a specified error band around the final value, measured from the 50% reference level instant of the response. The final value is defined to occur 1 s after the beginning of the step unless otherwise specified.

3.1.80 setup time interval (t_{SU}): The amount of time required for the digital inputs to remain deterministic prior to a leading transition of the update signal.

3.1.81 short-term settling time interval: Measured from the 50% point of the output, the time at which the step response enters and subsequently remains within a specified error band around the final value. The final value is defined to occur at a specified time less than or equal to one second after the beginning of the step.

3.1.82 signal-to-noise and distortion ratio (SINAD): For a pure sine-wave input of specified amplitude and frequency, the ratio of the root-mean-square (rms) amplitude of the digital-to-analog converter (DAC) filtered reconstructed output sine wave to the rms amplitude of the output noise and distortion

3.1.83 signal-to-noise ratio (SNR): For a pure sine-wave input of specified amplitude and frequency, the ratio of the root-mean-square (rms) amplitude of the digital-to-analog converter (DAC) filtered reconstructed output sine wave to the rms amplitude of the output noise (excluding the harmonics).

3.1.84 signed binary coding: A coding scheme in which the MSB represents the sign (positive or negative) of a binary number. In this scheme, with an 8-bit word, “–2” is represented by 10000010 and “2” is represented by 00000010.

3.1.85 slew rate: The maximum rate at which the digital-to-analog converter (DAC) output can change without resulting in a deviation from the response expected from a linear system.

3.1.86 spurious components: Persistent sine-wave components at frequencies other than harmonic frequencies of the fundamental.

3.1.87 spurious free dynamic range (SFDR): Specifies the available signal range as the difference in magnitude between the amplitude of the fundamental and the amplitude of the largest spurious component in the frequency band of interest.

NOTE—Some industry spec sheets include harmonics along with spurious components in their specification of SFDR. It is important to specify for any SFDR spec whether or not the harmonics are included.

3.1.88 stop-band rejection: The amount of attenuation of a frequency outside the pass band applied to the digital-to-analog converter (DAC), relative to a full-scale signal applied at the DAC input within the pass band.

3.1.89 temperature drift: The maximum change from the ambient (25 °C) value to the value at either TMIN or TMAX. For offset the drift is reported in ppm of full-scale range (FSR) per °C. For gain drift, the drift is reported in ppm per °C.

3.1.90 total harmonic distortion (THD): The ratio of the square root of the sum of the squares of the rms amplitudes of the harmonic components of the output sine wave (i.e., of sinusoidal components appearing at multiples of the fundamental output sine wave frequency) to the rms value of the output sine wave. It is typically expressed in decibels or percent.

3.1.91 total harmonic distortion plus noise (THD+N): The ratio of the square root of the sum of the squares of the amplitudes of all components of the output signal (excluding the fundamental) to the amplitude of the fundamental output, over a specified frequency band. It is typically expressed in decibels or percent. It is similar to THD, but also includes the noise.

3.1.92 transfer function: The function that describes the relationship between the digital input and the analog output.

3.1.93 transient response: The measured output response to an input code change having designated state levels corresponding to a full scale step signal. Transient response includes the combined behavior of transition duration, aberrations, and settling error.

3.1.94 transition duration (t_d): The difference between the two reference level instants of the same transition. Unless otherwise specified, the two reference levels are the 10% and 90% reference levels.

NOTE 1—See Figure 13 and Figure 15.

NOTE 2—The following are deprecated terms: risetime, falltime, leading edge, rising edge, trailing edge, falling edge, and transition time. The terms risetime, falltime, and transition time, although widely used, are deprecated because they are ambiguous and confusing. First, the use of the word time in this standard refers exclusively to an instant and not an interval. Also, if the first transition of a waveform within a waveform epoch (IEEE Std 181-2003) happens to be a negative transition, some users may refer to its transition duration as its risetime, and some others may refer to its transition duration as its falltime. If the use of these deprecated terms is required, then risetime is synonymous with the transition duration of a positive-going transition, and falltime is synonymous with the transition duration of a negative-going transition. If the upper and lower state boundaries of the two states are not the user-defined reference levels (for example, the 10% and 90% reference levels), then the duration of a transition is not equal to the transition duration.

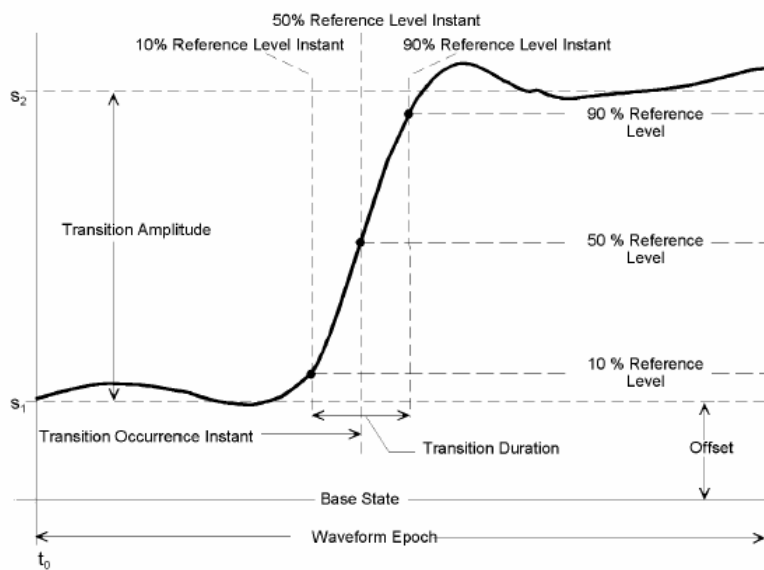


Figure 13—Positive single transition

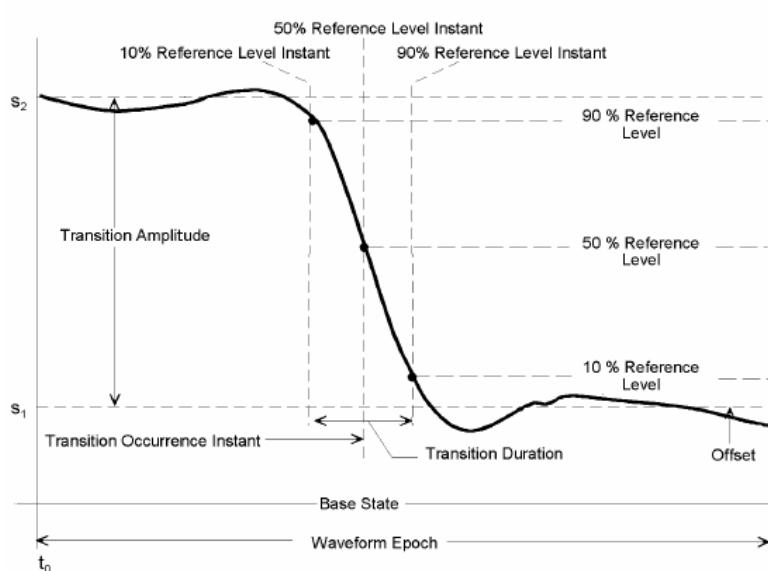


Figure 14—Negative single transition

3.1.95 two tone intermodulation distortion (IMD): The ratio of the rms amplitude of either of two equal-amplitude input tones to the rms amplitude of the worst third order intermodulation product; reported in dBc.

3.1.96 two tone SFDR: The ratio of the rms amplitude of either equal-amplitude input tone to the rms amplitude of the peak spurious component. The peak spurious component may or may not be an intermodulation distortion (IMD) product. It also may be reported in dBc (i.e., degrades as signal level is lowered) or in dBFS (i.e., always relates back to converter full scale).

3.1.97 unipolar: A signal that swings from zero to the positive full-scale, thus having only a positive polarity.

3.1.98 update rate (f_{UPDATE}): The rate at which analog values are updated at the output of the digital-to-analog converter (DAC).

3.1.99 zero-order-hold DAC: An ideal digital-to-analog converter (DAC) that produces an analog output proportional to its input word immediately after the data clock pulse corresponding to the word and maintains this output value until the next data clock pulse. This is mathematically equivalent to an impulse DAC followed by a filter whose impulse response is a constant proportional to the value of the input impulse for one data clock pulse duration and zero elsewhere.

3.2 Symbols

ε = error, used for total error and error band

ε_{rms} = root-mean-square value of ε

$\varepsilon[k]$ = difference between $U[k]$ and ideal value of $U[k]$ computed from G and V_{OS}

θ = phase, expressed as radians

π = constant, ratio of the circumference of a circle to the diameter

ρ = reflection coefficient

σ = standard deviation; sometimes used as a measure of noise amplitude, which is the standard deviation of the random component of a signal.

σ_{σ} = standard deviation of the standard deviation estimator (for example, standard deviation of the estimated noise amplitude)

σ_t = hold jitter

σ^2 = variance; sometimes used to describe random noise power

τ = sampling period, the inverse of f_s

$\omega = 2\pi f$ = angular frequency, expressed in radians per second

ω_i = angular input frequency in radians/second

a = general purpose real number

A = sinusoidal amplitude

B = test tolerance in fractions of a least significant bit (Q). Also used as an amplitude

BW_m = measurement bandwidth

C = offset