

IEEE Standard for Terminology and Test Methods of Digital-to- Analog Converter Devices

IEEE Instrumentation and Measurement Society

Developed by the
Waveform Generation, Measurement, and Analysis
Technical Committee (TC-10)

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Abstract: Terminology and test methods to clearly document prevalent world-wide terms used to describe and test digital-to-analog converters (DACs) are provided. It is restricted to monolithic, hybrid, and module DACs and does not cover systems encompassing DACs.

Keywords: DAC, digital-to-analog converter, IEEE 1658™, SFDR, SNR, spectrum, test methods, test terminology

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Introduction

This introduction is not part of IEEE Std 1658-2023, IEEE Standard for Terminology and Test Methods of Digital-to-Analog Converter Devices.

This standard is divided into 16 clauses plus annexes. [Clause 1](#) is a basic orientation. For further investigation, users of this standard can consult [Clause 2](#), which contains references to other IEEE standards on waveform measurement and relevant International Standardization Organization (ISO) documents. The definitions of technical terms and symbols used in this standard are presented in [Clause 3](#). [Clause 4](#) through [Clause 16](#) present a wide range of tests that measure the performance of a digital-to-analog converter. Annexes, containing the bibliography and informative comments on the tests presented in [Clause 4](#) through [Clause 16](#), augment the standard.

This standard defines the terms, definitions, and test methods used to specify, characterize, and test digital-to-analog converters (DACs). It is intended for the following:

- Individuals and organizations who specify DACs to be purchased
- Individuals and organizations who purchase DACs to be applied in their products
- Individuals and organizations whose responsibility is to characterize and write reports on DACs available for use in specific applications
- Suppliers interested in providing high-quality and high-performance DACs to acquirers

This standard is designed to help organizations and individuals:

- Incorporate quality considerations during the definition, evaluation, selection, and acceptance of supplier DACs for operational use in their equipment
- Determine how supplier DACs should be evaluated, tested, and accepted for delivery to end users

This standard is intended to satisfy the following objectives:

- Promote consistency within organizations in acquiring third-party DACs from component suppliers
- Provide useful practices on including quality considerations during acquisition planning
- Provide useful practices on evaluating and qualifying supplier capabilities to meet user requirements
- Provide useful practices on evaluating and qualifying supplier DACs
- Assist individuals and organizations judging the quality and suitability of supplier DACs for referral to end users

Several standards have previously been written that address the testing of DACs either directly or indirectly. These include the following:

- IEEE Std 1057™, which describes the testing of waveform recorders.
- IEEE Std 1241™, which addresses the testing of Analog-to-Digital Converters.
- IEEE Std 746™, which addresses the testing of Analog-to-Digital and Digital-to-Analog Converters, used for PCM television video signal processing.
- JEDEC Standard 99, addendum number 1, which deals with the terms and definitions used to describe Analog-to-Digital and Digital-to-Analog Converters. This standard does not include test methods.

- IEC 60748-4-1:1993, Semiconductor devices—Integrated circuits—Part 4: Interface integrated circuits—[Section 1](#): Blank detail specification for linear digital-to-analog converters (DAC).
- IEC 60748-4-2:1993, Semiconductor devices—Integrated circuits—Part 4: Interface integrated circuits—[Section 2](#): Blank detail specification for linear analog-to-digital converters (ADC).
- IEC 60748-4-3:2006, Semiconductor devices—Integrated circuits—Part 4-3: Interface integrated circuits—Dynamic criteria for analog-digital converters (ADC).

IEEE Std 1658 for digital-to-analog converters is intended to focus specifically on terms and definitions as well as test methods for DACs for a wide range of applications.

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IEEE Standard for Terminology and Test Methods of Digital-to-Analog Converter Devices

1. Overview

1.1 Scope

This standard defines terminology and test methods to clearly document prevalent world-wide terms used to describe and test digital-to-analog converters (DACs). Although principally applicable to monolithic, hybrid, module DACs, most of the definitions and test procedures can be applied to systems containing DACs.

1.2 Purpose

This standard is written to clear up confusion relating to the terms and definitions concerning DACs. Test methods are defined with expected output and analysis of the data generated from these test methods. Product specifications are defined in clear terms that will be understandable by all international users and manufacturers.

1.3 Word usage

The word *shall* indicates mandatory requirements strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*).^{6,7}

The word *should* indicates that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required (*should* equals *is recommended that*).

The word *may* is used to indicate a course of action permissible within the limits of the standard (*may* equals *is permitted to*).

The word *can* is used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

⁶The use of the word *must* is deprecated and cannot be used when stating mandatory requirements, *must* is used only to describe unavoidable situations.

⁷The use of *will* is deprecated and cannot be used when stating mandatory requirements, *will* is only used in statements of fact.

1.4 Discussion of scope and purpose

A digital-to-analog converter (DAC) receives digital input data and converts it to an analog output. The material presented in this standard is intended to provide common terminology and test methods for the testing and evaluation of DACs. The standard graphic symbol for a DAC is given in Figure 1, where N represents the width of the data word (in bits).



Figure 1—DAC graphic symbol

The information in this standard is useful both to manufacturers and users of DACs in that it provides a basis for evaluating and comparing existing devices, as well as providing a template for writing specifications for the procurement of new ones. This standard identifies DAC error sources and provides test methods to measure them. In some applications, the information provided by the tests described in this standard could be used to correct DAC errors, e.g., correction for gain and offset errors.

Note that this standard has many similarities to IEEE Std 1057 [B12]⁸ and IEEE Std 1241 [B13].

1.5 Digital-to-analog converter and analog-to-digital converter differences and similarities

DACs and analog-to-digital converters (ADCs) perform complementary functions. DACs receive a digital signal and generate an analog equivalent, while ADCs receive an analog signal and generate a digital equivalent. Some of the subtleties are summarized in the following list:

- a) Transfer curve differences (see Figure 2)
 - 1) For a DAC, each digital input corresponds to a single analog output value.
 - 2) For an ADC, each digital output corresponds to an interval of analog input values. The analog quantity defined in the transfer curve of an ADC, the code transition level $T[k]$, is usually defined to occur at the point where 50% of the output codes are greater than a specified digital output.

⁸The numbers in brackets correspond to those of the bibliography in Annex D.

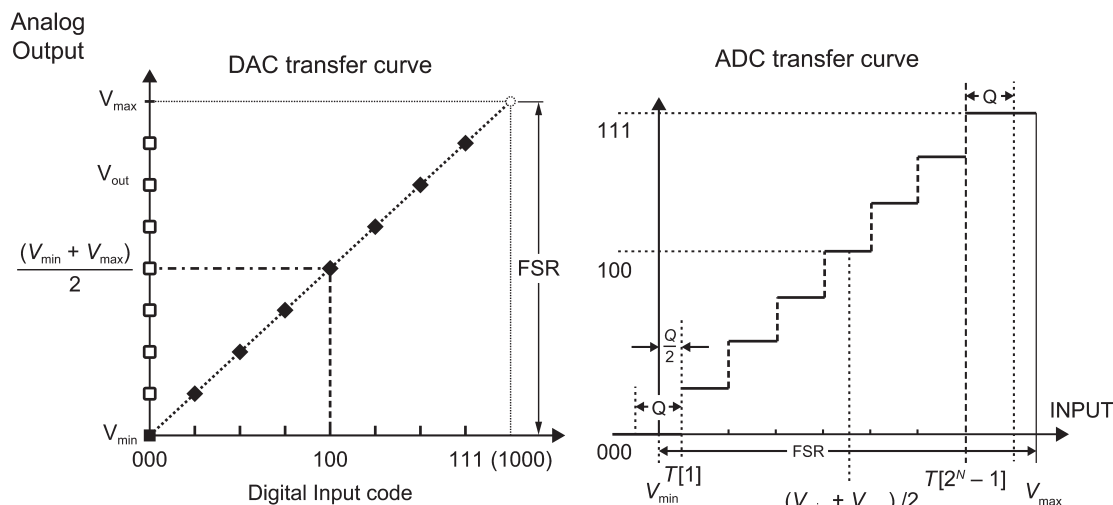


Figure 2—Transfer curves of ideal 3-bit unipolar DAC and ADC

- b) Quantization differences
 - 1) In a DAC, the input is a digital input code and the output is an analog representation of the input.
 - 2) In an ADC, the input is analog and the output is the quantized representation of the input.
- c) Time-domain differences
 - 1) A DAC with a constant input code produces a continuous nominally fixed analog output that may contain additive noise.
 - 2) An ADC with a constant input may generate a distribution of quantized outputs because of the presence of noise.
- d) Frequency-domain differences
 - 1) A DAC driven by a single-frequency digital sine wave at its input will produce at its output a single frequency between dc and 1/2 the output update rate, i.e., the rate at which codes are provided to the internal D/A section. Additionally, other frequencies will be produced that are at the multiples of the output update rate plus/minus the input frequency.
 - 2) An ADC with any fixed frequency analog input will produce a data record that will appear to contain frequencies only up to one half the sampling rate.
- e) Both a DAC and an ADC require an internal or external reference current or voltage that will cause them to have an output that can be in some way traced to standard units of voltage or current.

There are also some subtle differences between ADCs and DACs in the area of aliasing and image frequency generation. Aliasing is a phenomenon usually associated with ADCs while the generation of image frequencies is usually associated with DACs. The two phenomena are very closely related. In both cases there is a reference frequency, f_s . For an ADC this is the sampling frequency, the rate at which samples are taken. For a DAC this is the output update rate, the rate at which data words are supplied (after possible digital pre-processing) to the internal D/A section. Two positive frequencies, f_1 and f_2 , are said to be aliases of one another if they satisfy Equation (1):

$$f_2 - f_1 = lf_s, \text{ or } f_2 + f_1 = lf_s \quad (1)$$

where

l is any integer

Note that the integer l can be positive, negative, or zero. Recall that the n^{th} Nyquist band consists of all frequencies, f , satisfying $(n-1)f_s/2 \leq f < nf_s/2$. It is fairly easy to show that any frequency, f , has exactly one alias in each Nyquist band.

When an input signal of frequency, f , is supplied to an ADC the resulting samples will be a signal whose frequency is the alias of f in the first Nyquist band. Thus, many different frequencies get mapped into a single frequency. This phenomenon is called aliasing. Conversely, when an input sequence with a frequency in the first Nyquist band is supplied to a DAC, the output signal will generally contain components at all of the aliases of the input signal frequency. These spurious output frequencies are called images of the input frequency. Note that a sine-wave input sequence to a DAC can always be considered to be in the first Nyquist band because the sampled values of a sine wave in a higher Nyquist band are exactly equal to the sampled values of the signals alias in the first Nyquist band.

The aliasing phenomenon has complementary implications for the measurement of frequency response using sine-wave inputs for ADCs and DACs. For a DAC, inputs only need to be generated in the first Nyquist band, but the outputs need to be measured at the images of the input frequency in all bands of interest. For an ADC, the input signals shall be in all Nyquist bands of interest, but the outputs always appear at the alias in the first Nyquist band of the input signal.

1.6 Digital-to-analog converter background

This standard considers only those DACs whose output values have discrete values for discrete input words. Although different methods exist for representing a discrete sequence of binary words as a continuous analog signal, an underlying model implicit in many of the tests in this standard assumes that the relationship between the input code and the output value (transfer curve) approximates a straight line as depicted in [Figure 3](#) and [Figure 4](#). Applying this model to a code-input DAC, the full-scale output range (FSR) at the DAC is divided into uniform intervals, with nominal separation of Q . The number of code levels in the discrete transfer curve is equal to 2^N where N is the number of bits of the DAC. The number of intervals is $2^N - 1$. The full-scale outputs are generally defined as physical quantities (voltage or current) and are usually given as the values with code 0 applied, and code 2^N applied. The code for 2^N is generally a virtual code that does not exist but serves as a good definition of the DAC. Thus, a 0 V to 10 V 10-bit DAC will theoretically never actually generate 10.0 V. If the code $2^N - 1$ is applied (the last physically realizable code), the ideal output will be approximately 9.9902 V. The 3-bit DAC modeled in [Figure 3](#) could be described as an 8 V FS unipolar DAC, where each binary least significant bit would correspond to a 1 V increment in the output. Note that the DAC could not actually generate a +8 V output.

In addition to unsigned binary shown in [Figure 3](#), DACs may use two's complement, one's complement, sign-magnitude, Gray, Binary-Coded-Decimal (BCD), or other digital coding schemes. The 3-bit DAC modeled in [Figure 4](#) could be described as a ± 4 V bipolar two's complement DAC, where each binary least significant bit would correspond to a 1 V increment in the output. Note that the DAC could not actually generate a +4 V output.

DAC errors can be divided into the categories of static and dynamic. The static errors are usually caused by mismatch of the components and limit the accuracy at low speed. The static performance is often described by measures of differential and integral nonlinearities (DNL[k] and INL[k], where the DNL and INL are defined for each input word k). The dynamic errors, such as settling errors, glitches, etc., are important and they become more significant with higher update rates and when higher frequency waveforms are being synthesized by the DAC. To analyze the effect of errors, it is usually easier to consider the DAC's behavior in frequency domain using measures, such as the spurious free dynamic range (SFDR) and signal-to-noise and distortion (SINAD) ratio.

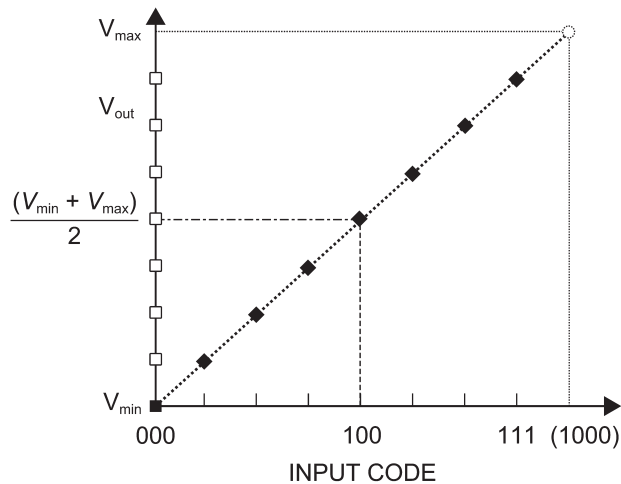


Figure 3—Elements of an ideal linear DAC transfer curve (unipolar)

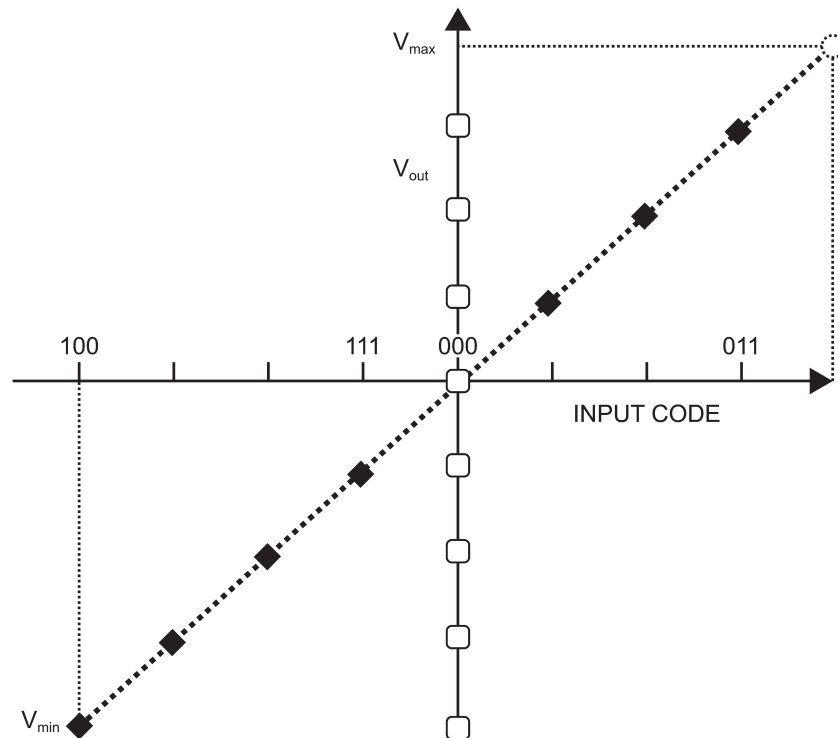


Figure 4—Elements of an ideal two's complement DAC transfer curve (bipolar)

DAC input architectures can be divided into parallel and serial. Parallel input converters receive parallel input codes that simultaneously control internal DAC switches that select a number of weights that are summed. Serial converters receive a serial input that is internally converted to a parallel word after a defined number of clocking cycles. The internal parallel word then functions in the same manner as a parallel input converter.

The general single-channel DAC architecture is shown in [Figure 5](#), which illustrates the main functional blocks that include the following:

- The digital pre-processing of the input data codes provided to the DAC at the input data rate f_{DATA} , which typically consists of one or more of the following procedures: filtering, pre-emphasis, interpolation, and re-sampling with higher resolution. Its output codes, which can have a different width N_{out} , are provided at the output update rate f_s . If no upsampling is applied, then $f_s = f_{DATA}$.
- The internal clock generation, which makes available a reference clock at f_s to be used for operating the internal D/A section.
- The internal D/A section, by which the stream of data codes at the output of the digital pre-processing is converted into an analog signal. This block marks the boundary between digital and analog domains.
- The analog post-processing, typically a low-pass filter. In some cases, a variable gain is also available. Its output is an analog signal that represents the output of the DAC.

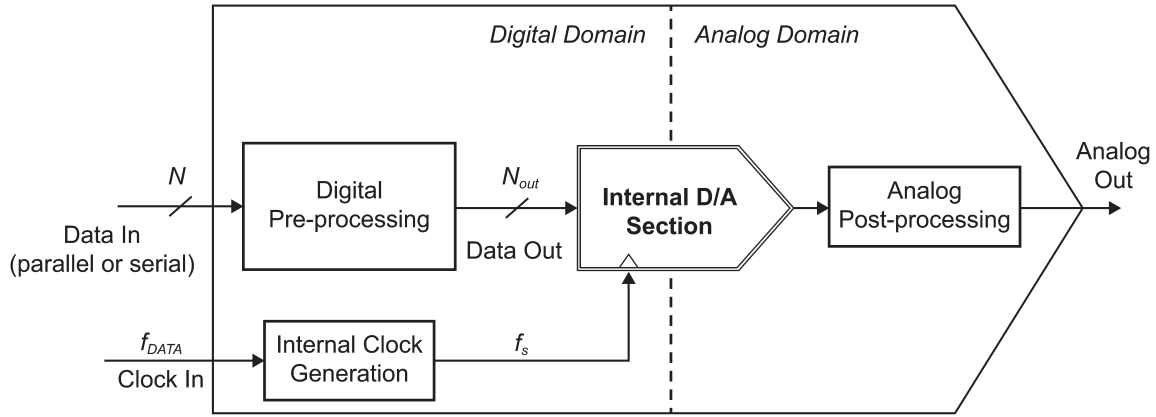


Figure 5—General architecture of a DAC (single channel, single D/A core)

From a circuital standpoint, the typical DAC consists of the following four major elements:

- The logic circuitry
- Some type of resistor or capacitor network
- A means of switching either a reference voltage or current to the proper input terminals of the network as a function of the digital value of each digital input bit
- A reference voltage or current

The following mathematical model is useful for discussing and analyzing the dynamic performance of a DAC. However, it should be kept in mind that this is an equivalent approximate mathematical model and does not necessarily reflect the physical operation of the DAC. This model constructs the output signal of the DAC by [Equation \(2\)](#):

$$V_{out}(t) = \left[\sum_{k=-\infty}^{\infty} w_k \delta(t - k\Delta t) \right] * f_R(t) = \sum_{k=-\infty}^{\infty} w_k f_R(t - k\Delta t) \quad (2)$$

where

w_k is the value of the word of width N_{out} at the input of the internal D/A section at time $k\Delta t$
 $\Delta t = 1/f_s$ is the time interval between words at the input of the internal D/A section
 $\delta(t)$ is the Dirac delta distribution

$f_R(t)$ is the impulse response of the reconstruction network implemented in the internal D/A section
* is the convolution operator

For the sake of simplicity, no analog post-processing is considered in the model of [Equation \(2\)](#).

For the special case of the zero-order-hold DAC, the impulse response is represented by [Equation \(3\)](#).

$$f_R(t) = f_{ZH}(t) = \begin{cases} 1 & \text{for } 0 \leq t < \Delta t \\ 0 & \text{otherwise} \end{cases} \quad (3)$$

A return-to-zero (RZ) DAC has an impulse response represented by [Equation \(4\)](#).

$$f_R(t) = f_{RZ}(t) = \begin{cases} a & \text{for } 0 \leq t < \tau \\ 0 & \text{otherwise} \end{cases} \quad (4)$$

where

$a > 1$ is a constant introduced to recover from gain losses
 τ is the duration of the output pulse from the internal D/A section, which is assumed to be less than Δt

The purpose for a return-to-zero DAC is to generate images of the applied sequence in higher Nyquist bands.

The zero-order-hold DAC is illustrated in [Figure 8](#), where a complex analog waveform is loaded into a DAC as a sequence of digital words. The DAC output is retained at its initial value until the next word is loaded.

An internal D/A section with a zero-order hold may be followed by an analog low-pass filter in order to make the reconstruction process more accurate by filtering out aliases of the applied sequence still arising above the first Nyquist band. In this case, the impulse response of the overall filtering procedure is the convolution of that of the analog filter and that of the zero-order hold in [Equation \(3\)](#).

In many cases it is desirable to consider the input word values, w_k , to be the sampled values of a function, $V_{in}(t)$, of continuous time. In that case, [Equation \(2\)](#) can be written as shown in [Equation \(5\)](#).

$$V_{out}(t) = \left[V_{in}(t) \sum_{k=-\infty}^{\infty} \delta(t - k\Delta t) \right] * f_R(t) \quad (5)$$

From this it follows that the Fourier transforms of the input and output signals are related by [Equation \(6\)](#).

$$\hat{V}_{out}(\omega) = \left[\hat{V}_{in}(\omega) \sum_{l=-\infty}^{\infty} \delta(\omega - l\omega_s) \right] \hat{f}_R(\omega) \quad (6)$$

where

ω_s is $2\pi f_s$
 $\hat{f}_R(\omega)$ is the Fourier transform of $f_R(t)$, i.e., the frequency response of the reconstruction network

The case study of $V_{in}(t) = \cos(\omega_{in} t)$, or $\hat{V}_{in}(\omega) = \frac{1}{2}(\delta(\omega - \omega_{in}) + \delta(\omega + \omega_{in}))$, is of particular interest. In this case, [Equation \(6\)](#) yields [Equation \(7\)](#).

$$\hat{V}_{out}(\omega) = \left[\frac{1}{2} \sum_{l=-\infty}^{\infty} (\delta(\omega - l\omega_s - \omega_{in}) + \delta(\omega - l\omega_s + \omega_{in})) \right] \hat{f}_R(\omega) \quad (7)$$

The frequencies $lf_s \pm f_{in}$, for $|l| \geq 1$, are called the image frequencies of f_{in} . Note that both positive and negative values of l and f_{in} are required to generate all of the image frequencies. In most cases it is desired for the reconstruction network to remove the image frequencies while retaining the input frequency. As the input frequency approaches one-half of f_s , the input frequency and the lowest image frequency become very close, placing stringent requirements on the reconstruction network.

The requirements on the reconstruction network and the analog filter are reduced with an interpolating DAC (also called an over-sampling DAC), whose internal D/A section operates at a rate f_s that is a multiple of the input data rate f_{DATA} . A block diagram of an interpolating DAC is shown in Figure 6, as a particular case of the general scheme of Figure 5 (only interpolation is addressed here; nonetheless, additional functionalities from Figure 5 can be found in an interpolating DAC, as well):

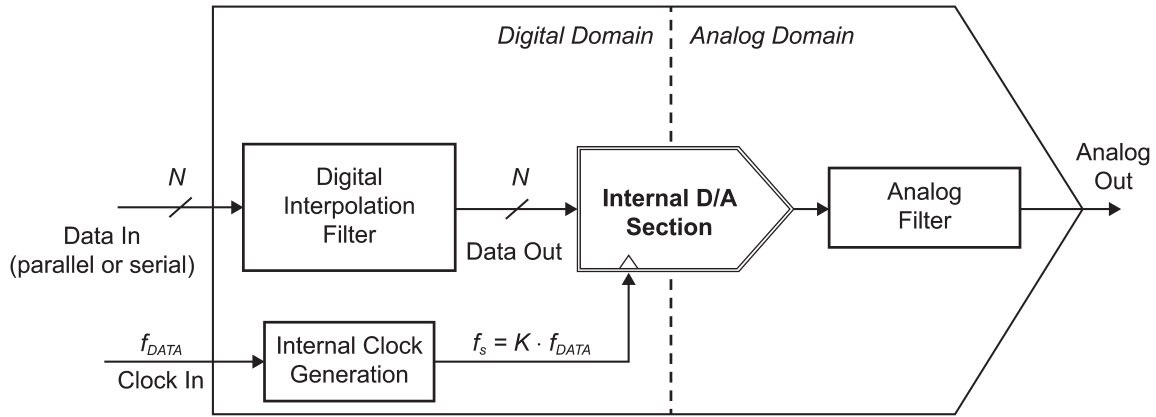


Figure 6—Block diagram for an interpolating DAC

The diagram in Figure 6 is a representation of a typical interpolating, or oversampling, DAC. If $K = 1$, then the DAC is a non-interpolating DAC, where the internal D/A section inputs are provided at a rate that coincides with the input data rate, i.e., $f_s \equiv f_{DATA}$. As in the case of Figure 5, when the term DAC is used without additional specification, it refers to the complete diagram, not to the internal D/A section. An interpolating DAC will usually have additional inputs to select parameters such as the oversampling factor K and the interpolation filter characteristics.

The interpolation filter is a digital block that converts the input word stream into a higher-rate digital time series that relaxes the design requirements of the reconstruction network and the analog filter.

The interpolation filter has an impulse response of the form shown in Equation (8).

$$f_i[n] = \sum_{k=-\infty}^{\infty} a_k \delta_{n, \frac{k}{K}} \quad (8)$$

where

- δ_{ij} is the Kronecker delta operator
- a_k is the parameters used to design the filter, which provide a frequency response that is periodic in frequency with period $f_s = K f_{DATA}$

In some sources it is stated that the image frequencies for an interpolating DAC are separated by f_s rather than by f_{DATA} , but this is incorrect. The interpolation filter block preserves digital image frequencies arising

from discrete-time operation at the same locations as those for a non-interpolating DAC with the same input data rate. However, the interpolation digital filter can be designed to reduce more effectively these image frequencies. Instead, it is true that the interpolation procedure gives rise to *additional* image frequencies around $\pm lf_s$, but these, too, can be even more effectively mitigated by the reconstruction network and the analog filter that follows in Figure 6.

This process can be better understood with frequency domain and time domain plots. Consider a PCM audio DAC with an input data rate of 44.1 kHz. The “Data in” data stream is set to generate 10 tones starting at 2 kHz and ending at 20 kHz. The desired spectrum of the waveform encoded by the “Data in” sequence is shown in Figure 7.

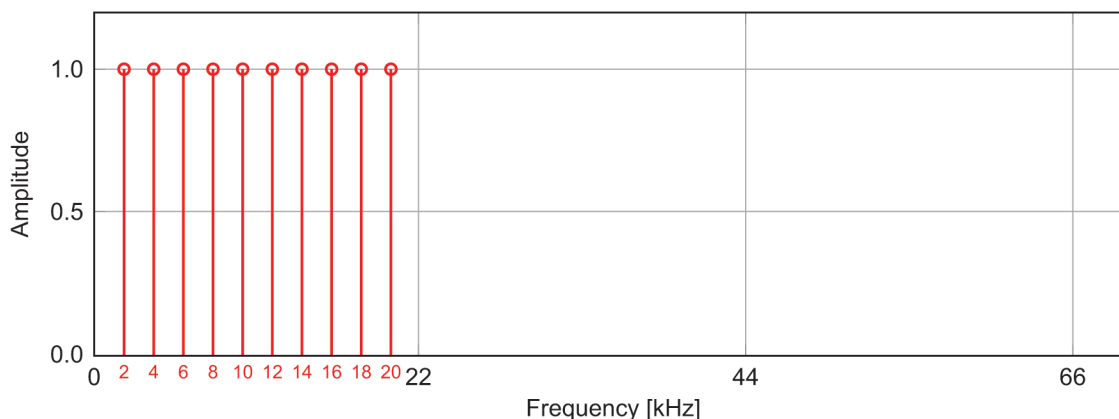


Figure 7—Spectrum of 10 tones of an audio signal that is applied to the DAC with an input data rate of 44.1 kHz shown in Figure 5 (normalized units)

If the factor K is set to 1, the zero-order-hold internal D/A section output will resemble the waveform shown in Figure 8 that is identified as “Unfiltered D/A section Output.” The desired output is also shown (without the time delay that is associated with the filtering process).

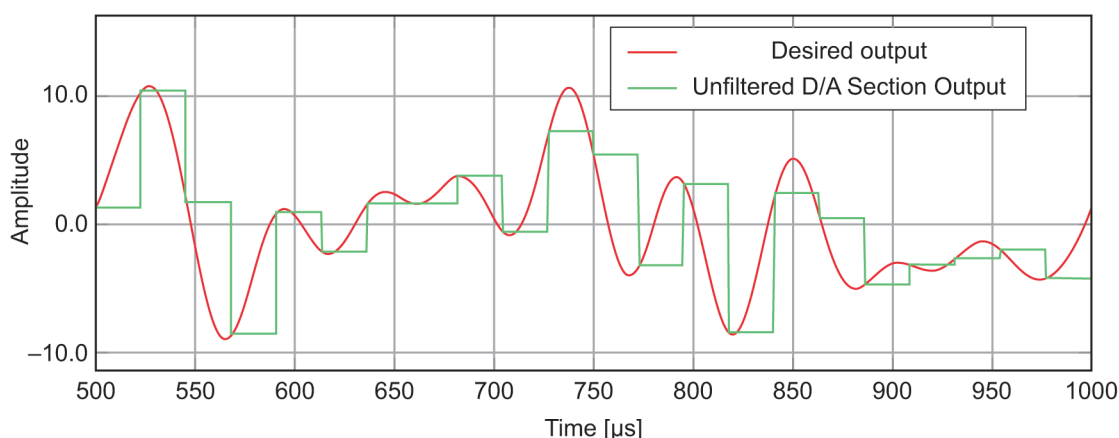


Figure 8—Plots of desired continuous signal and unfiltered D/A section output when $K = 1$ (exclusive of time delays) for the circuit shown in Figure 5

The spectrum of the analog waveform observed at the input of the analog filter will resemble that shown in Figure 9.

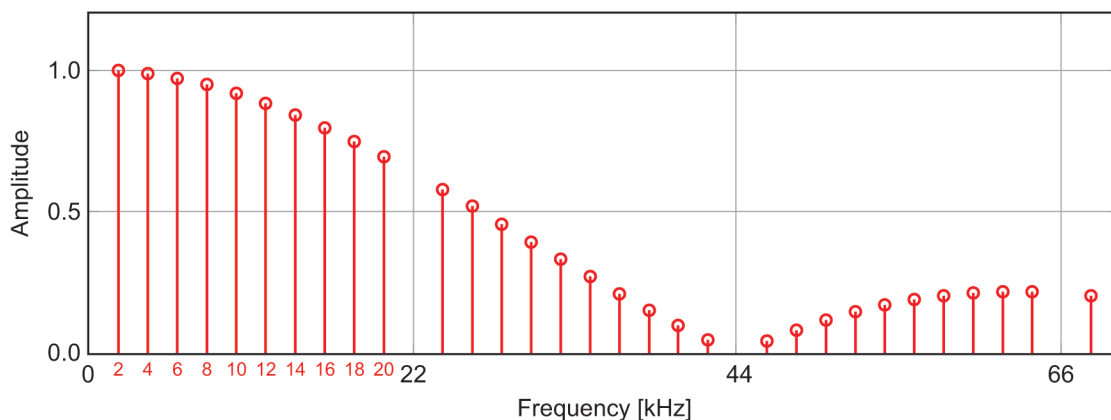


Figure 9—Spectrum of signal at the input to the analog filter for the circuit shown in Figure 5 when $K = 1$

The ideal analog output should have the same spectrum as that shown in Figure 7. In order to accomplish this, the analog filter should attenuate the unwanted image frequencies appropriately. It is very difficult to design an analog filter which will perform to the standards demanded by PCM audio users since the filter should implement (i) a precise post-emphasis to make the spectrum flat again in band and (ii) a sharp roll-off around 22 kHz.

For $K > 1$, a digital interpolation filter is used. It consists of an upsampling and a digital lowpass filter. If $K = 16$, the upsampling consists of adding $K-1 = 15$ zeros between each couple of adjacent samples. The digital lowpass filter should preserve the signal bandwidth and attenuate the image frequencies. The magnitude of the frequency response of a lowpass filter that can be used for this purpose is shown in Figure 10.

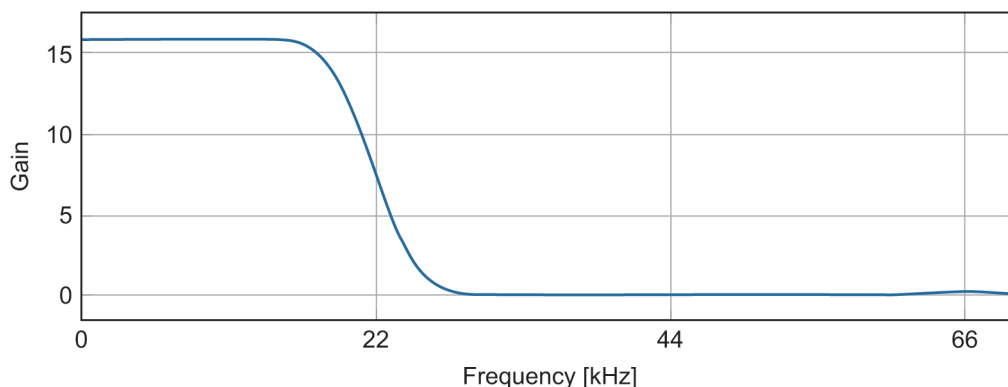


Figure 10—Magnitude of the frequency response of the lowpass digital filter for an interpolation of $K = 16$

The signal resulting from the interpolation is represented by the green line shown in Figure 11.

The time delays that are inherent in the reconstruction process are removed to clarify the description. It can be seen that the interpolated D/A section output is much closer to the desired output than that without interpolation (Figure 8).

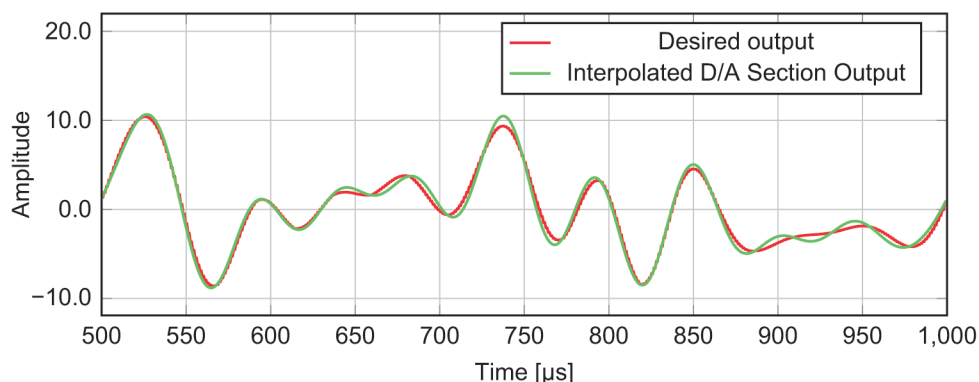


Figure 11—Plot of time domain signal for $K = 16$, and the desired output signal for the circuit shown in Figure 5 (time delays removed for clarity)

The spectrum of the signal generated downstream of the interpolation filter is shown in Figure 12. Note that $K = 16$ implies that the DAC update rate, f_s , is 16 times the input data rate of ~ 44.1 kHz or ~ 705.6 kHz. In the practice of DACs for high-performance audio applications K is not an integer, but it is slightly higher than 16, so that the update rate is 768 kHz.

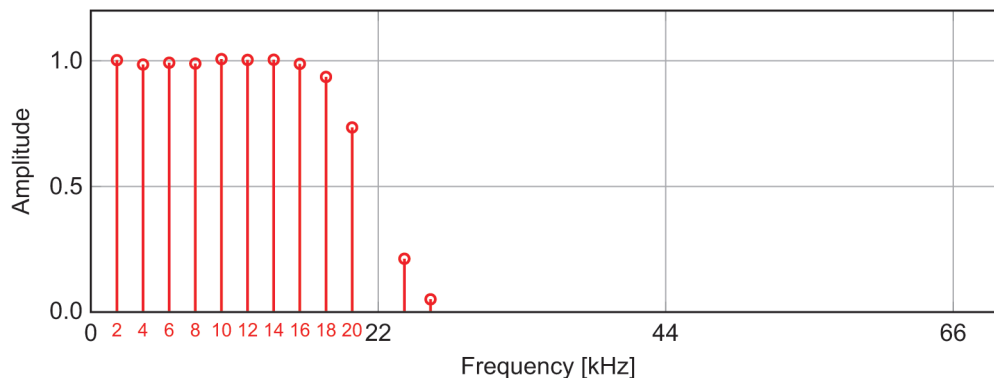


Figure 12—Spectrum of signal after the interpolation filter for the circuit shown in Figure 5

It can be observed that with the interpolation, the spectrum is flatter than without interpolation and that the image components are attenuated. However, due to the distortion of the filter, the spectrum may not be reasonably flat and some images can be still present. The analog filter can then be used to further remove the image components.

1.7 Guidance to the user

1.7.1 Interfacing

DACs present unique interfacing challenges, and without careful attention users can experience substandard results. As with all mixed-signal devices, DACs perform as expected only when the analog and digital domains

are brought together in a well-controlled fashion. The user should fully understand the manufacturer's recommendations with regard to proper signal buffering and loading, input signal connections, transmission line matching, circuit layout patterns, power supply decoupling, reference decoupling, and operating conditions. Edge characteristics for load-data pulse(s) and clock(s) should be carefully chosen to ensure that input signal purity is maintained with sufficient margin up to the digital input pin(s). Most manufacturers now provide excellent DAC evaluation boards, which demonstrate recommended layout techniques, signal conditioning, and interfacing for their DACs. If the characteristics of a new DAC are not well understood, then these boards should be analyzed or used before starting a new layout.

1.7.2 Coding

Some commonly used input data formats for digital-to-analog conversion are described in the paragraphs that follow.

Binary codes are most familiar in representing integers. In a natural binary integer code having N bits, the least significant bit (LSB) has a weight of 2^0 , the next bit has a weight of 2^1 , and so on up to the most significant bit (MSB), which has a weight of 2^{N-1} . The value of a binary number is obtained by adding up the weights of all nonzero bits. When the weighted bits are added up, they form a unique number having any value from zero to $2^N - 1$. Each additional trailing zero bit, if present, essentially doubles the size of the number.

In converter technology, because full scale is independent of the number of bits resolution, a more useful coding is fractional binary, which is always normalized to full scale. Integer binary can be interpreted as fractional binary if all integer values are divided by 2^N . The MSB has a weight of $1/2$, the next bit has a weight of $1/4$, and so forth down to the LSB, which has a weight of $1/2^N$. When the weighted bits are added up, they form a number with any of 2^N values, from zero to $(1 - 2^{-N})$, of the full scale.

With BCD, each decimal digit is represented by a group of four binary-coded digits (or “quad”).

In fractional BCD, the LSB of the most significant quad has a weight of 0.1, the LSB of the next has a weight of 0.01, the LSB of the next has a weight of 0.001, and so on. Each quad has 10 permissible levels with weights zero to nine. Group values in excess of nine are not permitted.

In Gray code, each bit represents a binary-weighted segment of the range and each code corresponds to a unique location in the range; but the bit weights do not readily combine to form a binary magnitude. In Gray code, as the number value changes, the transitions from one code to the adjacent code involve transitions of only one bit.

In complementary codes, all bits are represented by their complements. Complementary binary (or inverted binary) is the negative true binary system. It is identical to the binary code except that all binary bits are inverted. Thus, zero scale is all ones while full scale is all zeros. Complementary BCD, for each quad of a BCD coded converter, is the code obtained by representing all bits by their complements. In complementary BCD, zero is represented by 1111, and nine is represented by 0110.

For bipolar DACs, the most often used binary codes are as follows:

- Two's complement
- Sign-magnitude
- Offset binary
- One's complement

Two's complement code consists of a binary code for positive magnitudes (zero sign bit) and the two's complement of each positive number to represent its negative. The two's complement is formed arithmetically by complementing the code for the positive number and adding one.

One's complement code consists of a binary code for positive magnitudes (zero sign bit) and the one's complement of each positive number to represent its negative. The one's complement code for negative numbers is formed arithmetically by complementing the code for the positive number.

A sign-magnitude code determines the code appropriate for the magnitude of signed analog quantities and adds a polarity bit. The polarity bit can be either zero or one for positive values. Table 1 assumes a one for positive values.

In offset binary code, the weights are given by Equation (9).

$$w_m = 2^{m-1} \quad (9)$$

where

$$\begin{aligned} m & \text{ is } 1 \\ N & \text{ is } -1 \\ w_N & \text{ is } 2^{N-1} \end{aligned}$$

The offset binary code is widely used.

Note that the +FS output is represented by a virtual code that is 1 LSB greater than the maximum number that can be applied to the DAC. A similar phenomenon occurs at the −FS values for one's complement and sign-magnitude coding.

The parameter k represents the index of the input code. The total number of actual physical codes is 2^N for all the tabulated coding methods.

Table 1—Bipolar DAC input codes

Scale	k	Offset binary (and binary)	Two's complement	One's complement	Sign magnitude
+Full scale	2^N	—...—	—...—	—...—	—...—
+Full scale-1 LSB	2^N-1	1111...1111	0111...1111	0111...1111	1111...1111
+0.75 Full scale		1110...0000	0110...0000	0110...0000	1110...0000
+0.5 Full scale		1100...0000	0100...0000	0100...0000	1100...0000
+0.25 Full scale		1010...0000	0010...0000	0010...0000	1010...0000
+1 LSB		1000...0001	0000...0001	0000...0001	1000...0001
+0		1000...0000	0000...0000	0000...0000	1000...0000
−0		—...—	—...—	1111...1111	0000...0000
−1 LSB		0111...1111	1111...1111	1111...1110	0000...0001
−0.25 Full scale		0110...0000	1110...0000	1101...1111	0010...0000
−0.5 Full scale	2^{N-2}	0100...0000	1100...0000	1011...1111	0100...0000
−0.75 Full scale		0010...0000	1010...0000	1001...1111	0110...0000
−Full scale+ 1 LSB	1	0000...0001	1000...0001	1000...0000	0111...1111
−Full scale	0	0000...0000	1000...0000	—...—	—...—

1.7.2.1 Adjustment range

Many converter types require no adjustment as purchased to meet specified accuracy. However, there are cases where (i) adjustments are called for in the specifications, (ii) cost-savings can be affected by trimming inexpensive devices, with modest specs, for use over narrow ranges for better than specified accuracy, or (iii) long-term corrections are necessary after long periods of operation.

The adjustment range is defined by many DAC manufacturers, as the range that a recommended adjustment mechanism can be used to change the full scale range and the offset of a DAC. The adjustment mechanism can be used to correct for the gain and offset deviations from the nominal, or to compensate for other gain and offset errors in the system, or it can be used to change slightly the range of a DAC. A typical case of such a change would involve converting a ± 5 -V DAC to a ± 5.12 -V DAC. Adjustment of a DAC beyond the specified adjustment range may compromise the linearity and stability obtainable from the DAC.

The adjustment can be implemented through many mechanisms, including the following:

- a) Internal registers and DACs that can be programmed to adjust the gain and the offset.
- b) Nodes that can be connected to potentiometers to adjust the gain and the offset. The use of potentiometers is generally not recommended since the reliability of a potentiometer setting is reduced when many adjustments of parameters are made near the same region of a potentiometer setting.
- c) A node that can be connected to an external DAC to perform the functions described in mechanism a).

Proper adjustment of zero and full scale output in DACs is a procedure that requires great care and high-quality instruments. The meter used to read the output of a DAC shall have enough resolution so that the test instrument does not limit the adjustment value at both ends of the range of the converter, (at zero and full scale or minus full scale and plus full scale).

Bipolar converters require knowledge of the DAC architecture to be properly adjusted. Some adjustment mechanisms will adjust the offset at the negative full scale of the converter without affecting the range. Other adjustment mechanisms will have interaction between the gain and the offset adjustments.

Many bipolar binary converters that use offset binary or two's complement coding employ analog offsetting to convert a unipolar design into bipolar. For example, a zero to +10 V DAC may have its output amplifier offset by -5 V, resulting in an output of -5 V corresponding to 00...0 input and +5 V (minus 1 LSB) corresponding to a 11...1 input. Such a converter should have its "zero" adjusted at -5 V (100...0 in two's complement).

The specific instructions published in product datasheets should be followed.

It is not simple to calibrate a DAC based on the best-fit-straight-line algorithm. The best-fit approach is usually used to determine the worst-case INL error, where gains and offsets are not a factor. It is recommended that the adjustment of gain and offset be done at two specific codes in the range of the DAC. Typically, these codes correspond to minus Full Scale ($-FS$) and plus Full Scale-1 LSB ($+FS-1$ LSB). In some applications, the two points may be 20% of the FSR and 80% of the FSR.

1.7.3 Test conditions

DAC test specifications can be split into two groups: test conditions and test results. Typical examples of the former are temperature, power supply voltages, clock frequency, and reference voltages. Examples of the latter are power dissipation, effective number of bits, spurious free dynamic range (SFDR), and integral nonlinearity (INL). The test methods defined in this standard describe the measurement of test results for given test conditions.

DAC specification sheets will often give allowed ranges for some test conditions (e.g., power supply ranges). This implies that the DAC will function properly and that the test results will fall within their specified ranges for all test conditions within their specified ranges.

Since the test condition ranges are generally specified in continuous intervals, they describe an infinite number of possible test conditions, which obviously cannot be exhaustively tested. It is up to the manufacturer or tester of a DAC to determine from design knowledge and/or testing the effect of the test conditions on the test result, and from there to determine the appropriate set of test conditions needed to accurately characterize the range of test results. For example, knowledge of the design may be sufficient to know that the highest power dissipation (test result) will occur at the highest power supply voltage (test condition), so the power dissipation test need be run only at the high end of the supply voltage range to check that the dissipation is within the maximum of its specified range. It is very important that relevant test conditions be stated when presenting test results.

1.7.4 Test equipment

It shall be ensured that the performance of the test equipment used for these tests significantly exceeds the desired performance of the DAC under evaluation. Additional signal conditioning in the form of filters and pulse shapers may need to be included. Accessories such as terminators, attenuators, delay lines, and other such devices are usually needed to match signal levels and to provide signal isolation to avoid corrupting the output signal.

Quality testing requires following established procedures, most notably those specified in standard ISO 17025. In particular, traceability of instrumental calibration to a known standard is important. Commonly used test setups are described in 4.2.

1.7.5 Test selection

When choosing which parameters to measure, one should follow the outline and hints in this clause to develop a procedure that logically and efficiently performs all needed tests on each unique setup. The standard has been designed to facilitate the development of these test procedures. For example, most users require that the DAC meets or exceeds a minimum SINAD limit for their application and that the nonlinearity of the DAC be specified. Certainly, the extent to which this standard is applied will depend upon the application; hence, the procedure should be tailored for each unique characterization plan.

1.8 Manufacturer supplied information

1.8.1 General information

Manufacturers shall supply the following general information:

- a) Device part number
- b) Physical characteristics: dimensions, packaging, pin outs
- c) Power requirements
- d) Environmental conditions: safe operating, non-operating, and specified performance temperature range; altitude limitations; humidity limits, operating and storage temperature ranges; vibration tolerance; and compliance with applicable electromagnetic interference specifications
- e) Any special or peculiar characteristics
- f) Compliance with other specifications
- g) Control signal characteristics
- h) Output signal characteristics

- i) Pipeline delay (if any)
- j) Exceptions to the above parameters where applicable

1.8.2 Minimum specifications

The manufacturer shall provide the following specifications. See appropriate clauses for definitions.

- a) Number of bits N_{out}
- b) Input data rates and widths
- c) Analog bandwidth (minimum, maximum, typical)
- d) Output signal full-scale range with nominal reference signal levels
- e) Output impedance
- f) Output mode (current or voltage, differential or single-ended)
- g) Reference signal levels to be applied (minimum, maximum, typical)
- h) Supply voltages (minimum, maximum, typical)
- i) Supply currents (minimum, maximum, typical)
- j) Power dissipation (minimum, maximum, typical)
- k) Logic levels at digital inputs
- l) Number of channels

1.8.3 Additional specifications

- a) Gain error (minimum, maximum, typical)
- b) Offset error (minimum, maximum, typical)
- c) Differential nonlinearity (DNL) (minimum, maximum, typical)
- d) Harmonic distortion and spurious response (minimum, maximum, typical)
- e) Integral nonlinearity (INL) (minimum, maximum, typical)
- f) Unadjusted static error (minimum, maximum, typical)
- g) Signal-to-noise ratio (minimum, typical)
- h) Signal-to-noise and distortion ratio (SINAD) (minimum, typical)
- i) Total harmonic distortion (THD) (maximum, typical)
- j) Total harmonic distortion plus noise (THD+N) (maximum, typical)
- k) Spurious free dynamic range (SFDR) (minimum, typical)
- l) Effective number of bits (minimum, typical)
- m) Wideband effective number of bits (minimum, typical)
- n) Random noise and associated measurement bandwidth (maximum, typical)
- o) Frequency response
- p) Settling time (maximum, typical)

- q) Transition duration of step response (maximum, typical)
- r) Slew rate limit (minimum, maximum, typical)
- s) Timing uncertainty (short-term instability)
- t) Crosstalk (channel-to-channel, input-to-output, etc.)
- u) Monotonicity
- v) Intermodulation distortion (maximum, typical)
- w) Noise power ratio (minimum, typical)

1.8.4 Critical DAC parameters

Table 2 is presented as a guide for a few common DAC applications. The wide range of DAC applications makes a comprehensive listing impossible. This table is intended to be a helpful starting point for users to apply this standard to their particular applications.

Table 2—Critical DAC parameters

Typical applications	Critical DAC parameters	Performance issues
Audio	SNR, THD, SINAD (THD+N)	Audio quality
Video/RAMDAC	GE, DNL, INL, DG, DP, OV, SFDR, TR, CM, ST	Picture quality
Control	DNL, T_s , GE	DNL monotonicity is often critical
Communications	IMD, MTPR, ACLR	Communications quality of service

ACLR—adjacent channel leakage power ratio
 CM—channel matching
 DNL—differential nonlinearity
 ENOB—effective number of bits
 GE—gain error
 IMD—intermodulation distortion
 INL—integral nonlinearity
 OV—output voltage compliance range
 MTPR—Missing Tone Power Ratio
 SINAD—signal-to-noise and distortion ratio
 SFDR—spurious free dynamic range
 SNR—signal-to-noise ratio
 T_s —settling time
 THD—total harmonic distortion
 THD+N—THD plus noise
 TR—transient response

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they shall be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1057™, IEEE Standard for Digitizing Waveform Recorders.^{9,10}

IEEE Std 1241™, IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters.

⁹IEEE publications are available from The Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, Piscataway, NJ 08854, USA (<https://standards.ieee.org/>).

¹⁰The IEEE standards or products referred to in this clause are trademarks of The Institute of Electrical and Electronics Engineers, Inc.

IEEE Std 181™, IEEE Standard for Transition, Pulses, and Related Waveforms.

ISO 17025, General requirements for the competence of testing and calibration laboratories.¹¹

MIL Std 810F, Environmental Engineering Considerations and Laboratory Tests.¹²

3. Definitions, symbols, acronyms, and abbreviations

3.1 Definitions

For the purposes of this document, the following terms and definitions apply. The *IEEE Standards Dictionary Online* should be consulted for terms not defined in this clause.¹³

NOTE—The linearity specifications to follow (gain, offset, INL, DNL) depend on which transfer curve is used as a reference. One can have either “end-point” linearity or “best-fit” linearity. The first takes as reference curve a straight line between the minimum and maximum measured points. The second uses as reference a best-fit regression line through all measured points. Since “best-fit” linearity seems to be the most widely used, that definition is used as the standard. The main advantage of “best-fit” linearity is that it reduces the linearity error (INL) and thus in general will result in higher parametric yield. End-point linearity is relevant when post-processing does not allow a linear regression.¹⁴

absolute worst-case (total) error: For a device that uses an internal reference, or a specified external reference, the absolute value of the worst-case difference between the actual output value and the nominal output value for any input code, without gain, and offset correction (see Figure 13).

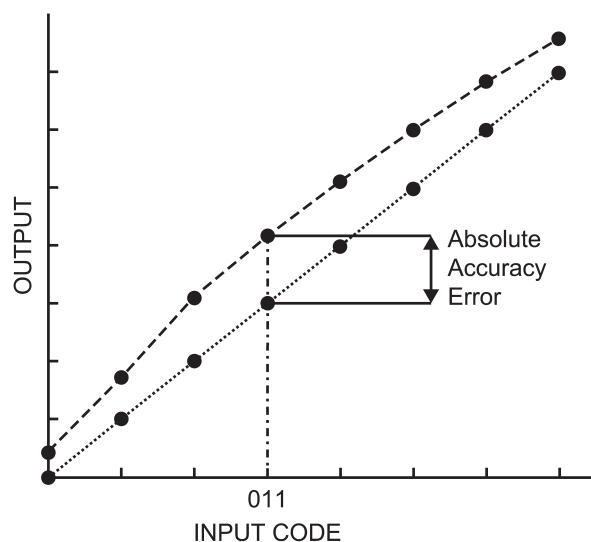


Figure 13—Absolute worst-case error of a DAC

¹¹ISO publications are available from the ISO Central Secretariat, 1, ch. de la Voie-Creuse, Case postale 56, CH-1211 Geneva 20, Switzerland (<http://www.iso.ch/>). ISO publications are also available in the United States from the Sales Department, American National Standards Institute, 25 West 43rd Street, 4th Floor, New York, NY 10036, USA (<https://www.ansi.org/>).

¹²MIL publications are available from Customer Service, Defense Printing Service, 700 Robbins Ave., Bldg. 4D, Philadelphia, PA 19111-5094.

¹³*IEEE Standards Dictionary Online* is available at: <http://dictionary.ieee.org>. An IEEE account is required for access to the dictionary, and one can be created at no charge on the dictionary sign-in page.

¹⁴Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

adjacent channel leakage ratio (ACLR): A ratio in dB between the measured power within a frequency channel relative to adjacent frequency channels.

bandwidth: The frequency at which the magnitude of the Fourier transform of the digital-to-analog converter's (DAC's) impulse response computed from the time derivative of its full-scale step response, is attenuated by $1/\sqrt{2}$ from its dc value. This definition of bandwidth is sample-rate independent and does not account for the $\sin(\pi fT)/(\pi fT)$ response arising from zero-order-hold waveform reconstruction.

channel matching (when applicable): Specifies the degree of matching between two or more digital-to-analog converters (DACs) in a single package.

clock and data feedthrough: Specifies the amount of energy in the digital-to-analog converter (DAC) output originating from clock and/or data signals respectively.

clock jitter: The standard deviation of variation in time of the active edge of a clock signal.

clock pulse width (latch pulse width): The minimum amount of time that the clock pulse should be left in the logic "1" state to achieve rated performance.

clock signal duty cycle: The fraction of the time the clock signal spends in excess of the logic threshold.

clock signal slew rate: The time derivative of the clock signal at the point where it crosses the logic threshold.

code bin (k): A digital input that corresponds to a particular nominal analog output value.

crosstalk: Undesired energy appearing in a digital-to-analog converter (DAC) channel as a result of coupling with another DAC channel in the same package.

cumulative distribution function (cdf): The integral of the probability density function defined in the definition for **output propagation delay**. This function is positive and monotonic.

differential nonlinearity (DNL): The differences between the output at adjacent input codes, divided by the measured average step width of the digital-to-analog converter (DAC) under test minus 1.

differential-output impedance: For a differential-mode output digital-to-analog converter (DAC), the impedance between the positive output and the negative output.

digital feedthrough: This is the glitch transferred to the output of a digital-to-analog converter (DAC) channel in response to a change in an input. It includes data feedthrough and clock feedthrough.

digital-to-analog converter (DAC): A converter that translates a digital input into an analog output.

dynamic range: *See: spurious free dynamic range (SFDR).*

effective number of bits (ENOB): A measure of the signal-to-noise-and-distortion ratio used to compare actual digital-to-analog converter (DAC) performance to the expected performance of an ideal DAC.

full-scale (FS) errors: The difference between the actual digital-to-analog converter (DAC) output and the expected nominal output when a digital code is applied, which should generate the maximum and the minimum outputs. Unlike gain error, offset error is included in the FS error measurement.

full-scale range (FSR): The difference between the most positive and most negative analog outputs of a converter's operating range. Generally, FSR includes the virtual codes at the minimum and the maximum outputs. Thus, a -10 V to $+10\text{ V}$ digital-to-analog converter (DAC) will have FSR equal to 20 V .

gain and offset: Gain and offset are the values by which the ideal output values are multiplied and then to which the ideal output values are added, respectively, to cause the output values to satisfy specified conditions. Two conditions are commonly used: “independently based” where the sum of the squared deviations from the ideal output values is minimized, and “terminal-based” where the ideal outputs are matched at the first and the last code.

gain matching: In a multichannel converter, the difference between the largest gain and the smallest gain, expressed in % FSR or dB.

glitch: A transient that leaves an initial state, enters the boundaries of another state for a duration less than the duration for state occurrence, and then returns to the initial state.

glitch area (GA): The time integral of the analog value of the glitch transient.

glitch energy (GE): The time integral of the electrical power of the glitch transient.

harmonic: A frequency that is an integer multiple of the fundamental.

harmonic distortion: For an assumed sine-wave signal, the amplitudes of the components at frequencies that are multiples of the signal frequency by integers greater than one.

hold time (t_H): The amount of time required for the digital inputs to remain deterministic after a trigger clock edge.

ideal code bin width (Q): The ideal full-scale output range (FSR) divided by the total number of codes.

impulse: A time signal that approximates a Dirac delta distribution.

impulse DAC: An idealized digital-to-analog converter (DAC) for which the output is a sequence of impulses proportional to the input word at the update rate.

impulse response: Response of a linear network to an impulse applied at the input.

input data rate (f_{DATA}): The rate at which input words are supplied to the digital-to-analog converter (DAC).

integral nonlinearity at code bin (k) (INL(k)): The difference between the ideal and actual analog output value corresponding to the code bin (k) after correcting for gain and offset.

integral nonlinearity (INL): The maximum difference between the ideal and actual analog output values after correcting for gain and offset.

intermodulation distortion (IMD): The ratio of amplitude of the intermodulation product with the largest amplitude to the largest amplitude generated test tone.

interpolation filter: The filter in an interpolating digital-to-analog converter (DAC) that converts the digital data at the input data rate to digital data at the update rate.

interpolation ratio: The ratio of the update rate to the input data rate in an interpolating digital-to-analog converter (DAC).

jitter: The deviation of a sequence of reference instants from their ideal values.

least significant bit (LSB): Synonymous with one ideal code bin width (Q), which corresponds to the digital input bit in a data converter code that has the smallest mathematical weight.