

Conformance Test Methodology for
IEEE Standards for Local and Metropolitan Area Networks:

**Supplement to Carrier Sense Multiple Access with
Collision Detection (CSMA/CD) Access Method and
Physical Layer Specifications:**

**Type 10BASE-T Medium Attachment Unit (MAU)
Conformance Test Methodology (Section 6)**

*Includes related changes to ISO/IEC 8802-3 : 1993
[ANSI/IEEE Std 802.3, 1993 Edition]*

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Abstract: Methods for conformance testing to satisfy requirements arising from the ISO/IEC 8802-3 [ANSI/IEEE Std 802.3] standard are defined. The conformance test suite is intended to detect incorrect implementations of the ISO/IEC 8802-3 standard, clause 14. It comprises two categories of test groups. The first category relates to basic interconnection testing and the second to capability and behavior testing. The test setups, adapters, and instruments used are described.

Keywords: abstract test suite, carrier sense multiple access with collision detection (CSMA/CD), compliance, conformance testing, 10BASE-T, local area networks, medium attachment unit (MAU), unshielded twisted pair (UTP)

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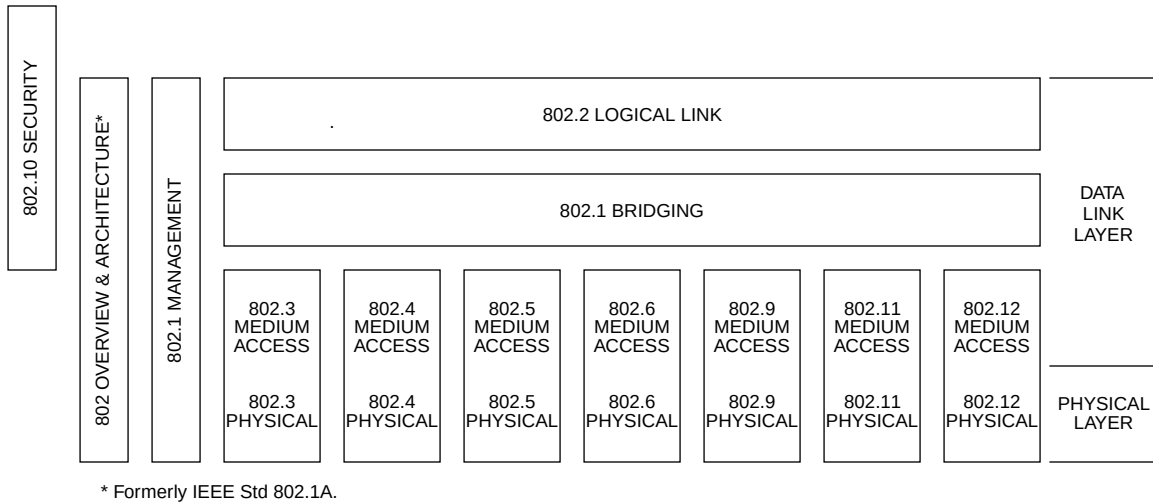
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Foreword

(This foreword is not a part of IEEE Std 1802.3d-1993.)

This standard is part of a family of standards for local and metropolitan area networks. The relationship between the standard and other members of the family is shown below. (The numbers in the figure refer to IEEE standard numbers.)



This family of standards deals with the Physical and Data Link layers as defined by the International Organization for Standardization (ISO) Open Systems Interconnection Basic Reference Model (ISO 7498 : 1984). The access standards define several types of medium access technologies and associated physical media, each appropriate for particular applications or system objectives. Other types are under investigation.

The standards defining these technologies are as follows:

- IEEE Std 802[†]: Overview and Architecture. This standard provides an overview to the family of IEEE 802 Standards. This document forms part of the 802.1 scope of work.
- ISO/IEC DIS 15802-2
[IEEE Std 802.1B and 802.1k]: LAN/MAN Management. Defines an Open Systems Interconnection (OSI) management-compatible architecture, and services and protocol elements for use in a LAN/MAN environment for performing remote management.
- ISO/IEC 10038
[ANSI/IEEE Std 802.1D]: MAC Bridging. Specifies an architecture and protocol for the interconnection of IEEE 802 LANs below the MAC service boundary.

[†]The 802 Architecture and Overview Specification, originally known as IEEE Std 802.1A, has been renumbered as IEEE Std 802. This has been done to accommodate recognition of the base standard in a family of standards. References to IEEE Std 802.1A should be considered as references to IEEE Std 802.

- ISO/IEC 15802-4[‡]
[IEEE Std 802.1E]: System Load Protocol. Specifies a set of services and protocol for those aspects of management concerned with the loading of systems on IEEE 802 LANs.
- ISO 8802-2 [ANSI/IEEE Std 802.2]: Logical Link Control
- ISO/IEC 8802-3 [ANSI/IEEE Std 802.3]: CSMA/CD Access Method and Physical Layer Specifications
- ISO/IEC 8802-4 [ANSI/IEEE Std 802.4]: Token Bus Access Method and Physical Layer Specifications
- ISO/IEC 8802-5 [ANSI/IEEE Std 802.5]: Token Ring Access Method and Physical Layer Specifications
- ISO/IEC 8802-6 [ANSI/IEEE Std 802.6]: Distributed Queue Dual Bus Access Method and Physical Layer Specifications
- IEEE Std 802.10: Interoperable LAN/MAN Security, *Currently Contains* Secure Data Exchange (SDE)

In addition to the family of standards, the following is a recommended practice for a common technology:

- IEEE Std 802.7: IEEE Recommended Practice for Broadband Local Area Networks

The following additional working groups have authorized standards projects under development:

- IEEE 802.9 Integrated Services (IS) LAN Interface at the Medium Access Control (MAC) and Physical Layers
- IEEE 802.11 Wireless LAN Medium Access Control (MAC) and Physical Layer Specifications
- IEEE 802.12 Demand Priority Access Method and Physical Layer Specifications

Conformance Test Methodology

An additional standards series, identified by the number 1802, has been established to identify the conformance test methodology documents for the 802 family of standards. This makes the correspondence between the various 802 standards and their applicable conformance test requirements readily apparent. Thus the conformance test documents for 802.3 are numbered 1802.3, the conformance test documents for 802.5 will be 1802.5, and so on.

IEEE Std 1802.3d-1993

This standard is a supplement to IEEE Std 1802.3-1991, which defines methods for conformance testing to satisfy requirements arising from ISO/IEC 8802-3 : 1993 [ANSI/IEEE Std 802.3, 1993 Edition]. At the time this standard was approved, the complete IEEE 802.3 family of standards consisted of the following published documents:

[‡]Available May 1994.

- ISO/IEC 8802-3 : 1993 [ANSI/IEEE Std 802.3, 1993 Edition]
- IEEE Std 802.3k-1992, Layer Management for 10 Mb/s Baseband Repeaters (Section 19)
- IEEE Std 802.3l-1992, Type 10BASE-T Medium Attachment Unit (MAU) Protocol Implementation Conformance Statement (PICS) Proforma (Section 14.10)
- IEEE Std 802.3q-1993, Guidelines for the Development of Managed Objects (GDMO) (ISO 10164-4) Format for Layer-Managed Objects (Section 5) and IEEE Std 802.3p-1993, Layer Management for 10 Mb/s Baseband Medium Attachment Units (MAUs) (Section 20)
- IEEE Std 1802.3-1991, Conformance Test Methodology for CSMA/CD Access Method and Physical Layer Specifications: Attachment Unit Interface (AUI) Cable (Section 4)

Information on the current revision state of this and other IEEE 802 standards may be obtained from

Secretary, IEEE Standards Board
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IEEE 802 committee working documents are available from

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Changes/Revisions to ISO/IEC 8802-3 : 1993 [ANSI/IEEE Std 802.3, 1993 Edition]

Change the second paragraph and the numbered list in 7.4.1.1 as follows:

The differential output voltage, V_{dm} , is alternately positive and negative in magnitude with respect to zero voltage. The value of V_{dm} into either of the two test loads identified above ($R = 73\ \Omega$ or $83\ \Omega \pm 1\%$) at the interface connector of the driving unit shall satisfy conditions defined by values V_1 , V_2 , and V_3 , V_{min} and V_{max} shown in Fig 7-11 for signals in between BR and BR/2 meeting the frequency and duty cycle tolerances specified for the signal being driven. The procedure for measuring and applying the test condition is as follows:

- (1) Construct a template representing the shaded area of Fig 7-11. Once constructed, the template may be shifted along the time axis in order to accommodate differences in the 10% to 50% and 50% to 90% transition times of the driver waveform.
- (2) Find the peak value of V_{dm} . This is V_{max} .
- (3) Find the minimum value of V_{dm} during the period between the shaded regions for the waveform's rising and falling transitions (time T1 in Fig 7-11). This minimum value is V_{min} .
- (4) V_{max} shall be $< 1315\text{ mV}$, V_{min} shall be $> 450\text{ mV}$, and V_{max}/V_{min} shall be < 1.37 .
- (5) V_{dm} shall remain $< 1170\text{ mV}$ 24 ns after a zero crossing.
- (6) The waveform shall remain within the shaded area limits.

Change the second paragraph under the numbered list in 7.4.1.1 as follows:

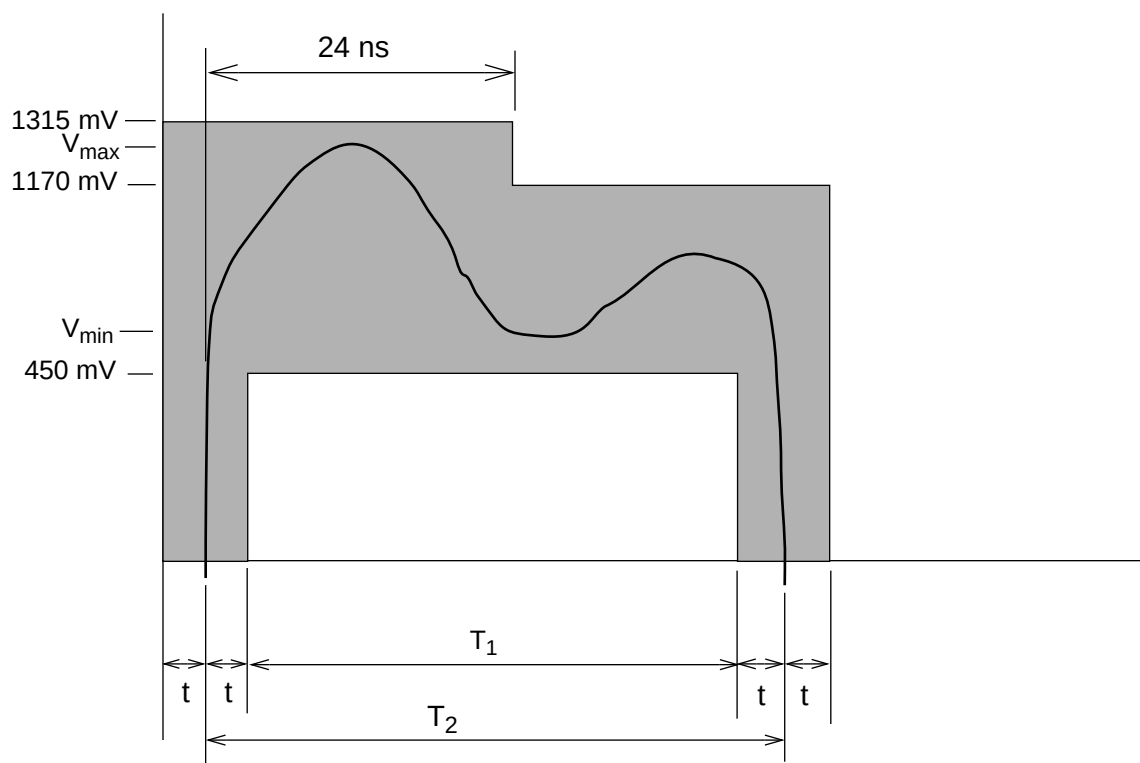
When a driver, connected to the appropriate two test loads identified above, enters the idle state, it shall maintain a minimum differential output voltage of at least $0.7 \times V_2$ mV 380 mV for at least 2 bit times after the last low to high transition.

Revise Fig 7-11 as follows:

Revise 7.4.1.2, 7.4.1.3, and 7.4.2.3 as shown below.

7.4.1.2 Requirements After Idle. When the driver becomes nonidle after a period of idle on the interface circuit, the differential output voltage at the interface connector shall meet the requirements of 7.4.1.1 beginning with the first second bit transmitted. ~~The first transition may occur asynchronously with respect to the timing of the following transitions. The first bit sent over the driver circuit may contain phase violations or invalid data.~~

7.4.1.3 AC Common-Mode Output Voltage. The magnitude of the ac component of the common-mode output voltage of the driver, measured between the midpoint of a test load consisting of a pair of matched $39\ \Omega \pm 1\%$ resistors and circuit VC, as shown in Fig 7-13, shall not exceed ~~40 mV peak, 2.5 V peak from 30 Hz to 40 kHz and 160 mV peak from 40 kHz to BR.~~



$t = 3.5 \text{ ns}$ at 1–10 MHz data rates
 $T_2 = (BT \text{ or } BT/2) \pm 2 \times T_j$, where T_j is the amount of MAU–DTE permissible edge jitter
 $T_1 = T_2 - 7.0 \text{ ns}$

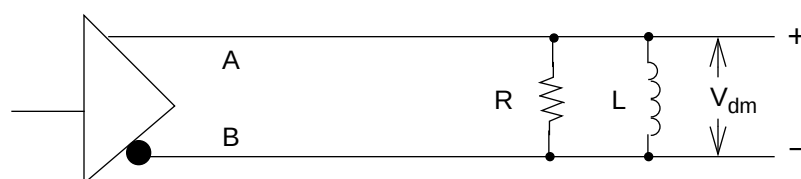


Fig 7-11
Differential Output Voltage, Loaded

7.4.2.3 AC Common-Mode Range. When the receiving interface circuit at the receiving equipment is driven by a differential input signal at either BR or BR/2 meeting the frequency and duty cycle tolerances specified for the circuit being driven, the receiver output shall assume the proper output state as specified in 7.4.2.1, in the presence of a peak common-mode ac sine wave voltage either of from 30 Hz to 40 kHz referenced to circuit VC in magnitude from 0 to 3 V, or in magnitude 0 to ~~100 mV~~ 200 mV for ac voltages of from 40 kHz to BR as shown in Fig 7-15.

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Conformance Test Methodology (Section 6)**

Revisions to IEEE Std 1802.3-1991

(These changes and additions are part of IEEE Std 1802.3d-1993.)

The following changes add references and abbreviations used by or referred to in 10BASE-T Conformance Testing (Section 6) to the appropriate places in IEEE Std 1802.3-1991. Editing instructions are shown in ***bold italics***.

1.3 Acronyms and Abbreviations

Add the following acronyms and abbreviations to the list in 1.3:

AWG	Arbitrary Waveform Generator
BAL	Balanced-Unbalanced Matching Transformer (Balun)
BT	Bit Time
CP	Current Probe
DP	Differential Probe
FG	Function Generator
HDP	High Performance Differential Probe
IDL	Idle Signal
IUT	Implementation Under Test
LTPG	Link Test Pulse Generator
MDI	Medium Dependent Interface
RD	Receive Data
SFD	Start Frame Delimiter
SOI	Start Of Idle
SQE	<i>signal_quality_error</i>
TD	Transmit Data
TPG	Test Pattern Generator
TPM	Twisted-Pair Model

1.8 References

Replace reference [3] in 1.8 with the following:

[3] ISO/IEC 8802-3 : 1993 [ANSI/IEEE Std 802.3, 1993 Edition], Information technology—Local and Metropolitan Area Networks—Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications.

Add the following references to 1.8 :

[6] IEEE Std 802.3I-1992 [ISO/IEC 8802-3, DAM17], IEEE Standards for Local and Metropolitan Area Networks: Supplement to Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications: Type 10BASE-T Medium Attachment Unit (MAU) Protocol Implementation Conformance Statement (PICS) Proforma (Section 14.10).

[7] IEC 60, High-voltage test techniques.

[8] IEC 950 : 1991 , Safety of information technology equipment, including electrical business equipment.

[9] ISO/IEC 8877 : 1992, Information technology—Telecommunications and information exchange between systems—Interface connector and contact assignments for ISDN Basic Access Interface located at reference points S and T.

6. Type 10BASE-T MAU Conformance Test Methodology

6.1 Scope of 10BASE-T MAU Conformance Test. The purpose of this section is to define abstract methods for the conformance testing of 10BASE-T MAU implementations in order to satisfy conformance requirements arising from the 10BASE-T MAU specification (Section 14 of ISO/IEC 8802-3 : 1993 [3]). Such methods will form the basis for any subsequent development of executable test cases. This document is applicable to the conformance testing of CSMA/CD 10BASE-T MAU (hereafter referred to as MAU) implementations that have been designed to Section 14 of ISO/IEC 8802-3 : 1993. Additional information about the implementation under test may be found in the PIXIT.

6.1.1 Embedded MAUs. Many of these tests do not apply to embedded MAUs where the physical AUI does not exist. In those cases, other standards may apply.

6.2 10BASE-T MAU Abstract Test Suite. This is comprised of one category of test groups. The category relates to capability testing. Within this category are a number of test groups, where each group is aimed at collecting individual test cases together that share some commonality in features tested or test methods used. The MAU test method is Local Single as per ISO 9646 [2]. The format for the test case headers follows the outline of 1.5, with the addition of a “PICS Reference:” line that cross-references the test case to a particular section/item of IEEE Std 802.3-1992 [ISO/IEC 8802-3, DAM17] [6].

Test Suite ID	: 1411
Test Suite Name	: 10BASE-T MAU Abstract Tests
Applicable Standards	: ISO/IEC 8802-3 : 1993 [3]
OSI RM Layer	: Physical
OSI RM Sublayer	: Medium Attachment Unit (MAU)
Class or Access	: CSMA/CD
Transmission Type	: 10BASE-T
Purpose	: To assess conformance of the physical interface to applicable standards.
General Setup	: Unless otherwise stated in individual test procedures, all tests shall start with “Apply power to the MAU and bring the MAU into Link Test Pass State.” In addition, all tests requiring the application of power to the MAU via the AUI shall be performed with 11.28 V applied through a 3.5 Ω 1% resistor to the VP circuit of the MAU and with 15.75 V applied through no series resistor to the VP circuit of the MAU, unless otherwise stated. For both voltage levels, all stray wiring and connection resistance for both the VP circuit and the VC circuit combined shall be limited to a maximum of 0.405 Ω excluding the resistance of conformant AUI connector connections at the source and MAU ends. All AUI applied voltages are with reference to circuit VC. When required, the MAU can be verified to be in a Link Test Fail state by monitoring the DI circuit for <i>input_idle</i> messages and the TD circuit for <i>TD_idle</i> messages.

6.2.1 Capability and Behavior Tests

6.2.1.1 Test Group 1411.01—Transmit Functions

Test Group ID	: 1411.01
Test Group Name	: Transmit Functions.
Test Group Purpose	: To verify the characteristics of the Transmit Function.

Test Case ID	:	1411.01.01
Test Case Name	:	Transmit signal polarity.
Status	:	MANDATORY
Standard Reference	:	14.2.1.1
PICS Reference	:	14.10.4.5.2/1, 14.10.4.5.2/2
History	:	
Test Purpose	:	To verify the polarity of the TD circuit signals in relation to the DO circuit signals.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DO circuit and the TD circuit for correct logical sense after the initial bit loss time and before the start of idle of a packet transmission.
Conformance	:	The MAU shall receive the signals on the DO circuit and send them to the TD circuit of the MDI. A positive signal on the A lead relative to the B lead of the DO circuit shall result in a positive signal on the TD+ (Transmit Data +) lead of the MDI with respect to the TD– lead.

Test Case ID	:	1411.01.02
Test Case Name	:	Transmit start-up bit loss.
Status	:	MANDATORY
Standard Reference	:	14.2.1.1
PICS Reference	:	14.10.4.5.2/3
History	:	
Test Purpose	:	To verify the number of bits received on the DO circuit and not transmitted on the TD circuit.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DO circuit and TD circuit. Measure the number of bits received on the DO circuit and not transmitted onto the TD circuit using the Start Frame Delimiter (SFD) for reference.
Conformance	:	At the start of a packet transmission, no more than 2 bits may be received by the MAU from the DO circuit and not transmitted on the TD circuit. It is permissible for the first bit sent to contain phase violations or invalid amplitude.

Test Case ID	:	1411.01.03
Test Case Name	:	Transmit settling time.
Status	:	MANDATORY
Standard Reference	:	14.2.1.1
PICS Reference	:	14.10.4.5.2/4
History	:	
Test Purpose	:	To verify the timing and signal level of the second bit cell transmitted.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DO circuit and TD circuit. Observe the second and subsequent bits on the TD circuit.

Conformance : The second bit transmitted on the TD circuit shall be transmitted with the correct timing and signal levels.

Test Case ID : 1411.01.04
 Test Case Name : Transmit steady-state delay.
 Status : MANDATORY
 Standard Reference : 14.2.1.1
 PICS Reference : 14.10.4.5.2/5
 History :
 Test Purpose : To verify the propagation delay between the DO circuit and the TD circuit.
 Note :
 Test Setup : Test setup B.
 Test Procedure : Apply test signal 1 to the DO circuit of the MAU. Monitor the DO circuit and TD circuit. Measure the propagation delay from a bit's zero crossing on the DO circuit to the corresponding bit's zero crossing on the TD circuit using the SFD for reference.
 Conformance : The steady-state propagation delay between the DO circuit input and the TD circuit shall not exceed 2 bit times.

Test Case ID : 1411.01.05
 Test Case Name : Transmit delay variability.
 Status : MANDATORY.
 Standard Reference : 14.2.1.1
 PICS Reference : 14.10.4.5.2/6
 History :
 Test Purpose : To verify the start-up delay variability between two packets.
 Note :
 Test Setup : Test setup B.
 Test Procedure : Apply test signals 2a–f to the DO circuit of the MAU. Monitor the DO circuit and TD circuit. Measure the start-up delay (bit loss plus steady state propagation delay) for a packet and the subsequent packet. Repeat the test 100 times to determine the largest variability.
 Conformance : For any two packets that are separated by 9.6 μ s or less, the start-up delay (bit loss plus steady-state propagation delay) of the first packet shall not exceed that of the second packet by more than 2 bit times.

Test Case ID : 1411.01.06
 Test Case Name : TP_IDL, silence duration and silence voltage.
 Status : MANDATORY
 Standard Reference : 14.2.1.1
 PICS Reference : 14.10.4.5.2/7, 14.10.4.5.2/8
 History :
 Test Purpose : To verify the timing of the TP_IDL signal.
 Note :
 Test Setup : Test setup B.
 Test Procedure : Apply test signal 1 to the DO circuit of the MAU. Monitor the TD circuit. Measure the period of silence between the start of TP_IDL and the link test pulse. Measure the time between repeating link test pulses.

Conformance : Whenever data is not being transmitted on the TD circuit, an idle signal, TP_IDL, shall be transmitted on the TD circuit. TP_IDL is a start of idle as defined in 14.3.1.2.1 followed by a repeating sequence of a $16\text{ ms} \pm 8\text{ ms}$ period of silence (the time where the differential voltage remains at $0\text{ mV} \pm 50\text{ mV}$) and a link test pulse (see 14.3.1.2.1).

Test Case ID : 1411.01.07
 Test Case Name : TP_IDL signal termination with respect to start of packet and link test pulse.
 Status : MANDATORY
 Standard Reference : 14.2.1.1
 PICS Reference : 14.10.4.5.2/9
 History :
 Test Purpose : To verify correct termination of the TP_IDL signal.
 Note : *This test case is considered untestable. It is not practical to measure and is not considered critical. Even though testing for compliance is not practical, conformance to the standard, **by design**, is the responsibility of the manufacturer with compliance status to be noted in the PICS.*

Test Setup :
 Test Procedure :
 Conformance : Transmission of TP_IDL may be terminated at any time with respect to the link test pulse. It shall be terminated such that no more than the first transmitted bit of a packet is corrupted and with no more delay than is specified for bit loss and steady-state propagation.

6.2.1.2 Test Group 1411.02—Receive Functions

Test Group ID : 1411.02
 Test Group Name : Receive Functions.
 Test Group Purpose : To verify the characteristics of the Receive Function.

Test Case ID : 1411.02.01
 Test Case Name : Receive start-up bit loss.
 Status : MANDATORY
 Standard Reference : 14.2.1.2
 PICS Reference : 14.10.4.5.3/3
 History :
 Test Purpose : To verify the number of bits received on the RD circuit and not transmitted on the DI circuit.

Note :
 Test Setup : Test setup L.
 Test Procedure : Apply test signal 1 to the DO circuit of the tester MAU. Monitor the RD circuit and DI circuit on the MAU under test. Measure the number of bits received on the RD circuit of the MAU under test and not transmitted on the DI circuit of the MAU under test using the SFD for reference.

Conformance : At the start of a packet reception from the RD circuit, no more than 5 bits may be received from the RD circuit and not transmitted onto the DI circuit.

Test Case ID	:	1411.02.02
Test Case Name	:	Receive steady-state delay.
Status	:	MANDATORY
Standard Reference	:	14.2.1.2
PICS Reference	:	14.10.4.5.3/5
History	:	
Test Purpose	:	To verify the propagation delay from the RD circuit to the DI circuit.
Note	:	
Test Setup	:	Test setup L.
Test Procedure	:	Apply test signal 1 to the DO circuit of the tester MAU. Monitor the DI circuit and RD circuit on the MAU under test. Measure the propagation delay between a bit's zero crossing on the RD circuit of the MAU under test and the corresponding bit's zero crossing on the DI circuit of the MAU under test using the SFD for reference.
Conformance	:	The steady-state propagation delay between the RD circuit and the DI circuit shall not exceed 2 bit times.

Test Case ID	:	1411.02.03
Test Case Name	:	Receive signal polarity.
Status	:	MANDATORY
Standard Reference	:	14.2.1.2
PICS Reference	:	14.10.4.5.3/1, 14.10.4.5.3/2
History	:	
Test Purpose	:	To verify the polarity of the DI circuit signals in relation to the RD circuit signals.
Note	:	
Test setup	:	Test setup L
Test Procedure	:	Apply test signal 1 to the DO circuit of the tester MAU. Monitor the DI circuit and RD circuit signals on the MAU under test for correct logical sense after the initial bit loss time and before the start of idle of the packet.
Conformance	:	The MAU shall receive the signals on the RD circuit of the MDI and send them to the DI circuit. A positive signal on the RD+ (Receive Data +) lead relative to the RD– lead of the MDI shall result in a positive signal on the A lead with respect to the B lead of the DI circuit.

Test Case ID	:	1411.02.04
Test Case Name	:	Receive delay variability.
Status	:	MANDATORY
Standard Reference	:	14.2.1.2
PICS Reference	:	14.10.4.5.3/6
History	:	
Test Purpose	:	To verify the start-up delay between two packets.
Note	:	
Test Setup	:	Test setup H.
Test Procedure	:	Apply test signals 24a–f to the RD circuit of the MAU under test. Monitor the DI circuit and RD circuit signals. Measure how much the start-up delay (bit loss plus steady-state propagation delay) exceeds the delay of the subsequent packet. Re-

Conformance : repeat the test 100 times and note the worst-case value.
For any two packets that are separated by 9.6 μ s or less, the start-up delay (bit loss plus steady-state propagation delay) of the first packet shall not exceed that of the second packet by more than 2 bit times.

Test Case ID : 1411.02.05
 Test Case Name : Receive settling time.
 Status : MANDATORY
 Standard Reference : 14.2.1.2
 PICS Reference : 14.10.4.5.3/4
 History :
 Test Purpose : To verify the timing and signal level of the second bit transmitted.
 Note :
 Test Setup : Test setup L.
 Test Procedure : Apply test signal 1 to the DO circuit of the tester MAU. Monitor the DI circuit and RD circuit on the MAU under test. Observe the second and subsequent bits on the DI circuit of the MAU under test.
 Conformance : It is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however all successive bits of the packet shall be sent with no more than the amount of jitter specified in 14.3.1.3.1.

6.2.1.3 Test Group 1411.03—Loopback Functions

Test Group ID : 1411.03
 Test Group Name : Loopback Functions.
 Test Group Purpose : To verify the functional characteristics of the Loopback Function.

Test Case ID : 1411.03.01
 Test Case Name : Loopback function when RD = idle and DO = active.
 Status : MANDATORY
 Standard Reference : 14.2.1.3
 PICS Reference : 14.10.4.5.4/1
 History :
 Test Purpose : To verify the Loopback function requirements when RD is idle and DO is active.
 Note :
 Test Setup : Test setup B.
 Test Procedure : Apply test signal 1 to the DO circuit of the MAU. Monitor the DI circuit.
 Conformance : When the MAU is transmitting on the TD circuit and is not receiving *RD_input* messages on the RD circuit, the MAU shall transmit on the DI circuit the signals received on the DO circuit in order to provide loopback of the transmitted signal.

Test Case ID : 1411.03.02
 Test Case Name : Loopback bit loss (DO to DI circuits).

Status	:	MANDATORY
Standard Reference	:	14.2.1.3
PICS Reference	:	14.10.4.5.4/2
History	:	
Test Purpose	:	To verify the number of bits transmitted on the DO circuit and not received on the DI circuit.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DI circuit and DO circuit. Measure the number of bits received on the DO circuit and not transmitted on the DI circuit using the SFD for reference.
Conformance	:	At the start of a packet transmission on the TD circuit, no more than 5 bits of information may be received from the DO circuit and not transmitted to the DI circuit.

Test Case ID	:	1411.03.03
Test Case Name	:	Loopback steady-state delay.
Status	:	MANDATORY
Standard Reference	:	14.2.1.3
PICS Reference	:	14.10.4.5.4/4
History	:	
Test Purpose	:	To verify the propagation delay from the DO circuit to the DI circuit.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DI circuit and DO circuit. Measure the propagation delay from a bit's zero crossing on the DO circuit to the corresponding bit's zero crossing on the DI circuit using the SFD for reference.
Conformance	:	The steady-state propagation delay between the DO circuit and the DI circuit shall not exceed 1 BT.

Test Case ID	:	1411.03.04
Test Case Name	:	Loopback settling time.
Status	:	MANDATORY
Standard Reference	:	14.2.1.3
PICS Reference	:	14.10.4.5.4/3
History	:	
Test Purpose	:	To verify the timing and signal level of the second bit cell transmitted.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DI circuit and DO circuit signals. Observe the second and subsequent bits of the DI circuit data.
Conformance	:	It is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall meet the jitter specified in 14.3.1.3.1 (that is, 13.5 ns + 1.5 ns).

6.2.1.4 Test Group 1411.04—Collision Functions

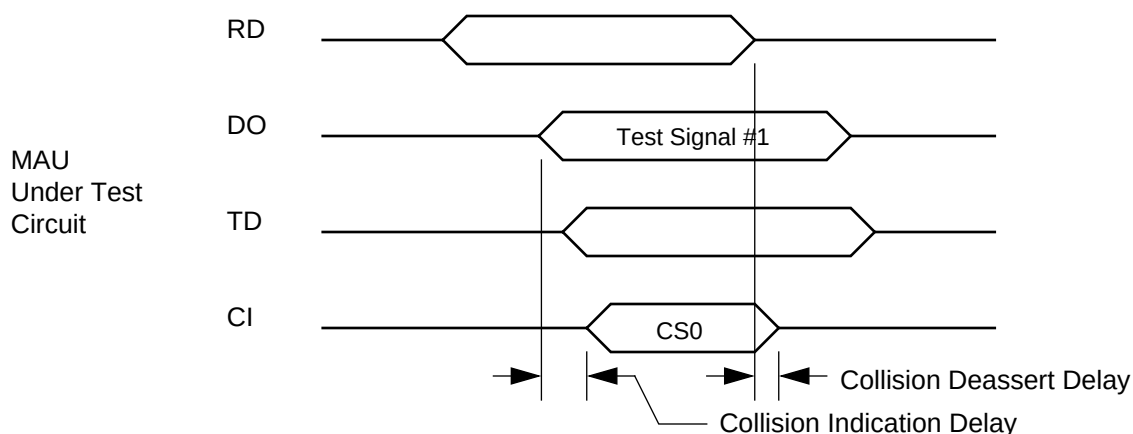
Test Group ID : 1411.04
Test Group Name : Collision Functions.
Test Group Purpose : To verify the functional characteristics of the Collision Function.

Test Case ID : 1411.04.01
Test Case Name : No collision state.
Status : MANDATORY
Standard Reference : 14.2.1.4
PICS Reference : 14.10.4.5.5/4
History :
Test Purpose : To verify the presence and the signal characteristics of IDL on the CI circuit when there is no collision, SQE test, or jabber.
Note :
Test Setup : Test setup M.
Test Procedure : Monitor the CI circuit of the MAU under test.
 (1) Apply test signal 1 to the DO circuit of the tester MAU and IDL to the DO circuit of the MAU under test.
 (2) Apply test signal 1 to the DO circuit of the MAU under test and IDL to the DO circuit of the tester MAU.
Verify that CI is asserting IDL while DI is active.
Conformance : The signal present on the CI circuit in the absence of a collision, SQE test, or jabber shall be the IDL signal.

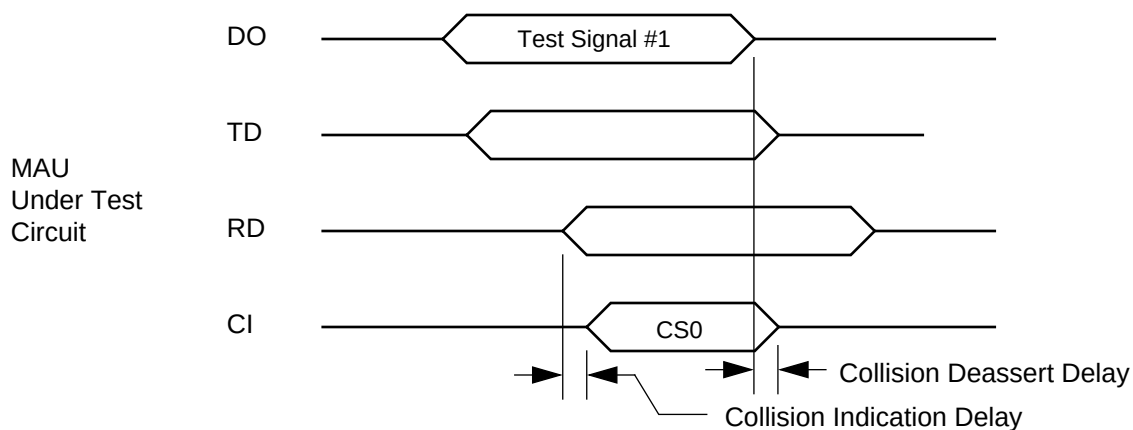
Test Case ID : 1411.04.02
Test Case Name : Collision state.
Status : MANDATORY
Standard Reference : 14.2.1.4
PICS Reference : 14.10.4.5.5/1
History :
Test Purpose : To verify the presence and the signal characteristics of CS0 on the CI circuit when there is a collision.
Note :
Test Setup : Test setup O.
Test Procedure : Monitor the CI circuit, DO circuit, and TD circuit of the MAU under test.
 (1) Apply test signal 1 to the DO circuit of the tester MAU. Apply test signal 1 to the DO circuit of the MAU under test to create a collision. Verify on the MAU under test that the signals on the DO circuit appear on the TD circuit and that CS0 is present on the CI circuit (see Fig 6-1a).
 (2) Apply test signal 1 to the DO circuit of the MAU under test. Apply test signal 1 to the DO circuit of the tester MAU to create a collision. Verify on the MAU under test that the signals on the DO circuit appear on the TD circuit and that CS0 is present on the CI circuit (see Fig 6-1b).
Conformance : While a collision is detected, a CS0 signal (see 7.3.1.2) shall be sent on the CI circuit.

Test Case ID	:	1411.04.03
Test Case Name	:	Collision indication delay.
Status	:	MANDATORY
Standard Reference	:	14.2.1.4
PICS Reference	:	14.10.4.5.5/2
History	:	
Test Purpose	:	To verify the delay between the collision start and the collision presence state indicated on CI circuit.
Note	:	
Test Setup	:	Test setup O.
Test Procedure	:	Monitor the CI circuit, DO circuit and RD circuit of the MAU under test.
		(1) Apply test signal 1 to the DO circuit of the tester MAU. Apply test signal 1 to the DO circuit of the MAU under test to create a collision. Measure the delay from collision start (application of the second test signal on the DO circuit of the MAU under test) to commencement of the CS0 signal on the CI circuit (see Fig 6-1a).
		(2) Apply test signal 1 to the DO circuit of the MAU under test. Apply test signal 1 to the DO circuit of the tester MAU to create a collision. Measure the delay from collision start (appearance of the second test signal on the RD circuit of the MAU under test) to commencement of the CS0 signal on the CI circuit (see Fig 6-1b).
Conformance	:	The CS0 signal shall be presented to the CI circuit no more than 9 bit times after the occurrence of a collision.

Test Case ID	:	1411.04.04
Test Case Name	:	Collision indication deassert delay.
Status	:	MANDATORY
Standard Reference	:	14.2.1.4
PICS Reference	:	14.10.4.5.5/3
History	:	
Test Purpose	:	To verify the cessation of the CS0 signal after the collision condition is removed.
Note	:	
Test Setup	:	Test setup O.
Test Procedure	:	Monitor the CI circuit, DO circuit and RD circuit of the MAU under test.
		(1) Apply test signal 1 to the DO circuit of the tester MAU. Apply test signal 1 to the DO circuit of the MAU under test to create a collision. Monitor the CI circuit for the presence of the CS0 signal. Stop the application of the test signal on the DO circuit of the tester MAU. Measure the time from the last transition of the test signal on the RD circuit of the MAU under test until the CS0 signal on the CI circuit stops (see Fig 6-1a).
		(2) Apply test signal 1 to the DO circuit of the MAU under test. Apply test signal 1 to the DO circuit of the tester MAU to create a collision. Monitor the CI circuit for the presence of the CS0 signal. Stop the application of the test signal on the DO circuit of the MAU under test. Measure the time from the last transition of the test



a) Test Signal Applied to Tester MAU, Then MAU Under Test



b) Test Signal Applied to MAU Under Test, Then Tester MAU

Fig 6-1
Test Signal Application Timing for Collision Functions

signal on the DO circuit of the MAU under test until the CS0 signal on the CI circuit stops (see Fig 6-1b).

Conformance : The CS0 signal on the CI circuit shall be deasserted within 9 bit times after the DO circuit or the RD circuit changes from active to idle.

Test Case ID : 1411.04.05

Test Case Name : DI circuit source switch delay from CS0 assert.

Status : MANDATORY

Standard Reference : 14.2.1.4

PICS Reference : 14.10.4.5.5/5

History :

Test Purpose : To verify the delay between the start of collision and the presence of RD data on the DI circuit.

Note :

Test Setup : Test setup M.

Test Procedure : Apply test signal 19a to the DO circuit of the MAU under test. Monitor the CI circuit and DI circuit of the MAU under test. Apply test signal 19b to the DO circuit of the tester MAU at least 65 BT after the test signal on the MAU under test is applied to create a collision. Monitor the CI circuit for the presence of the CS0 signal. Measure the delay between the assertion of CS0 and commencement of *input* on the DI circuit corresponding to the test signal applied to the tester MAU. The signals applied to the DO circuit of the tester MAU and the DO circuit of the MAU under test are different to facilitate differentiation between DO loopback and RD.

Conformance : When CS0 is asserted on the CI circuit due to a collision, the data on the RD circuit shall be sent to the DI circuit within 9 bit times.

Test Case ID : 1411.04.06

Test Case Name : DI circuit source switch delay from CS0 deassert.

Status : MANDATORY

Standard Reference : 14.2.1.4

PICS Reference : 14.10.4.5.5/6

History :

Test Purpose : To verify the delay between the end of collision and the presence of DO data on the DI circuit.

Note :

Test Setup : Test setup M.

Test Procedure : Apply the test signal 19a to the DO circuit of the MAU under test. Monitor the CI circuit, RD circuit and DI circuit of the MAU under test. Apply test signal 19b to the DO circuit of the tester MAU at least 65 BT after the test signal on the MAU under test is applied to create a collision. Monitor the CI circuit for the presence of the CS0 signal. After CS0 is asserted, stop transmitting on the DO circuit of the tester MAU. Measure the delay between idle on the RD circuit (14.2.2.5) and the presence of the DO circuit test signal on the DI circuit. The signals applied to the DO circuit of the tester MAU and the DO circuit of the MAU under test are different to facilitate differentiation between RD circuit data and DO loopback.

Conformance : When the RD circuit changes from active to idle and data is present on the DO circuit, the data on the DO circuit shall be sent to the DI circuit within 9 bit times.

6.2.1.5 Test Group 1411.05—SQE Test Functions

Test Group ID : 1411.05
 Test Group Name : *Signal_quality_error* Message (SQE) Test Functions.
 Test Group Purpose : To verify the functional characteristics of the SQE Test function.

Test Case ID : 1411.05.01
 Test Case Name : SQE_test_timer range.
 Status : CONDITIONAL (SQE Test function shall be performed by MAUs connected to DTEs and shall not be performed for MAUs connected to repeaters).
 Standard Reference : 14.2.1.5
 PICS Reference : 14.10.4.5.6/3, 14.10.4.5.6/4
 History :
 Test Purpose : To verify the duration of the SQE Test state after the end of a frame transmission.
 Note : Duration of CS0 is between first excursion outside 0 mV $\pm$ 40 mV and the last positive transition.
 Test Setup : Test setup B.
 Test Procedure : Apply test signal 1 to the DO circuit of the MAU. Monitor the CI circuit. Measure duration of the CS0 signal on the CI circuit.
 Conformance : The MAU shall send CS0 on the CI circuit for a time “SQE_test” beginning a time “SQE_test_wait” after the last positive transition on the DO circuit. The value of “SQE_test” shall be 10 bit $\pm$ 5 bit times.

Test Case ID : 1411.05.02
 Test Case Name : SQE_test_wait_timer range.
 Status : CONDITIONAL (SQE Test function shall be performed by MAUs connected to DTEs and shall not be performed for MAUs connected to repeaters).
 Standard Reference : 14.2.1.5
 PICS Reference : 14.10.4.5.6/2
 History :
 Test Purpose : To verify the duration of the SQE Test Wait state after the end of a frame transmission.
 Note : Duration of CS0 is between first excursion outside 0 mV $\pm$ 40 mV and the last positive transition.
 Test Setup : Test setup B.
 Test Procedure : Apply test signal 1 to the DO circuit of the MAU. Monitor the DO circuit and CI circuit. Measure time delay between the last positive transition of the data on the DO circuit and the assertion of CS0 on the CI circuit.
 Conformance : The MAU shall send CS0 on the CI circuit beginning a time “SQE_test_wait” after the last positive transition of a packet on the DO circuit. The value of “SQE_test_wait” shall be between 0.6 μ s and 1.6 μ s.

Test Case ID	: 1411.05.03
Test Case Name	: SQE Test function interference.
Status	: CONDITIONAL (SQE Test function shall be performed by MAUs connected to DTEs and shall not be performed for MAUs connected to repeaters).
Standard Reference	: 14.2.1.5
PICS Reference	: 14.10.4.5.6/1
History	:
Test Purpose	: To verify the effect of the SQE Test function on the TD and DI circuits.
Note	: Extraneous signal on the TD circuit is defined to be greater than ± 50 mV; extraneous signal on the DI circuit is defined to be greater than ± 40 mV.
Test Setup	: Test setup B.
Test Procedure	: Apply test signal 1 to the DO circuit of the MAU. Monitor the DI circuit and TD circuit for $3\text{ }\mu\text{s}$ after the end of frame transmission.
Conformance	: This function should not introduce extraneous signals on the TD circuit or the DI circuit.

Test Case ID	: 1411.05.04
Test Case Name	: SQE Test function in link fail state.
Status	: CONDITIONAL (SQE Test function shall be performed by MAUs connected to DTEs and shall not be performed for MAUs connected to repeaters).
Standard Reference	: 14.2.1.5
PICS Reference	: 14.10.4.5.6/5
History	:
Test Purpose	: To verify that the SQE Test function does not transmit a CS0 signal when MAU is in a Link Test Fail state.
Note	:
Test Setup	: Test setup N.
Test Procedure	: Apply power to the MAU under test. Monitor the AUI CI circuit of the MAU under test. Wait for 151 ms then apply test signal 1 to the DO circuit of the MAU under test. Check that the MAU is in a Link Test Fail state. Verify that CS0 is not asserted on the CI circuit for at least $3.1\text{ }\mu\text{s}$.
Conformance	: The CS0 signal shall not be sent by the SQE Test function while in any of the Link Test Fail states.

6.2.1.6 Test Group 1411.06—Jabber Functions

Test Group ID	: 1411.06
Test Group Name	: Jabber Functions.
Test Group Purpose	: To verify the functional characteristics of the Jabber Test function.

Test Case ID	: 1411.06.01
Test Case Name	: Xmit_max_timer range.
Status	: MANDATORY
Standard Reference	: 14.2.1.6
PICS Reference	: 14.10.4.5.7/2, 14.10.4.5.7/3

History	:	
Test Purpose	:	To verify that jabber transmission inhibit starts within the time required.
Note	:	
Test Setup	:	Test setup C.
Test Procedure	:	Apply test signal 3a to the DO circuit of the MAU. Monitor the DI circuit, TD circuit, and CI circuit. Check that the TD circuit and DI circuit signals are present up to 20 ms following the application of the input signal and that they are absent after 150 ms following the application of the input. Check that CS0 is asserted on the CI circuit after the 150 ms time period. Repeat the same procedure using test signal 3b.
Conformance	:	The MAU shall provide a window “xmit_max” during which time the Transmit function may continuously transmit <i>TD_output</i> messages to the TD circuit. The value of “xmit_max” shall be between 20 ms and 150 ms. If a transmission exceeds this duration, the Jabber function shall inhibit the Loopback function and the transmission of <i>TD_output</i> messages by the Transmit function and shall send the CS0 signal on the CI circuit.

Test Case ID	:	1411.06.02
Test Case Name	:	Jabber reset.
Status	:	MANDATORY
Standard Reference	:	14.2.1.6
PICS Reference	:	14.10.4.5.7/1, 14.10.4.5.7/4
History	:	
Test Purpose	:	To verify the jabber function reset mechanism.
Note	:	
Test Setup	:	Test setup C.
Test Procedure	:	Apply test signal 3a to the DO circuit of the MAU. Monitor the DI circuit, TD circuit, and CI circuit. When jabber is indicated (signals no longer present on the DI and TD circuits and CS0 is asserted on the CI circuit), stop the test signal. Wait 249 ms from when the test signal is stopped and verify that CS0 is still present on the CI circuit and that no signals are present on the TD circuit and DI circuit. Wait an additional 502 ms and verify that CS0 is no longer asserted on the CI circuit. Repeat the above procedure using test signal 3b.
Conformance	:	If a transmission exceeds “xmit_max” the Jabber function shall inhibit the Loopback function and the transmission of <i>TD_output</i> messages by the Transmit function and shall send the CS0 signal on the CI circuit. This shall continue until <i>output_idle</i> has been continuously present on the DO circuit for a time “unjab”. The value of “unjab” shall be 0.5 s ± 0.25 s.

Test Case ID	:	1411.06.03
Test Case Name	:	Jabber lockup protection.
Status	:	MANDATORY
Standard Reference	:	14.2.1.6
PICS Reference	:	14.10.4.5.7/5
History	:	

Test Purpose	:	To verify the MAU jabber lockup protection.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 26 to the DO circuit of the MAU. Monitor the TD circuit. Verify that the MAU does not enter jabber by verifying that the TD circuit remains active.
Conformance	:	The MAU shall not activate its Jabber function when the repeater's MAU Jabber Lockup Protection function operates at its longest permitted time as specified in 9.6.5.

6.2.1.7 Test Group 1411.07—Link Integrity Test Functions

Test Group ID	:	1411.07
Test Group Name	:	Link Integrity Test Functions.
Test Group Purpose	:	To verify the functional characteristics of the Link Test functions.

Test Case ID	:	1411.07.01
Test Case Name	:	Link loss timer.
Status	:	MANDATORY
Standard Reference	:	14.2.1.7
PICS Reference	:	14.10.4.5.8/1
History	:	
Test Purpose	:	To verify the value of the “link_loss” timer.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 4 to the DO circuit of the MAU. Monitor the DI circuit and TD circuit. Stop applying the link test pulses to the RD circuit. Measure the time from the last link test pulse to the loss of loopback on the DI circuit.
Conformance	:	If neither <i>RD_input</i> nor a link test pulse is received for a time “link_loss”, the MAU shall enter the Link Test Fail state and cause the <i>input_idle</i> message to be sent on the DI circuit and the <i>TD_idle</i> message to be sent on the TD circuit (Fig 14-6). The value of “link_loss” shall be between 50 ms and 150 ms.

Test Case ID	:	1411.07.02
Test Case Name	:	Acceptance range for consecutive link test pulses.
Status	:	MANDATORY
Standard Reference	:	14.2.1.7
PICS Reference	:	14.10.4.5.8/6, 14.10.4.5.8/7
History	:	
Test Purpose	:	To verify acceptance range for consecutive link test pulses.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply power to the MAU. Stop applying the link test pulses to the RD circuit. Check that the MAU is in a Link Test Fail state. Monitor the DO circuit and DI circuit. Apply a test signal consisting of 11 link test pulses that are spaced 7.1 ms apart to the RD circuit of the MAU. Apply test signal 1 to the DO circuit of the MAU. Verify loopback presence on the DI circuit. Repeat the test procedure with 24 ms spacing between link test pulses.