



IEEE Recommended Practice for Hardware-in-the-Loop (HIL) Simulation-Based Testing of Electric Power Apparatus and Controls

IEEE Power Electronics Society
and the
IEEE Industrial Electronics Society

Developed by the
Standards Committee
and the
Industrial Electronics Society Standards Committee

IEEE Std 2004™-2025

STANDARDS

IEEE Recommended Practice for Hardware-in-the-Loop (HIL) Simulation-Based Testing of Electric Power Apparatus and Controls

Developed by the

Standards Committee
of the
IEEE Power Electronics Society

and the

Industrial Electronics Society Standards Committee
of the
IEEE Industrial Electronics Society

Approved 12 February 2025

IEEE SA Standards Board

Abstract: Recommendations for the user to design, establish, and execute real-time based hardware-in-the-loop setups are provided in this document, along with analytical frameworks related to stability, accuracy, and sensitivity assessment, as well as experimental case studies. Additional informative material is provided in the annexes.

Keywords: controller hardware-in-the-loop, data acquisition, decoupling and parallelization methods, IEEE 2004™, interfacing methods, natural coupling, power amplification, power hardware-in-the-loop, power interface, protection methods, real-time, real-time simulation, relay testing, safety measures, simulation systems, stability and accuracy of HIL systems, synchronization, system modeling

The Institute of Electrical and Electronics Engineers, Inc.
3 Park Avenue, New York, NY 10016-5997, USA

Copyright © 2025 by The Institute of Electrical and Electronics Engineers, Inc. All rights reserved.
Published 31 August 2025. Printed in the United States of America.

IEEE is a registered trademark in the U.S. Patent & Trademark Office, owned by The Institute of Electrical and Electronics Engineers, Incorporated.

PDF: ISBN 979-8-8557-2368-7 STD28063
Print: ISBN 979-8-8557-2369-4 STDPD28063

IEEE prohibits discrimination, harassment, and bullying.

For more information, visit <https://www.ieee.org/about/corporate/governance/p9-26.html>.

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

Important Notices and Disclaimers Concerning IEEE Standards Documents

IEEE Standards documents are made available for use subject to important notices and legal disclaimers. These notices and disclaimers, or a reference to this page (<https://standards.ieee.org/ipr/disclaimers.html>), appear in all IEEE standards and may be found under the heading “Important Notices and Disclaimers Concerning IEEE Standards Documents.”

Notice and Disclaimer of Liability Concerning the Use of IEEE Standards Documents

IEEE Standards documents are developed within IEEE Societies and subcommittees of IEEE Standards Association (IEEE SA) Board of Governors. IEEE develops its standards through an accredited consensus development process, which brings together volunteers representing varied viewpoints and interests to achieve the final product. IEEE standards are documents developed by volunteers with scientific, academic, and industry-based expertise in technical working groups. Volunteers involved in technical working groups are not necessarily members of IEEE or IEEE SA and participate without compensation from IEEE. While IEEE administers the process and establishes rules to promote fairness in the consensus development process, IEEE does not independently evaluate, test, or verify the accuracy of any of the information or the soundness of any judgments contained in its standards.

IEEE makes no warranties or representations concerning its standards, and expressly disclaims all warranties, express or implied, concerning all standards, including but not limited to the warranties of merchantability, fitness for a particular purpose and non-infringement. IEEE Standards documents do not guarantee safety, security, health, or environmental protection, or compliance with law, or guarantee against interference with or from other devices or networks. In addition, IEEE does not warrant or represent that the use of the material contained in its standards is free from patent infringement. IEEE Standards documents are supplied “AS IS” and “WITH ALL FAULTS.”

Use of an IEEE standard is wholly voluntary. The existence of an IEEE standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEEE standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard.

In publishing and making its standards available, IEEE is not suggesting or rendering professional or other services for, or on behalf of, any person or entity, nor is IEEE undertaking to perform any duty owed by any other person or entity to another. Any person utilizing any IEEE Standards document should rely upon their own independent judgment in the exercise of reasonable care in any given circumstances or, as appropriate, seek the advice of a competent professional in determining the appropriateness of a given IEEE standard.

IN NO EVENT SHALL IEEE BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO: THE NEED TO PROCURE SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE PUBLICATION, USE OF, OR RELIANCE UPON ANY STANDARD, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE AND REGARDLESS OF WHETHER SUCH DAMAGE WAS FORESEEABLE.

Translations

The IEEE consensus balloting process involves the review of documents in English only. In the event that an IEEE standard is translated, only the English language version published by IEEE is the approved IEEE standard.

Use by artificial intelligence systems

In no event shall material in any IEEE Standards documents be used for the purpose of creating, training, enhancing, developing, maintaining, or contributing to any artificial intelligence systems without the express, written consent of IEEE SA in advance. “Artificial intelligence” refers to any software, application, or other system that uses artificial intelligence, machine learning, or similar technologies, to analyze, train, process, or generate content. Requests for consent can be submitted using the Contact Us form.

Official statements

A statement, written or oral, that is not processed in accordance with the IEEE SA Standards Board Operations Manual is not, and shall not be considered or inferred to be, the official position of IEEE or any of its committees and shall not be considered to be, or be relied upon as, a formal position of IEEE or IEEE SA. At lectures, symposia, seminars, or educational courses, an individual presenting information on IEEE standards shall make it clear that the presenter’s views should be considered the personal views of that individual rather than the formal position of IEEE, IEEE SA, the Standards Committee, or the Working Group. Statements made by volunteers may not represent the formal position of their employer(s) or affiliation(s). News releases about IEEE standards issued by entities other than IEEE SA should be considered the view of the entity issuing the release rather than the formal position of IEEE or IEEE SA.

Comments on standards

Comments for revision of IEEE Standards documents are welcome from any interested party, regardless of membership affiliation with IEEE or IEEE SA. However, **IEEE does not provide interpretations, consulting information, or advice pertaining to IEEE Standards documents.**

Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments. Since IEEE standards represent a consensus of concerned interests, it is important that any responses to comments and questions also receive the concurrence of a balance of interests. For this reason, IEEE and the members of its Societies and subcommittees of the IEEE SA Board of Governors are not able to provide an instant response to comments or questions, except in those cases where the matter has previously been addressed. For the same reason, IEEE does not respond to interpretation requests. Any person who would like to participate in evaluating comments or revisions to an IEEE standard is welcome to join the relevant IEEE SA working group. You can indicate interest in a working group using the Interests tab in the Manage Profile and Interests area of the [IEEE SA myProject system](#).¹ An IEEE account is needed to access the application.

Comments on standards should be submitted using the [Contact Us](#) form.²

Laws and regulations

Users of IEEE Standards documents should consult all applicable laws and regulations. Compliance with the provisions of any IEEE Standards document does not constitute compliance to any applicable regulatory

¹ Available at: <https://development.standards.ieee.org/myproject-web/public/view.html#landing>.

² Available at: <https://standards.ieee.org/about/contact/>.

requirements. Implementers of the standard are responsible for observing or referring to the applicable regulatory requirements. IEEE does not, by the publication of its standards, intend to urge action that is not in compliance with applicable laws, and these documents may not be construed as doing so.

Data privacy

Users of IEEE Standards documents should evaluate the standards for considerations of data privacy and data ownership in the context of assessing and using the standards in compliance with applicable laws and regulations.

Copyrights

IEEE draft and approved standards are copyrighted by IEEE under US and international copyright laws. They are made available by IEEE and are adopted for a wide variety of both public and private uses. These include both use by reference, in laws and regulations, and use in private self-regulation, standardization, and the promotion of engineering practices and methods. By making these documents available for use and adoption by public authorities and private users, neither IEEE nor its licensors waive any rights in copyright to the documents.

Photocopies

Subject to payment of the appropriate licensing fees, IEEE will grant users a limited, non-exclusive license to photocopy portions of any individual standard for company or organizational internal use or individual, non-commercial use only. To arrange for payment of licensing fees, please contact Copyright Clearance Center, Customer Service, 222 Rosewood Drive, Danvers, MA 01923 USA; +1 978 750 8400; <https://www.copyright.com/>. Permission to photocopy portions of any individual standard for educational classroom use can also be obtained through the Copyright Clearance Center.

Updating of IEEE Standards documents

Users of IEEE Standards documents should be aware that these documents may be superseded at any time by the issuance of new editions or may be amended from time to time through the issuance of amendments, corrigenda, or errata. An official IEEE document at any point in time consists of the current edition of the document together with any amendments, corrigenda, or errata then in effect.

Every IEEE standard is subjected to review at least every 10 years. When a document is more than 10 years old and has not undergone a revision process, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE standard.

In order to determine whether a given document is the current edition and whether it has been amended through the issuance of amendments, corrigenda, or errata, visit [IEEE Xplore](#) or [contact IEEE](#).³ For more information about the IEEE SA or IEEE's standards development process, visit the IEEE SA Website.

Errata

Errata, if any, for all IEEE standards can be accessed on the [IEEE SA Website](#).⁴ Search for standard number and year of approval to access the web page of the published standard. Errata links are located under the Additional

³ Available at: <https://ieeexplore.ieee.org/browse/standards/collection/ieee>.

⁴ Available at: <https://standards.ieee.org/standard/index.html>.

Resources Details section. Errata are also available in [IEEE Xplore](#). Users are encouraged to periodically check for errata.

Patents

IEEE standards are developed in compliance with the [IEEE SA Patent Policy](#).⁵

Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken by the IEEE with respect to the existence or validity of any patent rights in connection therewith. If a patent holder or patent applicant has filed a statement of assurance via an Accepted Letter of Assurance, then the statement is listed on the IEEE SA Website at <https://standards.ieee.org/about/sasb/patcom/patents.html>. Letters of Assurance may indicate whether the Submitter is willing or unwilling to grant licenses under patent rights without compensation or under reasonable rates, with reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to obtain such licenses.

Essential Patent Claims may exist for which a Letter of Assurance has not been received. The IEEE is not responsible for identifying Essential Patent Claims for which a license may be required, for conducting inquiries into the legal validity or scope of Patents Claims, or determining whether any licensing terms or conditions provided in connection with submission of a Letter of Assurance, if any, or in any licensing agreements are reasonable or non-discriminatory. Users of this standard are expressly advised that determination of the validity of any patent rights, and the risk of infringement of such rights, is entirely their own responsibility. Further information may be obtained from the IEEE Standards Association.

IMPORTANT NOTICE

Technologies, application of technologies, and recommended procedures in various industries evolve over time. The IEEE standards development process allows participants to review developments in industries, technologies, and practices, and to determine what, if any, updates should be made to the IEEE standard. During this evolution, the technologies and recommendations in IEEE standards may be implemented in ways not foreseen during the standard's development. IEEE standards development activities consider research and information presented to the standards development group in developing any safety recommendations. Other information about safety practices, changes in technology or technology implementation, or impact by peripheral systems also may be pertinent to safety considerations during implementation of the standard. Implementers and users of IEEE Standards documents are responsible for determining and complying with all appropriate safety, security, environmental, health, data privacy, and interference protection practices and all applicable laws and regulations.

Acknowledgements

Dedicated to the memory of our friend and colleague, Michael “Mischa” Steurer.

Michael “Mischa” Steurer, founding Chair of IEEE P2004 and Senior Research Faculty at Florida State University's Center for Advanced Power Systems, passed away in August 2023. Mischa led the IEEE P2004 Working Group, pioneering Hardware-in-the-Loop (HIL) simulation and interfacing techniques for real-time systems. His advising skills, mentoring, and positive attitude inspired many in academia and industry. Mischa's contributions leave a lasting legacy for future research and standards development.

⁵ Available at: <https://standards.ieee.org/about/sasb/patcom/materials.html>.

Participants

At the time this recommended practice was completed, the P2004 Working Group had the following membership:

Georg Lauss, *Chair*
Blake Lundstrom, *Vice Chair*

Charles Adewole	Krishnanjan Gubba	Juan Montoya
Mohammad Meraj Alam	Ravikumar	Ramin Mirzahosseini
John Amy	Nikos Hatziaargyriou	Dean Ouellette
Amjad Anvari-Moghaddam	Qiteng Hong	Gernot Pammer
Beat Arnet	Babak Hosseini	Mahendra Patel
Andrea Benigni	Victor Huang	Jean-Nicolas Paquin
Jordan Bell	Ruben Inzunza	Andrey Popov
Jean Bélanger	Christian Jegues	Frank Puschmann
Ron Brandl	Kyle Jennett	Athula Rajapakse
Geraint Chaffey	Steven A. Johnston	Matthew Reno
Ritwik Chowdhury	Shahab Karrari	Nicole Rexwinkel
Frederic Colas	Mohammed Masum	Bruce Rigby
Masoud Davari	Siraj Khan	Paul Roege
Giovanni De Carne	Axel Kiffe	Marina Sanz
Angel de Castro	Christoph Klie	Christian Schegan
Erik de Jong	Panos Kotsampopoulos	Karl Schoder
Ali Dehkordi	Jeykishan Kumar	Deda Seliman
Lalitha Devarakonda	James Langston	Ajinkya Sinkar
Matthias Deter	Jesse Leonhard	Srdjan Srdic
Christian Dufour	Wei Li	Mischa Steurer
Ewane Etinge	Yuan Liao	Thomas I. Strasser
Omar Faruque	Philippe Le-Huy	Kai Strunz
Aaron Findley	Rick Loenders	Olivier Trembley
Dale Finney	Deepak Maragal	Carlos Villegas
Normann Fischer	Richard Meeker Jr.	Jose Vivas
Giambattista Gruosso	Sakis Meliopoulos	Donald Ware
Francois Guay	Ismael Mendoza	James van de Ligt
Efren Guillo-Sansano	Fazel Mohammadi	Jaya Yellajosula
Dinesh Gurusinghe	Antonello Monti	Amin Zamini

The following members of the individual Standards Association balloting group voted on this recommended practice. Balloters may have voted for approval, disapproval, or abstention.

S. M. Alam	Fredric Friend	Mohammed Masum
Mihaela Albu	Jean-Sebastien Gagnon	Siraj Khan
John Amy	Kamal Garg	Yuri Khersonsky
Paul Barnhart	Dinesh Gurusinghe	Christoph Klie
Michael Basler	Randy Hamilton	Theo Laughner
Steven Bezner	Michael Higginson	Georg Lauss
Jens Boemer	Werner Hoelzl	Blake Lundstrom
Ron Brandl	Anderson Hoke	Jeffrey McElray
Paul Cardinal	Ali Hooshyar	Richard Meeker Jr.
Suresh Channarasappa	Yi Hu	Rishi Menon
Cheng-Jen Chen	Victor Huang	Paul Myrda
Ritwik Chowdhury	Richard Hunt	Nayeem Ninad
Ratan Das	Richard Jackson	Dean Ouellette
Donald Dunn	Anthony Johnson	Sivaraman P.
Christian Eder	Brian Johnson	Jan Paramalingam
Carl Fredericks	Geza Joos	Bansi Patel

Manish Patel
Radu Porumb
Mohammad Mohsen
Rahimian
Farnoosh Rahmatian
James Reilly

Matthew Reno
Ryandi Ryandi
Jesus Sanchez-
Rodriguez
Karl Schoder
Mark Siira
Wayne Stec

Michael Steurer
Thomas Strasser
Michael Thompson
John Vergis
Quintin Verzosa
Mina Yousef

When the IEEE SA Standards Board approved this recommended practice on 12 February 2025, it had the following membership:

Lei Wang, *Chair*
Vacant Position, *Vice Chair*
David J. Law, *Past Chair*
Alpesh Shah, *Secretary*

Edward Au
Ted Burse
Xiaofeng (Alfred) Chen
Doug Edwards
Nehad El-Sherif
J. Travis Griffith
Deborah R. Hagar
Guido R. Hiertz

Ronald W. Hotchkiss
Tyler L. Jaynes
Thomas Koshy
Howard Li
Xiaohui Liu
Kevin W. Lu
Hiroshi Mano

Daleep C. Mohla
Annette D. Reilly
Robby Robson
Jon Walter Rosdahl
Daniel Sabin
F. Keith Waters
Sha Wei
Luyang (Eric) Zhang

Introduction

This introduction is not part of IEEE Std 2004-2025, IEEE Recommended Practice for Hardware-in-the-Loop (HIL) Simulation-Based Testing of Electric Power Apparatus and Controls.

Digital real-time hardware-in-the-loop (HIL) simulation came of age in the 1990s and has rapidly accelerated in use to become a very widely used tool across many industries and fields of research. A substantial body of literature documenting advancements in HIL simulation technology and its many applications has existed for some time; however, a comprehensive recommended practice or standard with a common set of definitions, recommendations, and best practices for the general application of HIL simulation has long been missing. Seeing this need, work on this recommended practice was begun in 2017 when a large group of HIL practitioners, researchers, and vendors from across the world, representing many industries and fields of application, was recruited to help realize the vision for a first comprehensive recommended practice on HIL simulation. This recommended practice considers HIL simulation in which a closed loop between software models and hardware of interest is formed and simulations are executed in real-time. Software-only simulation, co-simulation, playback systems, open-loop testing, and other configurations not meeting this definition are not explicitly considered, though many sections of this recommended practice may still be useful.

This recommended practice is intended for use by HIL practitioners, researchers, and vendors across most industries or fields of application and at any level of experience with HIL simulation. The normative body of the document is structured with definitions ([Clause 3](#)) and overview ([Clause 4](#)) first, a description of the key characteristics of real-time models and simulation, along with recommendations on how to apply them in an HIL simulation application ([Clause 5](#)) next, followed by best practices and recommendations on how to establish ([Clause 6](#)) and execute ([Clause 7](#)) a successful HIL simulation. The informative annexes of the document provide many example applications of controller HIL (CHIL) simulation ([Annex B](#)) and power HIL (PHIL) simulation ([Annex H](#)) and a deep dive on important topics such as circuit decoupling techniques, accuracy, stability, HIL interfaces, power amplifiers, and power HIL protection techniques. Considerable references to relevant standards and guides, as well as key technical literature on HIL simulation, are provided throughout for readers wanting to learn more.

HIL simulation has become an important tool not only for industry studies and research, but also in the application of other IEEE standards. For example, in IEEE Std 1547.1™-2020 [[B49](#)], HIL simulation is identified as an important approach for verifying conformance of distributed energy resources (DERs) to IEEE Std 1547™.⁶ Also, IEEE P2800.2 describes the applicability of HIL simulation approaches for evaluating conformance of IBRs to IEEE Std 2800™-2022. This recommended practice provides valuable guidance in applying HIL simulation to these and other example applications.

⁶ The numbers in brackets correspond to those of the bibliography in [Annex J](#).

Contents

1. Overview	15
1.1 Scope	15
1.2 Word usage	15
2. Normative references	16
3. Definitions, acronyms, and abbreviations	16
3.1 Definitions	16
3.2 Acronyms and abbreviations	23
4. Overview of HIL simulation	25
4.1 General	25
4.2 Purpose of HIL simulation	25
4.3 CHIL Simulation versus PHIL simulation	26
4.4 HIL simulation architecture and principal setup	26
4.5 HIL simulation components	26
5. Real-time (RT) simulation	29
5.1 Overview	29
5.2 Key characteristics of RT simulation	29
5.3 Modeling techniques and simulation setup guidelines	30
6. Establishing an HIL simulation	32
6.1 Overview	32
6.2 Common aspects of establishing a HIL simulation	33
6.3 Specific aspects unique to CHIL	34
6.4 Specific aspects unique to PHIL	37
7. Executing an HIL simulation	39
7.1 Overview	39
7.2 CHIL execution procedure	39
7.3 PHIL execution procedure	40
Annex A (informative) RT simulation	42
Annex B (informative) Applications for CHIL simulation	59
Annex C (informative) PHIL interfaces	88
Annex D (informative) Metrics for accuracy and sensitivity of PHIL simulation	92
Annex E (informative) Stability assessment of PHIL simulation	100
Annex F (informative) Power amplifiers	102
Annex G (informative) Approaches for protection of PHIL simulation experiments	112
Annex H (informative) Applications for PHIL simulation	115
Annex I (informative) Letter symbols	130
Annex J (informative) Bibliography	137

List of Figures

Figure 1—Generalized CHIL simulation setup	17
Figure 2—Generalized PHIL simulation setup.....	19
Figure 3—Generic implementation of a PHIL interface.....	20
Figure 4—Multiple-input multiple-output (MIMO) PHIL experiment	21
Figure 5—Generalized system of interest (SOI) for (a) CHIL simulation and (b) PHIL simulation	22
Figure 6—Block diagram of HIL simulation system.....	28
Figure 7—Interconnection between EMT simulation and TS analysis.....	30
Figure 8—Model of the generalized CHIL simulation system	35
Figure 9—CHIL simulation without signal amplification in the interface.....	36
Figure 10—HIL simulation with signal amplification in the interface.....	36
Figure 11—PHIL system with voltage-type (VT) ideal transformer method (ITM) as applied PHIL interface coupling method (PHIL CM) and PHIL coupling algorithm (PHIL CA)	37
Figure A.1—Timing diagram of RT transmission path.....	45
Figure A.2—Co-simulation of multiple RTS platforms (type 1)	58
Figure A.3—Use case of a co-simulation RTS platform.....	58
Figure B.1—Analog and digital exchange with HOI (conventional approach).....	60
Figure B.2—Analog and digital exchange with HOI (IEC 61850 approach)	61
Figure B.3—Synchronous machine model and connection to generator relay as the HOI	69
Figure B.4—Synchronous machine control signals	73
Figure B.5—Protection performance for a ground fault at the generator terminal	75
Figure B.6—Protection performance for a ground fault near the generator neutral.....	76
Figure B.7—Protection performance for a turn-to-turn fault that shorts 10% of an A-phase branch.....	77
Figure B.8—Protection performance for a BC fault near the generator neutral.....	78
Figure B.9—Protection performance for an A-phase series fault	79
Figure B.10—Mho characteristics with the impedance trajectory.....	80
Figure B.11—Performance of loss of field protection elements on a field winding ground fault.....	81
Figure B.12—Stator voltages and currents (loss of prime mover).....	81
Figure B.13—Mho characteristics with two blinders and the impedance trajectory	82

Figure B.14—Single-pole-open on the GSU high-voltage (HV) terminals results in excessive unbalanced currents	83
Figure B.15—Accidental energization via closure of generator breaker	84
Figure B.16—Breaker failure element correctly detects the failure of a breaker to trip	85
Figure B.17—A-phase flashover of the GSU high-voltage breaker	86
Figure B.18—Backup distance protection for an uncleared phase fault at the generator terminals	87
Figure C.1—Architecture for linear IAs ELA	89
Figure D.1—Example system of interest	95
Figure D.2—PHIL System illustrating apparent impedance of MOI and HOI	96
Figure D.3—Systems with apparent impedance for MOI and HOI	96
Figure F.1—Simplified model of PHIL simulation system	103
Figure F.2—PHIL simulation requirements for a maximum system bandwidth of 2 kHz	105
Figure F.3—The use of MG set as a power amplifier for establishing a PHIL setup	106
Figure F.4—Example of using IEEE type 1 excitation system for voltage magnitude tracking	106
Figure F.5—Block diagram of an MG set's frequency behavior	107
Figure F.6—Frequency tracking performance of an MG set purely relying on its proprietary controller	108
Figure F.7—Overview of control structure to enable frequency and phase tracking	108
Figure F.8—Frequency tracking performance comparison with and without augmented frequency control loop	110
Figure F.9—Phase tracking performance comparison with and without augmented phase control loop	111
Figure H.1—SOI for single-component HIL	115
Figure H.2—Basic structure of systems and interface of PHIL simulation	116
Figure H.3—PHIL simulation implementation for single component PHIL	117
Figure H.4—Linear representation of single component HIL	118
Figure H.5—Block diagram for linear representation of PHIL simulation experiment	118
Figure H.6—Transfer function magnitude error for case 1 of example illustrating influence of damping impedance on accuracy with DIM IA	123
Figure H.7—Transfer function magnitude error for case 2 of example illustrating influence of damping impedance on accuracy with DIM IA	123
Figure H.8—Comparison of time-domain waveforms for 50 Hz source excitation for example illustrating influence of damping impedance on accuracy with DIM IA	124

Figure H.9—Comparison of time-domain waveforms for 200 Hz source excitation for example, illustrating influence of damping impedance on accuracy with DIM IA.....	124
Figure H.10—Transfer functions from voltage sensor disturbance for case 1 of example illustrating influence of PHIL-IA on sensitivity to disturbances.....	126
Figure H.11—Transfer functions from voltage sensor disturbance for case 2 of example illustrating influence of PHIL-IA on sensitivity to disturbances.....	127
Figure H.12—Comparison of voltages V_H for example illustrating influence of IA on sensitivity to disturbances	128
Figure H.13—Comparison of currents I_D for example illustrating influence of IA on sensitivity to disturbances	128

List of Tables

Table B.1—Signals exchange (RTS and HOI).....	59
Table C.1—Strengths and weaknesses of PHIL IAs.....	88
Table C.2—Ideal ELA gains and stimulus impedance values for common PHIL-IAs.....	91
Table D.1—Comparison of the two main HIL experiment accuracy estimation approaches.....	92
Table F.1—Comparison of CPU and FPGA based HIL simulation	104
Table H.1—Parameter for PHIL simulation with single-component HOI.....	121
Table H.2—Parameter value deviations for example illustrating influence of damping impedance on accuracy with DIM IA (case 1)	122
Table H.3—Parameter value deviations for example illustrating influence of damping impedance on accuracy with DIM IA (case 2)	122
Table H.4—Parameter value deviations for example, illustrating influence of IA on sensitivity to disturbances (case 1)	125
Table H.5—Parameter value deviations for example illustrating influence of IA on sensitivity to disturbances (case 2)	125

IEEE Recommended Practice for Hardware-in-the-Loop (HIL) Simulation-Based Testing of Electric Power Apparatus and Controls

1. Overview

1.1 Scope

This recommended practice provides established practices for the use of the method of hardware-in-the-loop (HIL) simulation-based testing of electric power apparatus and controls. It is intended to be generically applicable in synergy (in conjunction) with any specific testing standard (if applicable).

1.2 Word usage

The word *shall* indicates mandatory requirements strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*).^{7,8}

The word *should* indicates that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required (*should* equals *is recommended that*).

The word *may* is used to indicate a course of action permissible within the limits of the standard (*may* equals *is permitted to*).

The word *can* is used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

⁷ The use of the word *must* is deprecated and cannot be used when stating mandatory requirements; *must* is used only to describe unavoidable situations.

⁸ The use of *will* is deprecated and cannot be used when stating mandatory requirements; *will* is only used in statements of fact.

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

DIN/VDE 0105-100, Operation of electrical installations—Part 100: General requirements.

EN 50110-1, Operation of electrical installations—Part 1: General requirements.⁹

EN 61140, Protection against electric shock—Common aspects for installation and equipment.

IEC 60364-4-41, Protection for safety—Protection against electric shock.¹⁰

IEEE Std C37.115™-2003, IEEE Standard Test Method for Use in the Evaluation of Message Communications Between Intelligent Electronic Devices in an Integrated Substation Protection, Control and Data Acquisition System.^{11,12,13}

3. Definitions, acronyms, and abbreviations

3.1 Definitions

For the purposes of this document, the following terms and definitions apply. Further information on letter symbols can be found in [Annex I](#). The *IEEE Standards Dictionary Online* should be consulted for terms not defined in this clause.¹⁴

CHIL amplifier (CA): The components in a CHIL interface that transform quantities computed in the real-time simulator (RTS) into physical quantities provided to the hardware of interest (HOI). Not all CHIL interfaces require a CHIL amplifier (CA).

NOTE—Fiber optic links and binary input/output (I/O) over copper perform no amplification of physical quantities.

CHIL interface: The hardware-in-the-loop (HIL) interface used in controller HIL (CHIL) simulation systems. A CHIL interface does not intend to achieve natural coupling.

CHIL interface in hardware: The hardware portion of a CHIL interface.

CHIL interface in software: The software portion of a CHIL interface.

⁹ EN publications are available from the European Committee for Standardization (CEN) (<https://www.cen.eu/>).

¹⁰ IEC publications are available from the International Electrotechnical Commission (<https://www.iec.ch>) and the American National Standards Institute (<https://www.ansi.org/>).

¹¹ The IEEE standards or products referred to in Clause 2 are trademarks owned by The Institute of Electrical and Electronics Engineers, Incorporated.

¹² IEEE publications are available from The Institute of Electrical and Electronics Engineers (<https://standards.ieee.org/>).

¹³ IEEE Std C37.115™-2003 has been withdrawn; however, copies can be obtained from The Institute of Electrical and Electronics Engineers (<https://standards.ieee.org/>).

¹⁴ *IEEE Standards Dictionary Online* is available at: <http://dictionary.ieee.org>. An IEEE account is required for access to the dictionary, and one can be created at no charge on the dictionary sign-in page.

controller HIL (CHIL): Hardware-in-the-loop (HIL) where one or more hardware of interest (HOI) are interfaced at the signal level to a model of interest (MOI) where natural coupling is not intended to be preserved. A generalized controller HIL (CHIL) setup is shown in Figure 1.

NOTE—The delineation between CHIL and PHIL is that PHIL attempts to preserve natural coupling across the HIL interface whereas CHIL does not.¹⁵

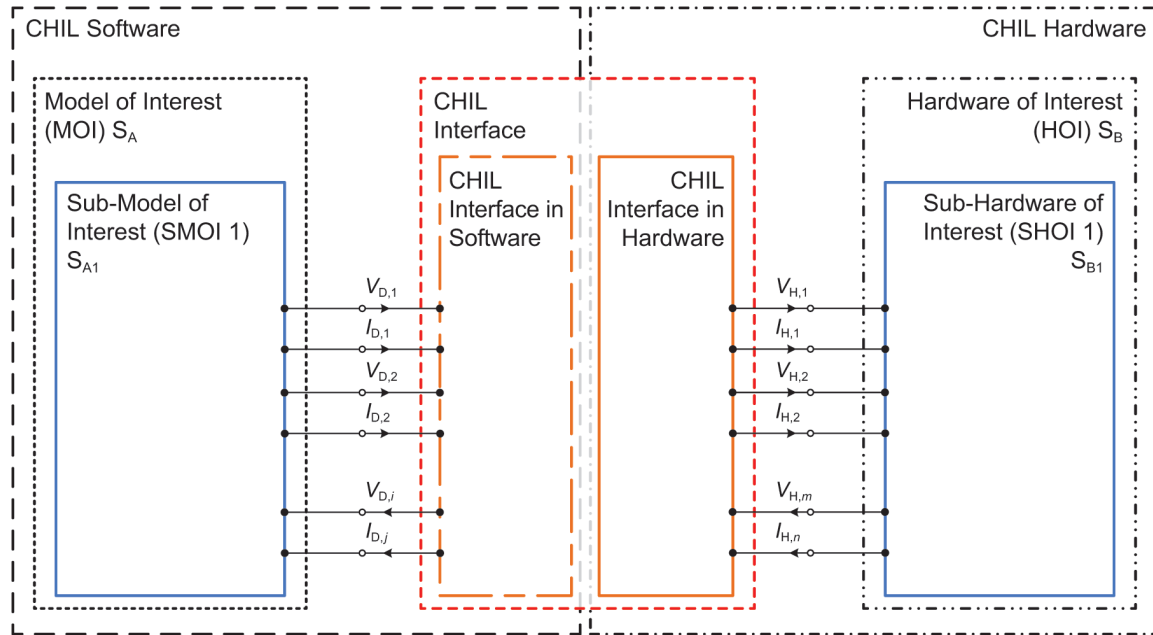


Figure 1—Generalized CHIL simulation setup

hardware of interest (HOI): The portion of the system of interest (SOI) existing in hardware and interacting with the model of interest (MOI) through HIL interfaces. The hardware of interest (HOI) always includes physical hardware (software-in-the-loop and other software-only simulations are outside of the scope of IEEE Std 2004™), but frequently that physical hardware also includes software that is essential and integral to the operation of the HOI that is evaluated during an HIL simulation. A HOI may be composed of multiple sub-hardware of interest (sub-HOIs).

NOTE—Alternatively, the terms hardware under test, device under test, equipment under test, hardware component under test, object under investigation, or power hardware are used in literature.

hardware-in-the-loop (HIL): A technique that allows closed-loop interaction between a hardware of interest (HOI) and a model of interest (MOI) using a real-time simulator (RTS).

NOTE—Closed-loop interaction means that both the HOI and the MOI have to exhibit responses to stimuli.

HIL interface: The interconnection facilitating the interaction between a model of interest (MOI) and a hardware of interest (HOI) in a hardware-in-the-loop (HIL) setup.

¹⁵ Notes in text, tables, and figures of a standard are given for information only and do not contain requirements needed to implement this standard.

model of interest (MOI): The portion of the system of interest (SOI) modeled and instantiated on a real-time simulator (RTS) and interacting with the hardware of interest (HOI) through HIL interfaces. A MOI may be composed of multiple sub-MOIs.

NOTE—The PHIL coupling structure (PHIL-CS) may contain a portion of the MOI which is therefore not represented in the MOI instantiation on the RTS.

natural coupling: The conservation of the through and across quantities at PHIL interfaces such that instantaneous power is conserved across the interface and the hardware of interest (HOI) is naturally (i.e., without additional scaling, conversion, etc.) coupled to the model of interest (MOI) (see [Figure 5b](#)). That is, with natural coupling, through quantities, across quantities, and instantaneous power on the hardware side of the PHIL interface, which is connected to the power interface of the hardware of interest (HOI), will “naturally” match those on the software side of the PHIL interface, which is interfaced to the model of interest (MOI) or sub-MOI (see [Figure 2](#)).

NOTE—Examples of through and across quantities are current and voltage, respectively, in electrical systems; velocity (angular velocity) and force (torque), respectively, in mechanical systems; and heat flux and temperature, respectively, in thermal systems.

PHIL amplifier: The ensemble of components in a PHIL interface which transforms the reference stimuli determined by the PHIL interface control (PHIL-IC) in the real-time simulator (RTS) into physical stimuli applied to the hardware of interest (HOI), forming part of the natural coupling between the hardware of interest (HOI) and the model of interest (MOI).

NOTE 1—All PHIL interfaces require a PHIL amplifier; the PHIL amplifier is always part of the PHIL interface in hardware.

NOTE 2—A PHIL amplifier may be required to absorb power.

NOTE 3—In electrical PHIL interfaces, the PHIL amplifier produces voltage and current. In mechanical PHIL interfaces, the PHIL amplifier produces forces (torque) and velocity (angular velocity). In thermal PHIL interfaces, the PHIL amplifier produces temperature and heat flux.

PHIL coupling algorithm (PHIL-CA): The set of equations used to generate the references for the PHIL coupling structure (PHIL-CS) from the measured quantities (see [Figure 3](#)).

NOTE—Examples of the PHIL coupling structure (PHIL-CS) reference include references for the stimuli (e.g., through and/or across variables) as well as impedances (or their mechanical and thermal equivalents).

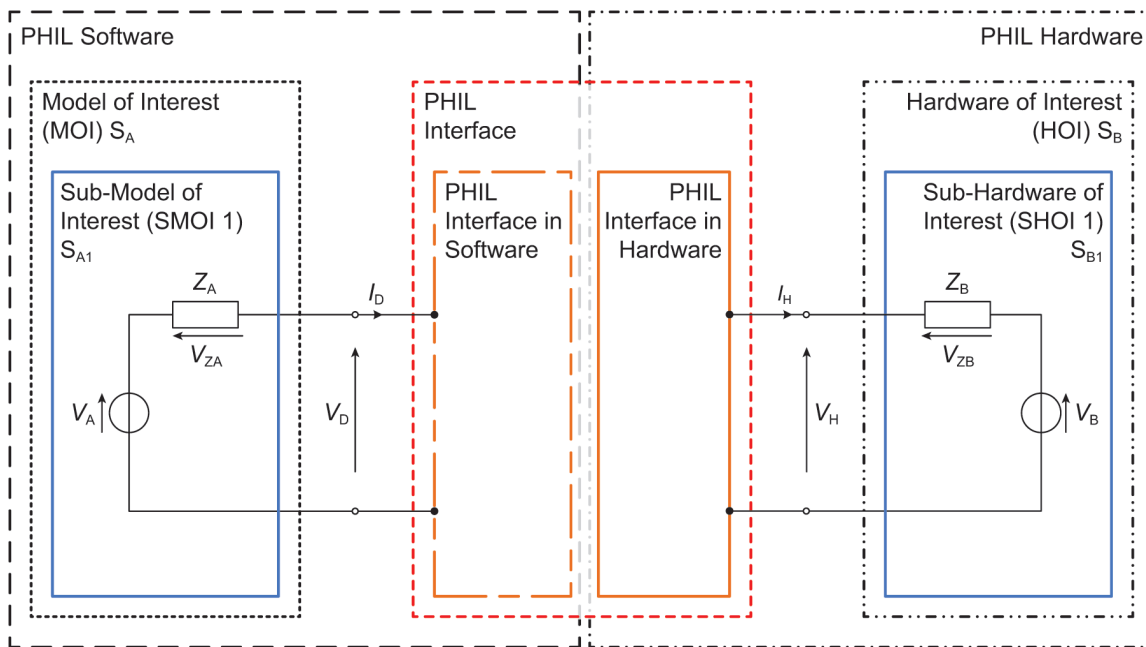


Figure 2—Generalized PHIL simulation setup

PHIL coupling structure (PHIL-CS): A selection of the circuit models within the PHIL interface, one at the model of interest (MOI) side (i.e., the PHIL interface in software) and one at the hardware of interest (HOI) side (i.e., the PHIL interface in hardware), that are used to couple the model of interest (MOI) to the hardware of interest (HOI). These models each include a selection of one or more stimuli sources and/or impedances, including associated names, measurement points, and the topology of how these circuit components and measurement points are connected (see [Figure 3](#)).

NOTE 1—Stimuli in this context refer to through and/or across quantities.

NOTE 2—The PHIL coupling structure (PHIL-CS) specifically does not include the PHIL amplifier characteristics.

PHIL hardware: The ensemble of hardware of interest (HOI), PHIL interface in hardware, protection devices, and other physical hardware employed as part of a power hardware-in-the-loop (PHIL) simulation.

PHIL interface: The HIL interface used in power hardware-in-the-loop (PHIL) simulation (see [Figure 3](#)). A PHIL interface intends to achieve natural coupling.

NOTE 1—Occasionally, the term power interface is used in literature.

NOTE 2—Multiple PHIL interfaces may exist within a single PHIL simulation.

NOTE 3—A PHIL interface may include application of constant scaling factors to through and/or across quantities resulting in a constant scaling of instantaneous power.

NOTE 4—A PHIL interface may represent a portion of the SOI (e.g., linking impedance) which is not explicitly represented in the MOI nor the HOI.

PHIL interface approach (PHIL-IA): The functional combination of compatible PHIL coupling algorithm (PHIL-CA) and PHIL coupling structure (PHIL-CS) (see Figure 3). Examples are shown in Annex C and Annex D.

NOTE—In literature this may sometimes be referred to as PHIL interface algorithm.

PHIL interface control (PHIL-IC): The implementation of the PHIL coupling algorithm (PHIL-CA) and any additional gains, filters, compensators, and so forth to implement the PHIL interface with the aim of achieving natural coupling (see Figure 3).

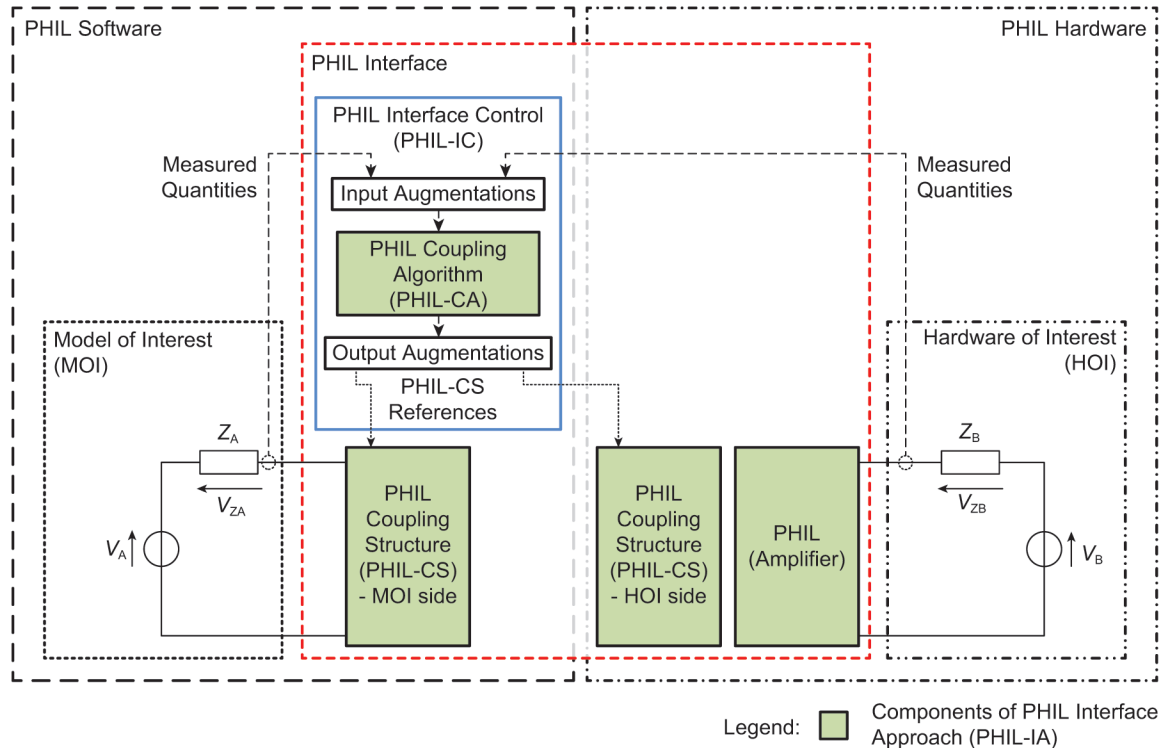


Figure 3—Generic implementation of a PHIL interface

PHIL interface in hardware: The hardware portion of a PHIL interface.

NOTE—It includes the PHIL amplifier, sensors, I/O modules, or filters.

PHIL interface in software: The software portion of a PHIL interface.

NOTE—It includes the instantiation of the software portions of the PHIL interface control (PHIL-IC), signal processing, or others.

PHIL software: The ensemble of model of interest (MOI), PHIL interface in software, and other implemented software employed as part of a power hardware-in-the-loop (PHIL) simulation.

power HIL (PHIL): Hardware-in-the-loop (HIL) simulation where the hardware of interest (HOI) interacts with the model of interest (MOI) while the natural coupling at the power interfaces that exists in the system of interest (SOI) is intended to be preserved. The generalized system description of a power hardware-in-the-loop (PHIL) setup is shown in Figure 2.

real-time (RT): The progression of time in the real world.

RT simulation: A computer simulation executed in synchronism with real-time (RT).

NOTE—Alternatively, the term emulation is used in literature and often described as such: Emulation is the process of imitating the behavior of one or several hardware pieces with another hardware piece, and a model that accepts the same inputs and produces the same outputs as a given system. It is the process of mimicking the outwardly observable behavior to match an existing target. The internal state of the emulation mechanism does not have to accurately reflect the internal state of the target which it is emulating.

RT simulator (RTS): A computer, processing device, or computer cluster (i.e., interlinked computers) executing RT simulations.

NOTE—Alternatively, the terms digital RTS (DRTS), real-time target (RTT), and real-time machine (RTM) are used in literature.

sub-HOI (SHOI): The functional decomposition of the hardware of interest (HOI) where interactions between sub-hardware of interest (sub-HOI) only exist via HIL interfaces and the model of interest (MOI) (see Figure 4).

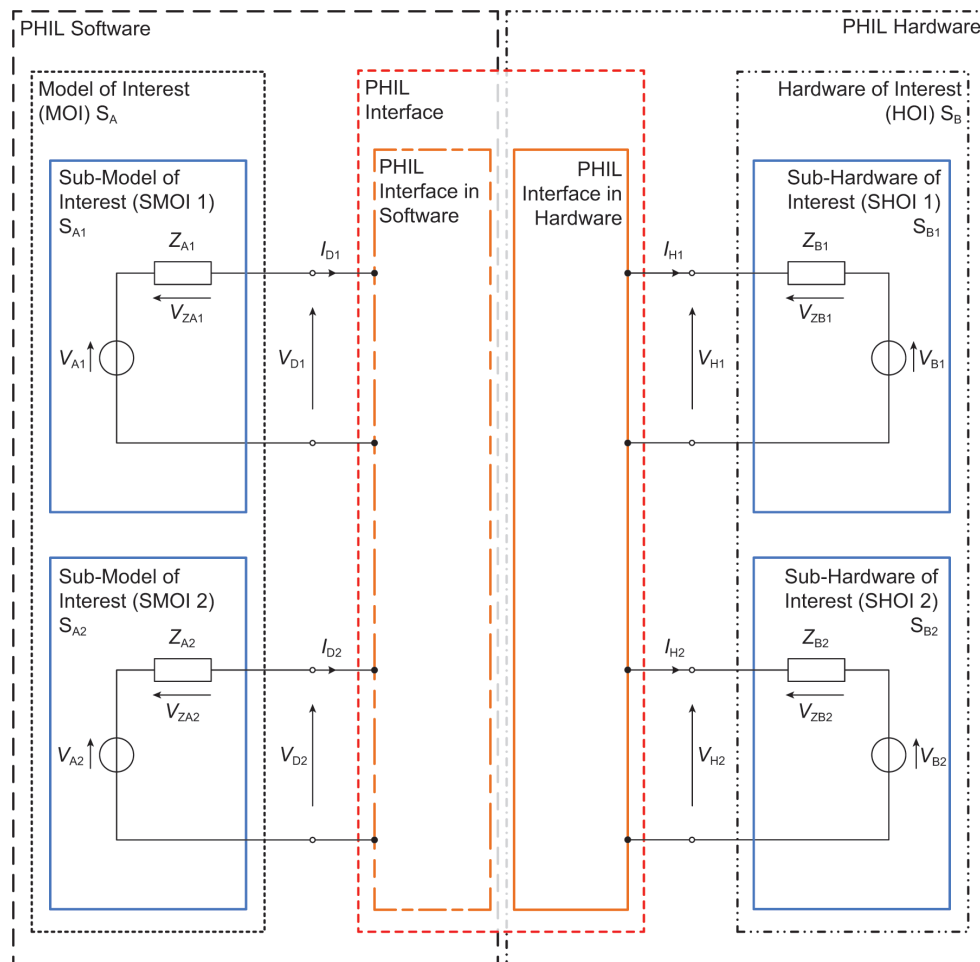


Figure 4—Multiple-input multiple-output (MIMO) PHIL experiment

sub-MOI (SMOI): The functional decomposition of the model of interest (MOI) where interactions between sub-model of interest (sub-MOI) only exist via HIL interfaces and the hardware of interest (HOI) (see Figure 4).

NOTE—Multiple-input multiple-output (MIMO) PHIL experiments involve more than a single HOI and a single MOI. In Figure 4, two sub-HOIs and two sub-MOIs are present, resulting in a MIMO case. This case is not the same as two independent single-input single-output (SISO) cases because each sub-MOI interacts with both sub-HOI.

system of interest (SOI): The complete real-world system decomposed into hardware of interest (HOI) and model of interest (MOI) and is analyzed via hardware-in-the-loop (HIL). The generalized system of interest (SOI) for controller hardware-in-the-loop (CHIL) and power hardware-in-the-loop (PHIL) simulation is shown in Figure 5.

NOTE—As the dual to Thévenin's theorem, the Norton's theorem may also be applied for the generalized SOI in Figure 5b.

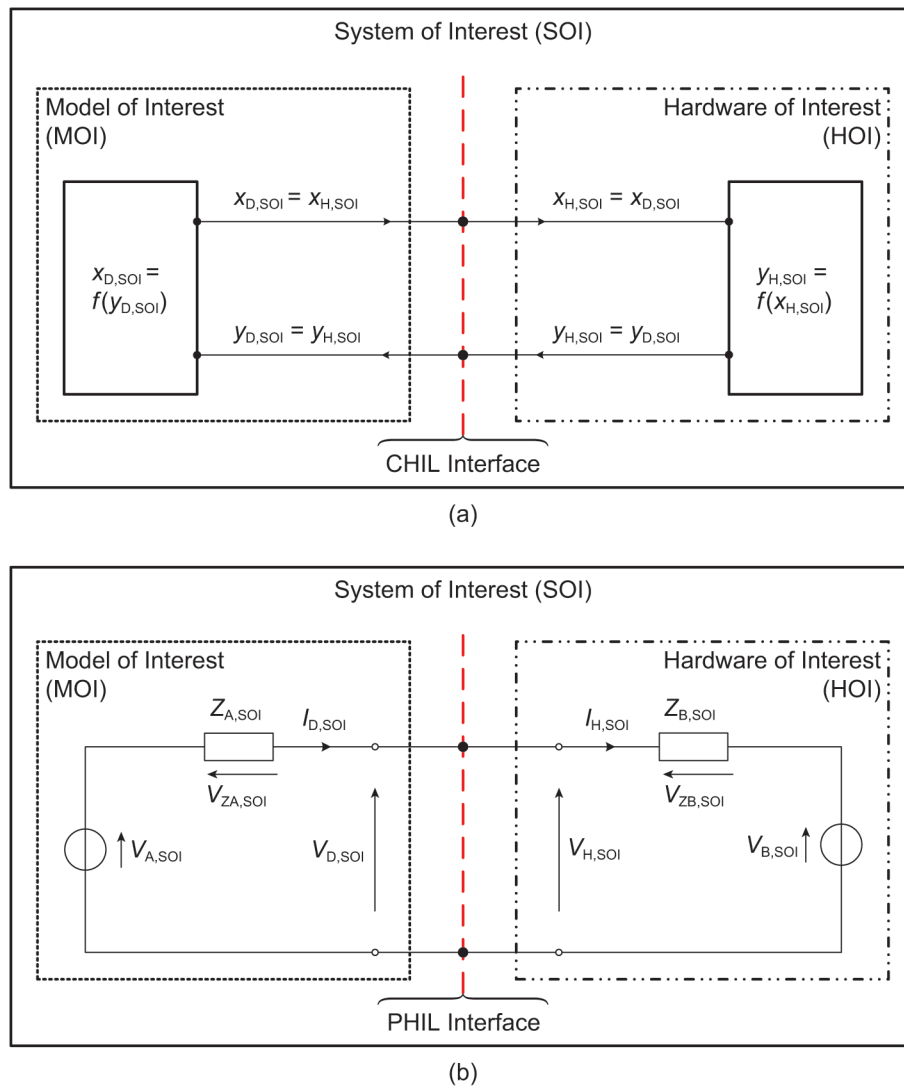


**Figure 5—Generalized system of interest (SOI) for
(a) CHIL simulation and (b) PHIL simulation**

3.2 Acronyms and abbreviations

ac	alternating current
A/D	analog-to-digital
ADC	analog-to-digital converter
ATL	artificial transmission line
AVR	automatic voltage regulator
CB	circuit breaker
CCVT	coupling capacitor voltage transformer
CHIL	controller hardware-in-the-loop
CPU	central processing unit
CSV	comma-separated values
CT	current-type
D/A	digital-to-analog
DAC	digital-to-analog converter
dc	direct current
DIM	damping impedance method
E-stops	emergency stops
ELA	extended Lawrence architecture
EMI	electromagnetic interference
EMT	electromagnetic transient
FPGA	field-programmable gate array
fps	frames per second
GCS	generation control system
GENE	generation of electric network equivalents
GNSS	global navigation satellite system
GOOSE	generic object-oriented substation events
GPS	global positioning system
GSU	generator step-up
HIL	hardware-in-the-loop
HOI	hardware of interest
HV	high-voltage
HVDC	high-voltage direct current
IA	interface approach
IBR	inverter-based renewable
IED	intelligent electronic device
I/O	input/output

IRIG-B	inter-range instrumentation group – time code format B
ITM	ideal transformer model
LV	low-voltage
MG	motor-driven synchronous generator
MIMO	multiple-input multiple-output
MMC	modular multilevel converter
MOI	model of interest
MOV	metal oxide varistor
MRP	multi-rate partitioning
MVDC	medium-voltage direct current
NIC	network interface card
OEL	over-excitation limiter
PCD	partial circuit duplication
PDC	phasor data concentrator
PH	power hardware
PHIL	power hardware-in-the-loop
PHIL-CA	power hardware-in-the-loop coupling algorithm
PHIL-CS	power hardware-in-the-loop coupling structure
PHIL-IA	power hardware-in-the-loop interface approach
PHIL-IC	power hardware-in-the-loop interface control
PI	proportional-integral
PID	proportional-integral-differential
PMU	phasor measurement unit
PSS	power system stabilizer
pu	per unit
PWM	pulse-width modulation
rms	root mean square
ROCOF	rate of change of frequency
RT	real-time
RTM	real-time machine
RTP	real-time processing core
RTS	real-time simulator
RTT	real-time target
SCADA	supervisory control and data acquisition
SECHL	stator end-core heating limit
SFA	shifted frequency analysis

SHOI	sub-hardware of interest
SISO	single-input single-output
SMOI	sub-model of interest
SND	spectral nested dissection
SOI	system of interest
SSN	state-space nodal
SSR	sub-synchronous resonance
STATCOM	static synchronous compensator
SV	sampled value
TCP	transmission control protocol
TF	transfer function
TFA	time-variant first-order approximation
T-Fr	transport frame
THD	total harmonic distortion
TLM	transmission line modeling
TS	transient stability
TSS	test suite specification
TTL	transistor-transistor logic
TVE	total vector error
TWR	traveling wave-based relay
UDP	user datagram protocol
UEL	under-excitation limiter
UTF	unicode transformation format
VT	voltage-type
WAMPAC	wide area monitoring, protection, and control

4. Overview of HIL simulation

4.1 General

HIL simulation is a specific type of system simulation, including controller and/or power hardware. This clause provides an overview of the topic.

4.2 Purpose of HIL simulation

The purpose of HIL simulations is to facilitate the study of closed-loop interactions between components of an SOI without the need to create the entire SOI in the real world. Among other potential uses, employing HIL simulations should be considered as soon as possible in the design cycle of a new SOI or the upgrade of an existing SOI with new components, as soon as such hardware components in the form of a surrogate or functional prototype become available. HIL simulations are not intended to replace testing of the entire SOI unless such testing is not practical due to considerations of cost, risk, schedule, etc.

4.3 CHIL Simulation versus PHIL simulation

The method of CHIL simulation should be used in cases where the HOI in the real world couples to other system components only via signal interfaces (i.e., the interfaces do not achieve natural coupling). The PHIL simulation method should be used in cases where the HOI in the real world couples with the other system components via at least one natural coupling interface. A combination of CHIL and PHIL simulation should be used if the HOI in the real world also exhibits signal interfaces between this HOI and the other system components relevant to the interactions of interest.

4.4 HIL simulation architecture and principal setup

An HIL simulation should consist of at least one HOI in closed-loop interaction with an MOI simulated on an RTS. Before establishing a HIL simulation, the user should decide which part of the system exists as HOI and which part exists as MOI. Such a HIL simulation may represent an entire SOI. The interfaces between the HOI and MOI should be chosen in such a way as to reduce their adverse effects on the anticipated results of the scenarios studied via such a HIL simulation. Since the effects of the interfaces cannot be completely eliminated, those effects should be characterized and documented along with the results obtained from the HIL simulation.

4.5 HIL simulation components

4.5.1 RTS

To perform HIL simulation, the simulated portion of the system (i.e., the MOI) should execute in real time at a simulation time-step size that is adequate for the purpose of the study. All time-dependent variables in the MOI should update in synchronism with the real-world time on an RTS with sufficient accuracy required for the application.¹⁶

4.5.2 HOI

Every HIL simulation should include an HOI, which may comprise multiple sub-HOIs. Any component(s) within the SOI can be the HOI.

4.5.3 Interfaces between HOI and RT simulation

A HIL simulation should include HIL interfaces to couple the physical HOI to the MOI sufficiently. The HIL interface should be chosen according to the interface requirements of the HOI. The RTS interfaces with external components to read inputs to the MOI and update outputs from the MOI to the HOI. Such outputs should be made available to the HOI at the appropriate signal level. Inputs to the RTS at PHIL interfaces should be made available via appropriate sensors and signal scaling. HIL experiments may use multiple interfaces and multiple types of interfaces within a single test as necessary.

The design and analysis of HIL experiments should account for the non-ideal aspects of the HIL interfaces, including time delay, bandwidth limitation, and noise injection, as these non-ideal aspects can affect the accuracy and stability of the HIL simulation.

4.5.3.1 CHIL interface

A CHIL interface should be employed at all interfaces between the MOI and HOI for which natural coupling does not exist (i.e., the HOI receives signals from the RT simulation through one part of the CHIL interface and sends feedback to the RTS through a different part of the CHIL interface).

¹⁶ What level is deemed sufficient can vary some by application, sensor accuracy achievable, etc., but in general instantaneous waveform and steady state error metrics with values of 1% or less are recommended. See [D.2](#) and its references for further explanation and examples.

CHIL interfaces take several distinct forms, listed as follows:

- Wired analog input/output (I/O) signals (e.g., a voltage typically between ± 10 V or a current typically between 4 mA and 20 mA representing a physical quantity).
- Wired digital I/O signals (i.e., transistor-transistor logic (TTL) type transitions representing individual logical low and high signals).
- Digital communication (i.e., transmission and reception of data via digital bit stream or digitized analog signal transmitted over a point-to-point or point-to-multipoint communication channel).

Interfaces should best match the application in the field. Depending on the specific interface and type of RTS, a CHIL interface has various properties (e.g., bandwidth, accuracy, acquisition, and update rate), which impact the accuracy of the signal provided to the HOI and influence the performance of the RT simulation. Therefore, careful consideration should be given to matching interface characteristics.

If required, wired signal levels should be matched between the RTS and the HOI via signal attenuation or amplification. Such amplification should not be confused with power amplification used in PHIL simulation. Corresponding scaling factors to account for those attenuations or amplifications need to be accounted for in the CHIL-IA.

4.5.3.2 PHIL interface

For PHIL experiments, the HOI should be coupled to the MOI through one or more PHIL interfaces intended to achieve natural coupling between the HOI and MOI, similar to that illustrated in [Figure 6](#). Each PHIL interface should instantiate a PHIL-IA, including a PHIL-CS used to apply stimuli to the HOI and MOI, along with a compatible PHIL-CA. Examples of PHIL-IAs are discussed in Annex C.1. References to the PHIL-CS for each power interface should be generated by a PHIL-IC, making use of measured quantities at the MOI and HOI. The PHIL-IC, which is typically implemented on the RTS, implements the PHIL-CA for the interface, and may also include augmentations to the PHIL-CA to improve stability, accuracy, and/or noise rejection characteristics for the PHIL experiment.

PHIL interfaces depend on the physical quantities naturally coupled at the boundary of the HOI in the real world (such as voltage and current, temperature and heat flux, force and velocity, and torque and angular velocity). Appropriate PHIL amplifiers should be used to allow the exchange of instantaneous power at the boundaries of the HOI and the interfacing amplifier. If required, several types of PHIL interfaces may exist in any given PHIL simulation. Most RTSs do not include the PHIL amplifier required for implementing a PHIL interface. PHIL amplifiers should be carefully selected for the purpose of the desired PHIL simulation. Consideration should be given to possible overload conditions often required to achieve natural coupling during transient phenomena of interest. Scaling factors to account for the gain of the PHIL amplifier should be represented in the PHIL-IA. Similarly, scaling factors of the instrumentation of PHIL feedback signals at the boundary of the HOI should also be part of the PHIL-IA.

A PHIL interface imposes inherent limitations on the RT simulation (e.g., bandwidth, resolution/accuracy, voltage rating, current rating, power rating, etc.), which may restrict the application or the phenomena that can be tested in particular applications. It is recommended to utilize the block diagram in [Figure 6](#) for the design and analysis of PHIL experiments to account for the non-ideal characteristics listed as follows:

- Time delays and distortion of reference signals due to limited bandwidth or uncompensated impedance of the physical stimuli.
- Disturbances introduced through noise in the reference signals or other sources (e.g., harmonics from switching amplifiers).
- Delays, signal distortions, and noise introduced by sensors.

- Delays associated with portions of the interface implemented in the RTS, including simulated and physical delays in reading measured quantities and in presenting stimuli to the MOI.

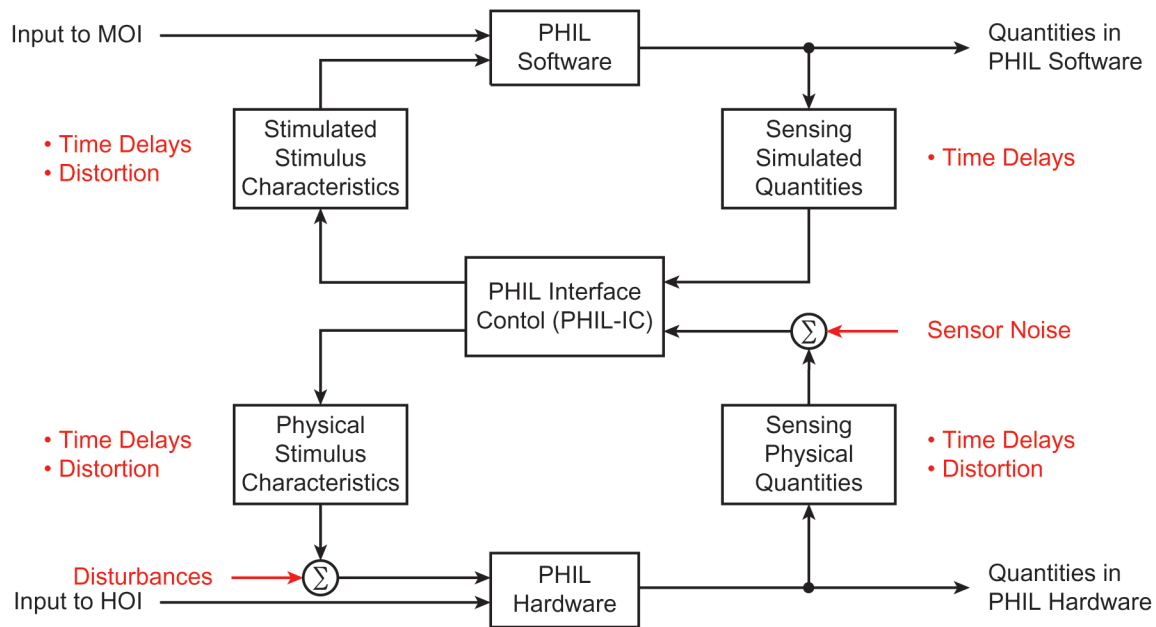


Figure 6—Block diagram of HIL simulation system

4.5.4 Accuracy and stability

The user should help ensure that the MOI accurately represents the corresponding system characteristics, leading to the phenomenon of interest in the SOI. One aspect of HIL simulation accuracy is the preservation of the stability characteristics of the SOI. In particular, instabilities within the SOI should be preserved in the HIL simulation.

Because HIL interfaces can introduce artifacts that adversely affect the accuracy of HIL simulations, the user should properly assess the accuracy of the entire HIL simulation. Therefore, the user should assess the accuracy of the HIL interface by comparing the input and outputs on both sides of the HIL interface. Whenever possible, the user should also assess the accuracy of the entire HIL simulation through comparison of HIL simulation results with observations from the SOI. Methods for analyzing accuracy are provided in [Annex D](#). Specific accuracy levels to be deemed sufficient can vary somewhat by application, achievable sensor accuracy, etc., but in general, instantaneous waveform and steady state error metrics with values of 1% or less are recommended. See [D.2](#) and its references for further explanation and examples.

Characteristics of HIL interfaces can introduce instabilities in the HIL simulation. Therefore, the user should analyze the stability of prospective HIL simulation experiments and, if necessary, take measures to stabilize the system and/or identify regions of operation that should be avoided. Additional accuracy assessments should be applied if any such stabilizing measures are introduced. Implementing protection systems that can shut down the experiment if the onset of unstable operation is detected is also recommended. Methods for analyzing and protecting against instabilities introduced by the PHIL interface are recommended in subsequent clauses.

The design and analysis of HIL experiments should also consider the sensitivity of the experiment to disturbances and noise, as small disturbances may be amplified within certain frequency ranges. Methods for assessment of disturbance sensitivity are also described in [6.4.1.4](#) and [Annex D](#).

5. Real-time (RT) simulation

5.1 Overview

In order to perform a HIL test, the MOI has to be simulated on an RTS and connected to the HOI. This clause provides recommendations on key characteristics, modeling techniques, and simulation guidelines for RT simulation. Further information can be found in [Annex A](#).

5.2 Key characteristics of RT simulation

RT simulation is a computer simulation of the MOI executed in synchronism with RT. In RT simulation, all required computations and servicing of I/O signals need to be executed in synchronism with the progression of time in the real world in every time-step of the simulation without exception. If any given RTS does not enforce that requirement, the user should carefully assess its impact on the overall accuracy and stability of the HIL simulation.

5.2.1 Electromagnetic transient (EMT) simulation

EMT simulation is based on solving differential equations governing the dynamics of the SOI, resulting in instantaneous waveforms of physical quantities such as voltages, currents, and other quantities of respective systems. The computation timing requirements for executing EMT simulation in RT are more stringent than for transient stability (TS) simulation and analysis since many differential equations need to be solved with shorter time step sizes typically ranging from approximately 100 ns to 100 μ s.¹⁷ These types of simulations are recommended for analyzing the SOI over a wide range of frequencies simultaneously, as required for studies related to power system stability, control interactions, protection, and harmonics.

5.2.2 Transient stability (TS) analysis and shifted frequency analysis (SFA)

TS analysis should be used to investigate transient power system phenomena occurring below the fundamental frequency. In this simulation technique, the power system is modeled in the phasor domain at the fundamental frequency provided that the phasor components change slowly enough over time, so this technique does not introduce significant error. However, experience shows that in power systems where penetration of inverter-based renewable (IBR) is important, it is recommended to use TS analysis only for IBR controls with a lower bandwidth. Moreover, it should be considered that EMT over TS analysis should be used to simulate the transient events caused by the faster power electronics protection functions that will also impact the stability of the power system with sufficient precision. In cases with very high penetration of IBR, EMT simulation or a combination of EMT and TS analysis is recommended.

Different ideas have been proposed to find an intermediate representation between EMT simulation and phasor analysis. A common element is the idea of substituting the signal with a base-band representation in terms of a complex number. This concept was initially introduced, adopting the terminology dynamic phasor representation, and is now designated as SFA. Further information can be found in [A.4.1.1.3](#).

5.2.3 Hybrid phasor-EMT simulation

Hybrid phasor-EMT simulation (the term “phasor” here designates TS analysis) combines the advantages of TS and EMT simulation tools. This type of simulation is recommended for analyzing phenomena requiring EMT simulation, while, for computational resource reasons, the MOI cannot be represented entirely in EMT simulation. Therefore, the portion of the MOI representing only phenomena below the fundamental frequency is modeled in the TS environment and coupled to the rest of the MOI modeled in the EMT environment, as shown in [Figure 7](#).

¹⁷ Parallel computation capability is often required to solve the power system model in EMT RT simulation mode.

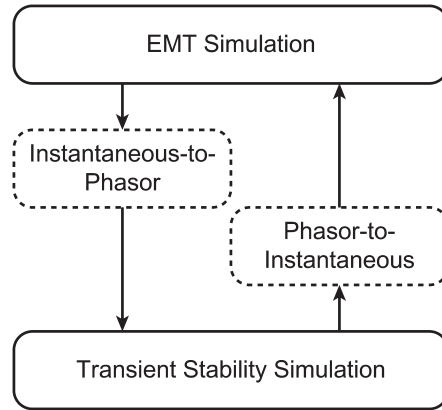


Figure 7—Interconnection between EMT simulation and TS analysis

5.3 Modeling techniques and simulation setup guidelines

To properly set up the simulation of MOI, the user should consider the following aspects of the simulation: accuracy, fidelity, reproducibility, and techniques for parallelization. These aspects are usually affected by the solution algorithm used for the network and components, the level of details considered for the components, the simulation time step, and the RTS platform.

5.3.1 Simulation accuracy and constraints related to solvers

In this context, accuracy is a measure of how well the differential equations of the SOI are numerically solved. The same measures for assessing the accuracy of non-RT simulation should be applied to RT simulation.

All the aspects of accuracy one considers important in non-RT simulation should also be paid attention to in the RT simulation for the purpose of HIL testing. However, RT simulation has its constraints because of limited available computation power and the limited accuracy/bandwidth of I/O interfaces. This discussion of simulation accuracy is only in the context of an RT HIL setup.

Simulation accuracy depends on both the simulation time step and the fidelity of the models' underlying mathematical implementation. Solvers in RT simulation often work differently from those in non-RT simulation, and therefore have particular constraints. The following is recommended:

- Whenever possible, simulation results are compared against analytical solutions.
- Whenever possible, simulation results are compared against laboratory experiments.
- Whenever possible, compare the results against measurements from actual installations. That is done to some extent, mainly by vendors, comparing to onsite measurements after installation of equipment or by comparing to fault recordings.
- Users find appropriate relations between simulation results and input parameters into the simulation tool using engineering intuition and judgement.
- Simulation results are compared against available benchmarks (e.g., CIGRE Electra [B11] and CIGRE Task Force TF-C6.04 [B12], etc.).
- Simulation results are compared against the results from the same simulation tool by reducing (or changing) the size of the timestep.
- Simulation results are compared against the results from other simulation tools or algorithms.

For EMT solvers, the following recommendations are made:

- The computation of the RT simulation model should be solved at a fixed time step (as opposed to variable time step solvers, which are often available in non-RT tools), as the solution has to be deterministic and able to update outputs to the HOI at a selected time step. Given this constraint and the requirement to execute in RT, only certain solver algorithms are available. For example, a solver algorithm with generalized interpolation is not possible while maintaining RT simulation.
- A simulation time step appropriate for the simulation study being conducted should be used.¹⁸
- When simulating power electronic converters, a simulation time step should be selected based on the highest frequency of interest and the switching frequency if a switching model of the converter is used.¹⁹

For phasor/TS analysis, the simulation time step should correspond to an integer multiple of the fundamental frequency—e.g., a time step of 20 ms for studying the fundamental frequency on a 50 Hz system.

5.3.2 Simulation fidelity considerations

Fidelity refers to the accuracy of the model's behavior in simulation when compared to the behavior of the actual device or system in the real world. Simulation fidelity indicates how faithfully the response of the simulation model corresponds to the real-world device that the simulation is trying to represent. All the aspects of fidelity that one considers important in non-RT simulation should also be paid attention to in the RT simulation for the purpose of HIL testing.²⁰

5.3.3 Considerations on the reproducibility of RT simulation

Simulation results for selected scenarios should be reproducible multiple times with the any given HIL setup. However, with the inclusion of discrete system models, HIL interfaces, I/O cards, global positioning system (GPS) clock time stamping, interface amplifiers, and the HOI, increased variability is introduced into the RT simulation. The following recommendations are made with respect to improved test consistency:

- If HOIs such as phasor measurement unit (PMU) or intelligent electronic device (IED) equipment utilize timestamping using GPS clocks, it is recommended to synchronize RT simulation with a GPS clock as well. In laboratory configurations, a single GPS clock is sufficient for the entire setup. However, multiple GPS clocks may be used to replicate the real system implementation.
- Wherever applicable, sequence events with reference to zero crossings or a specific time reference should be used.

5.3.4 RT simulation parallelization techniques

When the size and complexity of the system to be simulated increases (e.g., number of buses, machines, or power electronics converters), the computational cost of EMT simulations scale poorly and the RT execution requirement may become unsatisfiable. Consequently, RTS supports parallel execution so that the computation can be distributed across multiple processing units in order to satisfy the RT execution constraints.

The parallelization of EMT simulation has been the focus of extensive research efforts both in academia and industry. In summary, parallel execution takes place on the following two levels:

¹⁸ To limit the discretization error of simulating a 60 Hz sine wave with trapezoidal integration method to 1 degree, a timestep of less than 46.3 μ s ($1/60 \times 1/360$) is required. For a 50 Hz sine wave, a timestep of less than 55.6 μ s is required.

¹⁹ Typically, a time step corresponding to at least 6 to 10 times the highest frequency of interest is recommended. For many power system applications (e.g., voltage source converters), an appropriate time step is in the range of a few microseconds. For line-commutated HVDC converters, 30 microseconds to 50 microseconds could be adequate. For high switching frequencies, which are in the order of several tens of kHz, a sub-microsecond time step may be required to achieve adequate accuracy.

²⁰ US DoD AcqNotes—Modeling and Simulation/Fidelity (<https://acqnotes.com/acqnote/tasks/fidelity>).

- Network solution level (i.e., component outputs are used to update the network signals)
- Component level (i.e., components are simulated on different processing units)

Synchronized parallel execution is achieved either by directly applying parallel numerical methods in solving the network or by using decoupling techniques. An overview of the most commonly used methods in commercial RTSs is given in [Annex A](#).

5.3.5 Data analysis time resolution

For monitoring purposes, RTSs can provide lower-than-timestep resolution data (usually through a user interface). However, for data analysis, the user should always use the highest-time resolution data available.

5.3.6 Model development

During model development, the validation process proves that a power system model accurately depicts pertinent dynamic electrical, magnetic, and mechanical behaviors. The validation process should focus on the needs of a specific application being tested (one specific model may not be suitable for all applications). For example, in microgrid modeling, it is typical to build detailed models of steam boiler controls, governor hydraulic systems, gas turbine valve nonlinearities, wind turbine blade controls, reactive power controls, battery charging controls, generator transient models, complex load models, and more. These models should only be considered accurate enough once live performance test data are collected from real equipment and compared with model performance. To make RT power system models match field performance requires rigorous validation, which commonly takes more effort than building the model itself.

RT power system model developers may prove that their models accurately depict field phenomena that are relevant to planned studies. This evidence is best compiled into a model validation report to be delivered before the execution of HIL occurs. This recommended practice usually has individual validations of the following genres of behavior: steady-state electrical conditions, short-circuit conditions, power generation, active and reactive power controls, utility power system models, and load dynamics.

Steady-state electrical conditions should be validated by the tabulation of power flow results. These results should include bus voltages, island frequencies, active and reactive power flows, and generator outputs. Similarly, appropriate conditions should be validated for non-ac applications such as high-voltage direct current (HVDC). These tabulated values are compared to the known operation of similar power systems and known flows of installed equipment. Short-circuit conditions are validated by the tabulation of phase-to-ground and phase-to-phase fault values at several locations in the power system. These tabulated values are compared to known operations of similar power systems and known fault levels of installed equipment. Protection system testing should consider using electrical transient analyzer program models or similar models as references when building or replicating systems or subsystems for HIL testing. Modeling accuracy can be verified by comparing the results of such reference models with RT models embedded in the HIL setup, respectively.

6. Establishing an HIL simulation

6.1 Overview

[Clause 6](#) addresses the establishment of HIL simulation for the purpose of component testing and system analysis. Common aspects of both CHIL and PHIL simulation are elaborated and specific aspects unique to CHIL simulation are highlighted. Finally, specific aspects unique to PHIL simulation are presented with particular focus on modeling of PHIL setups for the purpose of system accuracy and stability analysis.

6.2 Common aspects of establishing a HIL simulation

In order to preserve the original characteristics of the SOI, the HIL interface should not adversely affect those characteristics. Any such effects should be properly determined by analysis. A test plan should be developed before establishing a HIL simulation and include at least the following aspects:

- Design of CHIL/PHIL simulation, including offline CHIL/PHIL simulation system model
- Stability, accuracy, sensitivity, and risk assessments of CHIL/PHIL simulation
- Generation of the CHIL/PHIL software
- Preparation of the CHIL/PHIL simulation, including safety and protection measures
- Setup and configuration of the CHIL/PHIL simulation system, including MOI and CHIL/PHIL interfaces
- Execution of the CHIL/PHIL simulation
- Analysis and documentation of the CHIL/PHIL simulation results

6.2.1 Appropriate data capture, measurement equipment, and methods

The RTS should always be used as the primary data capture mechanism for signals in the MOI. If additional data acquisition systems are used, captures from those systems should be time-correlated with the RTS data captures. The user should help ensure that the measured values are not influenced by the measurement equipment or the data capture process. Therefore, to achieve high fidelity in the results, a thorough assessment of the signal-capturing system should be performed.

A typical signal-capturing system is composed of: (a) sensors to transform the physical signal into a meaningful parameter; (b) signal conditioning processes for improving the suitability of the measured signal; and (c) analog-to-digital converter (ADC) devices for communicating the measured values with a digital system.

Verification and calibration of the sensors should be performed prior to the establishment of a HIL simulation. Calibration should be performed in conformity with the specifications of the test case to be evaluated to avoid inaccurate or unstable simulations. An analysis of sensor noise, delays, offsets, and gain errors should be performed to assess uncertainty. The impact of applying signal filtering (e.g., anti-aliasing, low pass, etc.) to achieve the needed signal conditioning should be evaluated before running the experiment to help ensure that excessive delay or bandwidth limitations have not been introduced. The user should select sampling rates that match the fastest event required to be measured, achieving an appropriate bandwidth limit for the HIL simulation. The user should perform a thorough evaluation of the required variables to demonstrate the objective of the test.

6.2.2 RT communication interfaces

RT data transfer is critical for HIL simulation. This clause discusses multiple forms of RT communication, including analog, discrete, or digital.

6.2.2.1 Analog I/O

The user should consider the following issues specific to analog I/Os:

- For each signal, scaling is required in order to reflect the entire range of the signal variation within the simulation and avoid saturation of output signals.
- Analog signals should be connected such that electromagnetic interference (EMI) is avoided.

- Analog signals should be wired with appropriate grounding arrangements such that common-mode and differential-mode noise and circulating currents are reduced.
- Impedance parameters of the interfacing wire or cable should be considered to reduce unwanted effects such as attenuation, noise, etc.

6.2.2.2 Digital I/O

Discrete digital I/O involves signals that represent 0 or 1 levels, such as trigger or pulse width modulation (PWM) signals. In addition to the analog wiring recommendations above, the user should also help as follows:

- Use appropriate interfacing cards on the RTS (e.g., specific cards may work best for PWM or time-stamped input signals).
- Confirm compatibility of HOI, I/O, RTS I/O for 0/1 threshold and minimum/maximum voltages.
- Verify adequacy of time resolution of pulsed signals (e.g., firing pulses such as triggers or PWM signals for power electronic switches or other devices in the MOI) through the I/O with respect to the pulse generation time resolution in the HOI.

6.2.2.3 Digital RT communication interfaces

Most RT data exchange in HIL applications uses high-speed digital data interfaces. High-speed digital interfaces use the following two different methods to transfer data:

- Non-synchronous data transfer
- Synchronous data transfer

Non-synchronous data transfer is not inherently designed to transfer RT data packages as required for HIL applications. Data packages transported from a sender to a receiver via the network have no defined transport delays, timing information, or fixed time step sizes. This type of data transfer should be avoided, when possible, unless it is used for monitoring purposes or non-time-critical control signals. Some of the most common non-synchronous data transfer occurs via IEEE 802.3 communication (Ethernet) with protocols like transmission control protocol (TCP) or user datagram protocol (UDP).

Synchronous data transfer should be used when possible to transport data streams for RT simulation. Ideal synchronous RT communication uses constant data frame size, constant data frame cycle time, constant transport delay, and synchronization between sender and receiver clocks. Currently, there is no public standard available for a HIL RT interface communication. Other protocols support synchronous data transfer, but care should be taken to help ensure the clock is synchronized with the RT simulation clock.

6.2.3 Safety measures

The user should always adhere to all applicable standards DIN/VDE 0105-100, EN 61140, EN 50110-1, IEC 60364-4-41, and all other relevant, country-specific standards.²¹

6.3 Specific aspects unique to CHIL

CHIL simulations should represent an SOI, as depicted in [Figure 5](#). Moreover, the CHIL simulation system should adhere to the structure depicted in [Figure 8](#).

²¹ Information on references can be found in [Clause 2](#).

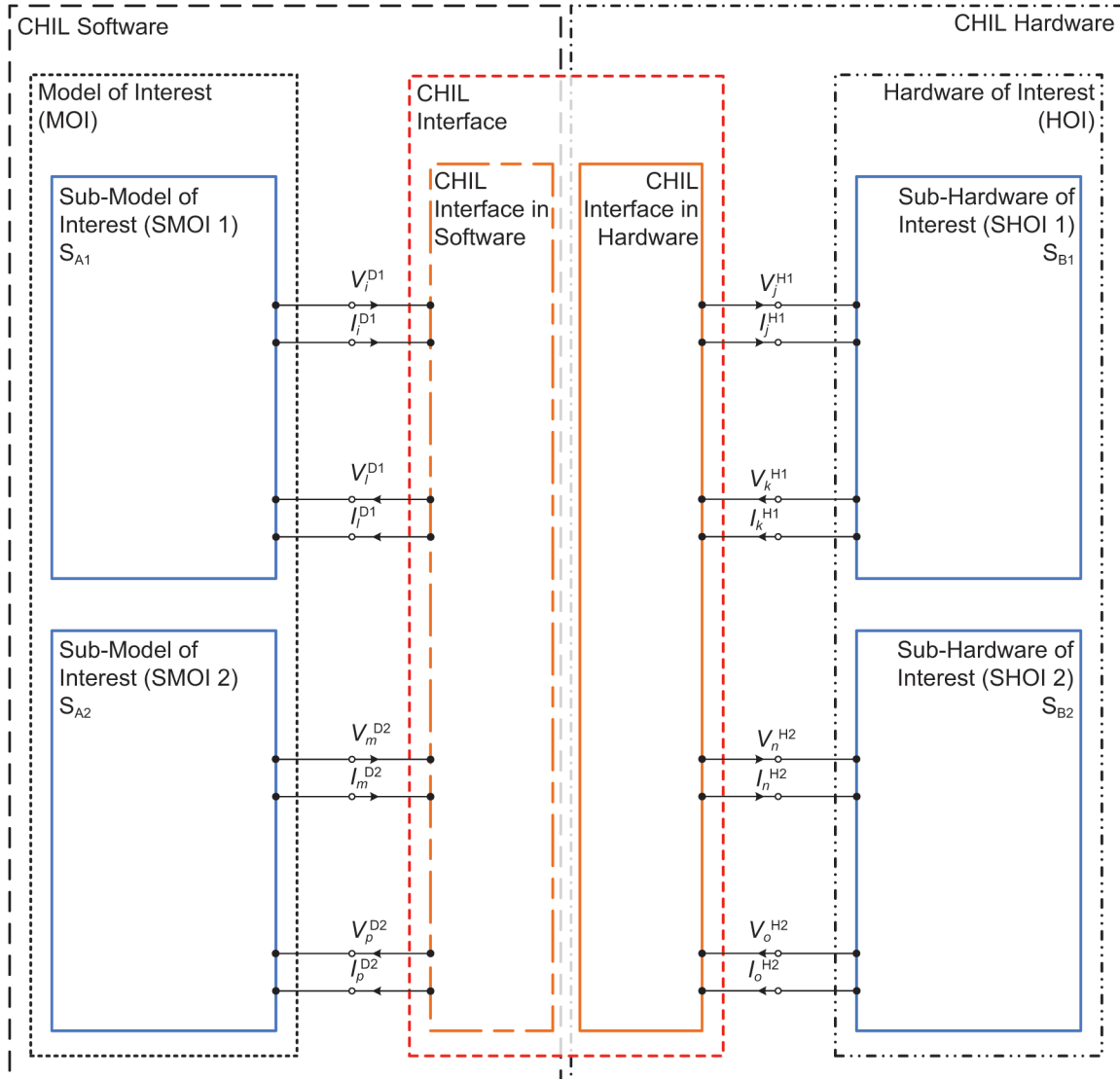


Figure 8—Model of the generalized CHIL simulation system

The output from the MOI (V^D , I^D) should become the input to the HOI (V^H , I^H), and the output from the HOI should become the input to the MOI. The corresponding signals should be routed through a CHIL interface composed of a CHIL interface in software and a CHIL interface in hardware. The user should define the necessary signal scaling and conditioning in both. The user may create SMOIs only if the respective portions of the MOI only interact with each other through the CHIL interface. Similarly, the user may create SHOIs if the respective portions of the HOI only interact with each other through the CHIL interface. In CHIL testing, a hardware controller is tested and linked to a system that is simulated entirely in the RT software. The hardware controller and the system model are interfaced by signal conditioning hardware, consisting of ADC and digital-to-analog converter (DAC) ports. Further information can be found in [Annex B](#).

6.3.1 Interfacing considerations

The user should choose appropriate CHIL interfaces related to given applications. Examples of application for CHIL simulation and interfacing techniques can be found in [Annex B](#).

To connect an RTS with an HOI for CHIL experiments the following distinction should be considered: In experiments without signal amplification the interfaces provided by the RTS (usually low power signals like analog and digital I/O signals, PWM signals, timing signals, etc.) should be connected directly with the HOI (i.e., the controller), as shown in Figure 9.

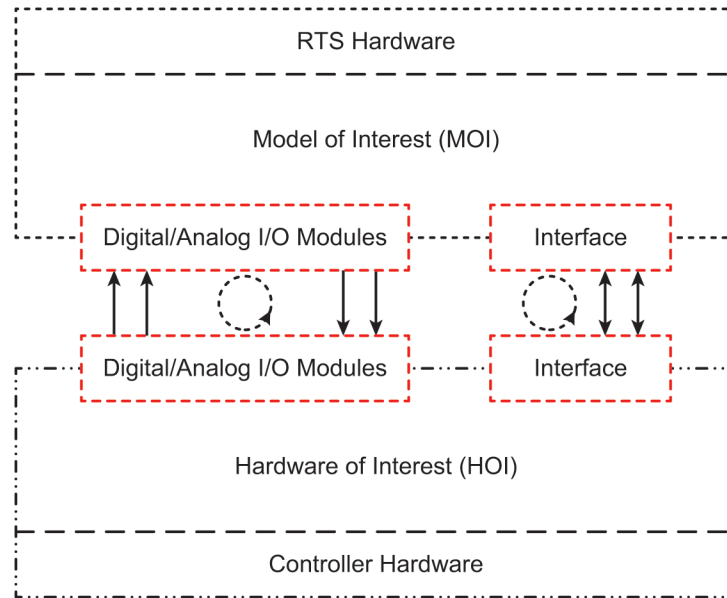


Figure 9—CHIL simulation without signal amplification in the interface

In experiments with signal amplification the interfaces provided by the RTS should be connected to a signal amplifier (usually low power rating) and its output should be connected to the HOI (i.e., the controller), as depicted in Figure 10.

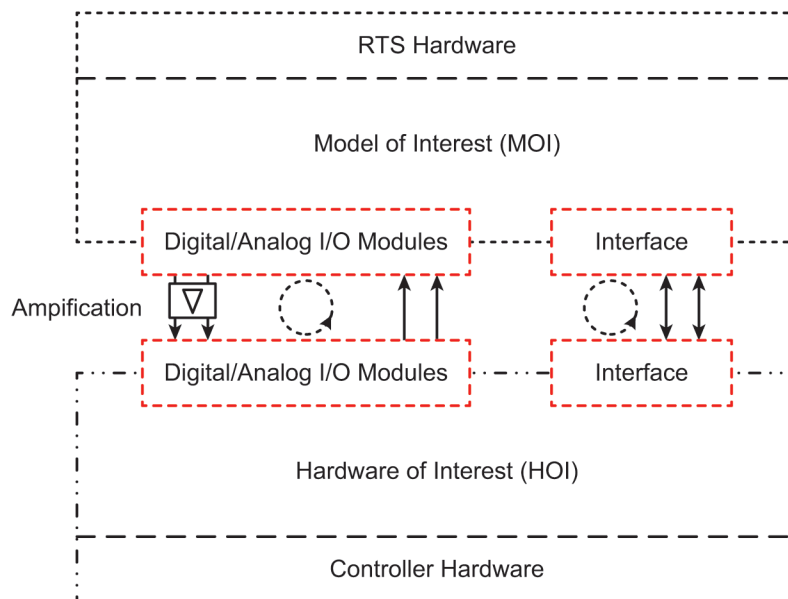


Figure 10—HIL simulation with signal amplification in the interface

In both cases, signal conditioning in the RTS may be necessary to get the required signal levels from the RTS. In the latter also a specific interface approach (IA) may be necessary (see also 6.4.4). Before conducting CHIL testing, the user should test all interfaces connected by removing the closed-loop interactions in the MOI.

6.3.2 Signal compatibility specific to CHIL simulation

The user should help ensure that signal levels of all interfaces are compatible with each other. For examples of compatibility consideration, see the requirements given in A.4.4 and Annex G.

6.4 Specific aspects unique to PHIL

6.4.1 System properties of PHIL simulation systems

System properties, including accuracy, stability, and sensitivity specific to the PHIL simulation, should be assessed in depth prior to execution. Modeling of PHIL simulation systems and corresponding block diagrams of the simulation circuit should support the user within this process.

6.4.1.1 Modeling of PHIL simulation systems

The user should model the SOI and the PHIL interfaces. The user should make sure that the subsystems related to the SOI, HOI, and PHIL interface are modeled, including all software and hardware related partitions. For purposes such as system analysis, protection, and overall execution of HIL experiments, the modeling of the HOI and PHIL amplifier should be RT simulation compatible. For the HOI and the PHIL interface, all existing time delays and occurring latencies should be included.²² The implementation of the PHIL amplifier model should not introduce additional artificial time delays. Based on the concept of HIL simulation in 4.4 and using models introduced in Figure 11, assessments on the system behavior of PHIL simulation setups should be performed. In what follows, the analytical determination of systematic properties such as stability, signal accuracy, and sensitivity is discussed. Based on this analytical framework, accurate estimations of the system behavior are facilitated for PHIL simulation experiments.

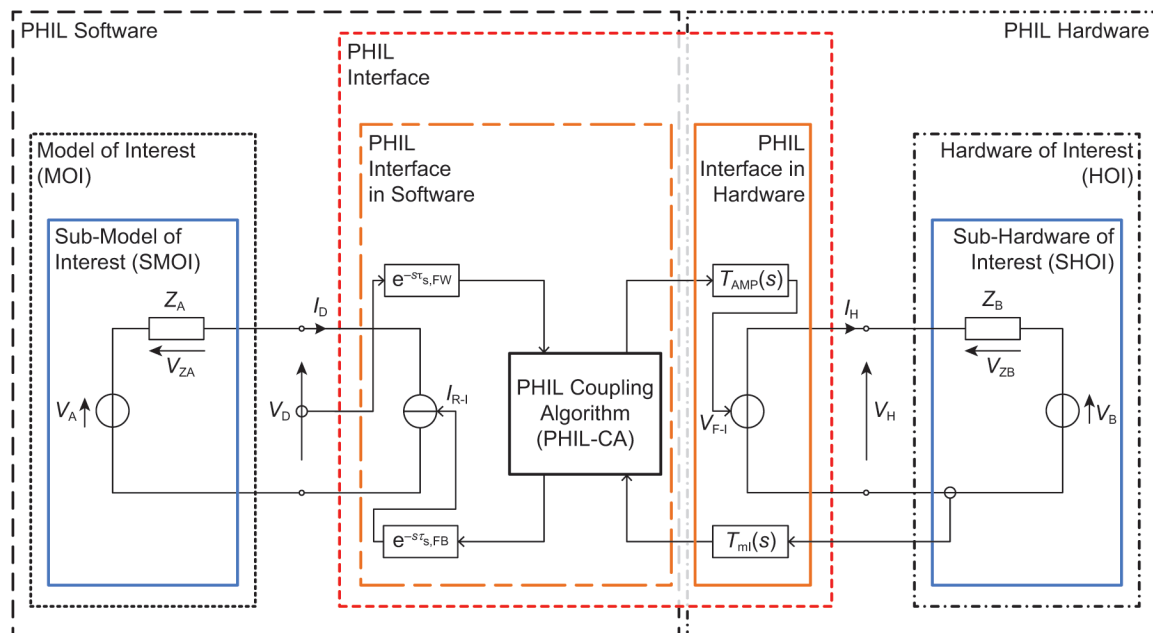


Figure 11—PHIL system with voltage-type (VT) ideal transformer method (ITM) as applied PHIL interface coupling method (PHIL CM) and PHIL coupling algorithm (PHIL CA)

²² For RT simulation, the time step size τ_S of the RTS equals the feedforward and the feedback time delays $\tau_{S,FW}$ and $\tau_{S,FB}$, respectively (i.e., $\tau_S := \tau_{S,FW} = \tau_{S,FB}$).

6.4.1.2 Stability assessment of PHIL simulation

The PHIL interface should not adversely affect the inherent stability characteristics of the SOI to be studied via the PHIL simulation. The complete, closed-loop system, including the PHIL interfaces, MOI, and HOI, should be assessed prior to execution in order to estimate stability properties. For this purpose, it is recommended to use metrics and methods for assessing and achieving stability characteristics, such as those reported in [Annex E](#).

6.4.1.3 Accuracy assessment of PHIL simulation

The accuracy of a simulation should be assessed using one or more of the metrics, such as those described in [Annex D](#). To avoid misleadingly large error estimates due to division by small quantities, an appropriate selection of absolute or relative error metrics should be made depending on the application at hand.

6.4.1.4 Sensitivity assessment of PHIL simulation

Sensitivity analysis of PHIL simulation setups is recommended to be performed according to metrics such as those described in [Annex D](#).

6.4.2 Power amplifiers

The user should be aware of the different types of amplification units available and their unique dynamic characteristics, such as allowable direction of power flow (i.e., unidirectional or bidirectional), latencies, bandwidths, and slew rates. The user should also consider the precise modeling of power amplifiers, which includes dynamic characteristics for voltage and current type amplifiers, as described in [Annex F](#).

6.4.3 PHIL IA

The user should select a suitable PHIL-IA based on dynamic characteristics and system topologies, and considerations such as stability, accuracy, and sensitivity to disturbances, as described in [Annex C](#), [Annex D](#), and [Annex E](#).

6.4.4 Protection measures/schemes for safe PHIL simulation

To reduce the risk of hardware damage and injury to personnel, the planning and implementation of protection systems should be included in a PHIL simulation experiment. Some of the considerations that are unique to PHIL simulation are described in [Annex G](#).

Possible failure modes of the PHIL experiment should be identified in the planning process, and appropriate measures should be implemented to mitigate identified risks. Where appropriate, multiple levels of action elements should be employed to avoid full experimental shutdown for all abnormal conditions. All protection measures should be tested prior to proceeding with PHIL experiments. As an RT simulation is inherently part of a PHIL experiment, a simulation of the PHIL hardware subsystem should be included for the purposes of testing the RTS-implemented detection and action elements. With this approach, the RT simulation should be designed so that the PHIL experiment may be executed either fully in simulation using a model of the HOI and the PHIL amplifier or with the actual HOI, such that execution of experiments fully in simulation exercise the protection systems and controls exactly as these would be operated with the actual HOI. Strict thresholds and rate limits should be included for any appropriate reference or feedback quantities to avoid exceeding the operating limits of components as identified for a given test. Based on the analysis of failure modes for experimental setups, detection elements should be implemented to identify any unsafe or abnormal conditions. Common types of detection elements that may warrant consideration for implementation are given in [Annex G](#). The actions that should be taken based on the abnormal conditions detected should be analyzed, considering the implications of protective actions to avoid unintended consequences. Considerations for appropriate actions are discussed in [Annex G](#).

6.4.5 Additional considerations related to the HOI

The following considerations related to the HOI should be considered when planning for PHIL testing:

- Space and cooling requirements.
- Weight with respect to ratings of foundations and structures on which or from which the HOI will be supported.
- Weight with respect to handling, transporting, lifting, and placing the HOI into the testbed location.
- Security requirements for proprietary, classified, or otherwise sensitive or restricted HOI. The necessary precautions and steps should be taken to protect and comply with the requirements.
- Shipping and transport to the PHIL test facility, commissioning and PHIL readiness testing, de-commissioning, packing, and return shipping transport, if applicable.
- Liability during testing and in shipment.

7. Executing an HIL simulation

7.1 Overview

This clause focuses on the execution of HIL simulations. Prior to execution, it is recommended to help ensure that the appropriate steps have been completed in establishing the HIL simulation as described in [Clause 5](#) and [Clause 6](#) and that the MOI and HIL systems represent the features of interest. In planning the execution of HIL simulations, it is recommended to consider initialization of the systems, execution of planned test sequences, recording of responses, and shutting down the system. The execution procedures for CHIL and PHIL are addressed in [7.2](#) and [7.3](#), respectively. Further information can be found in [Annex H](#).

7.2 CHIL execution procedure

Before executing HIL experiments, it is recommended to help ensure that the models are properly validated and interfacing is fully developed and tested, as this is necessary to help ensure the test results are accurate and contain a low degree of uncertainty.

7.2.1 Interface verification

I/O points between the devices should be confirmed. During this process, validation and, if necessary, calibration of interchanged signals is recommended.

7.2.2 Automation of CHIL simulations

It is recommended to automate execution of CHIL simulations in order to help ensure repeatability and consistency of results and minimal time for regression testing.

7.2.3 Startup of RT simulation model and initialization

It is recommended to bring the HIL system to a steady state condition. It is further recommended to review pre-event measurements and states of the controls within the model.

7.2.4 Record pre-event parameters

All pre-event parameters should be recorded prior to executing the HIL test, in order to properly document the pre-event conditions for review and analysis and to facilitate repeatability of a test case.

7.2.5 Executing the test sequence

In this step, the test sequence should be executed and recorded. CHIL testing of IED in integrated substation protection, control, and data acquisition systems applications should be done in accordance with IEEE Std C37.115™-2003.

7.3 PHIL execution procedure

7.3.1 Commissioning tests

It is recommended to execute tests to satisfy the following points as part of the commissioning phase:

- Test all RTS-implemented protection elements of interest by simulating the PHIL hardware. This should include verification of operation of all detection elements, as well as verification that all protection actions were executed as expected in each case.
- Test all measured signals from the test setup used by the RTS. It is recommended that a calibrated source be used to apply a quantity directly to each sensor, so that the entire path from the sensor to the RTS can be verified.
- Test data collection facilities and any fault recording facilities.
- Before connecting to the HOI, test references from the RTS to the physical stimuli (amplifiers, actuators, etc.) in an open-loop, direct control in order to verify that the stimuli are appropriately following the references.
- Where appropriate, test all protection measures in physical hardware to verify proper operation.

7.3.2 Bring system to open-loop steady state

It is recommended to bring the system to steady state prior to engaging feedback for PHIL-IAs. It is recommended to help ensure that all applicable protection systems have been enabled at this point.

7.3.3 Engage PHIL interfaces for closed-loop operation

From a stable open-loop operating point, it is recommended to gradually engage the feedback for each PHIL-IA sequentially. While engaging the feedback for an interface IA, the reference quantities for the associated PHIL-IC should be monitored closely for unexpected oscillations. If the oscillations continue to increase in magnitude beyond an acceptable level as the feedback for the IA is increased, it is recommended to halt the engagement process and return to open-loop operation. If the engagement of an IA is halted due to oscillations, the stability of the system should be reassessed for alternative implementations of the PHIL interface. Options for alternative implementations for consideration include the following:

- Consider the use of filters for the feedback signals of the IA and/or for the reference signals to attenuate the oscillations at the observed frequency. If the oscillations occur within a frequency range of interest for the experiment, this may not be an option.
- Consider the use of an alternative IA that may offer better stability properties (e.g., the partial circuit duplication (PCD), transmission line modeling (TLM), or damping impedance method (DIM) with damping impedance matched to the impedance of the HOI).
- Consider the use of other augmentations to the IA, such as use of a multi-rate implementation.

If a change has to be made to the IA, it is recommended to conduct stability analyses based on available models to assess the expected impact of the change. It is also recommended to conduct regression testing of RTS-implemented protection elements as appropriate before resuming testing.

7.3.4 Impedance measurements and analysis of stability, accuracy, and sensitivity

Once all PHIL-IAs have been fully engaged for the PHIL experiment, it is recommended, where possible, to obtain measurements of impedance values looking into the PHIL interfaces from the perspective of the HOI. The impedance measurements should be obtained over a frequency range sufficient to characterize the impedance up to the controllable bandwidth of the PHIL experiment. These impedance measurements may be taken through probing with the HOI, through the use of naturally occurring harmonics produced by the HOI, and/or through the use of a dedicated impedance measurement device intended for use with energized equipment. Note, however, that these measurements may not be reliable for frequency points/ranges for which the MOI or physical stimuli naturally produce components. It is recommended to conduct an accuracy and stability analysis (see [Annex E](#)) making use of the impedance measurements.

7.3.5 Execute planned tests and scenarios

Planned tests should be executed following the test plan developed. If issues with instability are encountered, the measures discussed in [7.3.3](#) should be considered.

7.3.6 Shutdown of experiment

When shutting down the experiment, it is recommended to gradually remove the feedback for all PHIL-IAs. This will bring the system to a safe, steady-state, and open-loop operating point. The final shutdown of power equipment may require disabling some of the PHIL protection elements.

7.3.7 Accuracy assessment

If appropriate, it is recommended to perform accuracy assessments following execution of the PHIL simulation experiments using the methods described in [Annex D](#).

Annex A

(informative)

RT simulation

A.1 Circuit decoupling techniques

Circuit decoupling techniques typically require specific model characteristics, and in certain situations, they may introduce significant artifacts in the simulation. In general, the goal of such methods is to exploit the natural latency introduced by reactive elements (e.g., transmission lines and relatively long cables) to decouple the system's network into multiple subsystems that can then be simulated in parallel.

The most intuitive approach for decoupling a simulation model is to use the ITM (see Faruque [B31] and Lauss et al. [B62]). Decoupling is achieved through the use of controlled sources and unit delays. While this approach provides very good parallelizability, it introduces a delay between the solutions of the obtained subsystems, which can lead to unstable or inaccurate results. Users of this method should always check for the best tradeoff between parallelizability and accuracy.

Another method that has been widely used in commercial RTS and that exploits the latency of system components is the TLM approach (see Christopoulos [B10]), where the wave propagation delay of long transmission lines is used to parallelize the solution process. It is important to highlight that using TLM will not simply exploit the naturally slow dynamic behavior of a part of the system (in relation to the used time step) to decouple the simulation. Still, the solution of the considered transmission line is directly used in the decoupling process. In this way, a system decoupled using TLM provides the same solution as the one provided by the original model. The TLM does not introduce the same concern about accuracy and stability as the ITM approach. The major requirement in using the TLM approach is that the wave propagation delay over the considered line should be larger than the time step used for the simulation.

In the absence of a physical transmission line with a minimum propagation delay larger than the simulation time step, it is possible to introduce an artificial transmission line (ATL) to decouple the network. Considering that the wave propagation delay of a transmission line is a function of its equivalent capacitance and inductance, the main idea of ATL is to exploit large reactive elements already presented in the system (e.g., transformer inductance) and add to the circuit the missing components (e.g., capacitive elements) so to create an equivalent circuit that can be exploited by the TLM approach. The ATL method does not suffer from the same stability problem as the ITM method, but nevertheless, concerns about accuracy may arise since the decoupled system is different from the original one.

Over the years, other approaches that do not exploit component latencies to decouple the system solution (e.g., parallel numerical methods) have also been developed. The main advantage of those methods is that they can be used to decouple the simulation of highly coupled systems that do not have the characteristics needed to use TLM and for which ITM or ATL will provide an inaccurate solution.

Current commercial RTSs have adopted different strategies in solving the power system circuit as follows:

- Some have utilized the nodal admittance algorithm in solving power system electromagnetic transients, first proposed by Dommel [B23]. Here, there is a natural parallelization opportunity that has been used. Various power system components are executed on different processing units in parallel, and they interact with another processing unit that solves the network equations and passive elements using nodal solution (see Wierckx [B108], Working Group F-8 [B109], Strunz and Carlson [B99]). In this context, the method generation of electric network equivalents (GENE) of Strunz and Carlson [B99] uses Norton's theorem to formulate exact miniature equivalents of power-electric and electronic network portion models that are discretized using implicit numerical integration. Those network

portions may be formulated using nodal analysis, state-space methods, or a combination of both and are integrated within a distributed and simultaneous solution. The nested structure of the method allows for the different network portions to be solved in parallel and simultaneously. Thus, even if parallelization is applied, the method GENE offers the same exact solution as if the solution were obtained in one whole piece.

- Other RTSs use the state-space approach to solve the power system circuit (network and components together) in parallel. The state-space nodal (SSN) method (Dufour, Mahseredjian, and Belanger [B26]) is an approach that enables parallel implementation of larger networks for the purpose of RT simulation. The main idea of the SSN approach is to combine arbitrary groups of components (modeled using state equations) in a single nodal admittance matrix. The group of components represented using state equations can then be solved in parallel, all components of the system are still discretized using an implicit integration method, and no delay is introduced between the solution of the obtained sub-systems. The SSN method has been validated on systems with hundreds of switches and has no hard-coded total switch limit. However, the user should limit the number of switches <per group> to a reasonable amount (6 to 12 typically) to allow pre-calculation of group equations as well as the number of nodes in the nodal solution part. At the interface between the state-space groups and the nodal solution, the user needs to specify the type of interface (i.e., Norton or Thevenin formulation). It should be noted that parallelization of the system's equations using the SSN solution generates the exact solution of a non-parallelized system and therefore adds no delay in the network solution. Notably, the computation of the SSN group can be done on different central processing unit (CPU) cores, in parallel, without any delays (see Dufour, Mahseredjian, and Belanger [B26] and Dufour and Belanger [B25]). The SSN solver also has the option to iterate its nodal solution for difficult cases involving, for instance, diode converters in electric aircraft with low-impedance feeding transformers or solid-state transformer cases. In these examples, fast transients in transformer circulating currents require solver iterations. Surge arresters are another type of element that may require iterations for accurate simulation, because of their highly nonlinear characteristics (see Dufour et al. [B27]).

A.2 Parallel numerical methods for network solution

The parallel numerical methods directly assist in the parallelization of the nodal solution itself, and not the components connected to it, such as electric machines and frequency-dependent transmission lines. The main advantage of such methods is that, typically, the parallelized solution is numerically precise.

A method of this type that is successfully used in a commercial RTS is the spectral nested dissection (SND). The SND (see Pothen Simon, and Wang [B87] and Maguire [B73]) is a method that takes advantage of the natural sparsity of the power system networks. It recursively divides the nodes of the network admittance matrix into sets of nodes to facilitate its separation into sub-matrices that can then be factored in parallel. The algorithm divides the system nodes into X and Y sets of nodes. The Y-set is solved on one processing unit, while the X-set and common X/Y-set are solved on another processing unit. Required information is exchanged at the boundary nodes during every time step. An important aspect of the SND method is to divide the network so that the number of shared nodes (i.e., X/Y nodes) is reduced. This is done by observing the eigenvalues and eigenvectors of the graph adjacency matrix; notably, the eigenvector corresponding to the second smallest eigenvalue is also known as the Fiedler vector.

A.2.1 Considerations for parallelization

Solving the power system network or the MOI in one subsystem provides the most precise solution. If, due to the complexity of the system or RT processing capabilities, such a solution was not possible, resort to the following recommendations for the decoupling of EMT simulation:

- Always evaluate the use of parallel numerical methods for network solution (e.g., SND) since they do not undermine simulation accuracy.