

IEEE Standard Definitions, Symbols, and Characterization of Metal-Nitride-Oxide Field-Effect Transistors

Sponsor

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Foreword

(This Foreword is not a part of IEEE Std 581-1978, Standard Definitions, Symbols, and Characterization of Metal-Nitride-Oxide Field-Effect Transistors.)

(3)

The purpose of this standard is to promote uniform definitions and notation of electrical quantities peculiar to MNOS (Metal-Nitride-Oxide-Semiconductor) transistors. In addition, it recommends test techniques that should permit the reliable presentation and reproduction of electrical characteristics of MNOS transistors.

The need for standardization has become increasingly apparent since 1966, when the MNOS transistor was first investigated for its use as a nonvolatile memory element. This need arises from the fact that instantaneous electrical characteristics of MNOS devices depend on potentially unknown previous electrical stresses. Moreover, these characteristics change with time. While both stress and time relationships are predictable, the history of a specific device may not be clearly defined.

In March 1973, the Air Force Avionics Laboratory organized a workshop to discuss standardization of MNOS devices. This resulted in the organization of a committee which held a meeting in April of 1973. In the following month this group was affiliated with the IEEE to form the MNOS Standardization Subgroup with Fritz Schuermeyer from the Air Force Avionics Laboratory as chairman. Over the course of the two years following, ten meetings were held which have resulted in the standard in its present form.

In the course of these discussions it became clear that there were no generally established standards on device characterization, definitions, and notations for MOS transistors. Thus the necessity of generating MOS standards as they apply to MNOS transistors has added to the length of this work.

Acknowledgment should be made of the skill and devotion of Ilse Wegener, who typed all three consecutive drafts, and who performed two major revisions of the final version.

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IEEE Standard Definitions, Symbols, and Characterization of Metal-Nitride-Oxide Field-Effect Transistors

1. Introduction

1.1 MOS and MNOS. The MNOS (metal-nitride-oxide-semiconductor) [1–5] transistor is a close relative of the MOS (metal-oxide-semiconductor) transistor. Both their active regions are described by a vertical Metal-Insulator-Silicon structure. In the MOS transistor, the insulator is a single layer of silicon oxide (Metal-Oxide-Silicon); in the MNOS transistor, the gate contains silicon nitride as an additional insulator between metal and oxide (Metal-Nitride-Oxide-Silicon).

MNOS and MOS transistors also have the same basic electrical characteristics. They differ only in one important aspect. For the MOS transistor, the threshold voltage (the gate voltage at which a specified minimum drain current starts to flow) remains fixed at a constant value. In contrast, the MNOS transistor provides the capability that this threshold voltage can be set and reset electrically to predetermined high and low values. Once set, a specific threshold voltage will remain near its value for an extended and predictable length of time, even after any source of power to the device has been removed.

Setting, or “writing,” requires voltages near 25 V of both positive and negative polarity and pulse lengths in the $1\mu\text{s}$ to 1 ms range. This results typically in threshold voltages of -2 and -10 V. The set threshold voltage may be retained for periods of hours to centuries, depending on the storage conditions and specific device properties.

The operating characteristics of MOS transistors have been described in several books [6–9] so that these sections will be concerned mainly with the one characteristic of the MNOS transistor that is different, namely, the controllable threshold voltage.

1.2 Description of this Standard. This standard has ten sections. The first is an introduction to [MNOS transistor structure, device theory and operation]. It limits the discussion to the

simplest, most commonly used configuration. Sections 2, 3, and 10 are summaries of all definitions and references used in the remaining sections. The remaining six sections are concerned with [the definitions and measurement of electrical characteristics that are peculiar to MNOS transistors]. These six sections share more or less the same basic plan. The subsection at the beginning defines the electrical characteristic to be measured and describes its general features. The second subsection deals with testing techniques, their description, recommended parameters, presentation of results, and notation standards. A third subsection is sometimes inserted that addresses itself to a special feature.

Section 4 is concerned with threshold voltage. Since the variability of threshold voltage of the MNOS memory transistor is its main difference with respect to the standard IGFET (insulated-gate field-effect transistor) and its fixed threshold voltage, the background subsection gives a brief review of general IGFET operation and a summary of the current-voltage relationships. The concept of threshold voltage arises naturally from this discussion. The special problems of defining and measuring a variable threshold voltage are then brought out. Three measurement procedures permit a choice that matches test environment with typical circuit applications. This is followed by a closer look at “read disturb” and associated notation standards.

Section 5 deals with writing characteristics. Writing is defined as the process by which the threshold is changed by the application of a large gate voltage. Referencing this change involves the problem of “normalization.” This is really a technique for erasing the results of previous electrical stresses by establishing a reproducible threshold voltage reference level at a known instant in time. There are two such procedures, and each is associated with a valid method of determining the writing charac-

teristics of a given MNOS transistor.

Retention is the subject of Section 6. The time span implied by retention begins when writing has ceased, and ends when the two threshold voltages defining logic 1 and logic 0 become electrically indistinguishable. Therefore, the end of retention depends very much on the method of interrogation and on the sense amplifier, since they decide distinctness. In addition, the time span during which distinguishable information is held, is strongly influenced by electrical stresses on the device during that time. There are three methods of defining and measuring retention, each of which may be important in a specific application. They differ by the gate bias used during retention. One is constant at zero, another is constant at an operational read bias level, the third adjusts itself by feedback to result in constant drain current of the MNOS transistor. For retention in excess of years it becomes important to address the problem of accelerating conditions in order to permit valid projections of long-term behavior in a short period of time.

The fifth section deals with the endurance of MNOS transistors. This property is defined as the ability of the device to withstand continuously repeated writing pulses of alternating polarities without changing its device characteristics. For a defined pulse length pattern, endurance is clearly a time period whose beginning and end can be defined. The end or limit of endurance varies somewhat with the details of the stress conditions, and it manifests itself in diverse ways. The most important effect observed is a reduction in retention. While the specification of test conditions is a straightforward matter, the presentation of data is a complex problem. Accelerated endurance tests become desirable when the life of a device must be projected over a period of years.

In Section 8, the effect of the MNOS gate structure on basic MOS device characteristics is examined. This effect arises in part from the time-dependent variability of the threshold voltage, which requires pulse measurements of I - V characteristics and gain. Another factor is the higher field at the silicon interface due to the thinner dielectric. This causes generally higher drain junction leakage currents and lower breakdown voltages. Finally, tests of dielectric strength are not necessarily destruc-

tive, but involve the determination of the I - V characteristics of the dielectric. All of these properties are related to details of device construction and processing.

The measurement of radiation effects on MNOS transistors is examined in Section 9. This is an important area, since the nonvolatility of information in MNOS transistors makes them desirable electronic components in isolated and hazardous environments. These measurements require careful planning, since not only the details of radiation exposure are crucial, but also the conditions of electrical stress and the variations of electrical characteristics with time are crucial. Both total dose testing and controlled dose rate pulse measurements must be defined, and their effects on memory and basic characteristics require detailed evaluation.

1.3 Mechanism of MNOS Memory Transistor.

A representative MNOS transistor (Fig 1) consists of a gate with a 500 Å thick nitride layer, a 25 Å thick oxide layer, and an n-silicon substrate with p^+ source and drain areas. The application of approximately 25 V of one polarity between gate and substrate causes current

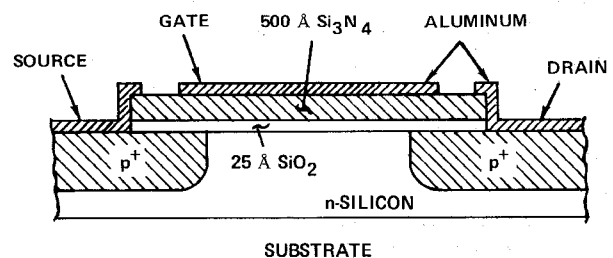


Fig 1
MNOS Transistor

to flow within the nitride-oxide insulator layer, which causes charge to accumulate near the nitride-oxide interface. Application of a gate-substrate voltage with the opposite polarity causes the removal of this charge or even a buildup of a charge with opposite polarity.

The behavior of the MNOS gate [1-5] can be described in a straightforward manner. In the simplest model one assumes that the accumulated charge σ lies in a plane at the nitride-oxide interface. At any instant of time the relationship between σ , the nitride field E_n , the oxide field E_o , and the applied voltage V_G can be described as follows:

$$E_n x_n + E_o x_o = V_G \quad (\text{Eq 1})$$

$$\epsilon_n E_n - \epsilon_o E_o = -\sigma, \quad (\text{Eq 2})$$

where ϵ_n and ϵ_o are the dielectric permittivity of the nitride and oxide layers, respectively, and x_n and x_o are the thicknesses.

When V_G is removed, the corresponding σ remains, so that when the transistor is interrogated, its flat-band voltage V_{FB} will have been shifted by an amount relating to σ . Assuming that V_{FB} is only due to σ , a simple relationship is obtained from the condition that $V_G = V_{FB}$ when $E_o = 0$. Therefore, from equations 1 and 2 we have

$$V_{FB} = -\sigma \frac{x_n}{\epsilon_n} \quad (\text{Eq 3})$$

Now equations 1, 2, and 3 may be solved for E_n and E_o :

$$E_o = \gamma \epsilon_n (V_G - V_{FB}), \quad (\text{Eq 4})$$

$$E_n = \gamma \epsilon_o (V_G + \beta V_{FB}), \quad (\text{Eq 5})$$

where $\gamma = (\epsilon_n x_o + \epsilon_o x_n)^{-1}$, and

$$\beta = \frac{\epsilon_n x_o}{\epsilon_o x_n}.$$

Equations 4 and 5 give E_o and E_n at any instant of time. To determine V_{FB} as a function of time, the equation of current continuity for the system must be used:

$$\epsilon_o \frac{dE_o}{dt} + j_o = \epsilon_n \frac{dE_n}{dt} + j_n \quad (\text{Eq 6})$$

This equation states that the sum of the displacement current and particle current is always the same in both layers. From equation 6,

$$t = \int \frac{V_{FB}^f}{V_{FB}^i} \frac{\epsilon_o dE_o - \epsilon_n dE_n}{j_n - j_o} \quad (\text{Eq 7})$$

where superscripts i and f represent initial and final states, respectively.

Differentiating equation 2, combining with equation 3, and substituting in equation 7, we obtain

$$t = \frac{\epsilon_n}{x_n} \int \frac{V_{FB}^f}{V_{FB}^i} \frac{dV_{FB}}{j_n - j_o} \quad (\text{Eq 8})$$

Equation 8 is a general result that applies to the introduction of charge into any two layer insulator system on a nondegenerate semicon-

ductor, provided that the assumption of a planar charge distribution is valid. Also, it holds for discharging with the appropriate limits, when V_G is zero, or small, and when the denominator is changed to $j_n + j_o$. To obtain V_{FB} as a function of time, it is necessary to integrate the equation using the appropriate functions for j_n and j_o and the proper limits. The terms j_n and j_o represent current-field relationships for the nitride and oxide, which can be expressed in terms of V_{FB} through equations 4 and 5.

All discussions in this standard are limited by choice to devices which depend on a large current through the oxide layer. If the conditions for Fowler-Nordheim tunneling [3] are applicable, then

$$j_o = A E_o^2 \exp(B/E_o) \quad (\text{Eq 9})$$

where A and B are constants. Substituting equation 9 into equation 8 and neglecting j_n , equation 8 can be solved explicitly to yield

$$t = [(\epsilon_n x_o / x_n + \epsilon_o) / AB] \cdot [\exp(B/E_o^f) - \exp(B/E_o^i)] \quad (\text{Eq 10})$$

Whenever the mechanism implied in equation 9 is applicable, equation 10 can be used to predict writing characteristics and retention (with a reversal of signs in the second square bracket). Both characteristics have a predicted dependence of threshold voltage (see equation 4) on the logarithm of time, which is in agreement with a large portion of observed data.

The simple derivation given here neglects some important details. This includes the fact that σ is not located at the plane defined by the oxide-nitride interface, but may be extended over tens of angstroms into the bulk of the nitride. In addition, the nitride current j_n may not be neglected; it becomes an important quantity for smaller values of V_{FB} . Finally, there are several mechanisms possible (acting simultaneously or in sequence) for charge transfer between silicon and insulator. They depend significantly on details of device structure and materials properties. Fortunately, they have the general relationship $J_o = j_\infty(E) \exp[f(E)]$. This mathematical form makes it plausible [10] that the change in flat-band voltage has the logarithmic time relationship over some orders of magnitude.

1.4 Restrictions. This standard considers *p*-channel devices only. Even though the memory effect is of an analog nature, this standard is concerned only with its use in digital applications. While memory effects have been observed in many insulator materials, only MNOS devices with a typical oxide thickness of 10 to 40 Å and a nitride thickness of 100 to 2000 Å are considered. It is also implied that the threshold voltage changes are due to tunneling through the oxide. Avalanche injection, conduction through the nitride, and other mechanisms are excluded from the present discussions. However, many structures representing these and other variants can be tested by applying the same standards with only slight modifications.

This standard discusses only MNOS field-effect transistors. Other electronic circuit elements, which would be required for the use of the MNOS device in integrated circuits, are not considered. Only the basic form of the MNOS memory transistor shown in Fig 1 is considered here. The more advanced "Protected Source-Drain" structure [11] (see Fig 28) does not affect measurement procedures and definitions, but it complicates the details of the *I*–*V* characteristics (Table 1). Its discussion must be left to a future date.

2. Letter Symbols and Definitions

In this section the letter symbols and definitions used throughout this standard are brought together. It must be kept in mind that they refer to MNOS transistors only. There is no generality implied in their use, so that applications to MOS capacitors, specific IGFETs, and devices within arrays must be done with caution.

In the choice of symbols the scheme of the IEEE Std 255-1963, Letter Symbols for Semiconductor Devices, was followed. In order to describe established usage, the symbols for the applied gate voltage were differentiated by a second letter in the subscript. Thus the gate voltage in a general application was designated V_{GS} ; when intended as write voltage it was designated V_{GW} ; when intended as read voltage it was designated V_{GR} ; and in the theoretical model it was given as V_G . The time variable was used with lower case *t* and lower case subscripts. The defined fixed time periods

represented by retention were not designated by a capital *T* to avoid their misreading as temperature. Instead, capital letter subscripts were used, such as t_{RO} .

A number of the letter symbols proposed here are not defined by a formal standard in existence at this time. There is, however, a continuing effort by the IEEE to establish standards for additional symbols which may affect some of those used here. Therefore present notation must be considered provisional until specific standards have been finalized.

2.1 Letter Symbols

C_G	Gate capacitance of IGFET
EL	Endurance limit
E_n	Electric field in the silicon nitride layer
E_o	Electric field in the silicon dioxide layer
I_{DS}	Drain current in IGFET
I_{DSO}	Drain to substrate reverse leakage current ($V_{GS} = 0$)
j_n	Current density (in amperes per unit area) in silicon nitride layer
j_o	Current density (in amperes per unit area) in silicon dioxide layer
K	Dielectric constant
k'	Specific gain factor in IGFET
ℓ	Length of channel in the direction of current flow
M	Number of read pulses
N	Number of write-high–write-low cycles
Q_B	Charge density in depletion region of silicon bulk
Q_I	Charge density in insulator (or at its interface with the semiconductor)
R_N	Resistor
R_S	Resistor
t_{CR}	Value of t_w at intersection in write characteristic
t_d	Decay time of stored threshold voltage
t_{d1}	Time at which first change in decay rate occurs
t_{d2}	Time at which second change in decay rate occurs
t_{HS}	Pulse width at which high conduction threshold voltage saturates
t_{LS}	Pulse width at which low conduction threshold voltage saturates
t_r	Read pulse width
t_R	Defined period of retention
t_{rd}	Delay time between write pulse and following read pulse

t_{RI}	Period of retention at constant I_{DS} , with gate tied to drain
t_{RO}	Period of retention at zero gate bias
t_{RV}	Period of retention at constant gate bias
t_{sat}	Pulse width at which threshold voltage saturates
t_t	Transition time
t_w	Write pulse width
t_{wd}	Delay time between any pulse and following write pulse
V_{DD}	Power supply voltage leading to drain of IGFET
V_{DS}	Voltage at drain of IGFET
V_{FB}	Flat-band voltage
V_G	Voltage at gate of MIS structure
V_{GR}	Voltage applied to gate of MNOS transistor for reading
V_{GS}	Voltage applied to gate of IGFET for general purposes
V_{GW}	Voltage applied to gate of MNOS transistor for writing
V_{GBD}	Breakdown voltage of gate insulator
ν_{HC}	High conduction threshold voltage of MNOS transistor
$\Delta\nu_{HL}$	Threshold voltage window of MNOS transistor
V_{IN}	Input voltage
ν_{LC}	Low conduction threshold voltage of MNOS transistor
ν_s	Sensed voltage
V_T	(Fixed) threshold voltage of IGFET
ν_T	(Variable) threshold voltage of MNOS transistor
ν_{TC}	Threshold voltage value of center of window
W	Width of IGFET channel at the silicon surface, at right angle to current flow
X	Thickness of gate dielectric in IGFET
x_o	Thickness of oxide layer in MNOS gate
x_n	Thickness of nitride layer in MNOS gate
β	Symbol for $\epsilon_n x_o / \epsilon_o x_n$
γ	Symbol for $(\epsilon_n x_o + \epsilon_o x_n) - 1$
ϵ	Dielectric permittivity of vacuum
ϵ_o	Dielectric permittivity of oxide
ϵ_n	Dielectric permittivity of nitride
μ	Carrier mobility
σ	Charge density per unit area (at oxide-nitride interface)
ϕ_s	Surface potential
ϕ_f	Fermi potential
ϕ_{ms}	Contact potential between gate metal and silicon

2.2 Definitions

annealing. In the context of MOS device properties under irradiation, annealing refers to the sometimes observed reduction of the radiation induced threshold voltage change over a period of seconds to hours after exposure to radiation has ceased.

body effect. This effect occurs when the potential in the substrate of a (p-channel) IGFET is more positive than the source potential. It can be expressed as an increment that increases the threshold voltage of an IGFET. The effect occurs routinely in integrated circuits.

channel. A surface layer of carriers connecting source and drain in an IGFET. This channel was formed by inversion with the help of a gate voltage, or by the presence of charges in the gate insulator, or by deliberate doping of the region.

constant current retention. Retention inherent in the MNOS transistor when gate and drain are biased to result in a constant drain current during information storage. The time period is defined by the intersection of the HC threshold voltage curve obtained under constant current condition, with the LC threshold voltage curve obtained under zero bias condition, when both are plotted against the logarithm of t_{rd} , the time elapsed between writing and the threshold voltage measurement.

constant voltage retention. Retention inherent in the MNOS transistor when source, drain, and substrate are grounded, and a fixed read bias V_{GR} is maintained at the gate. The time period is defined by the intersection of the two HC and LC threshold voltage curves obtained under this condition when plotted versus the logarithm of t_{rd} , the time elapsed between writing and threshold voltage measurement.

depletion. The state of the silicon surface in the IGFET structure when a gate voltage of such polarity has been applied that all majority carriers have been repelled. The space charge region so formed is depleted of all mobile majority carriers.

depletion mode transistor. An IGFET where the channel connecting source and drain is a preexisting thin layer of the same conductivity type as the source and drain.

dose rate. The time rate of deposition of radia-

tion expressed in rads in Si per second. The integration of dose rate over a specified period of time represents the total dose.

drain. Region in the device structure of an IGFET which contains the terminal into which charge carriers flow from the source through the channel. It has the potential which is more attractive than the source for the carriers in the channel.

dynamic radiation test. Test of the instantaneous effects of radiation obtained by monitoring electrical properties of interest continuously during and immediately after exposure.

endurance. The number of write-high—write-low cycles accumulated before any defined unacceptable changes in device properties occur.

enhancement mode transistor. An IGFET where the channel connecting source and drain was formed by the effects of an applied gate voltage.

example for write-high and write-low definition. As an example, for a p-channel device, the threshold voltage ν_{HC} of the device after a write-high operation could be in the -1 to -4 V range while the threshold voltage ν_{LC} of the device after a write-low operation could be in the -8 to -12 V range.

fast writing devices. MNOS memory transistors whose threshold window $\Delta\nu_{HL}$ is sufficiently large after a writing pulse width of t_w near $1\mu s$. A write cycle time of about $1\mu s$ makes these devices useful for RAM applications.

fixed threshold transistor. Another name for an MOS type transistor, used in contradistinction to the MNOS transistor, which has a variable threshold voltage.

flat-band voltage. Gate voltage that results in zero field at the surface of the silicon. It is related to the threshold voltage by a constant, generally small, voltage increment.

gate. This structural element of an IGFET controls the current between source and drain by a voltage applied to its terminal.

HC (high conduction) threshold voltage ν_{HC} . The threshold voltage level resulting from a write-high pulse, which puts the transistor into the HC (high-conduction) state.

IGFET (insulated-gate field-effect transistor). A four-terminal device consisting of two separate areas of one conductivity type called source and drain with a terminal each, separated from each other by a substrate of opposite conductivity type with its terminal and straddled by an electrode with terminal called gate, which is insulated from the silicon by a layer of insulator material, frequently silicon dioxide, called gate.

IGFET symbols. IGFET types may be categorized as memory—nonmemory, enhancement mode—depletion mode, and n-channel—p-channel. Standard symbols for memory transistors do not exist. Fig 3 presents the standard electrical symbols for the non-memory transistors and the symbols used in this standard for memory transistors. The symbols used for the memory transistors must be considered provisional until specific standards have been finalized.

inversion. The state of the silicon surface in the IGFET structure when the voltage leading to depletion has been further increased such that a thin layer of minority carriers becomes stable at the surface.

LC (low conduction) threshold voltage ν_{LC} . The threshold voltage level resulting from a write-low pulse, which puts the transistor into the LC (low-conduction) state.

MNOS transistor. In analogy with the MOS transistor, this acronym derives from the layer sequence in the gate region of the IGFET, namely, Metal-Nitride-Oxide-Semiconductor: MNOS Memory Transistor. Usually it has a variable threshold voltage. Some devices with this layer sequence have fixed threshold voltages.

MOS transistor. A type of IGFET, referring specifically to the layer sequence in the gate region of the IGFET, namely, Metal-Oxide-Semiconductor.

n-channel device. IGFET where source and drain are regions of n-type conductivity.

nonsaturation region of an IGFET. A portion of the I_{DS} versus V_{DS} characteristic where I_{DS} is strongly dependent on V_{DS} . This is true when $0 < |V_{DS}| < |V_{GS} - V_T|$.

p-channel device. IGFET where source and drain are regions of p-type conductivity.

radiation induced data loss characteristic. The collection of threshold voltage data as a function of total dose or dose rate after initial high-conduction or low-conduction threshold voltage levels had been written into the device.

rads in Si. Amount of radiation measured by its ionizing effect in silicon; 1 rad equals 100 erg of energy deposited in a gram of irradiated solid. This number can be translated into the density of electron-hole pairs (ehp/cm³) by the following operation:

$$n_{eh} [\text{ehp/volume}] = \gamma [\text{energy/mass}] \times \rho [\text{mass/volume}] \times N_{eh} [\text{ehp/energy}],$$

where

n_{eh} = volume density of ehp,

γ = total radiation dose as energy dissipated per unit mass, typically expressed in rads,

ρ = density of solid in mass/volume,

N_{eh} = number of ehp's created per energy dissipated.

In many solids, $N_{eh} \sim 1/bE_g$, and in silicon particularly, $b = 3.6[\text{ehp}]^{-1} \cdot *$

read delay t_{rd} . Time period between the end of the writing pulse and the start of the read condition (see for instance Fig 6.)

read disturb. A change in the instantaneous threshold voltage of an MNOS transistor due to the very act of measuring it.

read-mostly devices. MNOS memory transistors whose retention under constant read condition is in excess of one year. This makes these devices applicable in EAROMs (electrically-alterable read-only memories). A typical writing pulse width is 1 ms.

retention. The time period defined by the time elapsed between the instant of writing an MNOS transistor into a given (HC or LC) state, and the instant when either state becomes indistinguishable from the other.

retention characteristic. A plot of both HC and

*[15], and $E_g = 1.0\text{eV}$. This means that one ehp is created per 3.6 electron-volts of energy dissipated. In order to permit the use of the total dose expressed in rads directly, use is made of the identity that 1 erg = 6.2×10^{11} eV. From this $N_{eh} \sim 6.2 \times 10^{11} [\text{eV/erg}] [\text{ehp}]/3.6[\text{eV}]$, and since 1 rad = 100 ergs/g, this makes $N_{eh} \sim 1.7 \times 10^{13} [\text{ehp/g rads}]$. Thus, for silicon, $n_{eh} [\text{ehp/cm}^3] = 1.7 \cdot 10^{13} \times \gamma [\text{rads}] \times \rho [\text{g/cm}^3]$.

LC threshold voltages (ν_{HC} or ν_{LC}) as a function (commonly the logarithm) of the time t_{rd} elapsed after the instant of writing.

saturation region of an IGFET. A portion of the I_{DS} versus V_{DS} characteristic where I_{DS} is nearly constant regardless of the value of V_{DS} . This is true when $|V_{DS}| \gg |V_{GS} - V_T|$.

source. Region in the device structure of an IGFET which contains the terminal from which charge carriers flow into channel toward the drain. It has the potential which is less attractive than the drain for the carriers in the channel.

static radiation test. Test of the more or less permanent changes induced by radiation obtained by a comparison of characteristics before and after exposure.

stepped-gate structure. Also source-drain protected structure: a variant of the MNOS transistor whose gate dielectric along the channel is divided into two or three parts. One portion has the standard MNOS layer sequence of the memory device. On one or either side of the memory portion, particularly covering the lines where source and drain junction emerge at the silicon surface, is a gate dielectric that is used for the threshold IGFET in a given technology.

substrate. This IGFET region separates source from drain and is of opposite conductivity type. The potential on the substrate terminal can only be equally, or less attractive to the carriers in the channel than the source terminal.

threshold center voltage V_{TC} . The algebraic average of the HC and LC threshold voltages; that is, $(V_{LC} + V_{HC})/2$.

threshold voltage. Minimum gate voltage necessary for onset of current flow between source and drain of an IGFET. This is a serviceable general definition. There are three more specific definitions possible (refer to 4.1.3 for meaning of symbols).

$$(1) V_T = V_{GS} \text{ at } I_{DS} = 10 \mu\text{A},$$

$$\text{when } V_{GS} = V_{DS},$$

that is, V_T is the gate voltage necessary to result in a defined low current level;

$$(2) V_T = V_{GS} - \left[\frac{I_{DS} \ell}{k'W} \right]^{1/2},$$

that is, V_T is that value that gives the best fit to the I - V relationship of the IGFET;

$$(3) V_T = \phi_{ms} + \phi_s - \frac{Q_B}{C_G} - \frac{Q_I}{C_G},$$

that is, V_T is derived from inherent structural parameters only.

Definition (1) is commonly used in practice, and its use will be implied here unless otherwise specified. While normally I_{DS} is set at 10 μ A, a value of I_{DS} independent of lateral geometry is $I_{DS} = 0.5$ (W/ ℓ) μ A. Definition (3) suffers from the fact that in packaged devices, none of the terms can be verified by independent measurement.

threshold voltage saturation. For a given gate-to-source voltage, the transistor MNOS threshold voltage achieved in either of the two written states for which an order of magnitude increase in pulse width causes less than a 100 mV change in threshold voltage. This pulse width can also be achieved by sequence of shorter pulses of the same polarity.

threshold voltage window (Δv_{HL}). The algebraic difference between the two threshold voltages (the threshold voltage after a write-high operation minus the threshold voltage after a write-low operation).

total dose. The total amount of ionizing radiation deposited in the active area of a device over a given period of time. The unit of measure for total dose most commonly used in the present context is rads (Si).

triode region of an IGFET. The same as non-saturation region.

variable threshold transistor. An IGFET whose threshold voltage can be varied electrically to predetermined levels. The MNOS memory transistor is a specific example of this type.

walkout of reverse drain breakdown. This term describes an effect where the reverse current-voltage characteristic of the drain junction changes with time toward larger voltages as a function of applied bias. This effect is generally reversible.

wearout of reverse drain breakdown. This term describes an effect where the reverse current-voltage characteristic of the drain junction changes progressively and irreversibly

toward larger (leakage) currents at the same reverse voltages.

write high. Process of generating a threshold voltage condition which increases source to drain current (high-conductance state) for a given gate to source voltage.

write low. Process of generating a threshold voltage condition which decreases source to drain current (low-conductance state) for a given gate to source voltage.

writing characteristic. The collection of high-conduction and low-conduction threshold voltage data as a function of the writing pulse width of both writing voltage polarities.

zero bias retention t_{R0} . Also, relaxation time. This is the retention inherent in the MNOS transistor when all terminals are grounded during information storage. The time period is defined by an (extrapolated) zero window between the two HC and LC threshold voltage curves plotted versus the logarithm of t_{rd} , the time elapsed between writing and threshold voltage measurement.

3. References

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