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(Revision of IEEE 595-1976)

IEEE Standard Serial Highway Interface System (CAMAC¹)

Sponsor

**Instrumentation and Detectors Committee
of the
IEEE Nuclear and Plasma Sciences Society**

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Foreword

[This Foreword is not a part of ANSI/IEEE Std 595-1982, IEEE Standard Serial Highway Interface System (CAMAC).]

This standard defines a serial highway interface system for use with CAMAC crate assemblies in accordance with ANSI/IEEE Std 583-1982, Modular Instrumentation and Digital Interface System (CAMAC), and with other controlled devices. It is based on ERDA² Report TID-26488, Dec 1973, and ESONE Report ESONE/SH/01, Nov 1974 (modified by subsequently issued supplements), as developed by the NIM Committee of the US Department of Energy,* and the ESONE Committee of European Laboratories.** A parallel highway interface system, also intended for use with ANSI/IEEE Std 583-1982, is defined in ANSI/IEEE Std 596-1982, Parallel Highway Interface System (CAMAC). A report essentially identical to ANSI/IEEE Std 595-1982 has been issued by the ESONE Committee as EUR 6100.

This standard was reviewed and balloted by the Nuclear Instruments and Detectors Committee of the IEEE Nuclear and Plasma Sciences Society. Because of the broad applicability of this standard, coordination was established with numerous IEEE societies, groups, and committees, including the Communications Society, Computer Society, Industry Applications Society, Industrial Electronics and Control Instrumentation Group, Instrumentation and Measurement Group, and the Power Generation and Nuclear Power Engineering Committees of the Power Engineering Society. The revision of this standard was in conjunction with the 1981 review (1982 issue) of the entire family of IEEE CAMAC standards, undertaken to incorporate existing addenda and corrections directly into the standard.

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Abbreviations and Symbols used in this Standard

A	Subaddress (Dataway signal) ⁵
ACL	Auxiliary Controller Lockout
B	Busy (Dataway signal) ⁵
BCK	Byte Clock
C	Clear (Dataway signal) ⁵
CBY	Controller Busy
DSBY	Demand Busy
DERR	Delayed Error
DMI	Demand Message Initiate
DSQ	Delayed Q Response
DSX	Delayed Command Accepted Response
ERPT	External Repeat
ERR	Error bit
I	Inhibit (Dataway signal) ⁵
L	Look-at-Me (Dataway signal) ⁵
LAM	Look-at-Me (Demand)
LSB	Least Significant bit
MI	Message Identification
MSB	Most Significant bit
N	Station Number (Dataway signal) ⁵
NRZL	Non-Return-to-Zero-Level
PH	Parallel Highway of ANSI/IEEE Std 596
Q	Response, Status (Dataway signal) ⁵
S	Prefix for Serial Highway fields and bits
S1	Strobe (Dataway signal) ⁵
S2	Strobe (Dataway signal) ⁵
SA	Subaddress bit
SC	Crate Address bit
SCC	Serial Crate Controller
SCC-L2	Serial Crate Controller, Type L2
SD	Serial Driver
SF	Function bit
SGL	Serial Graded LAM (Demand)
SGLE	Demand Message bits from SGL-Encoder
SH	Serial Highway of ANSI/IEEE Std 595
SLP	Selected LAM Present
SN	Station Number bit
SQ	Q Response bit
SR	Read bit
STIM	Start Timer
SW	Write bit
SX	Command Accepted bit
T	Clock Period
TIMO	Time-Out
X	Command Accepted (Dataway signal) ⁵
Z	Initialize (Dataway signal) ⁵

⁵ANSI/IEEE Std 583-1982

CAMAC and NIM Standards and Reports

Title	IEEE, ANSI Std No	IEC No	DOE No	EURATOM (EUR) or ESONE No
CAMAC Instrumentation and Interface Standards*	SH08482* (Library of Congress No 8185060)	—	—	—
Modular Instrumentation and Digital Interface System (CAMAC)	ANSI/IEEE Std 583-1982	516	TID-25875 [†] and TID-25877 [†]	EUR 4100e
Serial Highway Interface System (CAMAC)	ANSI/IEEE Std 595-1982	640	TID-26488 [†]	EUR 6100e
Parallel Highway Interface System (CAMAC)	ANSI/IEEE Std 596-1982	552	TID-25876 [†] and TID-25877 [†]	EUR 4600e
Multiple Controllers in a CAMAC Crate	ANSI/IEEE Std 675-1982	729	DOE/EV-0007	EUR 6500e
Block Transfers in CAMAC Systems	ANSI/IEEE Std 683-1976 (Reaff 1981)	677	TID-26616 [†]	EUR 4100 suppl
Amplitude Analog Signals within a 50 Ω System	—	—	TID-26614	EUR 5100e
The Definition of IML: A Language for Use in CAMAC Systems	—	—	TID-26615	ESONE/IML/01
CAMAC Tutorial Articles	—	—	TID-26618	—
Real-Time BASIC for CAMAC	ANSI/IEEE Std 726-1982	‡	TID-26619 [†]	ESONE/RTB/03
Subroutines for CAMAC	ANSI/IEEE Std 758-1979 (Reaff 1981)	713	DOE/EV-0016 [†]	ESONE/SR/01
Recommendations for CAMAC Serial Highway Drivers and LAM Graders for the SCC-L2	—	—	DOE/EV-0006	ESONE/SD/02
Definitions of CAMAC Terms	Included in SH08482	678	DOE/ER-0104	ESONE/GEN/01
Standard Nuclear Instrument Modules NIM	—	547 [§]	TID-20893 (Rev 4)	—

*This is a hard cover book that contains ANSI/IEEE Std 58-1982 , ANSI/IEEE Std 595-1982 , ANSI/IEEE Std 596-1982 , ANSI/IEEE Std 675-1982 , ANSI/IEEE Std 683-1976 (Reaff 1981), ANSI/IEEE Std 726-1982 and IEEE Std 758-1979 (Reaff 1981), plus introductory material and a glossary of CAMAC terms.

[†]Superseded by corresponding IEEE Standard listed.

[‡]In preparation.

[§]Covers only mechanical features and connector pin assignments.

NOTE — Availability of Documents

ANSI	Sales Department, American National Standards Institute, 1430 Broadway, New York, NY 10018.
IEEE	IEEE Service Center, 445 Hoes Lane, Piscataway, New Jersey 08854, USA.
IEC	International Electrotechnical Commission, 1, rue de Varembe, CH-1211 Geneva 20, Switzerland.
DOE and TID Reports	National Bureau of Standards, Washington, D.C. 20234, USA, Attn: L. Costrell.
EURATOM	Office of Official Publications of the European Communities, P.O. Box 1003, Luxembourg.
ESONE	Commission of the European Communities, CGR-BCMN, B-2440 GEEL, Belgium, Attn: ESONE Secretariat, H. Meyer.

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An American National Standard

IEEE Standard Serial Highway Interface System (CAMAC)

1. Introduction

1.1 Aims

This standard defines a Serial Highway (SH) system using byte-organized messages, and configured as a unidirectional loop to which are connected a system controller and up to sixty-two CAMAC* crate assemblies in accordance with ANSI/IEEE Std 583-1982, [Modular Instrumentation and Digital Interface System (CAMAC*)] or other controlled devices. The highway transfers data and control information in either bit-serial mode (using one data signal and a bit-clock signal) or byte-serial mode (using eight data signals and a byte-clock signal). Clock rates up to 5 MHz may be used, depending on individual system characteristics.

In the primary application the controlled devices are CAMAC-crate assemblies, with Serial Crate Controllers (SCCs) which conform to a defined message structure. In this application the SH is intended to complement the Parallel Highway (PH) defined in ANSI/IEEE Std 596-1982, Parallel Highway Interface System (CAMAC). It will be attractive in certain applications that the PH was not designed to cover, for example, where there are long distances between crates, or where simplicity of inter-connections is desirable. However, the time required to perform a complete operation, including a Dataway cycle, will generally be longer in a serial system than on the PH.

In other applications, some or all of the controlled devices connected to the SH can be equipment that conforms to a subset of the full specification, and is not necessarily constructed in CAMAC format or controlled by CAMAC commands. SCCs conforming to the full specification and devices conforming to the subset can coexist on the highway without mutual interference. Other devices and buses, such as that of IEEE Std 488-1978, Digital Interface for Programmable Instrumentation and Related System Components, can be readily incorporated into the system through an interfacing module.

The SH system is defined primarily in terms of the message format and signal standards at the input and output ports of devices connected to the highway. Interconnections between devices may be made directly, using the defined signal standards, or indirectly through communications channels with other signal standards and types of modulation.

A recommended SCC Type L2 is defined and provides facilities for either bit-serial or byte-serial operation.

1.2 Interpretation

This standard is a reference text describing and specifying the CAMAC SH system. It should be read in conjunction with, and is supplementary to ANSI/IEEE Std 583-1982 .

No part of this standard is intended to supersede or modify ANSI/IEEE Std 583-1982 .

In this standard there are mandatory requirements, recommendations, and examples of permitted practice.

Mandatory clauses of the standard are enclosed in blocks, as here, and usually include the word *must*.

Definitions of recommended or preferred practice (to be followed unless there are sound reasons to the contrary) include the word *should*.

Examples of permitted practice generally include the word *may*, and leave freedom of choice to the designer or user.

In order to *conform* with the specification of the CAMAC SH system, an equipment or system must satisfy all the mandatory requirements in this standard, excluding the Appendix. If constructed as a CAMAC plug-in unit, the equipment must also satisfy the mandatory requirements of ANSI/IEEE Std 583-1982.

Section A1. of this standard's appendix defines SCC Type L2 in such a way that operationally interchangeable units can be produced by different manufacturers. The main text of this specification contains a less restrictive definition of SCCs that are not necessarily interchangeable.

The single letter designations *L*, *M*, *N*, *P*, and *R* (prefixed in some cases by "CC") are reserved for future use in connection with this standard and are not to be used until assigned.

In order to *conform* with this specification of the CAMAC SCC Type L2, an equipment must satisfy all the mandatory requirements of Section A1 of the appendix to this standard.

In order to be *compatible* with the CAMAC SH system, equipment need not satisfy all the mandatory requirements, but must not interfere with the full operation of all the features of the SH and SCC (including Type L2) as defined in this standard.

No part of this standard is intended to exclude the use of equipment that is compatible in the preceding sense, even if it does not conform fully to the specification or is not constructed as CAMAC plug-in units.

No license or other permission is needed in order to use this standard.

2. Principles of the Serial Highway System

This section summarizes the basic principles that apply to all devices connected to the SH.

All other sections of this standard are concerned with the primary application, where the connected devices are CAMAC crate assemblies with SCCs.

2.1 Configuration

The SH interconnects a master device [the Serial Driver (SD)] and up to sixty-two CAMAC crate assemblies or other controlled devices. At any time there is only one active master device, but the standard does not exclude systems in which more than one device is capable of acting as master. Fig 2-1 shows the basic configuration.

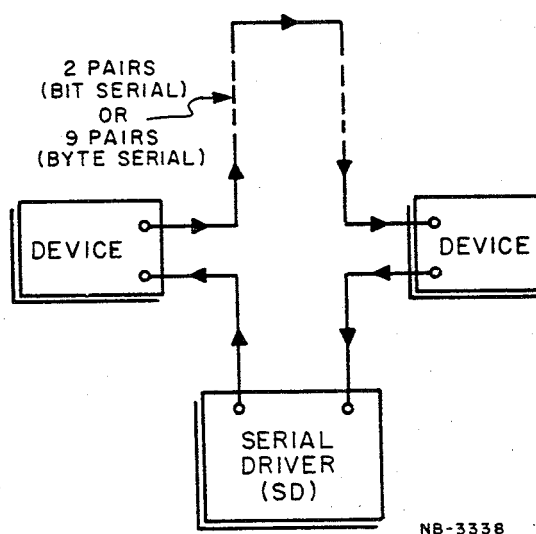


Figure 2-1—CAMAC SH Loop Configuration (Sixty-Two Addressable Devices)

The addressing scheme allows a maximum of sixty-two controlled devices, whose assigned addresses need not be related to the actual sequence of devices along the highway.

The SH forms a unidirectional loop from the output port of the SD, through each controlled device in turn, and back to the input port of the SD. (When describing conditions with respect to a particular device, it is often convenient to use the term 'upstream' to refer to the part of the SH between the output port of the SD and the device, and the term 'downstream' to refer to the part between the device and the input port of the SD.)

2.2 Messages

All messages transmitted on the SH consist of sequences of 8-bit bytes as shown in Fig 2-2. All information related to the message is contained within these 8-bit bytes.

The 8 bits constituting a byte are labeled Bit 1 (least significant) to Bit 8 (most significant). In all bytes, Bits 1–6 are available for information fields.

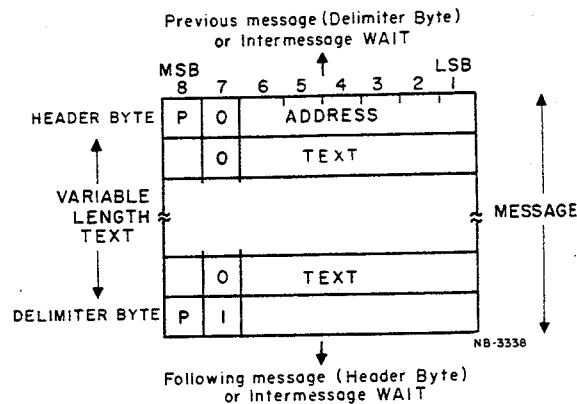


Figure 2-2—Basic Message Format

Bit 7 of every byte is a *Delimiter* bit, which allows receiving devices to identify the first and last bytes of each message.

Bit 8 is available for use as an odd-parity bit (with appropriate value so that the byte contains an odd number of bits in the logic **1** state). It is always used in this way in the first and last bytes of a message, and in all bytes of messages associated with CAMAC SCCs.

Every message starts with a *Header* byte. This includes a device address (a Crate Address when the device is an SCC). In a message from the SD the Header byte contains the address of the destination. In a message to the SD it contains the address of the source. Bit 7 of the Header byte is at logic **0** and Bit 8 conserves odd parity over the whole byte.

Every message ends with a *Delimiter* byte, in which Bit 7 is at logic **1**, and Bit 8 conserves odd parity.

The length and content of the 'text' between the Header byte and the Delimiter byte of a message can be chosen to suit the needs of the individual device. In principle it need not be uniform for all devices in a system. In each byte between the Header byte and the Delimiter byte, Bit 7 is at logic **0**.

If there are any bytes between the Delimiter byte of one message and the Header byte of the next, they are also Delimiter bytes, with Bit 7 at logic **1**.

Thus, the Header byte of a message can be identified because, after one or more bytes with Bit 7 at logic **1**, it is the first byte with Bit 7 at logic **0**. Similarly, the last byte of a message can be identified because, after one or more bytes with Bit 7 at logic **0**, it is the first byte with Bit 7 at logic **1**.

Error detection over a block of bytes constituting a message or part of a message can be provided by the combination of byte parity in Bit 8 of each byte and a set of column-parity bits in bits 1–6 of the last byte of the block. This *Geometric Error-Detection* code detects all 1 bit, 2 bit, and 3 bit errors, and most errors with 4 bits or more. The scheme offers good protection against bursts of errors and is easy to implement by hardware or software.

2.3 Transmission of Bytes

Bytes are transmitted either in bit-serial mode (using one data signal and an accompanying bit-clock signal) or in byte-serial mode (using eight data signals and an accompanying byte-clock signal). In bit-serial mode the 8-bit byte is transmitted with the least significant bit (Bit 1) first. It is preceded by a Start bit (logic **0**) and followed by a Stop bit and optional Pause bits (logic **1**), as shown in Fig 2-3. The Start and Stop bits form a 'byte frame' from which receiving devices can recover a byte clock.

In the text of this standard, the bit pattern of an 8-bit byte with least significant bit l and most significant bit m is represented by the bit string $(miiiiil)_2$. The same byte with Start and Stop bits is represented by the bit string $(1, miiiiil, 0)_2$.

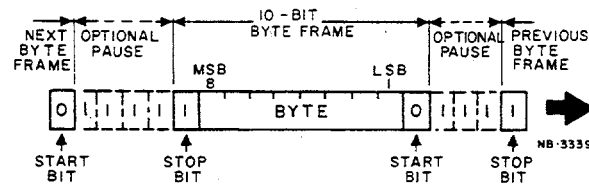


Figure 2-3—Bit-Serial Byte Frame

The message structure and protocol of the SH are identical in the two modes of transmission.

Throughout an SH system, bytes are transferred in synchronism with the byte clock, which accompanies the data in byte-serial mode and is derived from the byte framing in bit-serial mode.

In each byte-clock period, each device receives 1 byte and transmits 1 byte, but the contents (Bits 1 to 8) of the received and transmitted bytes are not always identical. Devices normally retransmit the contents of all received bytes, although the contents of a byte received in 1 byte period may be retransmitted in a later byte period. A device can generate a message by interrupting this process of retransmission. The contents of the required number of bytes are generated by the device, and the contents of a corresponding number of received bytes are not retransmitted. The message protocol should ensure that these received bytes do not contain important information. For example, they may be SPACE or WAIT bytes as defined in Section 3.

2.4 System Clock

System-clock signals, at bit rate or byte rate as appropriate, are generated at one point in the system (usually at or in the SD) and are retransmitted by each device connected to the SH.

The clock rate is therefore uniform throughout a system. The absolute maximum clock rate is 5.0 MHz, but the performance of the communications channels or of the connected devices may require a lower clock rate in particular systems.

2.5 Serial Highway Ports

The characteristics of the SH (such as signal standards, timing, message structure, and type of connector) are defined with respect to the ports¹ where the highway enters and leaves each connected device.

Nothing in this standard excludes the use of different standards within the connected devices or within any communications channel used between devices.

All devices connected to the highway have two ports, one for input and one for output. These ports either conform to the defined D -port standards or are related to the standards in such a way that the device could, in principle, be connected to D ports through an appropriate adaptor.

¹The term port implies an entrance or exit of a network, etc.

At each *D* port the data and clock signals are of balanced Non-Return-to-Zero-Level (NRZL) type, compatible with an existing standard (see Section 7.) for balanced voltage digital interface circuits. Each signal is carried by a separate pair of wires and is generated by a balanced transmitter and received by a differential receiver.

At each *D* port there is one pair of contacts for the system clock (at bit rate or byte rate) plus eight pairs for data (only one pair of which is used in bit-serial mode).

A section of the SH can be formed by a direct connection between the output *D* port of one device and the input *D* port of the next device, as shown in Fig 2-4, typically using dedicated 100 Ω twisted-pair cable. Alternatively, any section of the SH can include a communications channel whose signal standards and modulation technique are chosen to suit the particular overall system requirements, as shown in Fig 2-5. In this case, signal conditioning units are needed to convert the data and clock signals from the *D*-port standard to the communications-channel standard, and back to the *D*-port standard. In the context of this standard any interconnections that do not use the *D*-port standard are undefined and are described as *U*-port standards. Although the data and clock signals are on separate wire pairs at the *D* ports, they may be combined into one unidirectional channel between *U* ports, for example, by using a suitable modulation technique.

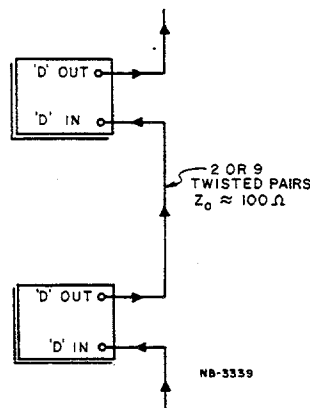


Figure 2-4—Direct D-Port Interconnection

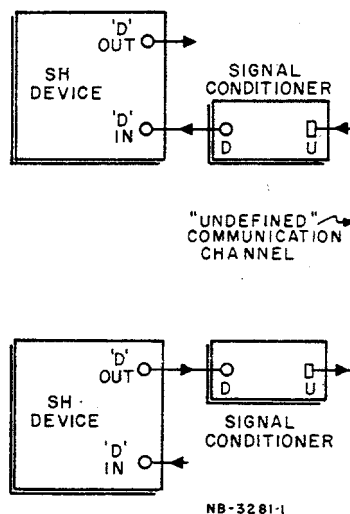


Figure 2-5—Indirect Connection Via Undefined Standard

Within an SH system some sections of the highway may use *D*-port standards while others use various *U*-port standards, all at the same system-clock rate. For example, a cluster of adjacent devices can have direct interconnections between *D* ports, with perhaps one signal conditioning unit at the input to the cluster and another at the output from the cluster.

2.6 Serial Driver

The SD is the link between the SH and (directly or indirectly) a computer or other system controller. It consists of a transmitting section associated with a *D*-output port, and a receiving section associated with a *D*-input port.

The transmitting section typically accepts commands and data from the computer and assembles them into the appropriate message format with Header byte and Delimiter byte. It transmits the resulting bit or byte stream to the SH, accompanied by the system-clock signals at bit or byte rate. It may generate an Error-Detection code within messages and interpose bytes between successive messages.

The receiving section typically accepts the bit or byte stream from the SH, together with the system-clock signals. It identifies the byte and message format, and passes the data, demands, and status information to the computer. It may check the Error-Detection code, implement error-recovery procedures, and discard any intermessage bytes.

The SD reacts to all messages received at its *D*-input port, whereas other devices only react to messages that are addressed to them.

This standard defines the SD only in terms of the signals, message structures, and message sequences at its *D* ports. Many of the activities concerned with generating and receiving messages can be handled either by hardware in the SD or by software in the associated computer.

Asynchronous serial communications ports are available on most modern minicomputers for interfacing to teletypewriters, visual display units, modems, etc. These ports can drive the SH in bit-serial mode through a simple adaptor, which is thus a special case of the SD.

2.7 Extended Uses of the Serial Highway

Every controlled device connected to the SH is transparent to messages that are addressed to other devices, irrespective of the internal structure or length of these messages. The SH can thus support many different types of compatible devices, provided these conform to the basic rules for signal standards, and the use of Header bytes and Delimiter bits to define the beginning and end of messages.

Compatible devices connected to the SH can consist, for example, of those shown in Fig 2-6:

- 1) CAMAC crates with recommended SCCs Type L2, conforming to Section A1. of this standard's appendix, and using the CAMAC message structures defined in this standard

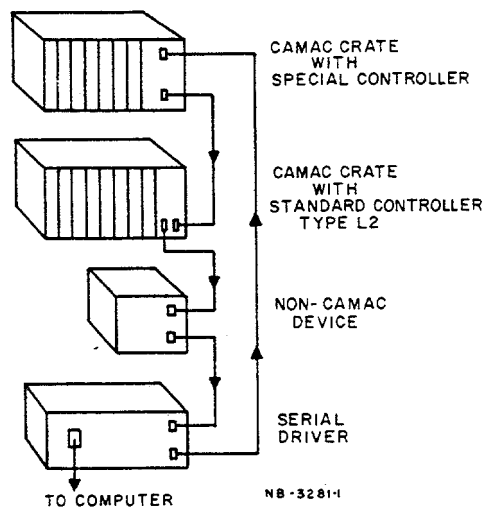


Figure 2-6—Compatible Devices

MSB		8	7	6	5	4	3	2	1	LSB	
b	0	SC32						SC1		HEADER BYTE	
b	0	0		0		SA8		SA1		BYTE 2	
b	0	1	SF16					SF1		BYTE 3	
b	0	1	SN16					SN1		BYTE 4	
b	0	SW24						SW19		BYTE 5 *	
b	0	SW18						SW13		BYTE 6 *	
b	0	SW12						SW7		BYTE 7 *	
b	0	SW6						SW1		BYTE 8 *	
b	0	c	c	c	c	c	c	SUM BYTE			
1	0	1	1	1	1	1	1	SPACE BYTES AS REQUIRED			
1	0	1	1	1	1	1	1				
1	1	1	0	0	0	0	0	0	END BYTE		
NB-3334											

NB-3334

- b* odd byte-parity bits
c Even column-parity bits
 * Bytes 5, 6, 7, 8 included if $SF16 = 1$ and $SF8 = 0$

Figure 3-1 — Command Message: Bit Assignments

- 2) CAMAC crates with other SCCs, conforming to the main body of this standard, and using messages that are possibly variants or extensions of the standard CAMAC messages
- 3) Devices in other mechanical formats or using other message structures

2.8 Serial Crate Controller

When a CAMAC crate assembly is connected to the SH, an SCC is used as the link between the SH and the Dataway highway in the crate. An SCC is a multiwidth CAMAC plug-in unit, occupying two or more stations, with Dataway connectors for the Control station and at least one Normal station. It has front-panel connectors for the two *D* ports.

3. Message Structure for Serial Crate Controllers

When a CAMAC crate with SCC conforming to this standard is connected to the SH, the message structure includes the following features:

Three types of messages are used by SCCs. *Command messages* are generated by the SD and instruct an addressed SCC to perform a CAMAC operation. The addressed crate controller should transmit a truncated form of the Command message. In response to a Command message the addressed crate controller sends a *Reply message* to the SD. The Command message from the SD to an SCC, and the resulting Reply message from the SCC to the SD, constitute a *Command/Reply transaction*. Any SCC may generate a *Demand message* to indicate that there is a Look-at-Me (LAM) request on the Dataway in the crate.

Bits in SH messages are distinguished from corresponding Dataway signals by the prefix *S*. For example, the bits *SA1-SA8* correspond to Dataway signals *A1-A8*.

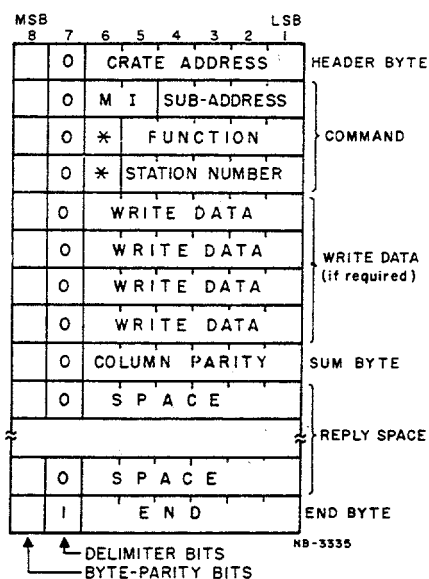
3.1 Command Message

Command messages can be either complete or truncated.

3.1.1 Complete Command Messages

The complete Command message must have the structure shown in Fig 3-1, where the group of bytes 5-8 is included for Write commands (*SF16=1* and *SF8=0*), but is omitted for Read and Control commands. The message must be transmitted as a consecutive sequence of bytes, starting with the Header byte (Crate Address) and finishing with the END byte.

The complete Command message consists of the following bytes, as shown in Fig. 3-2: a Header byte, in which the Crate Address field indicates the destination of the message; 3 bytes containing the Subaddress, Function, and Station Number fields of the CAMAC command; 4 bytes containing the 24 bit Write data, which are omitted when not required; and a SUM byte. This part of the message allows the addressed crate to assemble, check, and execute the CAMAC command. The message continues with a sequence of SPACE bytes (see Section 3.5.7) providing the opportunity for the SCC to transmit a reply; and concludes with an END Delimiter byte (see Section 3.5.3).

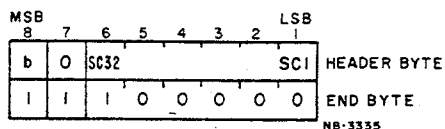


- * Reserved bits
MI Message Identifier Field

Figure 3-2 — Command Message: Field Assignments

3.1.2 Truncated Command Message

The addressed SCC should transmit a truncated form of the Command message, consisting of the Header byte followed by an END byte (see Fig 3-3 and 3-4, and Section 4.5).



- b* Odd byte-parity bit

Figure 3-3 — Truncated Command Message: Bit Assignments

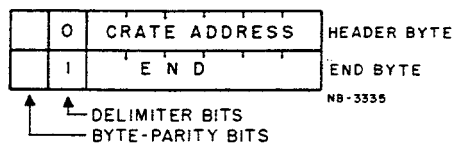
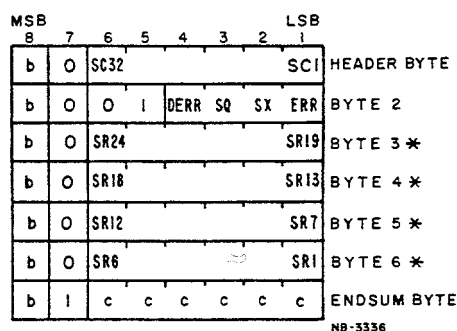


Figure 3-4 — Truncated Command Message: Field Assignments

3.2 Reply Message

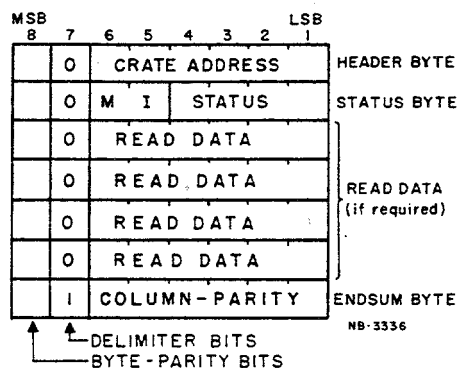
The Reply message must have the structure shown in Fig 3-5, where the group of bytes 3-6 is included in the reply to a Read command ($SF16=0$ and $SF8=0$) but is omitted in the reply to other commands. The message must be transmitted as a consecutive sequence of bytes, starting with the Header byte (Crate Address) and finishing with the ENDSUM byte.

Thus the Reply message consists of the following bytes, as shown in Fig 3-6: a Header byte, in which the Crate Address field indicates the source of the message; a Status byte; 4 bytes containing 24 bit Read data, which are omitted when not required; and an ENDSUM Delimiter byte.



- b* Odd byte-parity bits
c Even column-parity bits
 * Bytes 3, 4, 5, 6, included if $SF16 = 0$ and $SF8 = 0$

Figure 3-5 — Reply Message: Bit Assignments



MI Message Identifier Field

Figure 3-6 — Reply Message: Field Assignments

3.3 Demand Message

The Demand message must have the structure shown in Fig 3-7. The message must be transmitted as a consecutive sequence of bytes, starting with the Header byte (Crate Address) and finishing with the ENDSUM byte.

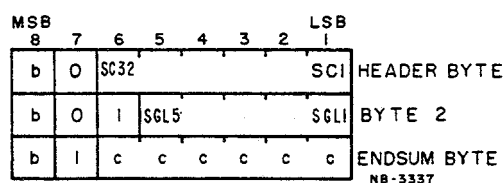
Thus the Demand message consists of the following bytes, as shown in Fig 3-8: a Header byte in which the Crate Address field indicates the source of the message; a byte further identifying the demand; and an ENDSUM Delimiter byte.

3.4 Message Fields

The information in the Command, Reply, and Demand messages is divided into message fields as follows:

3.4.1 Crate Address Field (6 Bits; SC1–SC32)

This field defines the destination address in Command messages and the source address in Reply and Demand messages.



b Odd byte-parity bits
c Even column-parity bits

Figure 3-7 — Demand Message: Bit Assignments

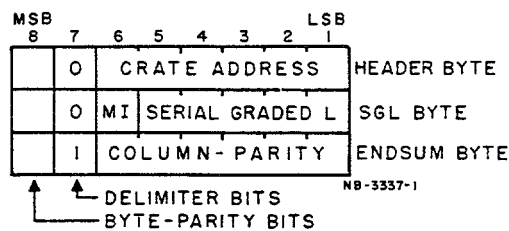
Each SCC must respond to any address assigned to it from the set $01_8 - 76_8$ and must not respond to either 00 or 77_8 .

The address 00 is reserved for use at the SD. Under certain error conditions a SPACE byte can be falsely identified as a Header byte. The recommended SPACE byte has a bit pattern corresponding to address 77_8 . This address is therefore not used, and there are 76_8 (62_{10}) available crate addresses.

3.4.2 Station Number Field (5 Bits: SN1-SN16)

This field in the Command message defines the Station Number within the CAMAC crate (see Section 5.1.1 of IEEE Std 583-1975).

In general the codes $N(1)$ to $N(23)$ are used as addresses of modules in the CAMAC crate. Internal features of the SCC are addressed by $N(30)$ (see Section 11.).



MI Message Identification Field

Figure 3-8 — Demand Message: Field Assignments

3.4.3 Subaddress Field (4 Bits; SA1-SA8)

This field in the Command message defines a subaddress at the selected station in the crate (see Section 5.1.2 of ANSI/IEEE Std 583-1982).

3.4.4 Function Field (5 Bits; SF1-SF16)

This field in the Command message defines the action to be performed at the selected Station and Subaddress in the crate (see Section 5.1.3 of ANSI/IEEE Std 583-1982).

The values of *SF16* and *SF8* in this field distinguish between Read, Write, and Control commands, and hence determine whether a data field is included in the Command or Reply message. The lengths of the Command and Reply messages corresponding to the various values of *SF16* and *SF8* are summarized in Table 3-1.

Table 3-1 — Length of Command/Reply Transactions

Operation	Function Field		Number of Bytes		
	F16	F8	Command from Header to SUM Inclusive	Reply from Header to END SUM Inclusive	Command Reply Transaction
Read	0	0	5	7	12*
Control	0	1	5	3	8*
	1	1	5	3	8*
Write	1	0	9	3	12*

*Minimum length, assuming that Reply Header is transmitted by SCC as First SPACE Byte is received and END SUM is transmitted as END Byte is received.

3.4.5 Write-Data Field (24 Bits; SW1-SW24)

This field is included in the Command message if *SF16*=1 and *SF8*=0. It contains the data associated with a Write command.

3.4.6 Read-Data Field (24 Bits; SR1-SR24)

This field is included in the Reply message if the Function field of the Command message had *SF16*=0 and *SF8*=0. It contains the data requested by a Read command.

3.4.7 Message Identification Field (2 Bits; M1-M2)

This field in the Command and Reply messages (2 bits) and in the Demand message (only $M2$) is used to identify the three types of message.

The significance of the Message Identification (MI) field must be as shown in Table 3-2.

This field is needed by the SD in order to distinguish between Reply and Demand messages of equal length. It may also be used by SCC to identify Command messages, as additional security against executing false commands.

Table 3-2—Contents of Message Identification Field

Message	Message Identification Field	
	M2	M1
Command	0	0
Reply	0	1
Demand	1	—

3.4.8 Status Field (4 Bits; Error, Response, Command Accepted, Delayed Error)

This field in the Reply message shows how the SCC has responded to the Command message. The Error (ERR) bit indicates whether the error detection checks on the Command message were satisfactory (see Section 15.5.1). The Delayed Error (DERR) bit provides similar information about the previous command. For a command that has been executed, the SQ and SX bits indicate the Response Q and Command Accepted X status of the feature of the module or controller that has been accessed by the command.

The contents of the Status field in the Reply message must conform to the requirements of Sections 12.2 and 15.5.

3.4.9 Serial Graded-L (SGL) Field (5 Bits; SGL1-SGL5)

This field of the Demand message identifies the type of demand, the source of the demand, or the action required by the demand. It may be derived from the L signals on the Dataway of the crate by any process of selection, grouping, priority coding, etc, that is performed by the SCC or by a separate SGL Encoder connected to the SCC (see Section 14.).

The SGL bit pattern 11111_2 must only be used to indicate the Hung Demand state (see Section 14.).

3.5 Formatting Bytes

The formatting bytes are an important part of the message structure, but do not contain information fields as defined in the previous section. They indicate the end of each message (END and ENDSUM), provide the column-parity component of the Geometric Error-Detection scheme (SUM and ENDSUM) and maintain the byte clock during intervals within messages (SPACE) and between messages (WAIT).

3.5.1 Delimiter Bytes

A Delimiter byte must have Bit 7 at logic 1, and Bit 8 with the appropriate value to conserve odd byte parity.

All other bytes that do not satisfy these conditions are Nondelimiter bytes. The class of Delimiter bytes includes END, ENDSUM, and WAIT bytes.

Delimiter bytes are used to indicate the last byte of each message and any bytes that occur between messages. Each message consists of a sequence of Nondelimiter bytes terminated by a Delimiter byte. It may possibly be followed by further Delimiter bytes (WAIT bytes). Delimiter bytes cannot occur legitimately elsewhere within messages.

Thus the first byte of a message (the Header byte) can be recognized by its context as the first Nondelimiter byte following one or more Delimiter bytes. The last byte of a message can be recognized by its context as the first Delimiter byte following one or more Nondelimiter bytes.

3.5.2 Column-parity Field

The SUM and ENDSUM bytes contain a column-parity field in Bits 1-6. This field provides the column-parity component of the Geometric Error-Detection scheme (see Section 15.3). Each bit of the column-parity field conserves even parity over the corresponding bit position in each byte, from the Header byte to the SUM or ENDSUM byte, inclusive.

The contents of the column-parity field are equivalent to the sum modulo-2 of all preceding bytes of the message, excluding bits 7 and 8 in each byte. (Hence the terms SUM and ENDSUM.)

3.5.3 END Byte

The END byte is a Delimiter byte generated by the SD to terminate complete Command messages and by SCCs to terminate truncated Command messages.

In the END byte, the Delimiter bit (Bit 7) is at logic 1, and Bit 8 conserves the odd byte parity.

An END byte, with bit-pattern 11100000_2 , equivalent to 340_8 , must be generated by the SD as the last byte of every Command message.

Although the END byte has the same binary pattern as the WAIT byte (see Section 3.5.4), it differs in context and in the requirements concerning its retransmission by SCCs. The END byte is always preceded by a Nondelimiter byte.

All unaddressed crate controllers must retransmit received END bytes unchanged. An addressed crate controller must either retransmit the received END byte of the Command message or replace it by an ENDSUM byte (see Section 4.1.4).

3.5.4 WAIT Byte

The WAIT byte is a Delimiter byte generated by the SD and by addressed SCCs. The SD may generate WAIT bytes between successive Command messages. An addressed SCC generates WAIT bytes, in response to received bytes, between the truncated Command message (see 3.1.2) and the Header byte of the Reply message and also, if required, between the ENDSUM byte of the Reply message and the completion of the Command/Reply transaction.

The WAIT byte has no information field, but the associated byte clock allows messages to propagate around the SH. Thus, although it is not mandatory for the SD to generate bytes during intervals between Command messages, the

generation of WAIT bytes is recommended in order to permit the propagation of Reply messages to be completed in a typical SH which includes logical delays.

Any bytes generated by an SD or SCC during intervals between messages must be WAIT bytes with the bit pattern 11100000_2 equivalent to 340_8 .

In this WAIT byte pattern, the Delimiter bit (Bit 7) is set to logic 1, and Bit 8 is at logic 1 to conserve odd byte parity over the whole byte.

The WAIT byte therefore has the same bit pattern as the END byte (see Section 3.5.3) but differs in context and in the requirements concerning its retransmission by SCCs. A WAIT byte always follows another Delimiter byte. Under certain conditions, connected with the generation of Demand messages, an SCC is permitted to transmit another byte in place of a received WAIT byte (see Section 5.).

A specific bit pattern has been defined for the WAIT byte in order to assist the process of establishing message synchronism (see Section 10.1.3), which normally takes place while the SD is generating a sequence of WAIT bytes. The chosen bit pattern is one of several that have the useful property, when they are transmitted repetitively in bit-serial mode, that each byte, including its associated Start and Stop bits, has only one transition from 0 to 1, and one transition from 1 to 0, thus assisting the establishment of byte synchronism.

3.5.5 ENDSUM Byte

The ENDSUM byte is a Delimiter byte, and is generated by SCC to terminate each Reply or Demand message. The column-parity field (Bits 1-6) conserves even column parity over all bytes between the Header byte and the ENDSUM byte, inclusive. The Delimiter bit (Bit 7) is at logic 1, and Bit 8 conserves odd byte parity.

3.5.6 SUM Byte

The SUM byte is a Nondelimiter byte, and is generated by the SD in the Command message (see Figs 3-1 and 3-2). The column-parity field (Bits 1-6) of this byte conserves even column parity over all bytes of the message between the Header byte and SUM byte, inclusive. The Delimiter bit (Bit 7) is at logic 0, and Bit 8 conserves odd byte parity over the whole of the SUM byte.

The addressed SCC uses the SUM byte in the Geometric Error-Detection test on the Command message, before deciding whether to execute the command.

3.5.7 SPACE Byte

The SPACE byte is a Nondelimiter byte. A sequence of SPACE bytes generated by the SD between the SUM and END bytes of the Command message forms the *Reply space*. The addressed SCC generates its Reply message in place of some or all of the SPACE bytes in the *Reply space*.

In the SPACE byte generated by the SD, the Delimiter bit (Bit 7) must be at logic 0, and Bit 8 must conserve odd byte parity.

The bit pattern of SPACE bytes generated by the SD should be 10111111_2 , equivalent to 277_8 .

An SSC that is expecting to receive SPACE bytes in the Reply space of a Command message must accept any Nondelimiter byte as a substitute for a SPACE byte.

Acceptable substitutes for SPACE bytes need not have the recommended bit pattern or conserve odd byte parity.

4. Command/Reply Message Sequences

This section defines the sequences of input and output bytes that occur when an SCC receives a Command message, performs a CAMAC Read, Write, or Control operation, and transmits a Reply message. Some features of the Reply space within the Command message are examined in more detail.

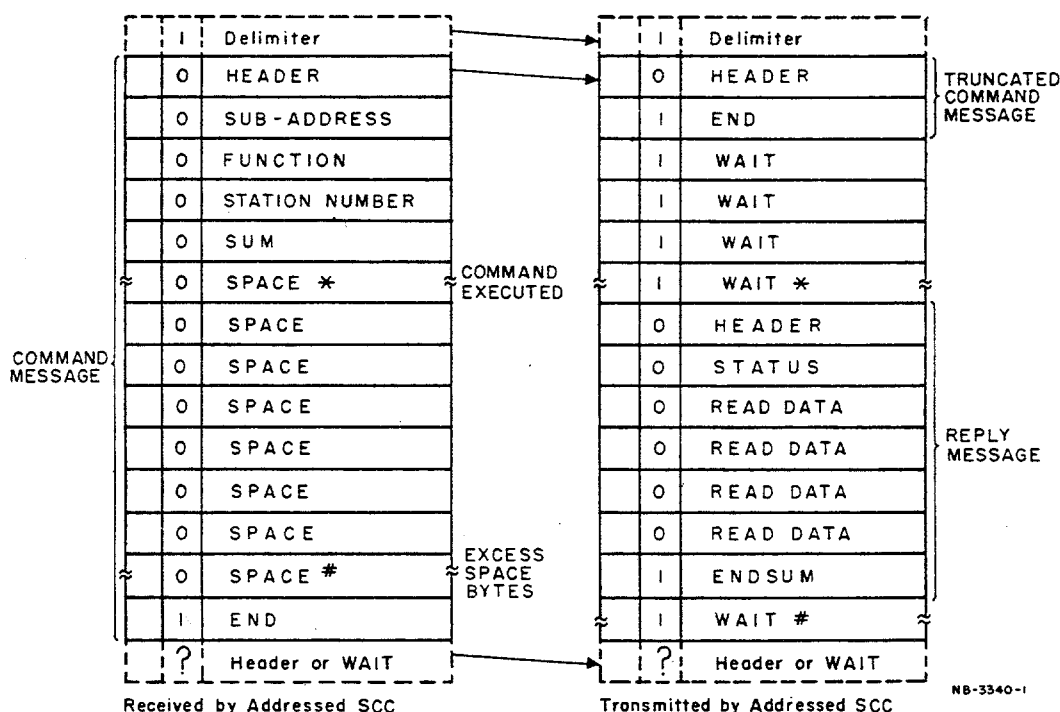
The message sequences for Read, Write, and Control operations in bit-serial mode are shown in Figs 4-1, 4-3, and 4-5, respectively. The corresponding sequences in byte-serial mode are shown in Figs 4-2, 4-4, and 4-6. All these figures show the normal conditions, with no errors and no Delay buffer switched into the message path in the SCC (see Section 5.2).

For a given mode, the sequences for Read, Write, and Control operations differ only in the presence or absence of data fields. For a given type of operation, the sequences for bit-serial and byte-serial modes differ only in the relative timing of received and retransmitted bytes at the beginning and end of the sequence. In bit-serial mode the retransmission of bytes (indicated by arrows in the figures) typically involves a delay of only one bit period, whereas in byte-serial mode there is typically a delay of one byte period.

These figures indicate that extra SPACE bytes can be added to the Reply space of the Command message for two reasons. Essential SPACE bytes, indicated by an asterisk, allow time for the execution of the command. The minimum number of these bytes is, in principle, zero, but a minimum of one byte may be more convenient to implement. Optional excess SPACE bytes, indicated by the number sign #, are used in one method of controlling the length of the Reply space (see Section 4.6.2). The minimum number of these bytes is zero.

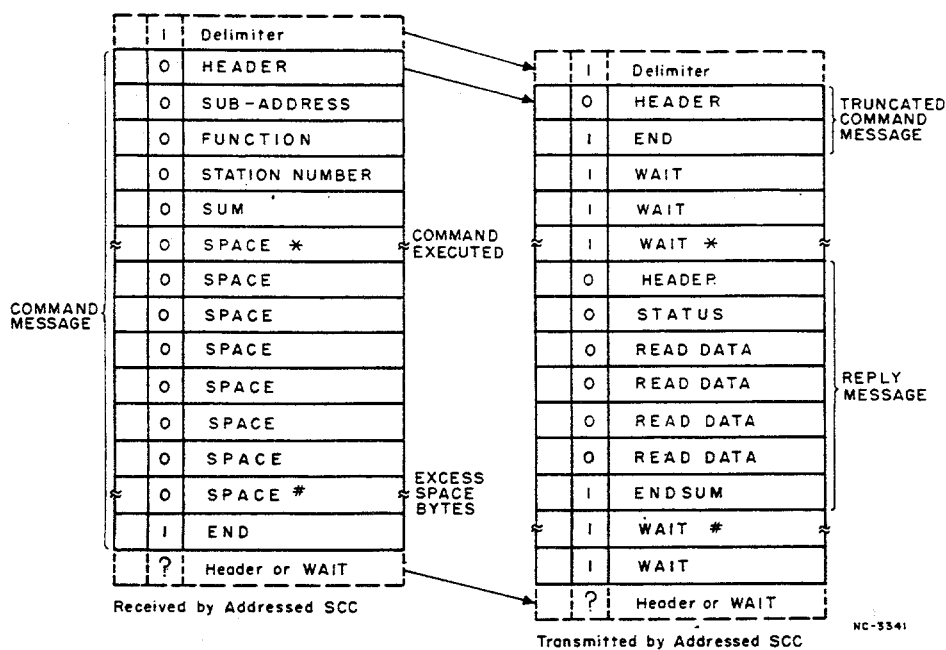
4.1 General Requirements

The SCC is normally awaiting a Header byte. The SD sends a Command message (see Section 3.1) consisting of a Header byte, the command and data bytes, the SUM byte, a sequence of SPACE bytes, and the END byte. The SCC recognizes the Header byte addressed to itself, receives and checks the command and data, executes the command, and sends a reply during the Reply space and, finally, terminates the transaction when it receives the END byte.



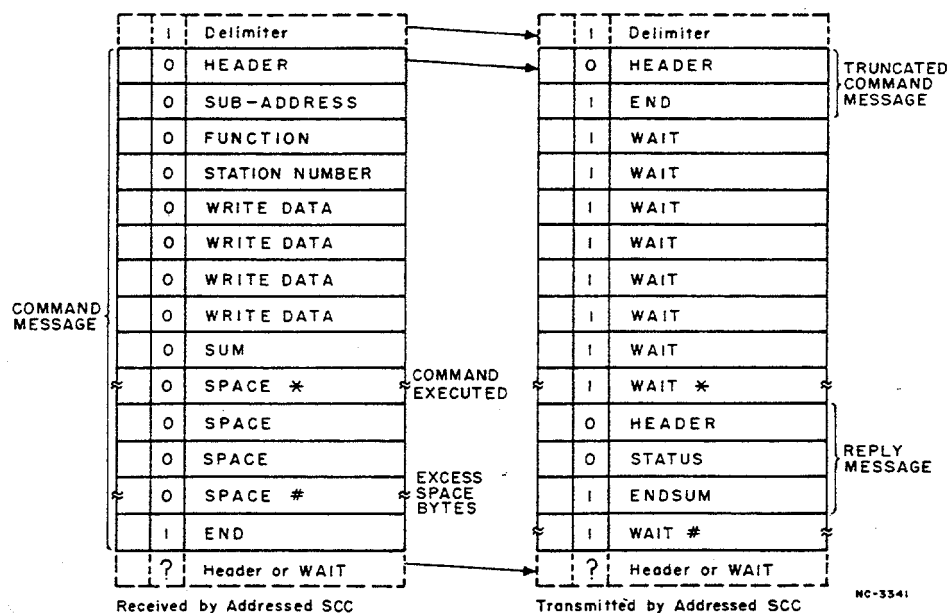
- * Number of bytes as required to accommodate execution of command: minimum number 0
 # Number of bytes as required to accommodate excess SPACE bytes: minimum number 0

Figure 4-1—Command/Reply Sequence: Read Operation, Bit-Serial Mode



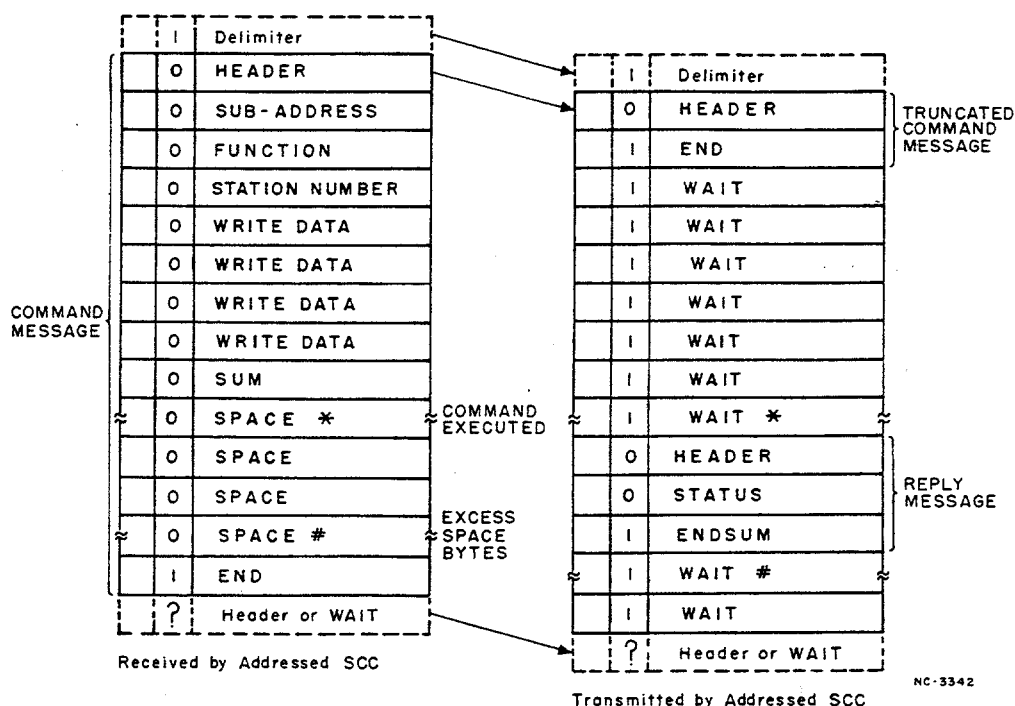
- * Number of Bytes as required to accommodate execution of command: minimum number 0
 # Number of Bytes as required to accommodate excess SPACE bytes: minimum number 0

Figure 4-2—Command/Reply Sequence: Read Operation, Byte-Serial Mode



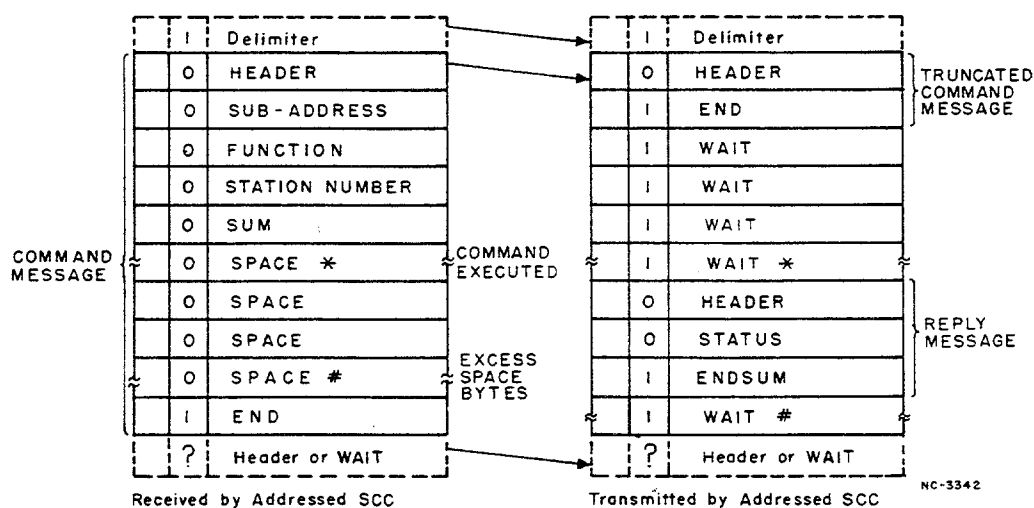
- * Number of bytes as required to accommodate execution of command: minimum number 0
 # Number of bytes as required to accommodate excess SPACE bytes: minimum number 0

Figure 4-3—Command/Reply Sequence: Write Operation, Bit-Serial Mode



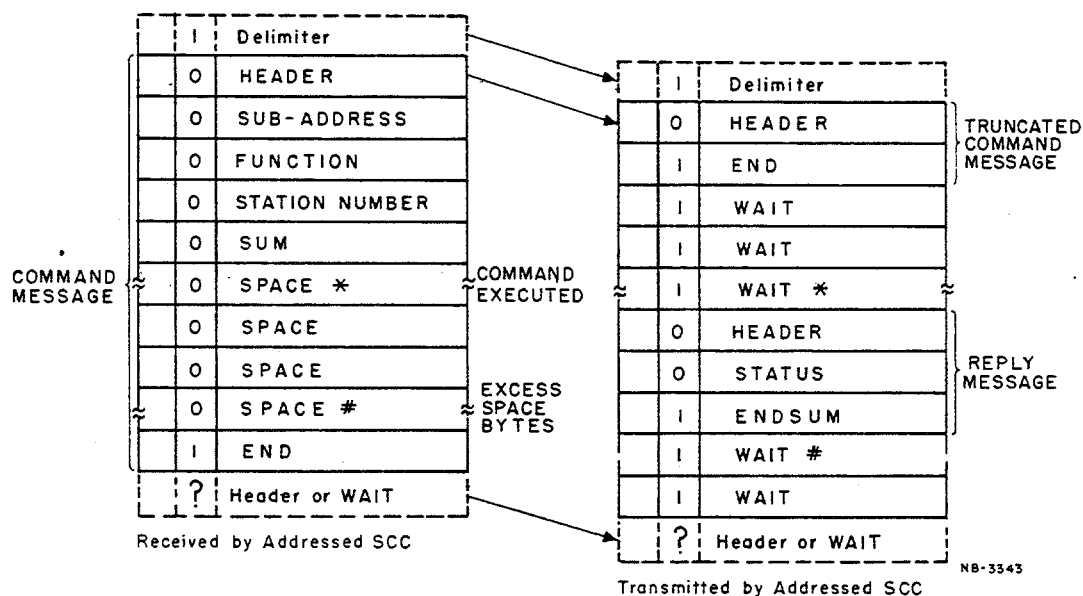
- * Number of bytes as required to accommodate execution of command: minimum number 0
 # Number of bytes as required to accommodate excess SPACE bytes: minimum number 0

Figure 4-4—Command/Reply Sequence: Write Operation, Byte-Serial Mode



- * Number of bytes as required to accommodate execution of command: minimum number 0
 # Number of bytes as required to accommodate excess SPACE bytes: minimum number 0

Figure 4-5—Command/Reply Sequence: Control Operation, Bit-Serial Mode



- * Number of bytes as required to accommodate execution of command: minimum number 0
 # Number of bytes as required to accommodate excess SPACE bytes: minimum number 0

Figure 4-6—Command/Reply Sequence: Control Operation, Byte-Serial Mode