

IEEE Standard Terminology for Semiconductor Memory

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Abstract: Guidelines under which data sheets for new semiconductor memories are to be generated are provided. Adherence to these guidelines is intended to produce data sheets that are concise and that consistently define the operation and characteristics of semiconductor memory devices. Terminology relevant to product description, product specification, and user information is covered.

Keywords: semiconductors, semiconductor memory devices, terminology

The Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street, New York, NY 10017-2394, USA

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Foreword

(This foreword is not a part of IEEE Std 662-1992, IEEE Standard Terminology for Semiconductor Memory.)

In 22 years, from 1970 to 1992, the semiconductor memory field has grown from a laboratory project to one of the largest single segments of the semiconductor industry. Along with this growth came a chaotic proliferation of symbols, terms, and language used to communicate information on device characteristics.

The first version of this standard, published in 1980, grew out of the realization by a group of semiconductor memory pioneers that this communication chaos was starting to inhibit an orderly growth of the industry. A working group initiated by Reese Brown and chaired by David House met monthly for two years to create a standard. This work was then substantially enhanced by contributions from JEDEC Committee JC-10. The resulting combined document met the original goal of providing standard symbols and terminology to allow nonambiguous communication of memory device characteristics.

Since IEEE Std 662-1980 was published, it has been widely accepted by both manufacturers and users as a basis for providing communication. In the intervening years, however, the semiconductor memory industry has changed and matured. As a result, situations have arisen for which IEEE Std 662-1980 was not adequate.

In 1985 a working group was organized to review the original standard and to incorporate those changes necessary to update it and to allow it to handle anticipated future situations. The resulting document is a fine-tuning of the original standard rather than a drastic revision of it. This fact serves as a testimonial to the insight of the original working group.

The original sponsoring committee, the IEEE Subcommittee on Computer Memory Standards, had gone out of existence prior to 1985. Sponsorship of the revision was provided by the IEEE Subcommittee on Test Technology Standards. The members of the working group that prepared the revision were:

J. Reese Brown, *Chair*

Alex Daly
Steve Grossman
Alan Grossmeyer
Charles Hochstedler

Manoj Kumar
Randy Lea
Fred Mann

Joe Miller
Bill Owen
Betty Prince
Dick Rogers

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Ray Chapman
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Donald W. Zipse

*Member Emeritus

Also included are the following nonvoting IEEE Standards Board liaisons:

Satish K. Aggarwal
James Beall
Richard B. Engelman
Stanley Warshaw

Mary Lynne Nielsen
IEEE Standards Project Editor

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1. Purpose

The purpose of this standard is to provide guidelines under which data sheets for semiconductor memories are to be generated. Adherence to these guidelines should produce data sheets that are concise and that consistently define the operation and characteristics of semiconductor memory devices. It is not intended that data sheets already in existence be revised specifically to conform to this format. However, data sheets being generated for the first time for new products should adhere to this standard. As part of the standard, a nomenclature for memory devices is presented. This nomenclature includes a format for defining electrical parameters and two alternative formats for timing parameters. The first timing parameter format uses a FROM-TO concept for explicitly defining most timing parameters that are needed to specify complex memory devices. The alternate form utilizes a functional description approach. Recommendations are also made for a uniform pin naming glossary of terms.

1.1 References. This standard shall be used in conjunction with the following publications. When the following standards are superseded by an approved revision, the revision shall apply.

[1] IEEE Std 91-1984, IEEE Standard Graphic Symbols for Logic Functions (ANSI, DoD).¹

[2] IEEE Std 991-1986, IEEE Standard for Logic Circuit Diagrams (ANSI, DoD).

[3] JEDEC Publication 95, Registered and Standard Outlines for Solid-State and Related Products.²

[4] JESD 21-C (1991), Configurations for Solid-State Memories.³

2. Product Description

Product description consists of information typically contained on the first pages of a memory data sheet. It should include all of the following information:

- (1) Product name and number
- (2) Name of the manufacturer
- (3) Summary of product features and advantages
- (4) Description of product
- (5) Identification of wafer process technology used
- (6) Functional block diagram

¹IEEE publications are available from the Institute of Electrical and Electronics Engineers, Service Center, 445 Hoes Lane, P. O. Box 1331, Piscataway, NJ 08855-1331, USA.

²JEDEC publications are available from JEDEC, 2001 Pennsylvania Avenue NW, Washington, DC 20006, USA.

³JEDEC Standards are available from Global Engineering, 2805 McGraw Avenue, P.O. Box 19539, Irvine, CA 92713-9539.

- (7) Pin assignments
- (8) Function tables
- (9) Logic symbols
- (10) Pin definitions
- (11) Description of device operation
- (12) Package styles available
- (13) References to IEEE Std 991-1986 [2] and JESD 21-C (1991) [4]⁴.

2.1 Logic Definitions. Care should be taken in all definitions and descriptive information to define logic states consistently, particularly in the use of the terms TRUE/FALSE, HIGH/LOW, Active/Inactive, and ONE/ZERO. A logic TRUE is by definition a logic ONE and is logically Active; it may be electrically a HIGH or a LOW. Conversely, a logic FALSE is by definition a logic ZERO, is logically Inactive, and may be an electrical HIGH or LOW. For positive logic a logic TRUE is a HIGH and a logic FALSE is a LOW, while the opposite is true for negative logic. For positive logic, a nonbarred signal is TRUE (Active) when HIGH, and a barred signal is TRUE (Active) when LOW. Positive logic is assumed unless otherwise stated. See Table 1.

Table 1
Logic Signal Polarity Definitions

Logical Terms	Electrical Terms	
	Positive Logic	Negative Logic
1 $\Leftrightarrow$ Active $\Leftrightarrow$ True 1	HIGH	LOW
0 $\Leftrightarrow$ Inactive $\Leftrightarrow$ False 0	LOW	HIGH

HIGH is defined as the more positive and LOW as the more negative logic level. Since it is very common to mix active HIGH and active LOW inputs/outputs on a single memory device, care should be taken not to confuse HIGH with logic ONE. It is recommended that input and output levels be referred to as HIGH and LOW. When it becomes necessary to describe the logical operation of a device, the preferred terms are TRUE and FALSE. The use of ONE (1) and ZERO (0) should be avoided on the data sheet.

2.2 Logic Diagrams or Functional Block Diagrams. The diagram should logically and functionally define the operation of the memory device. Drawings should adhere to IEEE Std 91-1984 [1] and IEEE Std 991-1986 [2].

2.3 Pin Definitions (Pin Names). The pin names and symbols contained in Appendix A should be used when applicable. In cases where a pin name is used and is not included in Appendix A, a complete definition of the name, along with the designated symbol, should be given in the data sheet in the product description section.

Pin symbols should begin with a letter and may contain any number of letters followed by any number of numerals, but should not include the transition designators H, L, V, X, or Z. To simplify the terminology for timing parameters, pin symbols should be kept as short as possible. Where multiple symbols of a single type are required, such as for multiple addresses and/or data inputs/outputs, numbering should begin at 0 and go to N-1. Unlike address and data inputs, multiple control inputs that perform the identical function, such as multiple chip selects, etc., should be numbered from 1 to N. Control inputs that do not perform identical functions should be given separate names.

⁴The numbers in brackets correspond to the references in 1.1.

A logical bar should be used over pin names and symbols to designate native TRUE (that is, active LOW, low TRUE). Where it is not possible or desirable to use the overbar as a negation symbol, there are alternate inline symbols defined in IEEE Std 991-1986 [2]. A trailing reverse slash is recommended where the approved symbols are not available.

2.4 Output Conditions. The state of the output should be defined for all combinations of any input(s), such as write enable, chip select, chip enable, or any other pin that affects the output. A function table is the recommended form for showing these relationships. The relationship of data IN to data OUT (that is, inverted or not inverted) should be clearly shown in the block diagram, logic symbol, pin names, pin symbol, and in the functional description.

2.5 Read Operation. A complete definition should be given for all conditions under which data may be read from the memory.

2.6 Write Operation. A complete definition should be given for all conditions under which data may be written into the memory. Any additional conditions that might result in alteration of data stored in the memory should be defined. It is recommended that these definitions be expressed in the form of a function table.

2.7 Other Operating Modes. If the device contains any additional operating modes, they should be thoroughly defined and explained using text and timing diagrams.

2.8 Start-Up Conditions. If the device requires any preconditioning such as voltage sequencing, dummy cycles, or signal sequencing before a valid operation, this preconditioning should be defined.

2.9 Terms and Symbols. When terms and symbols other than those defined in this standard are needed, they should follow the format of the terms and symbols defined in this standard, should not conflict with any of the terms and symbols herein, and should be clearly defined in the data sheet. A list of terms that are applicable to memory devices is given in JESD Std 21-C (1991) [4] or its successor. This document is periodically updated and can be relied on to give a list of all pin function and package-related terms that might be needed to specify or describe a memory device.

3. Product Specification

The product specification section of the data sheet consists of all the limits for parameters that the manufacturer warrants for the product. This section should contain as a minimum:

- (1) Absolute maximum ratings
- (2) Recommended operating conditions
- (3) Electrical parameters
- (4) Timing parameters
- (5) Capacitance parameters
- (6) Package characteristics
- (7) Test conditions

3.1 Absolute Maximum Ratings. The absolute maximum ratings define the range of conditions to which the device can be subjected without affecting the operation of the device after it is subsequently returned to the specified operating range. All conditions that might impair the operation of the device, such as temperature, signal and power supply sequencing, or electrostatic discharge conditions, should be clearly stated. Since the absolute maximum ratings