

# IEEE Recommended Practice for Block Transfers in CAMAC Systems

Sponsor

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## Foreword

(This foreword is not a part of IEEE Std 683-1976, Block Transfers in CAMAC Systems.)

A wide variety of block transfer algorithms (or modes) are possible in CAMAC systems. However, a restricted number of such algorithms can satisfy nearly all needs. This document presents recommended algorithms to encourage uniformity in design of CAMAC modules and controllers with resulting increased compatibility. It should be read in conjunction with, and is supplementary to, IEEE Standards 583-1975, Modular Instrumentation and Digital Interface System, 595-1976, Serial Highway Interface Systems, and 596-1976, Parallel Highway Interface System (CAMAC). The report on which this document is based, and with which it is technically identical (ERDA Report TID-26616, February 1976), was prepared by the NIM Committee of the United States Energy Research and Development Administration\* and the ESONE Committee of European Laboratories.†

This standard was reviewed and balloted by the Nuclear Instruments and Detectors Committee of the IEEE Nuclear and Plasma Sciences Society. Because of the broad applicability of this standard, coordination was established with numerous IEEE societies, groups, and committees, including the Communications Society, Computer Society, Industry Applications Society, Industrial Electronics and Control Instrumentation Group, Instrumentation and Measurement Group, and the Power Generation and Nuclear Power Engineering Committees of the Power Engineering Society.

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# **IEEE Recommended Practice for Block Transfers in CAMAC Systems**

## **1. Introduction**

The basic CAMAC specification (see Ref [1]) defines a single CAMAC operation as the activity which occurs in response to a single CAMAC command. This activity may consist of the transfer of a single data word between a CAMAC module and computer memory or the changing of the status of a module [for example,  $F(26)$ ,  $F(24)$ ] or return of a value for  $Q$  as the result of a test made on the module, or any compatible set of the previously named activities. A block transfer is defined as a sequence of single CAMAC operations involving data which the user specifies by a command said to be of a higher level than one which specifies a single CAMAC operation. The higher level command contains all the information required for the specification of the desired sequence of single CAMAC commands and is interpreted by a channel which governs the activity on the CAMAC highway. Control information such as the readiness of the computer to participate in a data transfer, the state of the CAMAC  $Q$  line and the state of certain LAMs (Look-at-Me's) or special synchronizing signals must be made available to the channel. The use made of the control information by the channel defines the block-transfer mode. If a module is to influence the sequence of operations within a block transfer, then it must have the features required by the algorithm.

A channel consists of an interface to the CAMAC system as well as a means for selecting and executing the algorithms of the implemented block-transfer modes. An algorithm may be implemented wholly in hardware or wholly in software or by a combination of hardware and software. The possibility of software implementation of any algorithm means that CAMAC block transfers can take place on a system which does not have the hardware (such as direct memory access) required to carry out "computer" block transfers. Note that a module behaves in the same way when it is accessed by a hardware algorithm as it does when accessed by conventional programmed computer input-output. Regardless of the method of channel implementation, the use of the channel results in reductions in both the CPU time required and in the programming effort through the use of pre-defined algorithms.

Many different block-transfer algorithms (or modes) may be defined, all of which are compatible with the CAMAC specifications. It is also possible to have a channel execute a sequence of CAMAC commands which does not involve the transfer of data. An example of such a "Multiple Action" mode is discussed in the Appendix. Many algorithms convey control information by either  $Q$  or a LAM signal or both. The requirements placed on these signals by one algorithm may conflict with those placed on them by another algorithm. Hence compatibility problems between modes and channels can occur. This is especially true if no restrictions are placed on the choice of a suitable block-transfer algorithm. However, experience with many different CAMAC systems and extensive analysis of the problem has revealed that a restricted number of block-transfer algorithms can satisfy nearly all needs. To encourage uniformity in future designs of modules and controllers, certain algorithms are recommended to be used whenever possible, and some additional algorithms are suggested for special applications that cannot practicably be implemented with the recommended algorithms. The possibility remains for a user to define other block-transfer algorithms to meet special needs.