

Information technology—
Telecommunications and information exchange between systems—
Local and metropolitan area networks—Specific requirements—

Supplement to Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications—

Physical Layer Parameters and Specifications for 1000 Mb/s Operation Over 4-Pair of Category 5 Balanced Copper Cabling, Type 1000BASE-T

Sponsor
**LAN MAN Standards Committee
of the
IEEE Computer Society**

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Abstract: Type 1000BASE-T PCS, type 1000BASE-T PMA sublayer, and type 1000BASE-T Medium Dependent Interface (MDI) are defined. This supplement provides fully functional, electrical and mechanical specifications for the type 1000BASE-T PCS, PMA, and MDI. This supplement also specifies the baseband medium used with 1000BASE-T.

Keywords: Auto-Negotiation, Category 5, copper, Ethernet, gigabit, MASTER-SLAVE, medium dependent interface, physical coding sublayer, Physical Layer, physical medium attachment

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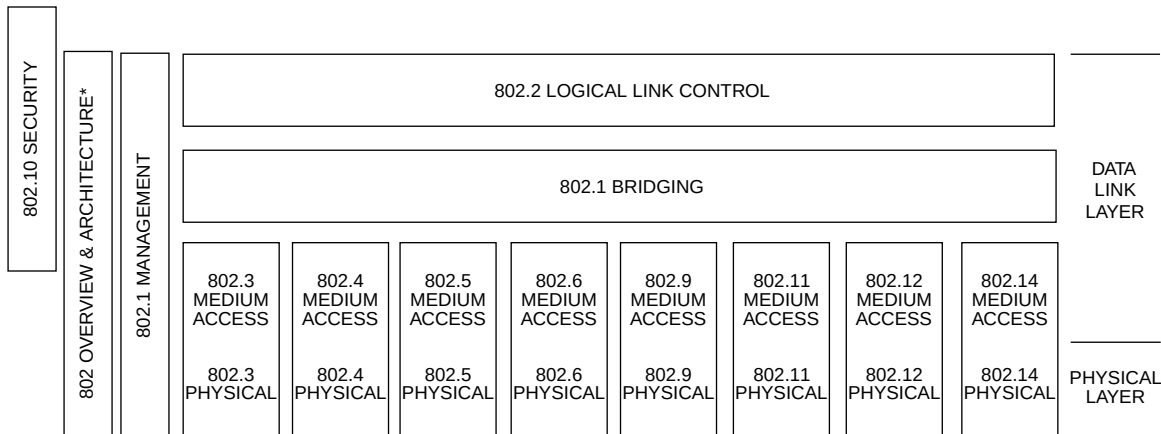
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Introduction to IEEE Std 802.3ab-1999

This standard is part of a family of standards for local and metropolitan area networks. The relationship between the standard and other members of the family is shown below. (The numbers in the figure refer to IEEE standard numbers.)



* Formerly IEEE Std 802.1A.

This family of standards deals with the Physical and Data Link layers as defined by the International Organization for Standardization (ISO) Open Systems Interconnection (OSI) Basic Reference Model (ISO/IEC 7498-1: 1994). The access standards define seven types of medium access technologies and associated physical media, each appropriate for particular applications or system objectives. Other types are under investigation.

The standards defining the technologies noted above are as follows:

- IEEE Std 802 *Overview and Architecture*. This standard provides an overview to the family of IEEE 802 Standards.
- ANSI/IEEE Std 802.1B and 802.1k [ISO/IEC 15802-2] *LAN/MAN Management*. Defines an OSI management-compatible architecture, and services and protocol elements for use in a LAN/MAN environment for performing remote management.
- ANSI/IEEE Std 802.1D *Media Access Control (MAC) Bridges*. Specifies an architecture and protocol for the interconnection of IEEE 802 LANs below the MAC service boundary.
- ANSI/IEEE Std 802.1E [ISO/IEC 15802-4] *System Load Protocol*. Specifies a set of services and protocol for those aspects of management concerned with the loading of systems on IEEE 802 LANs.
- ANSI/IEEE Std 802.1F *Common Definitions and Procedures for IEEE 802 Management Information*
- ANSI/IEEE Std 802.1G [ISO/IEC 15802-5] *Remote Media Access Control (MAC) Bridging*. Specifies extensions for the interconnection, using non-LAN communication technologies, of geographically separated IEEE 802 LANs below the level of the logical link control protocol.
- IEEE Std 802.1H [ISO/IEC TR 11802-5] *Media Access Control (MAC) Bridging of Ethernet V2.0 in Local Area Networks*
- ANSI/IEEE Std 802.2 [ISO/IEC 8802-2] *Logical Link Control*
- ANSI/IEEE Std 802.3 *CSMA/CD Access Method and Physical Layer Specifications*

- ANSI/IEEE Std 802.4 [ISO/IEC 8802-4] *Token Passing Bus Access Method and Physical Layer Specifications*
- ANSI/IEEE Std 802.5 [ISO/IEC 8802-5] *Token Ring Access Method and Physical Layer Specifications*
- ANSI/IEEE Std 802.6 [ISO/IEC 8802-6] *Distributed Queue Dual Bus Access Method and Physical Layer Specifications*
- ANSI/IEEE Std 802.9 [ISO/IEC 8802-9] *Integrated Services (IS) LAN Interface at the Medium Access Control (MAC) and Physical (PHY) Layers*
- ANSI/IEEE Std 802.10 *Interoperable LAN/MAN Security*
- ANSI/IEEE Std 802.11 [ISO/IEC DIS 8802-11] *Wireless LAN Medium Access Control (MAC) and Physical Layer Specifications*
- ANSI/IEEE Std 802.12 [ISO/IEC 8802-12] *Demand Priority Access Method, Physical Layer and Repeater Specifications*

In addition to the family of standards, the following is a recommended practice for a common Physical Layer technology:

- IEEE Std 802.7 *IEEE Recommended Practice for Broadband Local Area Networks*

The following additional working group has authorized standards projects under development:

- IEEE 802.14 *Standard Protocol for Cable-TV Based Broadband Communication Network*

Conformance test methodology

An additional standards series, identified by the number 1802, has been established to identify the conformance test methodology documents for the 802 family of standards. Thus the conformance test documents for 802.3 are numbered 1802.3.

IEEE Std 802.3ab-1999

This standard contains state-of-the-art material. The area covered by this standard is undergoing evolution. Revisions are anticipated to this standard within the next few years to clarify existing material, to correct possible errors, and to incorporate new related material. Details on the contents of this standard are provided on the following pages.

The IEEE 802.3 Working Group acknowledges and appreciates that many concepts embodied in this standard are based largely upon the CSMA/CD access method earlier described in *The Ethernet* specification as written jointly by individuals from Xerox Corporation, Digital Equipment Corporation, and Intel Corporation. Appreciation is also expressed to Robert M. Metcalfe and David R. Boggs for their pioneering work in establishing the original concepts.

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This standard is dedicated to the memory of our friend and colleague

Valerie E. Zelenty
IEEE Standards Editor 1993–1999

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Revisions to IEEE Std 802.3, 1998 Edition as supplemented by IEEE Std 802.3ac-1998

[These additions are part of IEEE Std 802.3, 1998 Edition.]

EDITORIAL NOTE—The editing instructions contained in this supplement define how to merge the material contained herein into the existing base standard to form the new comprehensive standard as created by the addition of IEEE Std 802.3ab-1999.

The editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~striketrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions.

1.3 Normative references

Insert the following references to 1.3:

ANSI/TIA/EIA-568-A, Commercial Building Telecommunications Cabling Standard.¹

IEC 61000-4-3, Electromagnetic Compatibility (EMC)—Part 4: Testing and measurement techniques—Section 3: Radiated, radio-frequency, electromagnetic field immunity test.²

MATLAB Matrix Laboratory Software.³

¹ANSI publications are available from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA (<http://www.ansi.org/>)

²IEC publications are available from the Sales Department of the International Electrotechnical Commission, Case Postale 131, 3, rue de Varembe, CH-1211, Genève 20, Switzerland/Suisse (<http://www.iec.ch/>). IEC publications are also available in the United States from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA.

³For information on MatLab contact: The MathWorks, 24 Park Way, Natick, MA, (www.mathworks.com).

1.4 Definitions

Change the following definitions in 1.4. These definitions will be renumbered in future editions.

1.4.53 Category 5 balanced cabling: Balanced 100 Ω and 120 Ω ~~unshielded twisted pair (UTP) cables and associated connecting hardware whose transmission characteristics are specified up to 100 MHz (i.e., performance meets the requirements of a Class D link as per ISO/IEC 11801:1995)~~ cabling components meet the performance specified in ISO/IEC 11801:1995. In addition to the requirements outlined in ISO/IEC 11801:1995, IEEE 802.3 Clauses 14, 23, 25, ~~and 32 and 40~~ specify additional requirements for ~~this cabling~~ when used with 10BASE-T, ~~and~~ 100BASE-TX and 1000BASE-T.

1.4.70 code-group: For IEEE 802.3, a set of encoded symbols representing encoded data or control information. For 100BASE-T4, a set of six ternary symbols that, when representing data, conveys an octet. For 100BASE-TX and 100BASE-FX, a set of five code bits that, when representing data, conveys a nibble. For 100BASE-T2, a pair of PAM5 $\times$ 5 symbols that, when representing data, conveys a nibble. For 1000BASE-X, a set of ten bits that, when representing data, conveys an octet. For 1000BASE-T, a vector of four 8B1Q4 coded quinary symbols that, when representing data, conveys an octet. (See IEEE 802.3, Clauses 23, 24, 32, ~~and 36, and 40.~~)

1.4.100 End-of-Stream delimiter (ESD): Within IEEE 802.3, a code-group pattern used to terminate a normal data transmission. For 100BASE-T4, the ESD is indicated by the transmission of five predefined ternary code-groups named eop1-5. For 100BASE-X, the ESD is indicated by the transmission of the code-group /T/R. For 100BASE-T2, the ESD is indicated by two consecutive pairs of predefined PAM5 $\times$ 5 symbols, (see Table 32-15) which are generated using unique Start-of-Stream delimiter (SSD)/ESD coding rules. For 1000BASE-T, the ESD is indicated by two consecutive vectors of four quinary symbols as specified in Table 40-1. (See IEEE Std 802.3, Clauses ~~22 and~~ 23, 32, and 40.)

1.4.152 master Physical Layer (PHY): Within IEEE 802.3, in a 100BASE-T2 or 1000BASE-T link containing a pair of PHYs, the PHY that uses an external clock for generating its clock signals to determine the timing of transmitter and receiver operations. It also uses the master transmit scrambler generator polynomial for side-stream scrambling. Master and slave PHY status is determined during the Auto-Negotiation process that takes place prior to establishing the transmission link. *See also:* **slave Physical Layer (PHY).**

1.4.157 Medium Dependent Interface (MDI): The mechanical and electrical interface between the transmission medium and the Medium Attachment Unit (MAU) (10BASE-T) or PHY (100BASE-T, 1000BASE-X, or 1000BASE-T).

1.4.195 Physical Coding Sublayer (PCS): Within IEEE 802.3, a sublayer used in 100BASE-T, 1000BASE-X, and 1000BASE-T to couple the Media Independent Interface (MII) or Gigabit Media Independent Interface (GMII) and the Physical Medium Attachment (PMA). The PCS contains the functions to encode data bits into code-groups that can be transmitted over the physical medium. ~~Four~~ Three PCS structures are defined for 100BASE-T—one for 100BASE-X, one for 100BASE-T4, and one for 100BASE-T2 ~~1000BASE-X~~. (See IEEE 802.3, Clauses 23, 24, ~~and 32, and 36.~~) One PCS structure is defined for 1000BASE-X and one PCS structure is defined for 1000BASE-T. (See IEEE 802.3 Clauses 36 and 40.)

1.4.196 Physical Layer entity (PHY): Within IEEE 802.3, the portion of the Physical Layer between the Medium Dependent Interface (MDI) and the Media Independent Interface (MII), or between the MDI and GMII, consisting of the Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA), and, if present, the Physical Medium Dependent (PMD) sublayers. The PHY contains the functions that transmit, receive, and manage the encoded signals that are impressed on and recovered from the physical medium. (See IEEE 802.3 Clauses 23–26, 32, 36, and 40.)

1.4.197 Physical Medium Attachment (PMA) sublayer: Within IEEE 802.3, that portion of the Physical Layer that contains the functions for transmission, collision detection, reception, and (depending on the PHY) clock recovery, and skew alignment. (See IEEE 802.3, Clauses 7, 12, 14, 16, 17, 18, 23, 24, 32, 36 and 40.)

1.4.210 receiver training: Within IEEE 802.3, a start-up routine in 100BASE-T2 and 1000BASE-T used to acquire receiver parameters and synchronize the scramblers of two connected Physical Layers (PHYs).

1.4.219 retraining: Within IEEE 802.3, the process of re-acquiring receiver parameters and synchronizing the scramblers of two connected 100BASE-T2 or 1000BASE-T PHYs. *See also:* **receiver training.**

1.4.233 side-stream scrambling: A data scrambling technique, used by 100BASE-T2 and 1000BASE-T to randomize the sequence of transmitted symbols and avoid the presence of spectral lines in the signal spectrum. Synchronization of the scrambler and descrambler of connected PHYs is required prior to operation.

1.4.237 slave Physical Layer (PHY): Within IEEE 802.3, in a 100BASE-T2 or 1000BASE-T link containing a pair of PHYs, the PHY that recovers its clock from the received signal and uses it to determine the timing of transmitter operations. It also uses the slave transmit scrambler generator polynomial for side-stream scrambling. Master and slave PHY status is determined during the Auto-Negotiation process that takes place prior to establishing the transmission link. *See also:* **master Physical Layer (PHY).**

1.4.244 Start-of-Stream delimiter (SSD): Within IEEE 802.3, a pattern of defined code words used to delineate the boundary of a data transmission sequence on the Physical Layer stream. The SSD is unique in that it may be recognized independent of previously defined code-group boundaries and it defines subsequent code-group boundaries for the stream it delimits. For 100BASE-T4, SSD is a pattern of three predefined sosb code-groups (one per wire pair) indicating the positions of the first data code-group on each wire pair. For 100BASE-X, SSD consists of the code-group sequence /J/K/. For 100BASE-T2, the SSD is indicated by two consecutive pairs of predefined PAM5×5 symbols (± 2 , ± 2) (± 2 , 0), which are generated using unique SSD/ESD coding rules. For 1000BASE-T, the SSD is indicated by two consecutive vectors of four quinary symbols as specified in Table 40-1.

1.4.247 symbol: Within IEEE 802.3, the smallest unit of data transmission on the medium. Symbols are unique to the coding system employed. 100BASE-T4 uses ternary symbols; 10BASE-T uses Manchester symbols; 100BASE-X uses binary symbols or code bits; 100BASE-T2 and 1000BASE-T uses quinary symbols.

1.4.248 symbol rate (SR): Within IEEE 802.3, the total number of symbols per second transferred to or from the Media Dependent Interface (MDI) on a single wire pair. For 100BASE-T4, the symbol rate is 25 MBaud; for 100BASE-X, the symbol rate is 125 MBaud; for 100BASE-T2, the symbol rate is 25 MBaud; for 1000BASE-T, the symbol rate is 125 MBaud.

1.4.250 Technology Ability Field: Within IEEE 802.3, an eight-bit field in the Auto-Negotiation base page that is used to indicate the abilities of a local station, such as support for 10BASE-T, 100 BASE-T4, and 100BASE-TX, and 100BASE-T2, as well as full duplex capabilities.

Insert the following definitions at the end of 1.4. These definitions will be renumbered in alphabetical order in a future edition and inserted in sequence.

1.4.268 4D-PAM5: The symbol encoding method used in 1000BASE-T. The four-dimensional quinary symbols (4D) received from the 8B1Q4 data encoding are transmitted using five voltage levels (PAM5). Four symbols are transmitted in parallel each symbol period. (See IEEE 802.3 Clause 40.)

1.4.269 8B1Q4: For IEEE 802.3, the data encoding technique used by 1000BASE-T when converting GMII data (8B-8 bits) to four quinary symbols (Q4) that are transmitted during one clock (1Q4). (See IEEE 802.3 Clause 40.)

1.4.270 Control mode: In 1000BASE-T, the period of operation in which the PHY is transmitting code-groups that represent control information. The end of a frame is accompanied by a transition to the Control mode, which immediately follows the Data mode and precedes the Idle mode. This occurs when the GMII signal TX_EN is set FALSE. During this time, several control fields are transmitted as code-groups to complete a stream. These include two convolutional encoder reset code-groups, two End-of-Stream delimiter (ESD) code-groups and, possibly, carrier extend code-groups. (See IEEE 802.3 Clause 40.)

1.4.271 Data mode: In 1000BASE-T, the period of operation in which the PHY is transmitting code-groups that represent data. This mode is preceded by a start of a frame during which the GMII signal TX_EN is set TRUE for data transmission. This mode begins with transmission of two Start-of-Stream delimiter code-groups followed by code-groups encoded from the data octets arriving on TXD<7:0> via the GMII. (See IEEE 802.3 Clause 40.)

1.4.272 Idle mode: In 1000BASE-T, the period of operation in which the PHY is transmitting special code-groups that use only the values {2, 0, -2}. Idle mode occurs during start-up when the PHYs at each end of a link are attempting to establish adaptive filter parameters and then synchronize both phase and timing so that normal operation can begin. Idle mode also occurs during normal operation between frames. Idle mode occurs after a control mode ends and before another Data mode begins. The Idle mode is not used between frames in a packet burst. (See IEEE 802.3 Clause 40.)

1.4.273 multiport device: A device with multiple instances of MDI. (See IEEE 802.3 Clause 40.)

1.4.274 quinary symbol: In 1000BASE-T, one of five numeric values corresponding to five voltage levels on a single balanced twisted pair. The values come from the set {2, 1, 0, -1, -2}. Table 40-1 lists groups of four quinary symbols. Idle is a special case where numeric values are limited to the set {2, 0, and -2}. (See IEEE 802.3 Clause 40.)

1.4.275 single-port device: A device with a single instance of MDI. (See IEEE 802.3 Clause 40.)

1.4.276 symbol period: In 1000BASE-T, the time interval for transmission of one code-group. This is equivalent to eight nanoseconds. (See IEEE 802.3 Clause 40.)

1.5 Abbreviations

Add the following abbreviation to 1.5:

DFE distributed feedback equalizer

22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

Change the name of Register 9 in Table 22-6 from “100BASE-T2 Control Register” to “MASTER-SLAVE Control Register.”

Change the name of Register 10 in Table 22-6 from “100BASE-T2 Status Register” to “MASTER-SLAVE Status Register.”

Delete Note b attached to Table 22-9 and its two references in the table.

Replace subclause 22.2.4.3.7 with the following:

22.2.4.3.7 MASTER-SLAVE control register (Register 9)

Register 9 provides bit values by 100BASE-T2 (as specified in 32.5) and 1000BASE-T (as specified in 40.5).

Replace subclause 22.2.4.3.8 with the following:

22.2.4.3.8 MASTER-SLAVE status register (Register 10)

Register 10 provides bit values by 100BASE-T2 (as specified in 32.5) and 1000BASE-T (as specified in 40.5).

28. Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair

EDITORIAL NOTE—The next change was originally specified in Clause 32 as 32.5.4.2. This change moves it to Clause 28.

Renumber 28.2.4.1.7 as 28.2.4.1.8, insert the following as 28.2.4.1.7, and renumber the remaining tables.

28.2.4.1.7 Auto-Negotiation Link Partner Ability register (Register 8) (RO)

Support for 100BASE-T2 and 1000BASE-T requires support for Next Page and the provision of an Auto-Negotiation Link Partner Next Page Ability register (register 8) to store Link Partner Next Pages as shown in Table 28-8. All of the bits in the Auto-Negotiation Link Partner Next Page Ability register are read only. A write to the Auto-Negotiation Link Partner Next Page Ability register shall have no effect.

The values contained in this register are only guaranteed to be valid after the Page Received bit (6.1) has been set to logical one or once Auto-Negotiation has successfully completed, as indicated by bit 1.5.

NOTE—If this register is used to store multiple Link Partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent Link Partner Next Pages.

Table 28-8—Link Partner Next Page Ability register bit definitions

Bit(s)	Name	Description	R/W
8.15	Next Page	see 28.2.3.4	RO
8.14	Acknowledge	see 28.2.3.4	RO
8.13	Message Page	see 28.2.3.4	RO
8.12	Acknowledge 2	see 28.2.3.4	RO
8.11	Toggle	see 28.2.3.4	RO
8.10:0	Message/Unformatted Code Field	see 28.2.3.4	RO

Insert the following as 28.2.6.3:

28.2.6.3 PMA_LINKPULSE.request

This primitive is generated by Auto-Negotiation to indicate that a valid Link Pulse, as transmitted in compliance with Figure 14-12, has been received.

28.2.6.3.1 Semantics of the service primitive

PMA_LINKPULSE.request (linkpulse)

The linkpulse parameter shall assume one of two values: TRUE or FALSE.

The linkpulse=FALSE mode shall be used by the Auto-Negotiation function to indicate that the Receive State Diagram has performed a state transition.

The linkpulse=TRUE mode shall be used by the Auto-Negotiation function to indicate that a valid Link Pulse has been received.

28.2.6.3.2 When generated

The Auto-Negotiation function shall generate this primitive to indicate to the PHY how to respond, in accordance with the state diagram of Figure 28-15.

Upon power-on or reset, if the Auto-Negotiation function is enabled (`mr_autoneg_enable=true`) the `PMA_LINKPULSE.request (FALSE)` message shall be issued to all technology-dependent PMAs. If Auto-Negotiation is disabled at any time including at power-on or reset, the state of `PMA_LINKPULSE.request (linkpulse)` is implementation dependent.

28.2.6.3.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the receiving technology-dependent PMA function, based on the intent specified in the primitive semantics.

Insert the following line at the bottom of the list of variable names that appears at the start of 28.3.1:

1GigT; represents that the 1000BASE-T PMA is the signal source.

Change linkpulse definition in 28.3.1 to read:

linkpulse
 This variable is defined in 28.2.6.3.1.

Change the title of subclause 28.5 to read:

28.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair

Change the first sentence of 28.5.1 to read:

28.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

Change column two, row two of 28.5.2.2 as follows:

28.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3, 1998 Edition, Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and <u>1000 Mb/s</u> Auto-Negotiation on twisted pair
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3, 1998 Edition.)	No [] Yes []

Date of Statement	
-------------------	--

Change the title of 28.5.4 to read:

28.5.4 PICS proforma tables for Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair

Add the following rows to the bottom of 28.5.4.7:

Item	Feature	Subclause	Status	Support	Value/Comment
11	The linkpulse parameter shall	28.2.6.3.1	M	Yes []	TRUE or FALSE.
12	The linkpulse=FALSE shall be used	28.2.6.3.1	M	Yes []	By the Auto-Negotiation function to indicate that the Receive State Diagram has performed a state transition.
13	The linkpulse=TRUE shall be used	28.2.6.3.1	M	Yes []	By the Auto-Negotiation function to indicate that a valid Link Pulse has been received.
14	The Auto-Negotiation function shall generate linkpulse	28.2.6.3.2	M	Yes []	To indicate to the PHY how to respond, in accordance with the state diagram of Figure 28-15.
15	Upon power-on or reset, if Auto-Negotiation is enabled (mr_autoneg_enable=true) the PMA_LINKPULSE.request(FALSE) message shall be	28.2.6.3.2	M	Yes []	Issued to all technology-dependent PMAs.
16	The effect of the receipt of linkpulse shall be governed	28.2.6.3.3	M	Yes []	By the receiving technology-dependent PMA function, based on the intent specified in the primitive semantics.

30.10 Mb/s, 100 Mb/s, and 1000 Mb/s Management

Delete notes attached to 30.3.2.1.2 and 30.3.2.1.3.

Delete note attached to 30.5.1.1.2.

Change the text for “BEHAVIOUR DEFINED AS” in 30.5.1.1.11 to read as follows:

This attribute takes the eight-bit value from the 100BASE-T2 MASTER-SLAVE Status register (MII management register 10) bits 7:0 “Idle Error Count” as described in 100BASE-T2 32.5.3.2.6 and 40.5.3.2.9.

Change “to be defined in Clause 40” to “as specified in Clause 40” in 30.6.1.1.5 (two instances).

Delete note attached to 30.6.1.1.5.

32. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2

EDITORIAL NOTE—These changes are required to generalize the names of Management Registers 9 and 10 in order to reflect their use by both 100BASE-T2 and 1000BASE-T.

In 32.5, change the third sentence in paragraph 2 to read as follows:

Register 8 is used to provide the Auto-Negotiation Link Partner NEXT Page Register, Register 9 is used to provide the ~~100BASE-T2 MASTER-SLAVE~~ Control Register, and Register 10 is used to provide the ~~100BASE-T2 MASTER-SLAVE~~ Status Register.

In 32.5.1, change all instances of “T2 Control Register” to “MASTER-SLAVE Control Register.”

In 32.5.1, change all instances of “T2 Status Register” to “MASTER-SLAVE Status Register.”

In rows 2 and 3 of Table 32-3, change “100BASE-T2” to “MASTER-SLAVE.”

In 32.5.3.1, change all instances of “100BASE-T2 Control Register” to “MASTER-SLAVE Control Register.”

In 32.5.3.2, change all instances of “100BASE-T2 Status Register” to “MASTER-SLAVE Status Register.”

In Table 32-7, change “100BASE-T2 Control Register” to “MASTER-SLAVE Control Register” (three instances).

In 32.6.1.2.1, change “100BASE-T2 Control Register” to “MASTER-SLAVE Control Register” (one instance).

In 32.6.1.3.2, change “100BASE-T2 Control Register” to “MASTER-SLAVE Control Register” (one instance).

In 32.13.5.8, change “100BASE-T2 Control Register” to “MASTER-SLAVE Control Register” (in PME 11, PME40).

EDITORIAL NOTE—The changes below reflect moving the definition of Management Register 8 from Clause 32 to Clause 28.

Delete 32.5.4.2.

Renumber 32.5.4.3 as 32.5.4.2.

Renumber 32.5.4.4 as 32.5.4.3.

34. Introduction to 1000 Mb/s baseband network

Delete the phrase “(under development in IEEE P802.3ab)” in the 1000BASE-T entry in the table in 34.1.2.

Insert the following item after b) in 34.4:

c) Within the section Balanced Cabling Link Class D (defined up to 100MHz):

CSMA/CD 1000BASE-T* ISO/IEC8802-3/DAD 19954

*To support 1000BASE-T applications, Class D links shall meet the requirements for return loss, ELFEXT and MDELTEXT specified in 40.7.

Insert the following text and table in Clause 34 as Table 34-2.

Suitable entries for table G4 of ISO/IEC 11801:1995 Annex G would be:

Table 34-2—Table G4 of ISO/IEC 11801:1995

	Balanced cabling							Performance based cabling per Clause 6											
	per clauses 5, 7, and 8							Class A			Class B			Class C			Class D		
	C a t 3 1 0 0 Ω	C a t 4 1 0 0 Ω	C a t 5 1 0 0 Ω	C a t 3 1 2 0 Ω	C a t 4 1 2 0 Ω	C a t 5 1 2 0 Ω	1 5 0 Ω	1 0 Ω	1 2 Ω	1 5 Ω	1 0 Ω	1 2 Ω	1 5 Ω	1 0 Ω	1 2 Ω	1 5 Ω	1 0 Ω	1 2 Ω	1 5 Ω
8802-3: 1000BASE-T			I ²														I ²		

NOTE—“I” denotes that there is information in the International Standard regarding operation on this media.

* 8802-3 imposes additional requirements on return loss, ELFEXT and MDELTEXT.

42. System considerations for multisegment 1000 Mb/s networks

Replace 42.2 item b) with the following:

b) Link distances not to exceed the lesser of 316 m or the segment lengths as shown in Table 42-1.

Insert the following paragraph in 42.3 as the third paragraph:

For a network consisting of two 1000BASE-T DTEs as shown in Figure 42-3, a crossover connection may be required if the auto-crossover function is not implemented. See 40.4 and 40.8.

Replace the text in Figure 42-3 with the following:

See Table 42-1 for maximum segment length.

Annex A

(informative)

Additional reference material

Insert the following references to Annex A. These references will be renumbered in future editions.

[B38] ANSI/TIA/EIA TSB95 (Proposed), Additional Transmission Performance Guidelines for 100 Ohm 4-Pair Category 5.

[B39] TIA/EIA TSB 67 (1995), Transmission Performance Specifications For Field Testing Of Unshielded Twisted-pair Cabling Systems.

Annex 28B

(normative)

IEEE 802.3 Selector Base Page definition

In Table 28B-1, change bit A6 from “Reserved for future technology” to:

Table 28B-1—Technology Ability Field bit assignments

Bit	Technology	Minimum cabling requirement
A6	Reserved for future technology. <u>Asymmetric PAUSE operation for full duplex Links.</u>	<u>Not Applicable</u>

Replace the third paragraph of 28B.2 with the following:

Setting Bit A5 or Bit A6 indicates that the DTE has implemented both the optional MAC control sublayer and the PAUSE function as specified in Clause 31 and Annex 31B. This capability is significant only when the link is configured for full duplex operation, regardless of data rate and medium. The encoding of Bits A5 and A6 is specified in Table 28B-2.

Insert Table 28B-2 after Table 28B-1.

Table 28B-2—Pause encoding

PAUSE (A5)	ASM_DIR (A6)	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. The ASM_DIR bit indicates that asymmetric PAUSE is supported. The value of the PAUSE bit when the ASM_DIR bit is set indicates the direction the PAUSE frames are supported for flow across the link. Asymmetric PAUSE configuration results in independent enabling of the PAUSE receive and PAUSE transmit functions as defined by Annex 31B. See 28B.3 regarding PAUSE configuration resolution.

Change 28B.3 to read as follows:

Since two devices may have multiple abilities in common, a prioritization scheme exists to ensure that the highest common denominator ability is chosen. The following list shall represent the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value, where priorities are listed from highest to lowest.

- a) 1000BASE-T full duplex
- b) 1000BASE-T
- c) 100BASE-T2 full duplex
- d) 100BASE-TX full duplex
- e) 100BASE-T2
- f) 100BASE-T4
- g) 100BASE-TX
- h) 10BASE-T full duplex
- i) 10BASE-T

The rationale for this hierarchy is straightforward. 10BASE-T is the lowest common denominator and therefore has the lowest priority. Full duplex solutions are always higher in priority than their half duplex counterparts. 1000BASE-T has a higher priority than 100 Mb/s technologies. 100BASE-T2 is ahead of 100BASE-TX and 100BASE-T4 because 100BASE-T2 runs across a broader spectrum of copper cabling and can support a wider base of configurations. 100BASE-T4 is ahead of 100BASE-TX because 100BASE-T4 runs across a broader spectrum of copper cabling. The relative order of the technologies specified herein shall not be changed. As each new technology is added, it shall be inserted into its appropriate place in the list, shifting technologies of lesser priority lower in priority. If a vendor-specific technology is implemented, the priority of all IEEE 802.3 standard technologies shall be maintained, with the vendor specific technology inserted at any appropriate priority location.

The use of the PAUSE operation for full duplex links (as indicated by bits A5 and A6) is orthogonal to the negotiated data rate, medium, or link technology. The setting of ~~this~~ these bits indicates the availability of additional DTE capability when full duplex operation is in use. The PAUSE function shall be enabled according to Table 28B-3 only if ~~both the Local Device and the Link Partner have bit A5 set and~~ the Highest Common Denominator is a full duplex technology. There is no priority resolution associated with the PAUSE operation.

Insert the following table at the end of the fourth paragraph of 28B.3:

Table 28B-3—Pause resolution

Local device		Link partner		Local device resolution	Link partner resolution
PAUSE	ASM_DIR	PAUSE	ASM_DIR		
0	0	Don't care	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	0	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	1	Enable PAUSE transmit Disable PAUSE receive	Enable PAUSE receive Disable PAUSE transmit
1	0	0	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	Don't care	1	Don't care	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive
1	1	0	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	1	0	1	Enable PAUSE receive Disable PAUSE transmit	Enable PAUSE transmit Disable PAUSE receive

Annex 28C

(normative)

Next Page Message Code Field definitions

Replace Table 28C-1 with the following:

Table 28C-1—Message code field values

Message Code #	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message Code Description
0	0	0	0	0	0	0	0	0	0	0	0	Reserved for future Auto-Negotiation use
1	0	0	0	0	0	0	0	0	0	0	1	Null Message
2	0	0	0	0	0	0	0	0	0	1	0	One UP with Technology Ability Field follows
3	0	0	0	0	0	0	0	0	0	1	1	Two UPs with Technology Ability Field follow
4	0	0	0	0	0	0	0	0	1	0	0	One UP with Binary coded Remote fault follows
5	0	0	0	0	0	0	0	0	1	0	1	Organizationally Unique Identifier Tagged Message
6	0	0	0	0	0	0	0	0	1	1	0	PHY Identifier Tag Code
7	0	0	0	0	0	0	0	0	1	1	1	100BASE-T2 Technology Message Code. 100BASE-T2 Ability Page to follow using Unformatted Next Page
8	0	0	0	0	0	0	0	1	0	0	0	1000BASE-T Technology Message Code. Two 1000BASE-T Ability Pages to follow using Unformatted Next Pages.
9.....	0	0	0	0	0	0	0	1	0	0	1	Reserved for future Auto-Negotiation use
.....2047	1	1	1	1	1	1	1	1	1	1	1	Reserved for future Auto-Negotiation use

Insert 28C.10

28C.10 Message Code #8 - 1000BASE-T technology message code

Clause 40 (1000BASE-T) uses Next Page Message Code 8 to indicate that 1000BASE-T implementations will follow the transmission of this page [the initial, Message (formatted) Next Page] with two unformatted Next Pages that contain information defined in 40.5.1.2.

Annex 28D

(normative)

Description of extensions to Clause 28 and associated annexes

In 28D.4, change “100BASE-T2 Control Register” to “MASTER-SLAVE Control Register” (one instance.)

In 28D.4 change “100BASE-T2 Status Register” to “MASTER-SLAVE Status Register” (one instance.)

Add 28D.5 to the end of Annex 28D:

28D.5 Extensions required for Clause 40 (1000BASE-T)

Clause 40 (1000BASE-T) makes special use of Auto-Negotiation and requires additional MII registers. This use is summarized below. Details are provided in 40.5.

- a) Auto-Negotiation is mandatory for 1000BASE-T. (40.5.1)
- b) 1000BASE-T requires an ordered exchange of Next Page messages. (40.5.1.2)
- c) 1000BASE-T parameters are configured based on information provided by the ordered exchange of NEXT Page messages.
- d) 1000BASE-T uses MASTER and SLAVE to define PHY operations and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER-SLAVE status. (40.5.2)
- e) 1000BASE-T transmits and receives Next Pages for exchange of information related to MASTER-SLAVE operation. The information is specified in MII registers 9 and 10 (see 32.5.2 and 40.5.1.1), which are required in addition to registers 0-8 as defined in 28.2.4.
- f) 1000BASE-T adds new message codes to be transmitted during Auto-Negotiation. (40.5.1.3)
- g) 1000BASE-T adds 1000BASE-T full duplex and half duplex capabilities to the priority resolution table. (28B.3) and MII Extended Status Register (22.2.4.4)
- h) 1000BASE-T is defined as a valid value for “x” in 28.3.1 (e.g., link_status_1GigT.) 1GigT represents that the 1000BASE-T PMA is the signal source.
- i) 1000BASE-T supports Asymmetric Pause as defined in Annex 28B.

Annex 30B

(normative)

GDMO and ASN.1 definitions for management

Change two instances in AutoNeg Technology of “to be defined in Clause 40” to read “as defined in Clause 40.”

Delete footnote #61 associated with PhyTypeValue that states that 1000BASE-T is under development.

Change three instances in TypeValue of “...to be defined in Clause 40” to read “...as specified in Clause 40.”

Information technology—

Telecommunications and information exchange between systems—

Local and metropolitan area networks—Specific requirements—

Supplement to Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications—

Physical Layer Parameters and Specifications for 1000 Mb/s Operation Over 4 Pair of Category 5 Balanced Copper Cabling, Type 1000BASE-T

40. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 1000BASE-T

40.1 Overview

The 1000BASE-T PHY is one of the Gigabit Ethernet family of high-speed CSMA/CD network specifications. The 1000BASE-T Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) and baseband medium specifications are intended for users who want 1000 Mb/s performance over Category 5 balanced twisted-pair cabling systems. 1000BASE-T signaling requires four pairs of Category 5 balanced cabling, as specified in ISO/IEC 11801:1995 and ANSI/EIA/TIA-568-A (1995) and tested for the additional performance parameters specified in 40.7 using testing procedures defined in proposed ANSI/TIA/EIA TSB95.

This clause defines the type 1000BASE-T PCS, type 1000BASE-T PMA sublayer, and type 1000BASE-T Medium Dependent Interface (MDI). Together, the PCS and the PMA sublayer comprise a 1000BASE-T Physical layer (PHY). Provided in this document are fully functional, electrical, and mechanical specifications for the type 1000BASE-T PCS, PMA, and MDI. This clause also specifies the baseband medium used with 1000BASE-T.

40.1.1 Objectives

The following are the objectives of 1000BASE-T:

- a) Support the CSMA/CD MAC
- b) Comply with the specifications for the GMII (Clause 35)
- c) Support the 1000Mb/s repeater (Clause 41)
- d) Provide line transmission that supports full and half duplex operation
- e) Meet or exceed FCC Class A/CISPR or better operation
- f) Support operation over 100 meters of Category 5 balanced cabling as defined in 40.7
- g) Bit Error Rate of less than or equal to 10^{-10}
- h) Support Auto-Negotiation (Clause 28)

40.1.2 Relationship of 1000BASE-T to other standards

Relations between the 1000BASE-T PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 CSMA/CD LAN Model are shown in Figure 40-1. The PHY sub-layers (shown shaded) in Figure 40-1 connect one Clause 4 Media Access Control (MAC) layer to the medium.

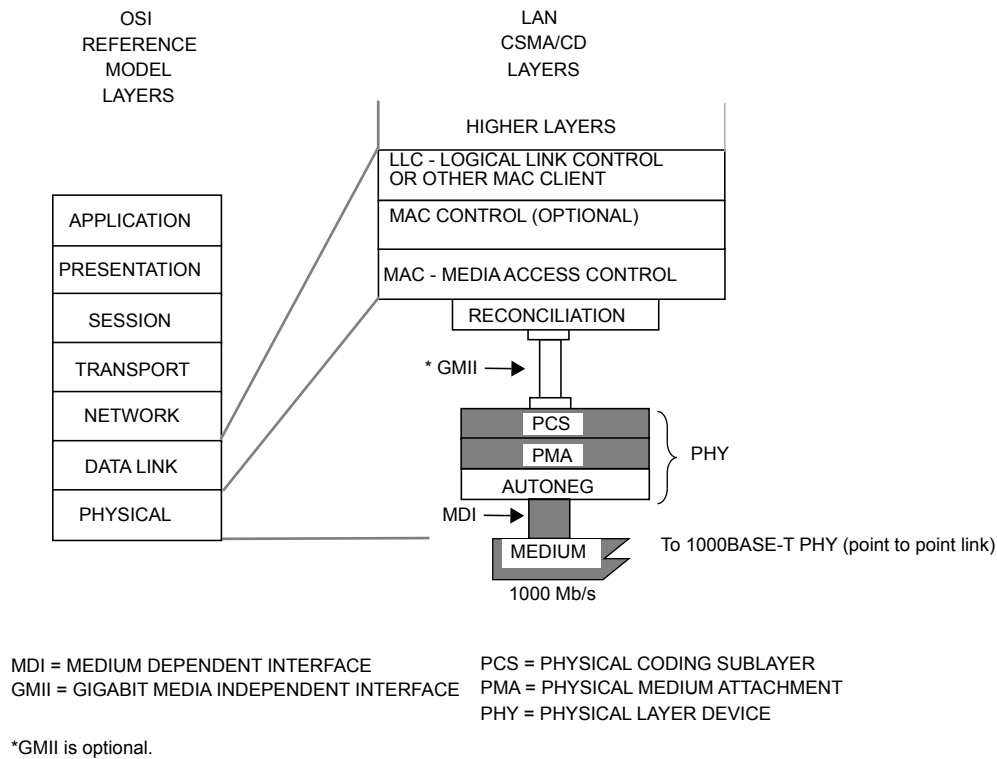


Figure 40-1—Type 1000BASE-T PHY relationship to the ISO Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model

40.1.3 Operation of 1000BASE-T

The 1000BASE-T PHY employs full duplex baseband transmission over four pairs of Category 5 balanced cabling. The aggregate data rate of 1000 Mb/s is achieved by transmission at a data rate of 250 Mb/s over each wire pair, as shown in Figure 40-2. The use of hybrids and cancellers enables full duplex transmission by allowing symbols to be transmitted and received on the same wire pairs at the same time. Baseband signaling with a modulation rate of 125 Mbaud is used on each of the wire pairs. The transmitted symbols are selected from a four-dimensional 5-level symbol constellation. Each four-dimensional symbol can be viewed as a 4-tuple (A_n , B_n , C_n , D_n) of one-dimensional quinary symbols taken from the set {2, 1, 0, -1, -2}. 1000BASE-T uses a continuous signaling system; in the absence of data, Idle symbols are transmitted. Idle mode is a subset of code-groups in that each symbol is restricted to the set {2, 0, -2} to improve synchronization. Five-level Pulse Amplitude Modulation (PAM5) is employed for transmission over each wire pair. The modulation rate of 125 Mbaud matches the GMII clock rate of 125 MHz and results in a symbol period of 8 ns.

A 1000BASE-T PHY can be configured either as a MASTER PHY or as a SLAVE PHY. The MASTER-SLAVE relationship between two stations sharing a link segment is established during Auto-

Negotiation (see Clause 28, 40.5, and Annex 28C). The MASTER PHY uses a local clock to determine the timing of transmitter operations. The SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in Figure 40-3. In a multiport to single-port connection, the multiport device is typically set to be MASTER and the single-port device is set to be SLAVE.

The PCS and PMA subclauses of this document are summarized in 40.1.3.1 and 40.1.3.2. Figure 40-3 shows the functional block diagram.

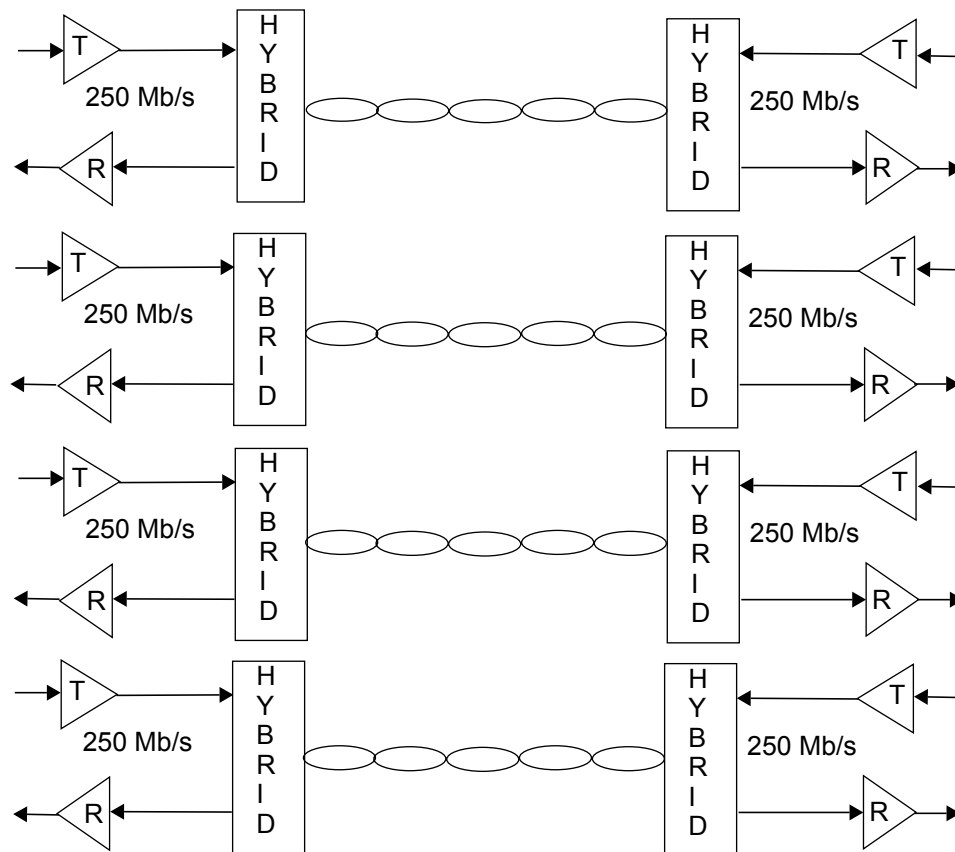
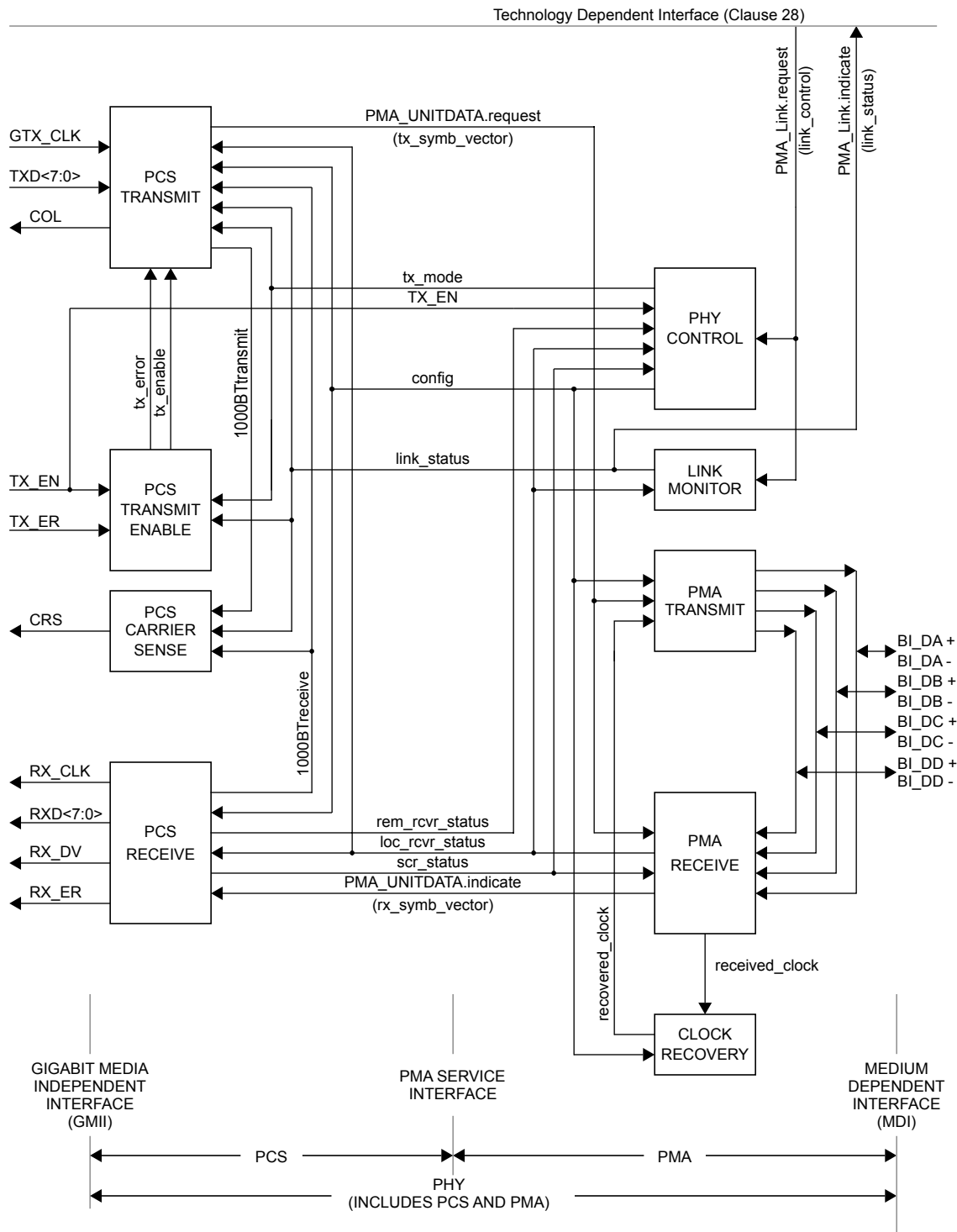


Figure 40-2—1000BASE-T topology



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back to PMA TRANSMIT for loop timing.

Figure 40-3—Functional block diagram

40.1.3.1 Physical Coding Sublayer (PCS)

The 1000BASE-T PCS couples a Gigabit Media Independent Interface (GMII), as described in Clause 35, to a Physical Medium Attachment (PMA) sublayer.

The functions performed by the PCS comprise the generation of continuous code-groups to be transmitted over four channels and the processing of code-groups received from the remote PHY. The process of converting data bits to code-groups is called 4D-PAM5, which refers to the four-dimensional 5-level Pulse Amplitude Modulation coding technique used. Through this coding scheme, eight bits are converted to one transmission of four quinary symbols.

During the beginning of a frame's transmission, when TX_EN is asserted from the GMII, two code-groups representing the Start-of-Stream delimiter are transmitted followed by code-groups representing the octets coming from the GMII. Immediately following the data octets, the GMII sets TX_EN=FALSE, upon which the end of a frame is transmitted. The end of a frame consists of two convolutional state reset symbol periods and two End-of-Stream delimiter symbol periods. This is followed by an optional series of carrier extend symbol periods and, possibly, the start of a new frame during frame bursting. Otherwise, the end of a frame is followed by a series of symbols encoded in the idle mode. The nature of the encoding that follows the end of a frame is determined by the GMII signals TX_ER and TXD<7:0> as specified in Clause 35.

Between frames, a special subset of code-groups using only the symbols {2, 0, -2} is transmitted. This is called idle mode. Idle mode encoding takes into account the information of whether the local PHY is operating reliably or not (see 40.4.2.4) and allows this information to be conveyed to the remote station. During normal operation, idle mode is followed by a data mode that begins with a Start-of-Stream delimiter.

Further patterns are used for signaling a transmit error and other control functions during transmission of a data stream.

The PCS Receive processes code-groups provided by the PMA. The PCS Receive detects the beginning and the end of frames of data and, during the reception of data, descrambles and decodes the received code-groups into octets RXD<7:0> that are passed to the GMII. The conversion of code-groups to octets uses an 8B1Q4 data decoding technique. PCS Receive also detects errors in the received sequences and signals them to the GMII. Furthermore, the PCS contains a PCS Carrier Sense function, a PCS Collision Presence function, and a management interface.

The PCS functions and state diagrams are specified in 40.3. The signals provided by the PCS at the GMII conform to the interface requirements of Clause 35. The PCS Service Interfaces to the GMII and the PMA are abstract message-passing interfaces specified in 40.2.

40.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PMA service interface onto the balanced cabling physical medium and provides the link management and PHY Control functions. The PMA provides full duplex communications at 125 MBaud over four pairs of balanced cabling up to 100 m in length.

The PMA Transmit function comprises four independent transmitters to generate five-level, pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD, as described in 40.4.3.1.

The PMA Receive function comprises four independent receivers for five-level pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD, as described in 40.4.3.2. This signal encoding technique is referred to as 4D-PAM5. The receivers are responsible for acquiring clock and providing code-groups to the PCS as defined by the PMA_UNITDATA.indicate message. The PMA also contains functions for Link Monitor.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control begins following the completion of Auto-Negotiation and provides the start-up functions required for successful 1000BASE-T operation. It determines whether the PHY operates in a normal state, enabling data transmission over the link segment, or whether the PHY sends special code-groups that represent the idle mode. The latter occurs when either one or both of the PHYs that share a link segment are not operating reliably.

PMA functions and state diagrams are specified in 40.4. PMA electrical specifications are given in 40.6.

40.1.4 Signaling

1000BASE-T signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over each wire pair. The signaling scheme achieves a number of objectives including

- a) Forward Error Correction (FEC) coded symbol mapping for data.
- b) Algorithmic mapping and inverse mapping from octet data to a quartet of quinary symbols and back.
- c) Uncorrelated symbols in the transmitted symbol stream.
- d) No correlation between symbol streams traveling both directions on any pair combination.
- e) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
- f) Idle mode uses a subset of code-groups in that each symbol is restricted to the set $\{2, 0, -2\}$ to ease synchronization, start-up, and retraining.
- g) Ability to rapidly or immediately determine if a symbol stream represents data or idle or carrier extension.
- h) Robust delimiters for Start-of-Stream delimiter (SSD), End-of-Stream delimiter (ESD), and other control signals.
- i) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
- j) Ability to automatically detect and correct for pair swapping and unexpected crossover connections.
- k) Ability to automatically detect and correct for incorrect polarity in the connections.
- l) Ability to automatically correct for differential delay variations across the wire-pairs.

The PHY operates in two basic modes, normal mode or training mode. In normal mode, PCS generates code-groups that represent data, control, or idles for transmission by the PMA. In training mode, the PCS is directed to generate only idle code-groups for transmission by the PMA, which enable the receiver at the other end to train until it is ready to operate in normal mode. (See the PCS reference diagram in 40.2.)

40.1.5 Inter-sublayer interfaces

All implementations of the balanced cabling link are compatible at the MDI. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and GMII (if the GMII is implemented) specifications are met. When the PHY is incorporated within the physical bounds of a single-port device or a multiport device, implementation of the GMII is optional. System operation from the perspective of signals at the MDI and management objects are identical whether the GMII is implemented or not.

40.1.6 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

The values of all components in test circuits shall be accurate to within $\pm 1\%$ unless otherwise stated.

Default initializations, unless specifically specified, are left to the implementor.

40.2 1000BASE-T Service Primitives and Interfaces

1000BASE-T transfers data and control information across the following four service interfaces:

- a) Gigabit Media Independent Interface (GMII)
- b) PMA Service Interface
- c) Medium Dependent Interface (MDI)
- d) Technology-Dependent Interface

The GMII is specified in Clause 35; the Technology-Dependent Interface is specified in Clause 28. The PMA Service Interface is defined in 40.2.2 and the MDI is defined in 40.8

40.2.1 Technology-Dependent Interface

1000BASE-T uses the following service primitives to exchange status indications and control signals across the Technology-Dependent Interface as specified in Clause 28:

PMA_LINK.request (link_control)

PMA_LINK.indicate (link_status)

40.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation algorithm to enable and disable operation of the PMA as specified in 28.2.6.2.

40.2.1.1.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PMA reports link_status=FAIL.PHY processes are disabled.
DISABLE	Set by the Auto-Negotiation algorithm in the event fast link pulses are detected. PHY processes are disabled. This allows the Auto-Negotiation algorithm to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions.

40.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in Clause 28.

40.2.1.1.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as defined in 40.4.2.5.

40.2.1.2 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 28.2.6.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation algorithm about the status of the underlying link.

40.2.1.2.1 Semantics of the primitive

PMA_LINK.indicate (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK.

FAIL	No valid link established.
READY	The Link Monitor function indicates that a 1000BASE-T link is intact and ready to be established.
OK	The Link Monitor function indicates that a valid 1000BASE-T link is established. Reliable reception of signals transmitted from the remote PHY is possible.

40.2.1.2.2 When generated

The PMA generates this primitive continuously to indicate the value of link_status in compliance with the state diagram given in Figure 40-16.

40.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 40.3.3.1.

40.2.2 PMA Service Interface

1000BASE-T uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indicate (tx_mode)
 PMA_CONFIG.indicate (config)
 PMA_UNITDATA.request (tx_symb_vector)
 PMA_UNITDATA.indicate (rx_symb_vector)
 PMA_SCRSTATUS.request (scr_status)
 PMA_RXSTATUS.indicate (loc_rcvr_status)
 PMA_REMRXSTATUS.request (rem_rcvr_status)

The use of these primitives is illustrated in Figure 40-4.

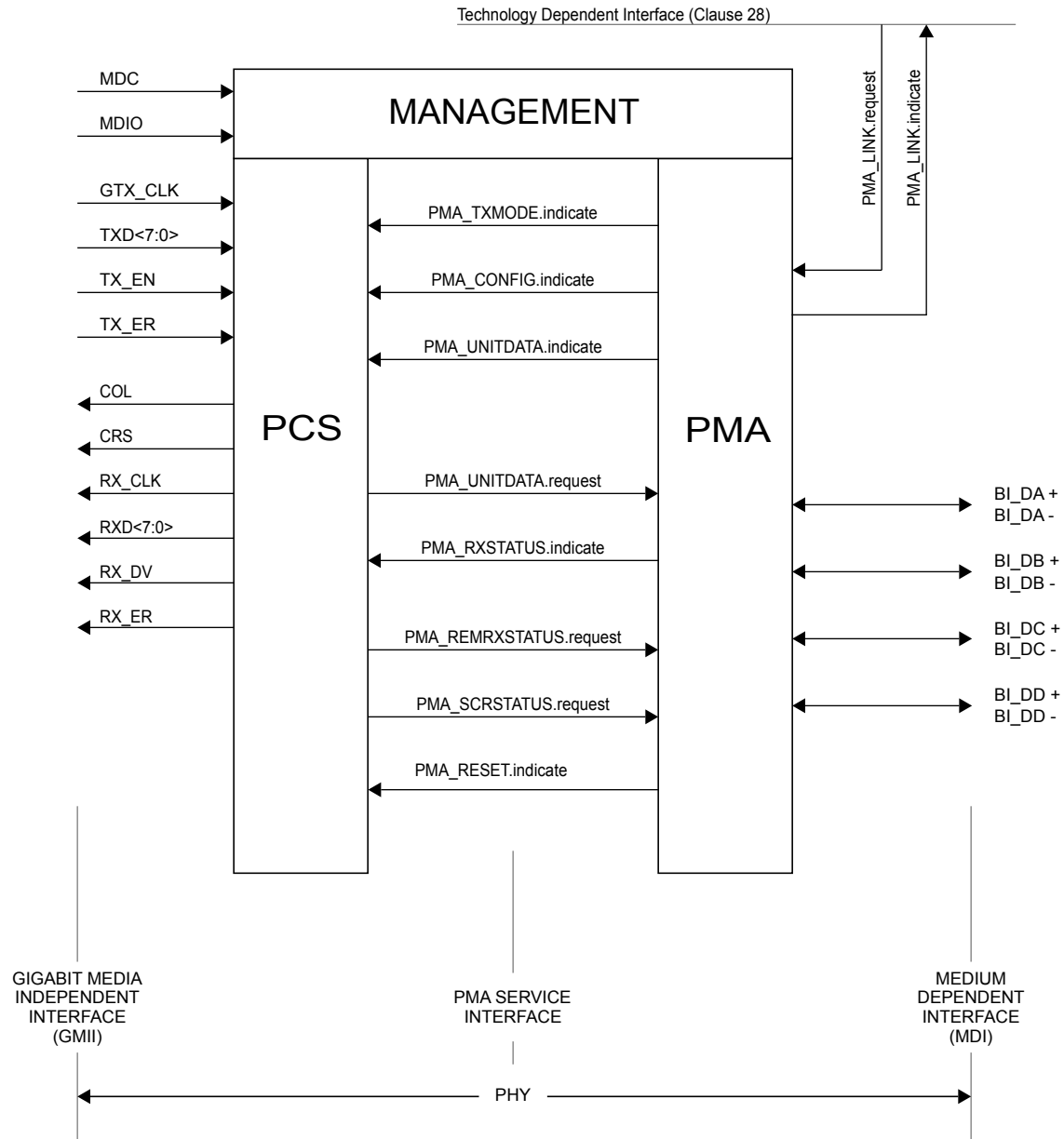


Figure 40-4—1000BASE-T service interfaces

40.2.3 PMA_TXMODE.indicate

The transmitter in a 1000BASE-T link normally sends over the four pairs, code-groups that can represent a GMII data stream, control information, or idles.

40.2.3.1 Semantics of the primitive

PMA_TXMODE.indicate (tx_mode)

PMA_TXMODE.indicate specifies to PCS Transmit via the parameter tx_mode what sequence of code-groups the PCS should be transmitting. The parameter tx_mode can take on one of the following three values of the form:

SEND_N	This value is continuously asserted when transmission of sequences of code-groups representing a GMII data stream (data mode), control mode or idle mode is to take place.
SEND_I	This value is continuously asserted in case transmission of sequences of code-groups representing the idle mode is to take place.
SEND_Z	This value is continuously asserted in case transmission of zeros is required.

40.2.3.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indicate messages continuously.

40.2.3.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Transmit function as described in 40.3.1.3.

40.2.4 PMA_CONFIG.indicate

Each PHY in a 1000BASE-T link is capable of operating as a MASTER PHY and as a SLAVE PHY. MASTER-SLAVE configuration is determined during Auto-Negotiation (40.5). The result of this negotiation is provided to the PMA.

40.2.4.1 Semantics of the primitive

PMA_CONFIG.indicate (config)

PMA_CONFIG.indicate specifies to PCS and PMA Transmit via the parameter config whether the PHY must operate as a MASTER PHY or as a SLAVE PHY. The parameter config can take on one of the following two values of the form:

MASTER	This value is continuously asserted when the PHY must operate as a MASTER PHY.
SLAVE	This value is continuously asserted when the PHY must operate as a SLAVE PHY.

40.2.4.2 When generated

PMA generates PMA_CONFIG.indicate messages continuously.

40.2.4.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter config.

40.2.5 PMA_UNITDATA.request

This primitive defines the transfer of code-groups in the form of the tx_symb_vector parameter from the PCS to the PMA. The code-groups are obtained in the PCS Transmit function using the encoding rules defined in 40.3.1.3 to represent GMII data streams, an idle mode, or other sequences.

40.2.5.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. The tx_symb_vector parameter takes on the form:

SYMB_4D A vector of four quinary symbols, one for each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. Each quinary symbol may take on one of the values -2 , -1 , 0 , $+1$, or $+2$.

The quinary symbols that are elements of tx_symb_vector are called, according to the pair on which each will be transmitted, tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD].

40.2.5.2 When generated

The PCS generates PMA_UNITDATA.request (SYMB_4D) synchronously with every transmit clock cycle.

40.2.5.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated quinary symbols. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD.

40.2.6 PMA_UNITDATA.indicate

This primitive defines the transfer of code-groups in the form of the rx_symb_vector parameter from the PMA to the PCS.

40.2.6.1 Semantics of the primitive

PMA_UNITDATA.indicate (rx_symb_vector)

During reception the PMA_UNITDATA.indicate simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on each of the four receive pairs BI_DA, BI_DB, BI_DC, and BI_DD. The rx_symb_vector parameter takes on the form:

SYMB_4D A vector of four quinary symbols, one for each of the four receive pairs BI_DA, BI_DB, BI_DC, and BI_DD. Each quinary symbol may take on one of the values -2 , -1 , 0 , $+1$, or $+2$.

The quinary symbols that are elements of rx_symb_vector are called, according to the pair upon which each symbol was received, rx_symb_vector[BI_DA], rx_symb_vector[BI_DB], rx_symb_vector[BI_DC], and rx_symb_vector[BI_DD].

40.2.6.2 When generated

The PMA generates PMA_UNITDATA.indicate (SYMB_4D) messages synchronously with signals received at the MDI. The nominal rate of the PMA_UNITDATA.indicate primitive is 125 MHz, as governed by the recovered clock.

40.2.6.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

40.2.7 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter `scr_status` conveys to the PMA Receive function the information that the descrambler has achieved synchronization.

40.2.7.1 Semantics of the primitive

PMA_SCRSTATUS.request (`scr_status`)

The `scr_status` parameter can take on one of two values of the form:

OK	The descrambler has achieved synchronization.
NOT_OK	The descrambler is not synchronized.

40.2.7.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages continuously.

40.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in 40.4.2.3, 40.4.2.4, and 40.4.6.1.

40.2.8 PMA_RXSTATUS.indicate

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter `loc_rcvr_status` conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that `loc_rcvr_status` is used by the PCS Receive decoding functions. The criterion for setting the parameter `loc_rcvr_status` is left to the implementor. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol streams that represent the idle mode.

40.2.8.1 Semantics of the primitive

PMA_RXSTATUS.indicate (`loc_rcvr_status`)

The `loc_rcvr_status` parameter can take on one of two values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

40.2.8.2 When generated

PMA Receive generates PMA_RXSTATUS.indicate messages continuously on the basis of signals received at the MDI.

40.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 40-15 and in subclauses 40.2 and 40.4.6.2.

40.2.9 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its `loc_rcvr_status` parameter. The parameter `rem_rcvr_status` conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The criterion for setting the parameter `rem_rcvr_status` is left to the implementor. It can be based, for example, on asserting `rem_rcvr_status` is NOT_OK until `loc_rcvr_status` is OK and then asserting the detected value of `rem_rcvr_status` after proper PCS receive decoding is achieved.

40.2.9.1 Semantics of the primitive

PMA_REMRXSTATUS.request (`rem_rcvr_status`)

The `rem_rcvr_status` parameter can take on one of two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

40.2.9.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages continuously on the basis on signals received at the MDI.

40.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 40-15.

40.2.10 PMA_RESET.indicate

This primitive is used to pass the PMA Reset function to the PCS (`pcs_reset=ON`) when reset is enabled.

The PMA_RESET.indicate primitive can take on one of two values:

TRUE	Reset is enabled.
FALSE	Reset is not enabled.

40.2.10.1 When generated

The PMA Reset function is executed as described in 40.4.2.1.

40.2.10.2 Effect of receipt

The effect of receipt of this primitive is specified in 40.4.2.1.

40.3 Physical Coding Sublayer (PCS)

The PCS comprises one PCS Reset function and four simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit Enable, PCS Transmit, PCS Receive, and PCS Carrier Sense. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 40-5, shows how the four operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive, and are not shown in Figure 40-5. Management is specified in Clause 30. See also Figure 40-7, which defines the structure of frames passed from PCS to PMA.

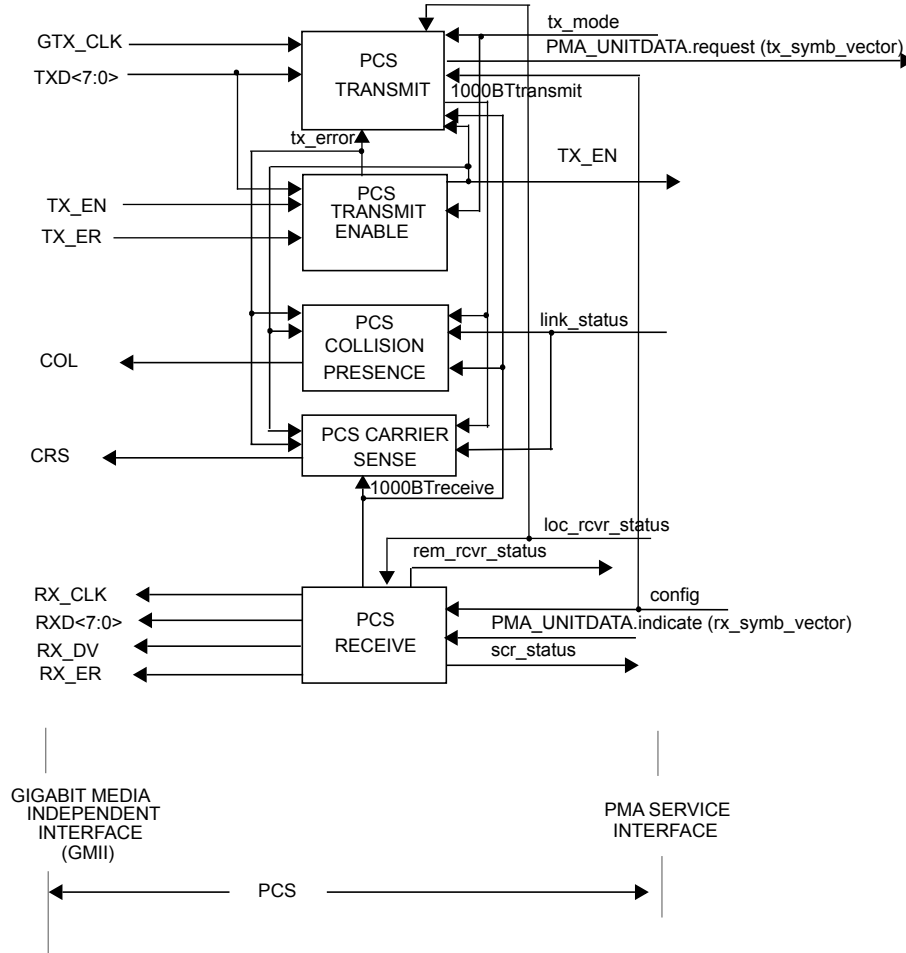


Figure 40-5—PCS reference diagram

40.3.1 PCS functions

40.3.1.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

- a) Power on (see 36.2.5.1.3).
- b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset=ON while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

40.3.1.2 PCS Data Transmission Enable

The PCS Data Transmission Enabling process generates the signals tx_enable and tx_error, which PCS Transmit uses for data and carrier extension encoding. The process uses logical operations on tx_mode,

TX_ER, TX_EN, and TXD<7:0>. The PCS shall implement the Data Transmission Enabling process as depicted in Figure 40-8 including compliance with the associated state variables as specified in 40.3.3.

40.3.1.3 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 40-9.

The PCS Transmit function generates the GMII signal COL based on whether a reception is occurring simultaneously with transmission. The PCS Transmit function is not required to generate the GMII signal COL in a 1000BASE-T PHY that does not support half duplex operation.

In each symbol period, PCS Transmit generates a code-group (A_n , B_n , C_n , D_n) that is transferred to the PMA via the PMA_UNITDATA.request primitive. The PMA transmits symbols A_n , B_n , C_n , D_n over wire-pairs BI_DA, BI_DB, BI_DC, and BI_DD respectively. The integer, n , is a time index that is introduced to establish a temporal relationship between different symbol periods. A symbol period, T , is nominally equal to 8 ns. In normal mode of operation, between streams of data indicated by the parameter tx_enable, PCS Transmit generates sequences of vectors using the encoding rules defined for the idle mode. Upon assertion of tx_enable, PCS Transmit passes a SSD of two consecutive vectors of four quinary symbols to the PMA, replacing the first two preamble octets. Following the SSD, each TXD<7:0> octet is encoded using an 4D-PAM5 technique into a vector of four quinary symbols until tx_enable is de-asserted. If TX_ER is asserted while tx_enable is also asserted, then PCS Transmit passes to the PMA vectors indicating a transmit error. Note that if the signal TX_ER is asserted while SSD is being sent, the transmission of the error condition is delayed until transmission of SSD has been completed. Following the de-assertion of tx_enable, a Convolutional State Reset (CSReset) of two consecutive code-groups, followed by an ESD of two consecutive code-groups, is generated, after which the transmission of idle or control mode is resumed.

If a PMA_TXMODE.indicate message has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indicate message has the value SEND_I, PCS Transmit generates sequences of code-groups according to the encoding rule in training mode. Special code-groups that use only the values $\{+2, 0, -2\}$ are transmitted in this case. Training mode encoding also takes into account the value of the parameter loc_rcvr_status. By this mechanism, a PHY indicates the status of its own receiver to the link partner during idle transmission.

In the normal mode of operation, the PMA_TXMODE.indicate message has the value SEND_N, and the PCS Transmit function uses an 8B1Q4 coding technique to generate at each symbol period code-groups that represent data, control or idle based on the code-groups defined in Table 40-1 and Table 40-2. During transmission of data, the TXD<7:0> bits are scrambled by the PCS using a side-stream scrambler, then encoded into a code-group of quinary symbols and transferred to the PMA. During data encoding, PCS Transmit utilizes a three-state convolutional encoder.

The transition from idle or carrier extension to data is signalled by inserting a SSD, and the end of transmission of data is signalled by an ESD. Further code-groups are reserved for signaling the assertion of TX_ER within a stream of data, carrier extension, CSReset, and other control functions. During idle and carrier extension encoding, special code-groups with symbol values restricted to the set $\{2, 0, -2\}$ are used. These code-groups are also generated using the transmit side-stream scrambler. However, the encoding rules for the idle, SSD, and carrier extend code-groups are different from the encoding rules for data, CSReset, CSExtend, and ESD code-groups. During idle, SSD, and carrier extension, the PCS Transmit function reverses the sign of the transmitted symbols. This allows, at the receiver, sequences of code-groups that represent data, CSReset, CSExtend, and ESD to be easily distinguished from sequences of code-groups that represent SSD, carrier extension, and idle.

PCS encoding involves the generation of the four-bit words $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$ from which the quinary symbols (A_n , B_n , C_n , D_n) are obtained. The four-bit words $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$ are determined (as explained in 40.3.1.3.2) from sequences of pseudorandom binary symbols derived from the transmit side-stream scrambler.

40.3.1.3.1 Side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indicate message assumes the value MASTER, PCS Transmit shall employ

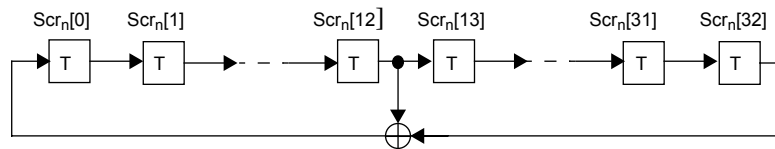
$$g_M(x) = 1 + x^{13} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. If the PMA_CONFIG.indicate message assumes the value of SLAVE, PCS Transmit shall employ

$$g_S(x) = 1 + x^{20} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. An implementation of master and slave PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 40-6. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementor. In no case shall the scrambler state be initialized to all zeros.

Side-stream scrambler employed by the MASTER PHY



Side-stream scrambler employed by the SLAVE PHY

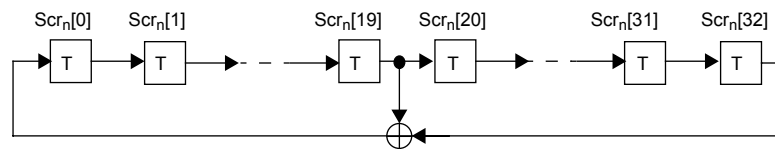


Figure 40-6—A realization of side-stream scramblers by linear feedback shift registers

40.3.1.3.2 Generation of bits $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$

PCS Transmit encoding rules are based on the generation, at time n , of the twelve bits $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$. The eight bits, $Sx_n[3:0]$ and $Sy_n[3:0]$, are used to generate the scrambler octet $Sc_n[7:0]$ for decorrelating the GMII data word $TXD<7:0>$ during data transmission and for generating the idle and training symbols. The four bits, $Sg_n[3:0]$, are used to randomize the signs of the quinary symbols (A_n , B_n , C_n , D_n) so that each symbol stream has no dc bias. These twelve bits are generated in a systematic fashion using three bits, X_n , Y_n , and $Scr_n[0]$, and an auxiliary generating polynomial, $g(x)$. The two bits, X_n and Y_n , are mutually uncorrelated and also uncorrelated with the bit $Scr_n[0]$. For both master and slave PHYs, they are

obtained by the same linear combinations of bits stored in the transmit scrambler shift register delay line. These two bits are derived from elements of the same maximum-length shift register sequence of length $2^{33} - 1$ as $Scr_n[0]$, but shifted in time. The associated delays are all large and different so that there is no short-term correlation among the bits $Scr_n[0]$, X_n , and Y_n . The bits X_n and Y_n are generated as follows:

$$X_n = Scr_n[4] \wedge Scr_n[6]$$

$$Y_n = Scr_n[1] \wedge Scr_n[5]$$

where $\wedge$ denotes the XOR logic operator. From the three bits X_n , Y_n , and $Scr_n[0]$, further mutually uncorrelated bit streams are obtained systematically using the generating polynomial

$$g(x) = x^3 \wedge x^8$$

The four bits $Sy_n[3:0]$ are generated using the bit $Scr_n[0]$ and $g(x)$ as in the following equations:

$$Sy_n[0] = Scr_n[0]$$

$$Sy_n[1] = g(Scr_n[0]) = Scr_n[3] \wedge Scr_n[8]$$

$$Sy_n[2] = g^2(Scr_n[0]) = Scr_n[6] \wedge Scr_n[16]$$

$$Sy_n[3] = g^3(Scr_n[0]) = Scr_n[9] \wedge Scr_n[14] \wedge Scr_n[19] \wedge Scr_n[24]$$

The four bits $Sx_n[3:0]$ are generated using the bit X_n and $g(x)$ as in the following equations:

$$Sx_n[0] = X_n = Scr_n[4] \wedge Scr_n[6]$$

$$Sx_n[1] = g(X_n) = Scr_n[7] \wedge Scr_n[9] \wedge Scr_n[12] \wedge Scr_n[14]$$

$$Sx_n[2] = g^2(X_n) = Scr_n[10] \wedge Scr_n[12] \wedge Scr_n[20] \wedge Scr_n[22]$$

$$Sx_n[3] = g^3(X_n) = Scr_n[13] \wedge Scr_n[15] \wedge Scr_n[18] \wedge Scr_n[20] \wedge Scr_n[23] \wedge Scr_n[25] \wedge Scr_n[28] \wedge Scr_n[30]$$

The four bits $Sg_n[3:0]$ are generated using the bit Y_n and $g(x)$ as in the following equations:

$$Sg_n[0] = Y_n = Scr_n[1] \wedge Scr_n[5]$$

$$Sg_n[1] = g(Y_n) = Scr_n[4] \wedge Scr_n[8] \wedge Scr_n[9] \wedge Scr_n[13]$$

$$Sg_n[2] = g^2(Y_n) = Scr_n[7] \wedge Scr_n[11] \wedge Scr_n[17] \wedge Scr_n[21]$$

$$Sg_n[3] = g^3(Y_n) = Scr_n[10] \wedge Scr_n[14] \wedge Scr_n[15] \wedge Scr_n[19] \wedge Scr_n[20] \wedge Scr_n[24] \wedge Scr_n[25] \wedge Scr_n[29]$$

By construction, the twelve bits $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$ are derived from elements of the same maximum-length shift register sequence of length $2^{33} - 1$ as $Scr_n[0]$, but shifted in time by varying delays. The associated delays are all large and different so that there is no apparent correlation among the bits.

40.3.1.3.3 Generation of bits $Sc_n[7:0]$

The bits $Sc_n[7:0]$ are used to scramble the GMII data octet $TXD[7:0]$ and for control, idle, and training mode quartet generation. The definition of these bits is dependent upon the bits $Sx_n[3:0]$ and $Sy_n[3:0]$ that are

specified in 40.3.1.3.2, the variable tx_mode that is obtained through the PMA Service Interface, the variable tx_enable_n that is defined in Figure 40-8, and the time index n .

The four bits $Sc_n[7:4]$ are defined as

$$Sc_n[7:4] = \begin{cases} Sx_n[3:0] & \text{if } (tx_enable_n = 1) \\ [0\ 0\ 0\ 0] & \text{else} \end{cases}$$

The bits $Sc_n[3:1]$ are defined as

$$Sc_n[3:1] = \begin{cases} [0\ 0\ 0] & \text{if } (tx_mode = SEND_Z) \\ Sy_n[3:1] & \text{else if } (n-n_0) = 0 \pmod{2} \\ (Sy_{n-1}[3:1] \wedge [1\ 1\ 1]) & \text{else} \end{cases}$$

where n_0 denotes the time index of the last transmitter side-stream scrambler reset.

The bit $Sc_n[0]$ is defined as

$$Sc_n[0] = \begin{cases} 0 & \text{if } (tx_mode = SEND_Z) \\ Sy_n[0] & \text{else} \end{cases}$$

40.3.1.3.4 Generation of bits $Sd_n[8:0]$

The PCS Transmit function generates a nine-bit word $Sd_n[8:0]$ from Sc_n that represents either a convolutionally encoded stream of data, control, or idle mode code-groups. The convolutional encoder uses a three-bit word $cs_n[2:0]$, which is defined as

$$cs_n[1] = \begin{cases} Sd_n[6] \wedge cs_{n-1}[0] & \text{if } (tx_enable_{n-2} = 1) \\ 0 & \text{else} \end{cases}$$

$$cs_n[2] = \begin{cases} Sd_n[7] \wedge cs_{n-1}[1] & \text{if } (tx_enable_{n-2} = 1) \\ 0 & \text{else} \end{cases}$$

$$cs_n[0] = cs_{n-1}[2]$$

from which $Sd_n[8]$ is obtained as

$$Sd_n[8] = cs_n[0]$$

The convolutional encoder bits are non-zero only during the transmission of data. Upon the completion of a data frame, the convolutional encoder bits are reset using the bit $csreset_n$. The bit $csreset_n$ is defined as

$$csreset_n = (tx_enable_{n-2}) \text{ and } (\text{not } tx_enable_n)$$

The bits $Sd_n[7:6]$ are derived from the bits $Sc_n[7:6]$, the GMII data bits $TXD_n[7:6]$, and from the convolutional encoder bits as

$$Sd_n[7] = \begin{cases} Sc_n[7] \wedge TXD_n[7] & \text{if } (csreset_n = 0 \text{ and } tx_enable_{n-2} = 1) \\ cs_{n-1}[1] & \text{else if } (csreset_n = 1) \\ Sc_n[7] & \text{else} \end{cases}$$

$$Sd_n[6] = \begin{cases} Sc_n[6] \wedge TXD_n[6] & \text{if } (csreset_n = 0 \text{ and } tx_enable_{n-2} = 1) \\ cs_{n-1}[0] & \text{else if } (csreset_n = 1) \\ Sc_n[6] & \text{else} \end{cases}$$

The bits $Sd_n[5:3]$ are derived from the bits $Sc_n[5:3]$ and the GMII data bits $TXD_n[5:3]$ as

$$Sd_n[5:3] = \begin{cases} Sc_n[5:3] \wedge TXD_n[5:3] & \text{if } (tx_enable_{n-2} = 1) \\ Sc_n[5:3] & \text{else} \end{cases}$$

The bit $Sd_n[2]$ is used to scramble the GMII data bit $TXD_n[2]$ during data mode and to encode loc_rcvr_status otherwise. It is defined as

$$Sd_n[2] = \begin{cases} Sc_n[2] \wedge TXD_n[2] & \text{if } (tx_enable_{n-2} = 1) \\ Sc_n[2] \wedge 1 & \text{else if } (loc_rcvr_status = \text{OK}) \\ Sc_n[2] & \text{else} \end{cases}$$

The bits $Sd_n[1:0]$ are used to transmit carrier extension information during $tx_mode = \text{SEND_N}$ and are thus dependent upon the bits $cext_n$ and $cext_err_n$. These bits are dependent on the variable tx_error_n , which is defined in Figure 40-8. These bits are defined as

$$cext_n = \begin{cases} tx_error_n & \text{if } ((tx_enable_n = 0) \text{ and } (TXD_n[7:0] = 0x0F)) \\ 0 & \text{else} \end{cases}$$

$$cext_err_n = \begin{cases} tx_error_n & \text{if } ((tx_enable_n = 0) \text{ and } (TXD_n[7:0] \neq 0x0F)) \\ 0 & \text{else} \end{cases}$$

$$Sd_n[1] = \begin{cases} Sc_n[1] \wedge TXD_n[1] & \text{if } (tx_enable_{n-2} = 1) \\ Sc_n[1] \wedge cext_err_n & \text{else} \end{cases}$$

$$Sd_n[0] = \begin{cases} Sc_n[0] \wedge TXD_n[0] & \text{if } (tx_enable_{n-2} = 1) \\ Sc_n[0] \wedge cext_n & \text{else} \end{cases}$$