



**IEEE Standard for
Information technology—
Telecommunications and information
exchange between systems—
Local and metropolitan area networks—
Specific requirements**

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

**Amendment 1: Physical Layer and Management Parameters
for 10 Gb/s Operation, Type 10GBASE-T**

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

IEEE
3 Park Avenue
New York, NY 10016-5997, USA

1 September 2006

IEEE Std 802.3an™-2006
(Amendment to
IEEE Std 802.3™-2005)

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**LAN/MAN Standards Committee
of the
IEEE Computer Society**

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Abstract: This amendment to IEEE Std 802.3-2005 specifies a new Physical Coding Sublayer interface and a new Physical Medium Attachment sublayer interface for 10 Gb/s Ethernet. 10GBASE-T specifies a LAN interconnect for up to 100 m of balanced twisted-pair structured cabling systems.

Keywords: 802.3an, 10GBASE-T, 10 Gigabit Ethernet, Auto-Negotiation, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, structured cabling, XAUI, XGMII

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Introduction

This introduction is not part of IEEE Std 802.3an-2006, IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements CSMA/CD Access Method and Physical Layer Specifications, Amendment 1: Physical Layer and Management Parameters for 10 Gb/s Operation, Type 10GBASE-T

IEEE Std 802.3 was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3an-2006). A historical listing of projects that have added to or modified IEEE Std 802.3 is included in IEEE Std 802.3-2005.

The media access control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new protocol capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x™ specified full duplex operation and a flow control protocol, IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet) and IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile). These major additions are all now included in IEEE Std 802.3-2005 and are not maintained as separate documents. This amendment adds additional capabilities for 10 Gb/s operation.

At the date of publication of IEEE Std 802.3an-2006, IEEE Std 802.3 is comprised of the following documents:

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4a. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s physical layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s physical layer specifications. It also includes specification of 802.3 link aggregation.

Section Four—Includes Clause 44 through Clause 54 and Annex 44A through Annex 50A. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s physical layer specifications.

Section Five—Includes Clause 56 through Clause 67 and Annex 58A through Annex 67A. Section Five includes subscriber access physical layers and sublayers for operation from 512 kb/s to 1000 Mb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network.

IEEE Std 802.3-2005/Cor 1-2006

This corrigendum clarifies and corrects isolation text for twisted pair Ethernet physical interfaces, including harmonization for both powered and unpowered Medium Dependent interfaces.

IEEE Std 802.3an-2006

This amendment includes changes to IEEE Std 802.3-2005 and adds Clause 55 and Annex 55A and Annex 55B. This amendment adds a new Physical Layer for 10 Gb/s operation over balanced twisted-pair structured cabling systems. IEEE 802.3 will continue to evolve.

New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Conformance test methodology

An additional standard, IEEE Std 1802.3™-2001, provides conformance test information for 10BASE-T.

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Portions of this standard can be downloaded from the Internet. Material include PICS tables, data tables, and code. URLs are listed in the text in the appropriate sections. Annex 55A includes normative information that is part of this standard but not included in this document. This information can be accessed from the IEEE World Wide Web site.

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Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment 1: Physical Layer and Management Parameters for 10 Gb/s Operation, Type 10GBASE-T

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~striketrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editorial notes will not be carried over into future editions because the changes will be incorporated into the base standard.

1. Introduction

1.3 Normative references

Insert the following normative reference in alphanumeric order.

ANSI/TIA-TSB-155 (draft 4, 2006); Additional guidelines for 4-pair 100 Ω Category 6 Cabling for 10GBASE-T Applications.¹

ANSI/TIA/EIA-568-B.2-10 (draft 4, 2006); Transmission performance specifications for 4-pair 100 Ω augmented Category 6 cabling.

ISO/IEC 11801 Edition 2.1 (draft); Information technology—Generic cabling for customer premises. Draft document number ISO/IEC JTC 1/SC 25 N 755.²

ISO/IEC 24750; Guidelines for the support of 10GBASE-T over Copper Balanced Pairs of Class E and Class F as per ISO/IEC 11801: 2002 and IEEE Std 802.3an and a Working Draft for an amendment to ISO/IEC 11801:2002, Generic cabling for customer premises.

1.4 Definitions

Change subclause 1.4.335 as follows:

1.4.335 Technology Ability Field: Within IEEE 802.3, a ~~an~~ seven ~~eight~~ bit field in the Auto-Negotiation base page that is used to indicate the abilities of a local station, such as support for 10BASE-T, 100BASE-T4, and 100BASE-TX, as well as full duplex.

Insert the following definitions in alphanumeric order:

1.4.xxx 10GBASE-T: IEEE 802.3 Physical Layer specification for a 10 Gb/s LAN using four pairs of Class E or Class F balanced copper cabling. (See IEEE Std 802.3, Clause 55.)

1.4.xxx 64B/65B transmission code: A block oriented encoding where 64-bit blocks are prepended with a single bit to indicate whether the block contains only data or a mix of data and control information. (See IEEE Std 802.3, Clause 55.)

1.4.xxx DSQ128: The 128 point double square (DSQ) constellation mapping used in 10GBASE-T. This constellation is obtained by taking a 2D constellation with 16-level pulse amplitude modulation (PAM16) on each dimension and eliminating half the points to create a checkerboard pattern. This constellation is based on a lattice called RZ² in the literature. (See IEEE Std 802.3, Clause 55.)

NOTE—See also Forney [B28A]^{3, 4}

¹ANSI publications are available from the Sales Department, American National Standards Institute, 25 West 43rd Street, 4th Floor, New York, NY 10036, USA (<http://www.ansi.org/>).

²ISO/IEC publications are available from the ISO Central Secretariat, Case Postale 56, 1 rue de Varembe, CH-1211, Genève 20, Switzerland/Suisse (<http://www.iso.ch/>). ISO/IEC publications are also available in the United States from Global Engineering Documents, 15 Inverness Way East, Englewood, Colorado 80112, USA (<http://global.ihs.com/>). Electronic copies are available in the United States from the American National Standards Institute, 25 West 43rd Street, 4th Floor, New York, NY 10036, USA (<http://www.ansi.org/>).

³The numbers in brackets correspond to those of the bibliography in Annex A.

⁴Notes in text, tables, and figures are given for information only, and do not contain requirements needed to implement the standard.

1.4.xxx hybrid: A circuit (implementable with active or passive components) that enables full duplex transmission by allowing symbols to be transmitted and received on the same wire pair at the same time. It is often used together with an echo canceller to get adequate separation of transmit and receive signals.

1.4.xxx LDPC(1723,2048) frame: 64B/65B transmission code blocks mapped into a low density parity check (LDPC) frame with 1723 coded bits, 325 check bits and 1536 uncoded bits. (See IEEE 802.3, Clause 55.)

1.4.xxx Tomlinson-Harashima precoder (THP): A precoding technique for intersymbol interference mitigation. (See IEEE 802.3, Clause 55.)

1.5 Abbreviations

Insert the following abbreviations in alphanumeric order:

AN	Auto-Negotiation
CAT6	Category 6 balanced cabling
DSQ	double square
FIR	finite impulse response
LD	local device
LDPC	low density parity check
LP	link partner
NP	next page
SFDR	spurious free dynamic range
THP	Tomlinson-Harashima precoder
XNP	extended Next Page

Change title of Clause 28 as shown

28. Physical Layer link signaling for ~~10 Mb/s, 100 Mb/s, and 1000 Mb/s~~ Auto-Negotiation on twisted pair

28.2 Functional specifications

Change the first sentence of the second paragraph of subclause 28.2 as follows, note that the figure numbers are auto-adjusted from IEEE Std 802.3-2005 (Figure 28-14 from IEEE Std 802.3-2005 is now Figure 28-16, Figure 28-15 from IEEE Std 802.3-2005 is now Figure 28-17, etc.).

The Auto-Negotiation function shall provide the Auto-Negotiation Transmit, Receive, ~~and Arbitration, and NLP Receive Link Integrity Test~~ functions and comply with the state diagrams of ~~Figures 28-14 to 28-17~~ Figure 28-16 to Figure 28-18. The Auto-Negotiation function shall provide the NLP Receive Link Integrity Test function and comply with the state diagram of Figure 28-19 if the PHY supports 10BASE-T operation.

28.2.1.1.1 FLP burst encoding

Change the first paragraph of subclause 28.2.1.1.1 as follows

~~FLP Bursts shall be composed of link pulses meeting the requirements of Figure 14-12. All link test pulses in the FLP Burst sequence shall meet the template requirements of Figure 14-12 when measured across each of the test loads defined in Figure 14-11; both with the load connected directly to the TD circuit and with the load connected through all of the cable types and distances supported by the advertised capabilities. A Fast Link Pulse Burst consists of 33 pulse positions. The 17 odd-numbered pulse positions shall contain a link pulse and represent clock information. The 16 even-numbered pulse positions shall represent data information as follows: a link pulse present in an even-numbered pulse position represents a logic one, and a link pulse absent from an even-numbered pulse position represents a logic zero. Clock pulses are differentiated from data pulses by the spacing between pulses as shown in Figure 28-5 and enumerated in Table 28-1. An extended FLP Burst contains 97 similarly defined pulse positions with 49 odd-numbered clock pulses and 48 even-numbered data pulses.~~

28.2.1.1.2 Transmit timing

Change the second paragraph of 28.2.1.1.2 to read as follows:

~~The first link pulse in consecutive FLP Bursts shall occur at a 16 ms $\pm$ 8 ms interval when using non-optimized FLP Burst to FLP Burst timing, see parameter T6 (Figure 28-6). Devices supporting extended Next Pages shall use optimized FLP Burst to FLP Burst timing. The first link pulse in consecutive FLP Bursts shall occur at a 8.25 ms $\pm$ 0.25 ms interval when using optimized FLP Burst to FLP Burst timing, see parameter T7 (Figure 28-6). Optimized FLP Burst to FLP Burst limits are intended to reduce negotiation time.~~

Replace Figure 28-6 with the following:

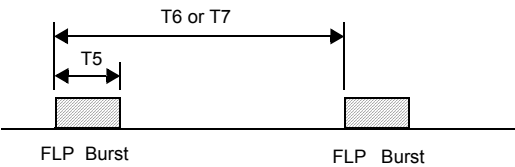


Figure 28–6—FLP Burst to FLP Burst timing

Change Table 28–1, adding row T7 and changing T4 and T5 as shown.

Table 28–1—FLP Burst timing summary

#	Parameter	Min.	Typ.	Max.	Units
T1	Clock/Data Pulse Width (Figure 14–12)		100		ns
T2	Clock Pulse to Clock Pulse	111	125	139	μs
T3	Clock Pulse to Data Pulse (Data = 1)	55.5	62.5	69.5	μs
T4	Pulses in a Burst	17 for 16-bit 49 for 48-bit		33 for 16-bit 97 for 48-bit	#
T5	Burst Width		2 for 16-bit 6 for 48-bit		ms
T6	FLP Burst to FLP Burst	8	16	24	ms
T7	Optimized FLP Burst to FLP Burst	8		8.5	ms

28.2.1.2 Link Codeword encoding

Replace Figure 28–7 with the following:

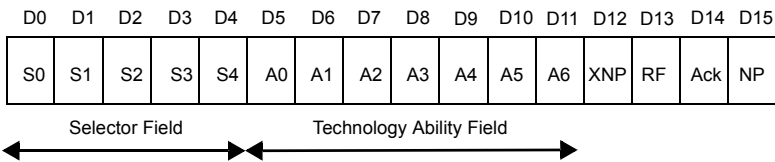


Figure 28–7—Base page encoding

Change the first paragraph of 28.2.1.2.2 as follows:

28.2.1.2.2 Technology Ability Field

Technology Ability Field (A[76:0]) is an ~~seventeen~~^{seventy-eight} bit wide field containing information indicating supported technologies specific to the selector field value. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. The Technology Ability Field encoding for the IEEE 802.3 selector is described in Annex 28B.2 and in Annex 28D. Multiple technologies may be advertised in the Link Codeword. A device shall support the data service ability for a technology it advertises. It is the responsibility of the Arbitration function to determine the common mode of operation shared by a Link Partner and to resolve multiple common modes.

Insert 28.2.1.2.3 and renumber subsequent subclauses

28.2.1.2.3 Extended Next Page

Extended Next Page (XNP) is encoded in bit D12 of the base Link Codeword. The extended Next Page bit indicates that the local device supports transmission of extended Next Pages when set to a logic one, and indicates that the local device does not support extended Next Pages when set to a logic zero. The use of extended Next Page is orthogonal to the negotiated data rate, medium, or link technology. The extended Next Page bit is used in accordance with the extended Next Page function specifications in 28.2.3.4.

When the selector field value is the IEEE Std 802.5 value or the IEEE Std 802.9 value the extended Next Page function is not supported and bit D12 is defined as being an additional Technology Ability Field bit A7, extending the Technology Ability Field to be an eight bit wide field (A[7:0]).

28.2.2.1 FLP Burst ability detection and decoding

Change the fifth paragraph 28.2.2.1 to read as follows:

FLP Bursts conforming to the `nlp_test_min_timer` and `nlp_test_max_timer` timing as shown in Figure 28–10 shall be considered to have valid separation. The `nlp_test_min_timer` range for devices that do not support extended Next Pages is shown in Figure 28–10. The range of `nlp_test_min_timer` for devices that support extended Next Pages is specified in 28.3.2.

28.2.3.4 Next Page function

Change first paragraph of subclause 28.2.3.4 as follows:

The Next Page function uses the standard Auto-Negotiation arbitration mechanisms to allow exchange of arbitrary pieces of data. Data is carried by optional Next Pages of information, which follow the transmission and acknowledgment procedures used for the base Link Codeword. ~~Two~~ Four types of Next Page encodings are defined: Message Pages, ~~and~~ Unformatted Pages, extended Message Pages, and extended Unformatted Pages.

Change third, fourth and fifth paragraphs of subclause 28.2.3.4 as follows:

Next Page operation is controlled by the same ~~two~~ three mandatory control bits, Next Page, ~~extended Next Page~~, and Acknowledge, used in the Base Link Codeword. Setting the NP bit in the Base Link Codeword to logic one indicates that the device is Next Page able. Setting the extended Next Page bit in the Base Page Link Codeword to logic one indicates that the device is extended Next Page able. If both a device and its Link Partner are Next Page able, then Next Page exchange may occur. If both a device and its Link Partner are extended Next Page able, then any Next Page exchange that occurs shall use the extended Next Page encoding. If one or both devices are not Next Page able, then Next Page exchange will not occur and, after the base Link Codewords have been exchanged, the FLP LINK GOOD CHECK state will be entered. The Toggle bit is used to ensure proper synchronization between the Local Device and the Link Partner.

Next Page exchange occurs after the base Link Codewords have been exchanged. Next Page exchange consists of using the normal Auto-Negotiation arbitration process to send Next Page messages. ~~Two~~ Four message encodings are defined: Message Pages, ~~which contain predefined 11-bit codes, and~~ Unformatted Pages, extended Message Pages, and extended Unformatted Pages. Unformatted Pages can be combined to send extended messages. If the Selector Field values do not match, then each series of Unformatted Pages shall be preceded by a Message Page containing a message code that defines how the following Unformatted Pages will be interpreted. If the Selector Field values match, then the convention governing the use of Message Pages shall be as defined by the Selector Field value definition. Any number of Next Pages may be sent in any order; however, it is recommended that the total number of Next Pages sent be kept small to minimize the link startup time.

Next Page transmission ends when both ends of a link segment set their Next Page bits to logic zero, indicating that neither has anything additional to transmit. It is possible for one device to have more pages to transmit than the other device. Once a device has completed transmission of its Next Page information, it shall transmit Message Pages, or extended Message Pages, with Null message codes and the NP bit set to logic zero while its Link Partner continues to transmit valid Next Pages. An Auto-Negotiation able device shall recognize reception of Message Pages, or extended Message Pages, with Null message codes as the end of its Link Partner's Next Page information.

Insert subclause 28.2.3.4.2 and renumber subsequent subclauses, and insert Figures 28-13 and 28-14. Renumber figures that follow.

28.2.3.4.2 Extended Next Page encodings

Extended Next Pages shall use the encoding shown in Figure 28–13 and Figure 28–14 for the NP, Ack, MP, Ack2, and T bits. The 11-bit field D10:D0 shall be encoded as a Message Code Field if the MP is a logic one and an Unformatted Code Field if the MP bit is set to logic zero.

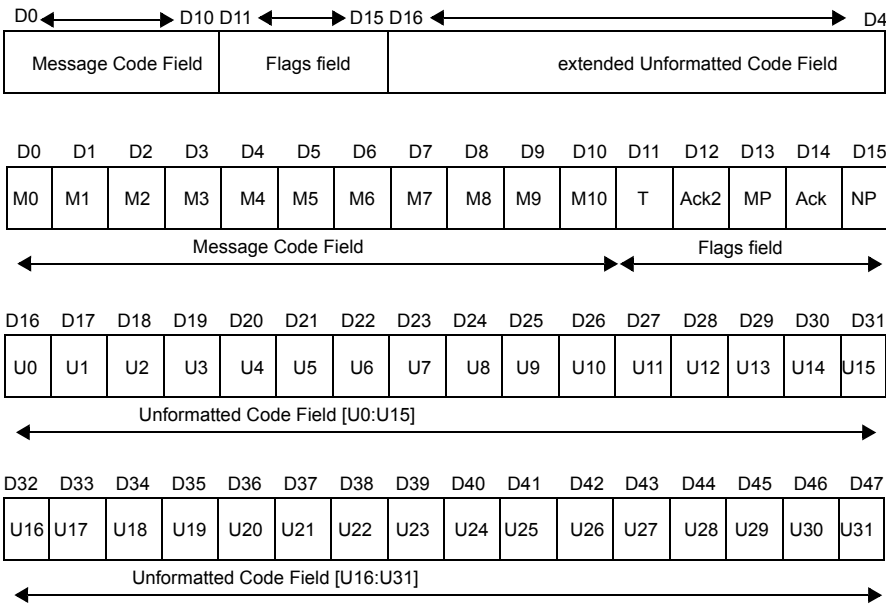


Figure 28–13—Extended Message Page encoding

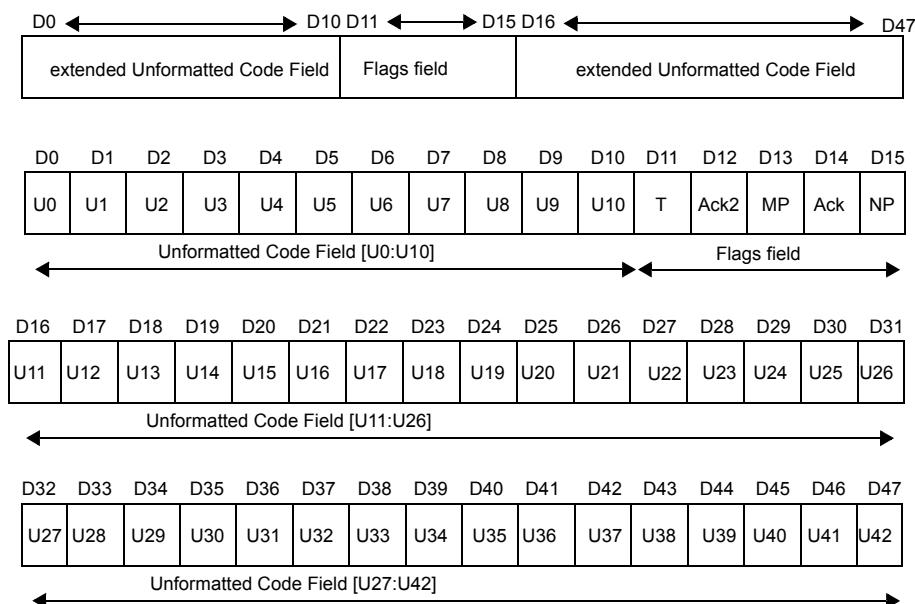


Figure 28-14—Extended Unformatted Page encoding

Insert subclause 28.2.3.4.12 after existing 28.2.3.4.10 (renumbered to 28.2.3.4.11), and renumber subsequent subclauses.

28.2.3.4.12 Extended Unformatted Code Field

The extended Unformatted Code Field is a 32-bit or 43-bit wide field, which may contain an arbitrary value. The field is 32 bits wide in an extended Message Page and 43 bits wide in an extended Unformatted Page.

28.2.3.4.13 Use of Next Pages

Change subclause 28.2.3.4.13 (renumbered from 28.2.3.4.11) as follows, adding bullets b), d), and i), and relettering other bullets appropriately.

- a) Both devices must indicate Next Page ability for either to commence exchange of Next Pages.
- b) Both devices must indicate extended Next Page ability for either to commence exchange of extended Next Pages.
- c) If both devices are Next Page able, then both devices shall send at least one Next Page.
- d) If both devices are extended Next Page able, then both devices only transmit extended Next Pages.
- e) Next Page exchange shall continue until neither device on a link has more pages to transmit as indicated by the NP bit. A Message Page with a Null Message Code Field value shall be sent if the device has no other information to transmit.
- f) A Message Code can carry either a specific message or information that defines how following Unformatted Page(s) should be interpreted.
- g) If a Message Code references Unformatted Pages, the Unformatted Pages shall immediately follow the referencing Message Code in the order specified by the Message Code.
- h) Unformatted Page users are responsible for controlling the format and sequencing for their Unformatted Pages.
- i) An extended Next Page provides a Message Code and extended Unformatted Code Field. The Message Code Field can carry either a specific message or information that defines how the following extended Unformatted Code Field should be interpreted.

28.2.4.1.3 Auto-Negotiation advertisement register (Register 4) (R/W)

Change the first paragraph of subclause 28.2.4.1.3 and Table 28-2 as follows:

This register contains the Advertised Ability of the PHY. (See Table 28–2). The bit definition for the base page is defined in 28.2.1.2. On power-up, before Auto-Negotiation starts, this register shall have the following configuration: The Selector Field (4.4:0) is set to an appropriate code as specified in Annex 28A. The Acknowledge bit (4.14) is set to logic zero. The Technology Ability Field (4.~~11+2~~:5) is set based on the values set in the MII status register (Register 1) (1.15:11) or equivalent. See also 28.2.1.2.3 and Annex 28D.

Table 28–2—Advertisement register bit definitions

Bit(s)	Name	Description	R/W ^a
4.15	Next Page	See 28.2.1.2	R/W
4.14	Reserved	Write as zero, ignore on read	RO
4.13	Remote Fault	See 28.2.1.2	R/W
<u>4.12</u>	<u>extended Next Page</u>	<u>See 28.2.1.2</u>	<u>R/W</u>
4. ~~11+2~~ :5	Technology Ability Field	See 28.2.1.2	R/W
4.4:0	Selector Field	See 28.2.1.2	R/W

^aRO = Read Only, R/W = Read/Write.

Change the third paragraph of subclause 28.2.4.1.3 as follows:

The management entity may initiate renegotiation with the Link Partner using alternate abilities by setting the Selector Field (4.4:0) and Technology Ability Field (4.~~11+2~~:5) to indicate the preferred mode of operation and setting the Restart Auto-Negotiation bit (0.9) in the control register (Register 0) to logic one.

28.2.4.1.4 Auto-Negotiation link partner ability register (Register 5) (RO)

Change Table 28-3 as follows:

Table 28–3—Link partner ability register bit definitions (Base Page)

Bit(s)	Name	Description	R/W ^a
5.15	Next Page	See 28.2.1.2	RO
5.14	Acknowledge	See 28.2.1.2	RO
5.13	Remote Fault	See 28.2.1.2	RO
<u>5.12</u>	<u>extended Next Page</u>	<u>See 28.2.1.2</u>	<u>RO</u>
5. ~~11+2~~ :5	Technology Ability Field	See 28.2.1.2	RO
5.4:0	Selector Field	See 28.2.1.2	RO

^aRO = Read Only.

28.2.4.1.8 State diagram variable to MII register mapping

Change Table 28-8 as shown

Table 28-8—State diagram variable to MII register mapping

State diagram variable	MI I register	MDIO register
mr_adv_ability[16:1]	4.15:0 Auto-Negotiation advertisement register	<u>7.16.15:0 AN advertisement register</u>
mr_autoneg_complete	1.5 Auto-Negotiation Complete	<u>7.1.5 Auto-Negotiation Complete</u>
mr_autoneg_enable	0.12 Auto-Negotiation Enable	<u>7.0.12 Auto-Negotiation Enable</u>
mr_lp_adv_ability[16:1]	For Base Page: 5.15:0 Auto-Negotiation <u>link partner</u> ~~Link Partner~~ ability register For Next Page(s): If 6.6=1 and 6.5=1 then 8.15:0 is Auto-Negotiation <u>link partner</u> ~~Link Partner~~ Received Next Page register If 6.6=1 and 6.5= 0 then 5.15:0 is Auto-Negotiation <u>link partner</u> ~~Link Partner~~ ability register If 6.6=0 then 8.15:0 or 5.15:0 is Auto-Negotiation <u>link partner</u> ~~Link Partner~~ Next Page ability register	<u>7.19.15:0 AN LP Base page ability register</u>
mr_lp_autoneg_able	6.0 Link Partner Auto-Negotiation Able	
mr_lp_np_able	6.3 Link Partner Next Page <u>able</u> ~~Able~~	
mr_main_reset	0.15 Reset	<u>7.0.15 Reset</u>
mr_next_page_loaded	Set on write to Auto-Negotiation Next Page Transmit register; cleared by Arbitration state diagram	
mr_np_able	6.2 Next Page <u>able</u> ~~Able~~	
mr_np_tx[16:1]	7.15:0 Auto-Negotiation Next Page Transmit Register	<u>7.22.15:0 AN XNP transmit register</u>
<u>mr_np_tx[32:17]</u>	<u>extended Next Pages not supported by MII register interface</u>	<u>7.23.15:0 Unformatted Code Field 1</u>
<u>mr_np_tx[48:33]</u>	<u>extended Next Pages not supported by MII register interface</u>	<u>7.24.15:0 Unformatted Code Field 2</u>
mr_page_rx	6.1 Page Received	<u>7.1.6 Page Received</u>
mr_parallel_detection_fault	6.4 Parallel Detection Fault	
mr_restart_negotiation	0.9 Auto-Negotiation Restart	<u>7.0.9 Auto-Negotiation Restart</u>
set if Auto-Negotiation is available	1.3 Auto-Negotiation Ability	<u>7.1.3 Auto-Negotiation Ability</u>

28.3 State diagrams and variable definitions

Change the first paragraph of subclause 28.3 as follows.

Replace Figure 28-13 with the figure shown below (will be renumbered to Figure 28-15).

The notation used in the state diagrams (Figures 28-14 to 28-17) (Figure 28-16 to Figure 28-19) follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set. Variables using the “mr_x” notation do not have state diagram defaults; however, their appropriate initialization conditions when mapped to the MII interface are covered in 28.2.4 and 22.2.4, and Clause 45 MDIO management interface. The variables, timers, and counters used in the state diagrams are defined in 28.3, 14.2.3, and 28.2.6.

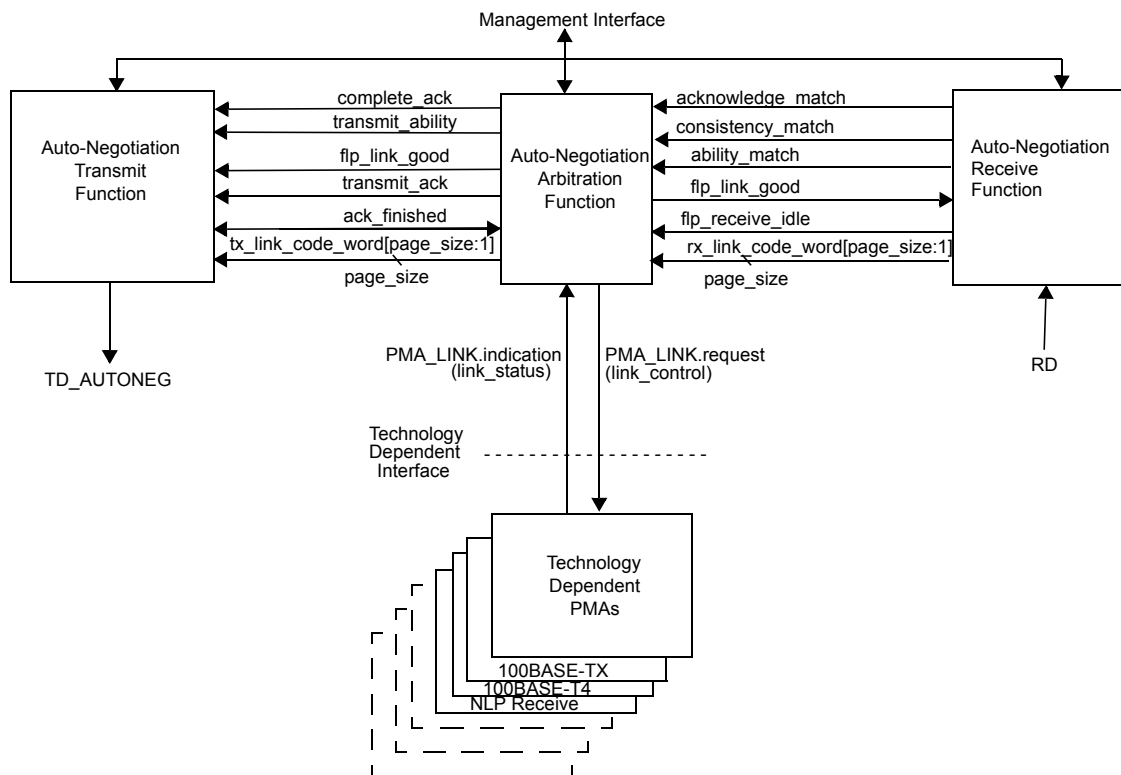


Figure 28-15—Functional reference diagram

28.3.1 State diagram variables

Insert the 10GigT after “all” and before “1GigT” in the variable list.

10GigT; represents that the 10GBASE-T PMA is the signal source.

Change mr_np_tx variable as shown.

mr_np_tx[16page_size:1]

A 16-bit or 48-bit array that contains the new Next Page to transmit.

For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

Insert the page_size variable before the power_on variable.**page_size**

Status indicating the size of Next Page that the device is prepared to transmit and receive.

Values: 16; the device does not support extended Next Pages or extended Next Page ability has not been enabled.

48; extended Next Page ability is supported and has been enabled.

NOTE— This variable is set by this variable definition; it is not set explicitly in the state diagrams. The variable takes on the value of 16 upon entry into the TRANSMIT DISABLE state and is updated upon entry into the NEXT PAGE WAIT state.

Change rx_link_code_word variable as shown.**rx_link_code_word[~~16~~page_size:1]**

A 16-bit or 48-bit array that contains the data bits to be received from an FLP Burst.

For each element within the array:

Values: zero; data bit is a logical zero.

one; data bit is a logical one.

Change the transmit_ability, transmit_ack, transmit_disable, and tx_link_code_word variables as shown.**transmit_ability**Controls the transmission of the Link Codeword containing tx_link_code_word[~~16~~page_size:1].Values: false; any transmission of tx_link_code_word[~~16~~page_size:1] is halted (default).true; the transmit state diagram begins sending tx_link_code_word[~~16~~page_size:1].**transmit_ack**Controls the setting of the Acknowledge bit in the tx_link_code_word[~~16~~page_size:1] to be transmitted.Values: false; sets the Acknowledge bit in the transmitted tx_link_code_word[~~16~~page_size:1] to a logic zero (default).true; sets the Acknowledge bit in the transmitted tx_link_code_word[~~16~~page_size:1] to a logic one.**transmit_disable**Controls the transmission of tx_link_code_word[~~16~~page_size:1].Values: false; tx_link_code_word[~~16~~page_size:1] transmission is allowed (default).true; tx_link_code_word[~~16~~page_size:1] transmission is halted.**tx_link_code_word[~~16~~page_size:1]**

A 16-bit or 48-bit array that contains the data bits to be transmitted in an FLP Burst. This array may be loaded from mr_adv_ability or mr_np_tx.

For each element within the array:

Values: Zero; data bit is logical zero.

One; data bit is logical one.

28.3.2 State diagram timers***Change first paragraph of link_fail_inhibit_timer as follows:*****link_fail_inhibit_timer**

Timer for qualifying a link_status=FAIL indication or a link_status=READY indication when a specific technology link is first being established. A link will only be considered “failed” if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The link_fail_inhibit_timer shall expire 750 ms to 1000 ms after entering the FLP LINK GOOD

CHECK state for devices operating at 10/100/1000 Mb/s. The link_fail_inhibit_timer shall expire 2000 ms to 2250 ms after entering the FLP LINK GOOD CHECK state for devices operating at 10 Gb/s.

Change nlp_test_min_timer as follows:

nlp_test_min_timer

Timer for the minimum time between two consecutive FLP Bursts. The nlp_test_min_timer shall expire ~~5 ms~~ 5 ms to 7 ms after being started or restarted; for devices that do not support extended Next Pages, and shall expire 6.75 ms to 7.25 ms after being started or restarted for devices that do support extended Next Pages.

Change transmit_link_burst_timer as follows:

transmit_link_burst_timer

Timer for the separation of a transmitted FLP Burst from the next FLP Burst. The transmit_link_burst_timer shall expire 5.7 ms to 22.3 ms after the last transmitted link pulse in an FLP Burst when extended Next Pages are not supported. When extended Next Pages are supported, the timer shall expire 5.7 ms to 6.8 ms after the last transmitted link pulse when transmitting 16-bit pages, and shall expire 1.3 ms to 3.1 ms after the last transmitted pulse when transmitting 48-bit pages.

Change Table 28-9 as shown.

Table 28–9—Timer min./max. value summary

Parameter	Min.	Typ.	Max.	Units
autoneg_wait_timer	500		1000	ms
break_link_timer	1200		1500	ms
data_detect_min_timer	15		47	μs
data_detect_max_timer	78		100	μs
flp_test_min_timer	5		25	μs
flp_test_max_timer	165		185	μs
interval_timer	55.5	62.5	69.5	μs
link_fail_inhibit_timer (10/100/1000 Mb/s devices)	750		1000	ms
<u>link_fail_inhibit_timer (10 Gb/s devices)</u>	<u>2000</u>		<u>2250</u>	<u>ms</u>
nlp_test_max_timer	50		150	ms
nlp_test_min_timer (no support of extended Next Pages)	5		7	ms
<u>nlp_test_min_timer</u> (support of extended Next Pages)	<u>6.75</u>		<u>7.25</u>	<u>ms</u>

Table 28–9—Timer min./max. value summary (continued)

Parameter	Min.	Typ.	Max.	Units
transmit_link_burst_timer (no support of extended Next Pages)	5.7	14	22.3	ms
transmit_link_burst_timer (support of extended Next Pages when page_size is 16)	<u>5.7</u>	<u>6.25</u>	<u>6.8</u>	<u>ms</u>
transmit_link_burst_timer (support of extended Next Pages when page_size is 48)	<u>1.3</u>	<u>2.25</u>	<u>3.2</u>	<u>ms</u>

28.3.3 State diagram counters

Change rx_bit_cnt and tx_bit_cnt as follows:

rx_bit_cnt

A counter that may take on integer values from 0 to ~~17~~ (page_size+1). This counter is used to keep a count of data bits received from an FLP Burst and to ensure that when erroneous extra pulses are received, the first ~~16~~ page_size bits are kept while the rest are ignored. When this variable reaches ~~16 or 17~~ page_size or (page_size+1), enough data bits have been received. This counter does not increment beyond ~~17~~ (page_size+1) and does not return to 0 until it is reinitialized.

Values: not_done; 1 to ~~15~~ (page_size–1) inclusive.
done; ~~16 or 17~~ page_size or (page_size+1)
init; counter is reset to zero.
rx_bit_cnt_check; 10 to 17 inclusive.

tx_bit_cnt

A counter that may take on integer values from 1 to ~~17~~ (page_size+1). This counter is used to keep a count of data bits sent within an FLP Burst. When this variable reaches ~~17~~ (page_size+1), all data bits have been sent.

Values: not_done; 1 to ~~16~~ page_size inclusive.
done; ~~17~~ (page_size+1).
init; counter is initialized to 1.

28.3.4 State diagrams

Replace Figure 28-16 (renumbered to Figure 28-18) with the following:

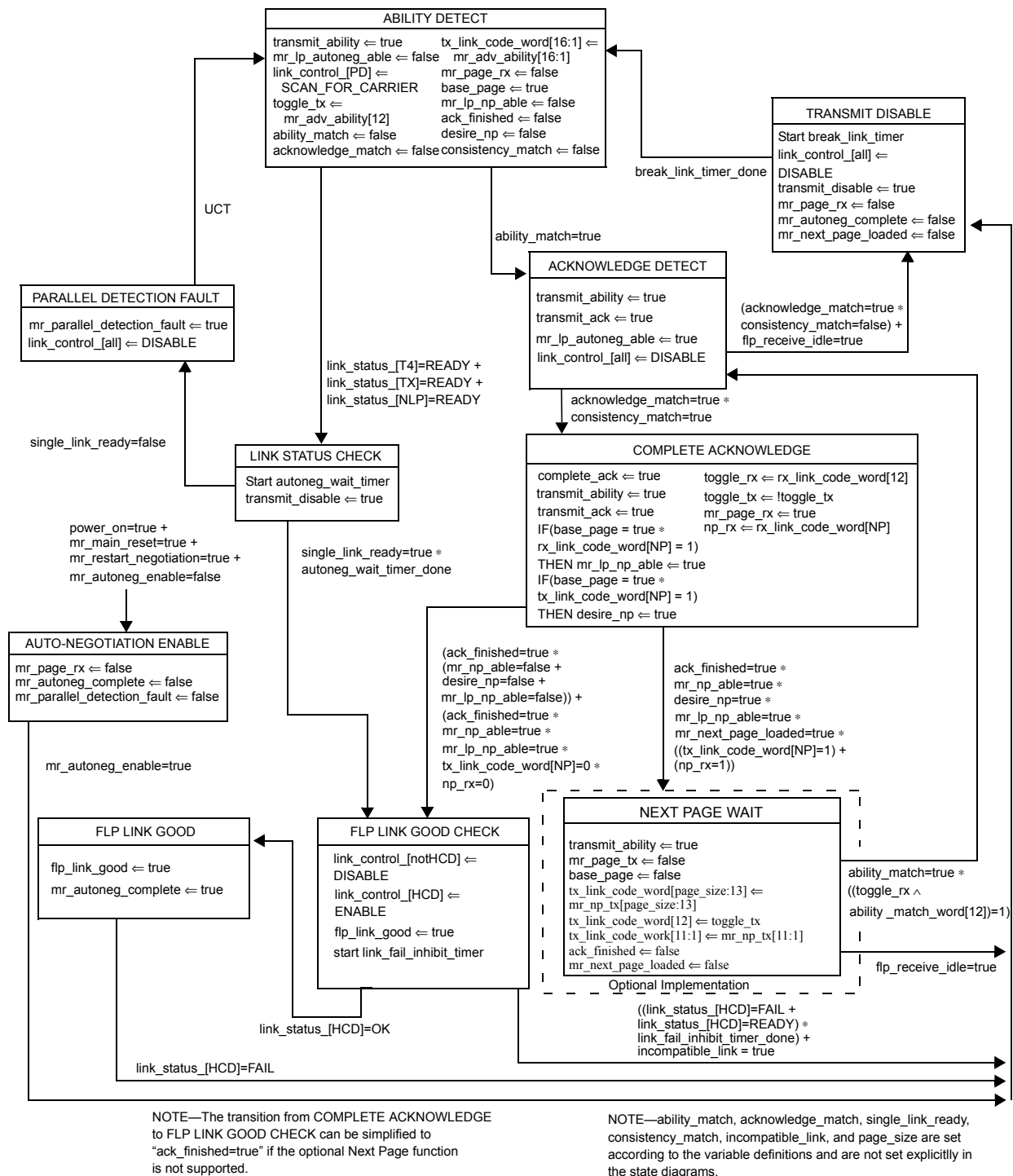


Figure 28–18—Arbitration state diagram

Change title of subclause 28.5 as shown

28.5 Protocol implementation conformance statement (PICS) proforma for Clause 28, Physical Layer link signaling for ~~10 Mb/s, 100 Mb/s, and 1000 Mb/s~~ Auto-Negotiation on twisted pair⁵

28.5.1 Introduction

Change first paragraph of subclause 28.5.1 as shown:

The supplier of a protocol implementation that is claimed to conform to Clause 28, Physical Layer link signaling for ~~10 Mb/s, 100 Mb/s, and 1000 Mb/s~~ Auto-Negotiation on twisted pair, shall complete the following protocol implementation conformance statement (PICS) proforma.

28.5.3 Major capabilities/options

*Insert rows at end of table to add *ENP, *OPT, and *10G as follows:*

Item	Feature	Subclause	Status	Support	Value/comment
*ENP	Implementation supports extended Next Pages	28.2.3.4.2	O		N/A
*OPT	Implementation supports optimized FLP burst to FLP burst timing	28.2.1.1.2	ENP:M !ENP:O		N/A
*10G	Implementation supports a 10GBASE-T PHY	55	O		N/A

Change subclause 28.5.4 heading as shown:

28.5.4 PICS proforma tables for Physical Layer link signaling for ~~10 Mb/s, 100 Mb/s, and 1000 Mb/s~~, Auto-Negotiation on twisted pair

28.5.4.2 Auto-Negotiation functions

Change item 4 as shown:

Item	Feature	Subclause	Status	Support	Value/comment
4	NLP Receive Link Integrity Test	28.2	<u>10BT</u> :M		Complies with Figure 28–19

⁵Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

28.5.4.3 Transmit function requirements

Change item 3 and insert item 8a to table as follows:

Item	Feature	Subclause	Status	Support	Value/comment
3	FLP Burst pulse definition	28.2.1.1.1	M		~~47-6~~ Odd-numbered pulse positions represent clock information; ~~46~~ even-numbered pulse positions represent data information
8a	Consecutive FLP Bursts	28.2.1.1.2	OPT:M		The first link pulse in each FLP Burst is separated by 8.25 ms $\pm$ 0.25 ms

28.5.4.5 Arbitration functions

Insert item 34 as follows:

Item	Feature	Subclause	Status	Support	Value/comment
34	extended Next Page exchange	28.2.3.4	ENP:M		If both device and link partner are ENP able, any NP exchange uses extended Next Pages.

28.5.4.8 State diagrams

Change row 11 and insert the following rows to table as follows.

Item	Feature	Subclause	Status	Support	Value/comment
11	link_fail_inhibit_timer (~~10/100/1000 Mb/s~~)	28.3.2	~~!~~ 10G:M		Expires ~~750–1000~~ 750 ms to 1000 ms after entering the FLP LINK GOOD CHECK state
11a	link_fail_inhibit_timer (10 Gb/s)	28.3.2	10G:M		Expires 2000 ms to 2250 ms after entering the FLP LINK GOOD CHECK state upon successful master/slave resolution
13a	nlp_test_min_timer (with extended Next Page)	28.3.2	ENP:M		Expires between 6.75 ms to 7.25 ms after being started if not restarted
14	transmit_link_burst_timer (with no optimized timing)	28.3.1	~~!~~ OPT:M		Expires ~~5.7–22.35~~ 5.7 ms to 22.3 ms after the last transmitted link pulse in an FLP Burst
14a	transmit_link_burst_timer (with optimized timing and 16-bit pages)	28.3.1	OPT:M		Expires 5.7 ms to 6.8 ms after the last transmitted link pulse in an FLP Burst
14b	transmit_link_burst_timer (with optimized timing and 48-bit pages)	28.3.1	OPT:M		Expires 1.3 ms to 3.2 ms after the last transmitted link pulse in an FLP Burst containing extended Next Pages

28.5.4.10 Auto-Negotiation annexes*Insert item 7a to table as follows:*

Item	Feature	Subclause	Status	Support	Value/comment
7a	Order of Unformatted Code Fields within extended Pages	Annex 28C	NP:M		Pages to be in order specified by Message Code

30. Management

30.2.5 Capabilities

Insert the following new rows into Table 30–1e below aIdleErrorCount, and insert the new column (10GBASE-T Package) in Table 30–1 to the right of PHY Error Monitor Capability in the MAU column.

Table 30–1e—Capabilities

--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

30.3.2.1.2 aPhyType

Insert 10GBASE-T after 10GBASE-W.

10GBASE-T Clause 55 10 Gb/s DSQ128

30.3.2.1.3 aPhyTypeList

Insert 10GBASE-T after 10GBASE-W.

10GBASE-T Clause 55 10 Gb/s DSQ128

30.5.1.1.2 aMAUType

Insert 10GBASE-T after 10GBASE-SW.

10GBASE-T Four-pair twisted-pair balanced copper cabling PHY as specified in Clause 55

Insert the following new management attributes for the 10GBASE-T package:

30.5.1.1.17 aSNROpMarginChnIA

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current SNR operating margin measured at the slicer input for channel A for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel A register (see 45.2.1.63).;

30.5.1.1.18 aSNROpMarginChnIB

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current SNR operating margin measured at the slicer input for channel B for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel B register (see 45.2.1.64).;

30.5.1.1.19 aSNROpMarginChnIC

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current SNR operating margin measured at the slicer input for channel C for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel C register (see 45.2.1.65).;

30.5.1.1.20 aSNROpMarginChnID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current SNR operating margin measured at the slicer input for channel D for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel D register (see 45.2.1.66).;

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert 10GBASE-T after Rem Fault2.

10GBASE-T 10GBASE-T PHY as specified in Clause 55

Change the SECTION FOUR title to include Clause 55:

SECTION FOUR: This section includes Clause 44 through Clause ~~54~~55 and Annex 44A through Annex ~~50A~~55B.

44. Introduction to 10 Gb/s baseband network

44.1 Overview

44.1.1 Scope

Change the first paragraph of 44.1.1 to include 10GBASE-T:

10 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer, connected through a 10 Gigabit Media Independent Interface (XGMII) to Physical Layer entities such as 10GBASE-SR, 10GBASE-LX4, 10GBASE-CX4, 10GBASE-LR, 10GBASE-ER, 10GBASE-SW, 10GBASE-LW, ~~and 10GBASE-EW~~, and 10GBASE-T.

44.1.2 Objectives

Insert new objective g) and shift existing objective g) to h):

- g) Support operation over selected copper media from ISO/IEC 11801:2002.

44.1.3 Relationship of 10 Gigabit Ethernet to the ISO OSI reference model

Replace Figure 44-1 to include 10GBASE-T:

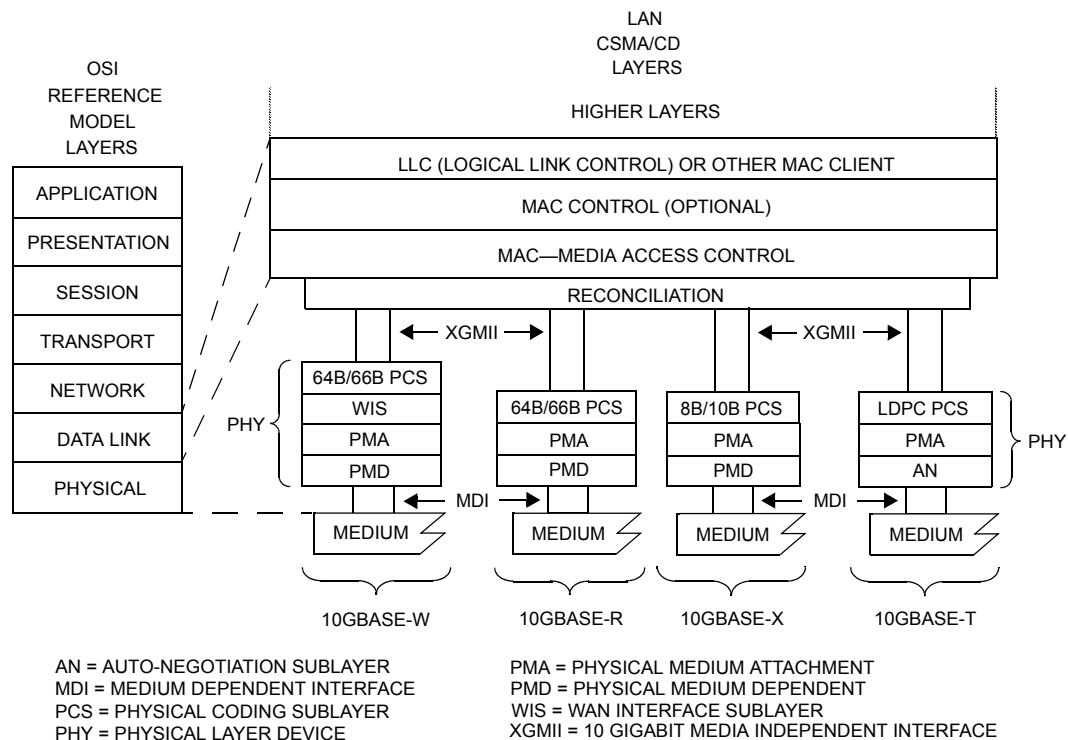


Table 44-1—Architectural positioning of 10 Gigabit Ethernet

Change bullet d) of second paragraph of 44.1.3 to include a reference to Clause 55:

- d) The MDI as specified in Clause 53 for 10GBASE-LX4, in Clause 54 for 10GBASE-CX4, in Clause 55 for 10GBASE-T and in Clause 52 for other PMD types.

44.1.4 Summary of 10 Gigabit Ethernet sublayers

44.1.4.1 Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

Change second paragraph of 44.1.4.1 to add reference to Clause 55:

While the XGMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for Clauses 47, Clause 48, ~~and Clause 49~~, and Clause 55.

44.1.4.4 Physical Layer signaling systems

Change Table 44–1 to include a new row and column for 10GBASE-T:

Table 44–1—Nomenclature and clause correlation

Nomenclature	Clause									
	48 8B/10B PCS & PMA	49 64B/66B PCS	50 WIS	51 Serial PMA	52			53 1310 nm WDM PMD	~~54~~ 54 4-Lane electrical PMD	<u>55</u> <u>Twisted-</u> <u>pair PCS</u> <u>& PMA</u>
10GBASE-SR		M ^a		M	M					
10GBASE-SW		M	M	M	M					
10GBASE-LX4	M							M		
10GBASE-CX4	M								M	
10GBASE-LR		M		M		M				
10GBASE-LW		M	M	M		M				
10GBASE-ER		M		M			M			
10GBASE-EW		M	M	M			M			
<u>10GBASE-T</u>										<u>M</u>

^aM = Mandatory

Insert text for 10GBASE-T before last paragraph of 44.1.4.4:

The term 10GBASE-T, specified in Clause 55, refers to a specific Physical Layer implementation based upon 64B/65B data coding placed in a low density parity check (LDPC) frame that is mapped to a 128 double-square (DSQ128) constellation for transmission on 4-pair, twisted-pair copper cabling.

Change last paragraph of 44.1.4.4 to read:

~~Specifications of each physical~~ Physical layer device specifications are contained in Clause 52, Clause 53, ~~through Clause 54~~, and Clause 55-inclusive.

44.3 Delay constraints

Change Table 44–2 as follows:

Table 44–2—Round-trip delay constraints (informative)

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Notes
MAC, RS and MAC Control	8192	16	See 46.1.4.
XGXS and XAUI	4096	8	Round-trip of 2 XGXS and trace for both directions. See 47.2.2.
10GBASE-X PCS and PMA	2048	4	See 48.5
10GBASE-R PCS	3584	7	See 49.2.15.
WIS	14336	28	See 50.3.7.
LX4 PMD	512	1	Includes 2 meters of fiber. See 53.2.
CX4 PMD	512	1	See 54.3.
Serial PMA and PMD	512	1	Includes 2 meters of fiber. See 52.2.
<u>10GBASE-T PHY</u>	<u>25 600</u>	<u>50</u>	<u>See 55.11.</u>

44.4 Protocol implementation conformance statement (PICS) proforma

Change first paragraph of 44.4 to include Clause 55:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 45 through Clause ~~54~~55, demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

44.5 Relation of 10 Gigabit Ethernet to other standards

Replace the first paragraph of 44.5 with the following text and tables:

Supported applications for 10 Gigabit Ethernet can be found in ISO/IEC 11801: 2002, Annex F. Suitable entries for Table F.1 of ISO/IEC 11801: 2002, Annex F, are exemplified in Table 44–4.

Table 44–4—Table F.1 of ISO/IEC 11801: 2002

Application	Specification reference	Date	Additional name
Class E (defined up to 250 MHz)^a			
CSMA/CD 10GBASE-T	IEEE Std. 802.3an-2006	2006	10 Gigabit Ethernet
Class F (defined up to 600 MHz)^a			
CSMA/CD 10GBASE-T	IEEE Std. 802.3an-2006	2006	10 Gigabit Ethernet

^aCabling must also conform to ISO/IEC TR-24750

Suitable entries for Table F.2 of ISO/IEC 11801: 2002, Annex F, are exemplified in Table 44–5.

Table 44–5—Table F.2 of ISO/IEC 11801: 2002

Application	Pins 1 & 2	Pins 3 & 4	Pins 5 & 6	Pins 7 & 8
CSMA/CD 10GBASE-T	Class E	Class E	Class E	Class E
CSMA/CD 10GBASE-T	Class F	Class F	Class F	Class F

Insert paragraph after Table 44–5 as shown:

Suitable entries for Table F.4 of ISO/IEC 11801: 2002, Annex F, are exemplified in Table 44–6.

Change title of Table 44–6 (renumbered from Table 44–4) as follows:

Table 44–6—Table ~~F4~~ E.4 of ISO/IEC 11801: 2002

Change the second paragraph of 44.5 and title of Table 44–7 (renumbered from Table 44–5) as follows:

Suitable entries for Table ~~F5~~ E.5 of ISO/IEC 11801: 2002, Annex F, are exemplified in Table 44–~~5~~ 44–7.

Table 44–7—Table ~~F5~~ E.5 of ISO/IEC 11801:2002

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

Change Table 45–1 and renumber reserved device address range as shown below.

Table 45–1—MDIO Manageable Device addresses

Device address	MMD name
0	Reserved
1	PMA/PMD
2	WIS
3	PCS
4	PHY XS
5	DTE XS
6	TC
7	<u>Auto-Negotiation</u>
8 through 28	Reserved
29	Clause 22 extension
30	Vendor specific 1
31	Vendor specific 2

Change or insert rows to Table 45–2 as appropriate:

Table 45–2— Devices in package registers bit definitions

Bit(s) ^a	Name	Description	R/W ^b
m.5.15:8	Reserved	Ignore on read	RO
<u>m.5.7</u>	<u>Auto-Negotiation present</u>	<u>1 = Auto-Negotiation present in package</u> <u>0 = Auto-Negotiation not present in package</u>	<u>RO</u>

^am = address of MMD accessed (see Table 45–1)

^bRO = Read Only

45.2.1 PMA/PMD registers

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change or insert rows to Table 45–3 as appropriate:

Table 45–3—PMA/PMD registers

Register address	Register name
1.7	~~40G~~ PMA/PMD control 2
1.9	10G <u>PMA</u> /PMD transmit disable
1.16 through 1.29	<u>Reserved</u>
1.110 through 1.32 767 ~~128~~	<u>Reserved</u>
<u>1.129</u>	<u>10GBASE-T status</u>
<u>1.130</u>	<u>10GBASE-T pair swap and polarity</u>
<u>1.131</u>	<u>10GBASE-T TX power backoff setting</u>
<u>1.132</u>	<u>10GBASE-T test mode</u>
<u>1.133</u>	<u>10GBASE-T SNR operating margin channel A</u>
<u>1.134</u>	<u>10GBASE-T SNR operating margin channel B</u>
<u>1.135</u>	<u>10GBASE-T SNR operating margin channel C</u>
<u>1.136</u>	<u>10GBASE-T SNR operating margin channel D</u>
<u>1.137</u>	<u>10GBASE-T minimum margin channel A</u>
<u>1.138</u>	<u>10GBASE-T minimum margin channel B</u>
<u>1.139</u>	<u>10GBASE-T minimum margin channel C</u>
<u>1.140</u>	<u>10GBASE-T minimum margin channel D</u>
<u>1.141</u>	<u>10GBASE-T RX signal power channel A</u>
<u>1.142</u>	<u>10GBASE-T RX signal power channel B</u>
<u>1.143</u>	<u>10GBASE-T RX signal power channel C</u>
<u>1.144</u>	<u>10GBASE-T RX signal power channel D</u>
<u>1.145 through 1.146</u>	<u>10GBASE-T skew delay</u>
<u>1.147 through 1.32 767</u>	<u>Reserved</u>
1.32 768 through 1.65 535	Vendor specific

Replace row 3 and row 7 of Table 45–4 as shown below:

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.0.13	Speed selection	$\begin{array}{ll} \begin{array}{c} 13 \\ 1 \end{array} \begin{array}{c} 6 \\ 1 \end{array} & = \text{bits 5:2 select speed} \\ 1 \ 0 & = 1000 \text{ Mb/s} \\ 0 \ 1 & = 100 \text{ Mb/s} \\ 0 \ 0 & = 10 \text{ Mb/s} \end{array} $	R/W
1.0.6	Speed selection	$\begin{array}{ll} \begin{array}{c} 13 \\ 1 \end{array} \begin{array}{c} 6 \\ 1 \end{array} & = \text{bits 5:2 select speed} \\ 1 \ 0 & = 1000 \text{ Mb/s} \\ 0 \ 1 & = 100 \text{ Mb/s} \\ 0 \ 0 & = 10 \text{ Mb/s} \end{array} $	R/W

^aR/W = Read/Write, SC = Self Clearing

Change first two paragraphs of 45.2.1.1.3 as shown:

~~Speed selection bits 1.0.13 and 1.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.~~

For devices operating at 10, 100, or 1000 Mb/s the speed of the PMA/PMD may be selected using bits 13 and 6. The speed abilities of the PMA/PMD are advertised in the PMA/PMD speed ability register. These two bits use the same definition as the speed selection bits defined in Clause 22.

For devices not operating at 10, 100, or 1000 Mb/s, the speed of the PMA/PMD may be selected using bits 5 through 2. When bits 5 through 2 are set to 0000 the use of a 10G PMA/PMD is selected. More specific selection is performed using the PMA/PMD control 2 register (Register 1.7) (see 45.2.1.6). The speed abilities of the PMA/PMD are advertised in the PMA/PMD speed ability register. A PMA/PMD may ignore writes to the PMA/PMD speed selection bits that select speeds it has not advertised in the PMA/PMD speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

NOTE—The encoding of bits 13 and 6 is stated to be the same as Clause 22 in the body text above but Table 45–4 is not aligned to the Clause 22 definition. This encoding of these bits in Table 45–4 is expected to be aligned to the Clause 22 definition in amendment IEEE P802.3ap, at date of publication.

45.2.1.4 PMA/PMD speed ability (Register 1.4)

Change or add rows to Table 45–6 as appropriate:

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W ^a
~~1.4.15:3~~	Reserved for future speeds	Value always 0, writes ignored	RO
<u>1.4.6</u>	<u>10M capable</u>	<u>1 = PMA/PMD is capable of operating at 10 Mb/s</u> <u>0 = PMA/PMD is not capable of operating as 10 Mb/s</u>	<u>RO</u>
<u>1.4.5</u>	<u>100M capable</u>	<u>1 = PMA/PMD is capable of operating at 100 Mb/s</u> <u>0 = PMA/PMD is not capable of operating at 100 Mb/s</u>	<u>RO</u>
<u>1.4.4</u>	<u>1000M capable</u>	<u>1 = PMA/PMD is capable of operating at 1000 Mb/s</u> <u>0 = PMA/PMD is not capable of operating at 1000 Mb/s</u>	<u>RO</u>
1.4.2	10PASS-TS capable	1 = PMA/PMD is capable of operating as 10PASS-TS 0 = PMA/PMD is not capable of operating as 10PASS-TS	RO
1.4.1	2BASE-TL capable	1 = PMA/PMD is capable of operating as 2BASE-TL 0 = PMA/PMD is not capable of operating as 2BASE-TL	RO
1.4.0	10G capable	1 = PMA/PMD is capable of operating at 10 Gb/s 0 = PMA/PMD is not capable of operating at 10 Gb/s	RO

^aRO = Read Only

Insert new paragraphs 45.2.1.4.1, 45.2.1.4.2, and 45.2.1.4.3 and renumber existing paragraphs.

45.2.1.4.1 10M capable (1.4.6)

When read as a one, bit 1.4.6 indicates that the PMA/PMD is able to operate at a data rate of 10 Mb/s. When read as a zero, bit 1.4.6 indicates that the PMA/PMD is not able to operate at a data rate of 10 Mb/s.

45.2.1.4.2 100M capable (1.4.5)

When read as a one, bit 1.4.5 indicates that the PMA/PMD is able to operate at a data rate of 100 Mb/s. When read as a zero, bit 1.4.5 indicates that the PMA/PMD is not able to operate at a data rate of 100 Mb/s.

45.2.1.4.3 1000M capable (1.4.4)

When read as a one, bit 1.4.4 indicates that the PMA/PMD is able to operate at a data rate of 1000 Mb/s. When read as a zero, bit 1.4.4 indicates that the PMA/PMD is not able to operate at a data rate of 1000 Mb/s.

Change subclause 45.2.1.6 text and Table 45–7 as indicated:

45.2.1.6 ~~10G~~-PMA/PMD control 2 register (Register 1.7)**Table 45–7—~~10G~~-PMA/PMD control 2 register bit definitions**

Bit(s)	Name	Description	R/W ^a
1.7.15:4 ~~3~~	Reserved	Value always 0, writes ignored	R/W
1.7.2 ~~3~~ :0	PMA/PMD type selection	3 2 1 0 1 1 1 1 = <u>10BASE-T PMA type</u> 1 1 1 0 = <u>100BASE-TX PMA/PMD type</u> 1 1 0 1 = <u>Reserved</u> 1 1 0 0 = <u>1000BASE-T PMA type</u> 1 0 1 1 = <u>Reserved</u> 1 0 1 0 = <u>Reserved</u> 1 0 0 1 = <u>10GBASE-T PMA type</u> 1 0 0 0 = <u>Reserved</u> 0 1 1 1 = 10GBASE-SR PMA/PMD type 0 1 1 0 = 10GBASE-LR PMA/PMD type 0 1 0 1 = 10GBASE-ER PMA/PMD type 0 1 0 0 = 10GBASE-LX4 PMA/PMD type 0 0 1 1 = 10GBASE-SW PMA/PMD type 0 0 1 0 = 10GBASE-LW PMA/PMD type 0 0 0 1 = 10GBASE-EW PMA/PMD type 0 0 0 0 = 10GBASE-CX4 PMA/PMD type	R/W

^aR/W = Read/Write

Change 45.2.1.6.1 text as follows:

45.2.1.6.1 PMA/PMD type selection (1.7.32:0)

The PMA/PMD type of the ~~10G~~-PMA/PMD shall be selected using bits 2 3 through 0. The PMA/PMD type abilities of the ~~10G~~-PMA/PMD are advertised in bits 9 and 7 through 0 of the ~~10G~~-PMA/PMD status 2 register and bits 8 through 0 ~~bit 0~~ of the ~~10G~~-PMA/PMD extended ability register. A ~~10G~~-PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised in the

status 2 register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

The PMA/PMD type selection defaults to a supported ability.

45.2.1.7 10G PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Change first paragraph of 45.2.1.7.4 as follows:

When read as a one, bit 1.8.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.8.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.8.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The description of the transmit fault function for serial PMDs is given in 52.4.8. The description of the transmit fault function for WWDm PMDs is given in 53.4.10. The description of the transmit fault function for the 10GBASE-CX4 PMD is given in 54.5.10. The description of the transmit fault function for the 10GBASE-T PMA is given in 55.4.2.2. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 1.8.11 is zero.

45.2.1.7.5 Receive fault (1.8.10)

Change the first paragraph of 45.2.1.7.5 as follows: and then remove the second paragraph.

When read as a one, bit 1.8.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.8.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.8.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The description of the receive fault function for serial PMDs is given in 52.4.9. The description of the receive fault function for WWDm PMDs is given in 53.4.11. The description of the receive fault function for the 10GBASE-CX4 PMD is given in 54.5.11. The description of the receive fault function for the 10GBASE-T PMA is given in 55.4.2.4. The receive fault bit shall be implemented with latching high behavior.

~~The default value of bit 1.8.10 is zero.~~

Change first paragraph of 45.2.1.8 as shown:

45.2.1.8 10G PMA/PMD transmit disable register (Register 1.9)

The assignment of bits in the 10G PMD transmit disable register is shown in Table 45–10. The transmit disable functionality is optional and a PMD's ability to perform the transmit disable functionality is advertised in the PMD transmit disable ability bit 1.8.8. A PMD that does not implement the transmit disable functionality shall ignore writes to the 10G PMD transmit disable register and may return a value of zero for all bits. A PMD device that operates using a single wavelength and has implemented the transmit disable function shall use bit 1.9.0 to control the function. Such devices shall ignore writes to bits 1.9.4:1 and return a value of zero for those bits when they are read. The transmit disable function for serial PMDs is described in 52.4.7. The transmit disable function for wide wavelength division multiplexing (WWDm) PMDs is described in 53.4.7. The transmit disable function for the 10GBASE-CX4 ~~four-lane electrical~~ PMD is described in 54.5.6. The transmit disable function for the 10GBASE-T PMA is described in 55.4.2.3.

Change 45.2.1.10 title as shown:

45.2.1.10 ~~40G~~-PMA/PMD extended ability register (Register 1.11)

Change 45.2.1.10 text and Table 45-11 as shown:

The assignment of bits in the ~~40G~~-PMA/PMD extended ability register is shown in Table 45–11. All of the bits in the ~~40G~~-PMA/PMD extended ability register are read only; a write to the ~~40G~~-PMA/PMD extended ability register shall have no effect.

Table 45–11—~~40G~~-PMA/PMD Extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.11.15:9 ~~4~~	Reserved	Ignore on read	RO
<u>1.11.8</u>	<u>10BASE-T</u>	<u>1 = PMA/PMD is able to perform 10BASE-T</u> <u>0 = PMA/PMD is not able to perform 10BASE-T</u>	<u>RO</u>
<u>1.11.7</u>	<u>100BASE-TX</u>	<u>1 = PMA/PMD is able to perform 100BASE-TX</u> <u>0 = PMA/PMD is not able to perform 100BASE-TX</u>	<u>RO</u>
<u>1.11.6</u>	<u>Reserved</u>	<u>Ignore on read</u>	<u>RO</u>
<u>1.11.5</u>	<u>1000BASE-T</u>	<u>1 = PMA/PMD is able to perform 1000BASE-T</u> <u>0 = PMA/PMD is not able to perform 1000BASE-T</u>	<u>RO</u>
<u>1.11.4</u>	<u>Reserved</u>	<u>Ignore on read</u>	<u>RO</u>
<u>1.11.3</u>	<u>Reserved</u>	<u>Ignore on read</u>	<u>RO</u>
<u>1.11.2</u>	<u>10GBASE-T ability</u>	<u>1 = PMA/PMD is able to perform 10GBASE-T</u> <u>0 = PMA/PMD is not able to perform 10GBASE-T</u>	<u>RO</u>
<u>1.11.1</u>	<u>Reserved</u>	<u>Ignore on read</u>	<u>RO</u>
1.11.0	10GBASE-CX4 ability	1 = PMA/PMD is able to perform 10GBASE-CX4 0 = PMA/PMD is not able to perform 10GBASE-CX4	RO

^aRO = Read Only

Insert subclauses 45.2.1.10.1 through 45.2.1.1.10.5.

45.2.1.10.1 10BASE-T ability (1.11.8)

When read as a one, bit 1.11.8 indicates that the PMA/PMD is able to operate as a 10BASE-T PMA/PMD type. When read as a zero, bit 1.11.8 indicates that the PMA/PMD is not able to operate as a 10BASE-T PMA/PMD type.

45.2.1.10.2 100BASE-TX ability (1.11.7)

When read as a one, bit 1.11.7 indicates that the PMA/PMD is able to operate as a 100BASE-TX PMA/PMD type. When read as a zero, bit 1.11.7 indicates that the PMA/PMD is not able to operate as a 100BASE-TX PMA/PMD type.

45.2.1.10.3 1000BASE-T ability (1.11.5)

When read as a one, bit 1.11.5 indicates that the PMA/PMD is able to operate as a 1000BASE-T PMA/PMD type. When read as a zero, bit 1.11.5 indicates that the PMA/PMD is not able to operate as a 1000BASE-T PMA/PMD type.

45.2.1.10.4 10GBASE-T ability (1.11.2)

When read as a one, bit 1.11.2 indicates that the PMA/PMD is able to operate as a 10GBASE-T PMA/PMD type. When read as a zero, bit 1.11.2 indicates that the PMA/PMD is not able to operate as a 10GBASE-T PMA/PMD type.

45.2.1.10.5 10GBASE-CX4 ability (1.11.0)

When read as a one, bit 1.11.0 indicates that the PMA/PMD is able to operate as a 10GBASE-CX4 PMA/PMD type. When read as a zero, bit 1.11.0 indicates that the PMA/PMD is not able to operate as a 10GBASE-CX4 PMA/PMD type.

Insert subclauses 45.2.1.59 through 45.2.1.75.

45.2.1.59 10GBASE-T status (Register 1.129)

The assignments of in the 10GBASE-T status register is shown in Table 45–48.

45.2.1.59.1 LP information valid (1.129.0)

When read as a one, bit 1.129.0 indicates that the startup protocol defined in 55.4.2.5 has been completed, and that the contents of bits 1.130.11:0, 1.131.15:10, 1.145.14:8, 1.146.14:8, and 1.146.6:0, which are established during the startup protocol, are valid. When read as a zero, bit 1.129.0 indicates that the startup process has not been completed, and that the contents of these bits that are established during the startup protocol are invalid. A 10GBASE-T PMA shall return a value of zero in bit 1.129.0 if PMA link_status=FAIL.

Table 45–48—10GBASE-T status register bit definitions

Bit(s)	Name	Description	R/W ^a
1.129.15:1	Reserved	Value always 0, writes ignored	RO
1.129.0	LP information valid	1 = Link partner information is valid 0 = Link partner information is invalid	RO

^aRO = Read Only

45.2.1.60 10GBASE-T pair swap and polarity register (Register 1.130)

Register 1.130 reflects the status of the pair-to-pair connectivity between the local device and the link partner (see Table 45–49). The polarity of each individual pair is also indicated.

Table 45–49—10GBASE-T pair swap and polarity register bit definitions

Bit(s)	Name	Description	R/W ^a															
1.130.15:12	Reserved	Value always 0, writes ignored	RO															
1.130.11	Pair D polarity	1 = Polarity of pair D is reversed 0 = Polarity of pair D is not reversed	RO															
1.130.10	Pair C polarity	1 = Polarity of pair C is reversed 0 = Polarity of pair C is not reversed	RO															
1.130.9	Pair B polarity	1 = Polarity of pair B is reversed 0 = Polarity of pair B is not reversed	RO															
1.130.8	Pair A polarity	1 = Polarity of pair A is reversed 0 = Polarity of pair A is not reversed	RO															
1.130.7:2	Reserved	Value always 0, writes ignored	RO															
1.130.1:0	MDI/MDI-X connection	<table><tr><td>1</td><td>0</td><td></td></tr><tr><td>1</td><td>1</td><td>= No crossover</td></tr><tr><td>1</td><td>0</td><td>= Pair A/B crossover only</td></tr><tr><td>0</td><td>1</td><td>= Pair C/D crossover only</td></tr><tr><td>0</td><td>0</td><td>= Pair A/B and pair C/D crossover</td></tr></table>	1	0		1	1	= No crossover	1	0	= Pair A/B crossover only	0	1	= Pair C/D crossover only	0	0	= Pair A/B and pair C/D crossover	RO
1	0																	
1	1	= No crossover																
1	0	= Pair A/B crossover only																
0	1	= Pair C/D crossover only																
0	0	= Pair A/B and pair C/D crossover																

^aRO = Read Only**45.2.1.60.1 Pair D polarity (1.130.11)**

When read as zero, bit 1.130.11 indicates that the polarity within pair D is not reversed. When read as one, bit 1.130.11 indicates that the polarity of pair D is reversed.

45.2.1.60.2 Pair C polarity (1.130.10)

When read as zero, bit 1.130.10 indicates that the polarity within pair C is not reversed. When read as one, bit 1.130.10 indicates that the polarity of pair C is reversed.

45.2.1.60.3 Pair B polarity (1.130.9)

When read as zero, bit 1.130.9 indicates that the polarity within pair B is not reversed. When read as one, bit 1.130.9 indicates that the polarity of pair B is reversed.

45.2.1.60.4 Pair A polarity (1.130.8)

When read as zero, bit 1.130.8 indicates that the polarity within pair A is not reversed. When read as one, bit 1.130.8 indicates that the polarity of pair A is reversed.

45.2.1.60.5 MDI/MDI-X connection (1.130.1:0)

Bits 1.130.1:0 indicate the resolution of the automatic MDI/MDI-X configuration defined in 55.4.4. This function is intended to eliminate the need for crossover cables between similar devices. The automatic configuration method used shall comply with 40.4.4.1 and 40.4.4.2.

45.2.1.61 10GBASE-T TX power backoff and PHY short reach setting (Register 1.131)

The complete assignment of bits in the 10GBASE-T TX power backoff and short reach mode settings register is shown in Table 45–50.

45.2.1.61.1 10GBASE-T TX power backoff settings (1.131.15:10)**Table 45–50—10GBASE-T TX power backoff and PHY short reach setting register bit definitions**

Bit(s)	Name	Description	R/W ^a
1.131.15:13	Link partner TX power backoff setting	$\begin{array}{ccc} \underline{15} & \underline{14} & \underline{13} \\ 1 & 1 & 1 = 14 \text{ dB} \\ 1 & 1 & 0 = 12 \text{ dB} \\ 1 & 0 & 1 = 10 \text{ dB} \\ 1 & 0 & 0 = 8 \text{ dB} \\ 0 & 1 & 1 = 6 \text{ dB} \\ 0 & 1 & 0 = 4 \text{ dB} \\ 0 & 0 & 1 = 2 \text{ dB} \\ 0 & 0 & 0 = 0 \text{ dB} \end{array}$	RO
1.131.12:10	TX power backoff setting	$\begin{array}{ccc} \underline{12} & \underline{11} & \underline{10} \\ 1 & 1 & 1 = 14 \text{ dB} \\ 1 & 1 & 0 = 12 \text{ dB} \\ 1 & 0 & 1 = 10 \text{ dB} \\ 1 & 0 & 0 = 8 \text{ dB} \\ 0 & 1 & 1 = 6 \text{ dB} \\ 0 & 1 & 0 = 4 \text{ dB} \\ 0 & 0 & 1 = 2 \text{ dB} \\ 0 & 0 & 0 = 0 \text{ dB} \end{array}$	RO
1.131.9:1	Reserved	Value always 0, writes ignored	
1.131.0	Short reach mode	1 = PHY is operating in short reach mode 0 = PHY is not operating in short reach mode	R/W

^aRO = Read Only, R/W = Read/Write

The 10GBASE-T TX power backoff settings reflects the TX power backoff selected during the startup negotiation process. The startup negotiation process and all TX power backoff settings are defined in 55.4.2.5 and 55.4.5.1. If LP information valid bit, 1.129.0, is set to one then bits 1.131.15:13 indicates the TX power backoff setting of the link partner and bits 1.131.12:10 indicates the TX power backoff setting of the local device.

45.2.1.61.2 PHY short reach mode (1.131.0)

The short reach mode of the 10GBASE-T PHY provides a means for operation on a cable plant that has parametric performance equivalent to 30 m of Class F and Class E_A cabling as defined in 55.5.4.5. If bit 1.131.0 is a one, the PHY is in short reach mode. If bit 1.131.0 is a zero the PHY is operating in normal mode. The default value for this bit is zero.

45.2.1.62 10GBASE-T test mode register (Register 1.132)

The assignment of bits in the 10GBASE-T test mode register is shown in Table 45–51. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–51—10GBASE-T test mode register bit definitions

Bit(s)	Name	Description	R/W ^a
1.132.15:13	Test mode control	<u>15</u> <u>14</u> <u>13</u> 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal operation	R/W
1.132.12:10	Transmitter test frequencies	<u>12</u> <u>11</u> <u>10</u> 1 1 1 = Reserved 1 1 0 = Dual tone 5 1 0 1 = Dual tone 4 1 0 0 = Dual tone 3 0 1 1 = Reserved 0 1 0 = Dual tone 2 0 0 1 = Dual tone 1 0 0 0 = Reserved	R/W
1.132.9:0	Reserved	Value always 0, writes ignored	RO

^aR/W = Read/Write**45.2.1.62.1 Test mode control (1.132.15:13)**

Transmitter test mode operations defined by bits 1.132.15:13, are described in 55.5.2 and Table 55–7. The default value for bits 1.132.15:13 is zero.

45.2.1.62.2 Transmitter test frequencies (1.132.12:10)

When test mode 4 is selected by setting bits 1.132.15:13 to one, zero, zero respectively, bits 1.132.12:10 select the transmit test frequency as shown in Table 45–51. Detailed use and operation of these transmitter test frequencies is described in 55.5.2.

45.2.1.63 SNR operating margin channel A register (Register 1.133)

Register 1.133 contains the current SNR operating margin measured at the slicer input for channel A for the 10GBASE-T PMA. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.64 SNR operating margin channel B register (Register 1.134)

Register 1.134 contains the current SNR operating margin measured at the slicer input for channel B for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.65 SNR operating margin channel C register (Register 1.135)

Register 1.135 contains the current SNR operating margin measured at the slicer input for channel C for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.66 SNR operating margin channel D register (Register 1.136)

Register 1.136 contains the current SNR operating margin measured at the slicer input for channel D for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.67 Minimum margin channel A register (Register 1.137)

The Minimum margin channel A register contains a latched copy of the lowest value observed in the SNR operating margin channel A register (1.133) since the last read. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.68 Minimum margin channel B register (Register 1.138)

The Minimum margin channel B register contains a latched copy of the lowest value observed in the SNR operating margin channel B register (1.134) since the last read. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.69 Minimum margin channel C register (Register 1.139)

The Minimum margin channel C register contains a latched copy of the lowest value observed in the SNR operating margin channel C register (1.135) since the last read. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.70 Minimum margin channel D register (Register 1.140)

The Minimum margin channel D register contains a latched copy of the lowest value observed in the SNR operating margin channel D register (1.136) since the last read. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.71 RX signal power channel A register (Register 1.141)

The RX signal power channel A register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.72 RX signal power channel B register (Register 1.142)

The RX signal power channel B register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within

the range of -20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by $0x8000$. Implementation of this register is optional.

45.2.1.73 RX signal power channel C register (Register 1.143)

The RX signal power channel C register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of -20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by $0x8000$. Implementation of this register is optional.

45.2.1.74 RX signal power channel D register (Register 1.144)

The RX signal power channel D register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of -20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by $0x8000$. Implementation of this register is optional.

45.2.1.75 10GBASE-T skew delay register (Registers 1.145 and 1.146)

The skew delay register reports the current skew delay on each of the pair with respect to physical pair A (see Table 45–52). It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number reported is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceed the maximum amount that can be represented by the range (-80 ns to $+78.75$ ns), the field displays the maximum respective value. The value shall be updated at least once per second.

Table 45–52—10GBASE-T skew delay register bit definitions

Bit(s)	Name	Description	R/W ^a
1.145.15	Reserved	Value always 0, writes ignored	RO
1.145.14:8	Skew delay B	Skew delay for pair B	RO
1.145.7:0	Reserved	Value always 0, writes ignored	RO
1.146.15	Reserved	Value always 0, writes ignored	RO
1.146.14:8	Skew delay D	Skew delay for pair D	RO
1.146.7	Reserved	Value always 0, writes ignored	RO
1.146.6:0	Skew delay C	Skew delay for pair C	RO

^aR/O = Read Only, R/W = Read/Write

45.2.3 PCS registers

Change Table 45–65 to Table 45–70 as shown and renumber all subsequent tables.