



**IEEE Standard for
Information technology—
Telecommunications and information
exchange between systems—
Local and metropolitan area networks—
Specific requirements**

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment 4: Ethernet Operation over Electrical Backplanes

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

IEEE
3 Park Avenue
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IEEE Std 802.3ap™-2007
(Amendment to
IEEE Std 802.3™-2005)

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IEEE Computer Society**

Approved 22 March 2007

IEEE-SA Standards Board

Abstract: This amendment to IEEE Std 802.3-2005 includes the new Clause 69 through Clause 74. Clause 69 provides an overview of Ethernet operation over electrical backplanes. Clause 70 through Clause 72 define three new PMDs developed for operation over electrical backplanes. 1000BASE-KX specifies 1 Gb/s serial operation, 10GBASE-KX4 specifies 10 Gb/s 4-lane operation, and 10GBASE-KR specifies 10 Gb/s serial operation. Clause 73 specifies an Auto-Negotiation function for use over electrical backplanes. Finally, Clause 74 specifies an optional forward error correction (FEC) sublayer for 10GBASE-R PHYs for improved link performance.

Keywords: 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, 10GBASE-R, 10 Gigabit Ethernet, 802.3ap, Auto-Negotiation, Backplane Ethernet, backplane, forward error correction (FEC), Gigabit Ethernet, physical medium dependent sublayer (PMD)

The Institute of Electrical and Electronics Engineers, Inc.
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Introduction

This introduction is not part of IEEE Std 802.3ap-2007, IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements CSMA/CD Access Method and Physical Layer Specifications, Amendment 4: Ethernet Operation over Electrical Backplanes.

IEEE Std 802.3 was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ap-2007). A historical listing of projects that have added to or modified IEEE Std 802.3 is included in IEEE Std 802.3-2005.

The media access control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new protocol capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x™ specified full duplex operation and a flow control protocol, IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet) and IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile). These major additions are all now included in IEEE Std 802.3-2005 and are not maintained as separate documents.

At the date of IEEE Std 802.3ap-2007 publication, IEEE Std 802.3 is comprised of the following documents:

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications. It also includes specification of IEEE 802.3 link aggregation.

Section Four—Includes Clause 44 through Clause 54 and Annex 44A through Annex 50A. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 74 and Annex 58A through Annex 74A. Section Five includes subscriber access Physical Layers and sublayers for operation from 512 kb/s to 1000 Mb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network.

IEEE Std 802.3-2005/Cor 1-2006

This corrigendum clarifies and corrects isolation text for twisted pair Ethernet physical interfaces, including harmonization for both powered and unpowered Medium Dependent interfaces.

IEEE Std 802.3anTM-2006

This amendment includes changes to IEEE Std 802.3-2005 and adds Clause 55 and Annex 55A and Annex 55B. This amendment adds a new Physical Layer for 10 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3aqTM-2006

This amendment includes changes to IEEE Std 802.3-2005 and adds Clause 68. This amendment adds a new Physical Layer for 10 Gb/s operation over installed multimode fiber.

IEEE Std 802.3asTM-2006

This amendment includes changes to IEEE Std 802.3-2005. It extends the size of the IEEE 802.3 frame format with an envelope frame.

IEEE Std 802.3ap-2007

This amendment includes changes to IEEE Std 802.3-2005 and adds Clause 69 through Clause 74 and Annex 69A, Annex 69B, Annex 73A and Annex 74A. This amendment adds new Physical Layers that support the exchange of IEEE Std 802.3 format frames over electrical backplanes at 1 Gb/s and 10 Gb/s.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Conformance test methodology

An additional standard, IEEE Std 1802.3TM-2001, provides conformance test information for 10BASE-T.

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Robert M. Grow, *Working Group Chair*

David J. Law, *Working Group Vice-Chair*

Wael W. Diab, *Working Group Secretary*

Steven B. Carlson, *Working Group Executive Secretary*

Bradley Booth, *Working Group Treasurer*

Adam Healey, *IEEE P802.3ap Task Force Chair*

John D'Ambrosia, *IEEE P802.3ap Task Force Secretary*

Schelto vanDoorn, *IEEE P802.3ap Task Force Editor-in-Chief—Phase 1*

Ilango S. Ganga, *IEEE P802.3ap Task Force Editor-in-Chief—Phase 2*

IEEE P802.3ap Task Force Editors

Schelto vanDoorn, *Clauses 1-44, 70,71 and Annex A, Annex 30B*

Arthur Marris, *Clause 45*

Adam Healey, *Clause 69, Annex 69A, Annex 69B*

Charles Moore, *Clause 69, Annex 69A, Annex 69B*

Tom Palkert, *Clause 72*

Pat Thaler, *Clause 73, Annex 73A*

Ilango S. Ganga, *Clause 74, Annex 74A, Clauses 1-49, 70,71, Annex A, Annex 30B*

Ali Abaye
 John Abbott
 Joe Abler
 Luc Adriaennsens
 Puneet Agarwal
 Jan Alexander
 Arne Alping
 Michael Altman
 Stephen D. Anderson
 Lewis Aronson
 Joseph N. Babanezhad
 Chet Babla
 Hugh Barrass
 Howard Baumer
 Denis Beaudoin
 Michael Beck
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 Mike Bennett
 Ernest E. Bergmann
 Sudeep Bhoja
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 Peter Bradshaw
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 Richard Brand
 Ralf-Peter Braun
 Robert D. Brink
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 Kevin Brown
 Brian Brunn
 Robert Brunner
 Robert Busse
 Jeff Cain
 Luke Chang
 Kok-Wui Cheong
 Jae hun Cho
 Rahul Chopra
 George Claseman
 Terry Cobb
 Larry Cohen
 Edward Cornejo
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Butch Anton
Jacob Ben Ary
Hugh Barrass
Howard A. Baumer
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Printed Character	Meaning	Font
*	Boolean AND	Symbol
+	Boolean OR, arithmetic addition	Symbol
^	Boolean XOR	Times New Roman
!	Boolean NOT	Symbol
×	Multiplication	Symbol
<	Less than	Symbol
≤	Less than or equal to	Symbol
>	Greater than	Symbol
≥	Greater than or equal to	Symbol
=	Equal to	Symbol
≠	Not equal to	Symbol
←	Assignment operator	Symbol
∈	Indicates membership	Symbol
∉	Indicates nonmembership	Symbol
±	Plus or minus (a tolerance)	Symbol
°	Degrees	Symbol
∑	Summation	Symbol
√	Square root	Symbol
—	Big dash (em dash)	Times New Roman
–	Little dash (en dash), subtraction	Times New Roman
	Vertical bar	Times New Roman
†	Dagger	Times New Roman
‡	Double dagger	Times New Roman
α	Lower case alpha	Symbol
β	Lower case beta	Symbol
γ	Lower case gamma	Symbol
δ	Lower case delta	Symbol
ε	Lower case epsilon	Symbol
λ	Lambda	Symbol
μ	Micro	Times New Roman
Ω	Omega	Symbol

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IEEE Standard for Information technology—
Telecommunications and information exchange between systems—
Local and metropolitan area networks—
Specific requirements

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment 4: Ethernet Operation over Electrical Backplanes

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editorial notes will not be carried over into future editions because the changes will be incorporated into the base standard.

1. Introduction

1.4 Definitions

Delete 1.4.312, which provided the definition for Selector field, and renumber as appropriate:

1.4.312 ~~Selector field:~~ A five-bit field in the Base Link Codeword encoding that is used to encode up to 32 types of messages that define basic abilities. For example, selector field 00001 indicates that the base technology is IEEE 802.3. (See IEEE 802.3, Clause 28.)

Delete 1.4.335, which provided the definition for Technology Ability Field, and renumber as appropriate (IEEE Std 802.3an-2006):

1.4.335 ~~Technology Ability Field:~~ Within IEEE 802.3, a seven-bit field in the Auto-Negotiation base page that is used to indicate the abilities of a local station, such as support for 10BASE-T, 100BASE-T4, and 100BASE-TX, as well as full duplex.

Insert the following new definitions into the definitions list, in alphanumerical order:

1.4.xxx 1000BASE-KX: IEEE 802.3 Physical Layer specification for 1 Gb/s using 1000BASE-X encoding over an electrical backplane. (See IEEE 802.3 Clause 70.)

1.4.xxx 10GBASE-KR: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-R encoding over an electrical backplane. (See IEEE 802.3 Clause 72.)

1.4.xxx 10GBASE-KX4: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-X encoding over an electrical backplane. (See IEEE 802.3 Clause 71.)

1.4.xxx Differential Manchester encoding: Data encoding system used in Backplane Ethernet for Auto-Negotiation signaling and 10GBASE-KR training frame control channel encoding. (See IEEE 802.3 72.6.10.2.2 and 73.5.)

1.5 Abbreviations

Insert the following abbreviations in alphabetical order:

BP	backplane
DME	Differential Manchester encoding

30. Management

30.2.5 Capabilities

Insert the following new rows into Table 30-1e above aSNROpMarginChnlA, and insert the new column [Forward Error Correction Package (Optional)] in Table 30-1e to the right of 10GBASE-T Operating Margin package (IEEE Std 802.3an-2006).

Table 30-1e—Capabilities

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30.3.2.1.3 aPhyTypeList

Change paragraph after “BEHAVIOUR DEFINED AS:” to read:

A read-only list of the possible types that the PHY could be, identifying the ability of the PHY. If Clause 28, ~~or~~ Clause 37, or Clause 73, Auto-Negotiation, is present, then this attribute will map to the local technology ability or advertised ability of the local device.;

30.5.1.1.2 aMAUType

Insert 1000BASE-KX after 1000BASE-CXFD.

1000BASE-KX X PCS/PMA over an electrical backplane PMD as specified in Clause 70

Insert 10GBASE-KX4 after 10GBASE-CX4.

10GBASE-KX4 X PCS/PMA over an electrical backplane PMD as specified in Clause 71

Insert 10GBASE-KR before 10GBASE-LR.

10GBASE-KR R PCS/PMA over an electrical backplane PMD as specified in Clause 72

Change last two sentences of first paragraph of aMAUType, BEHAVIOUR DEFINED AS as follows:

If Clause 28, ~~or Clause 37, or Clause 73~~ Auto-Negotiation is operational, then this will change the advertised ability to the single enumeration specified in the SET operation, and cause an immediate link renegotiation. A change in the MAU type will also be reflected in aPHYType.

30.5.1.1.13 aFECAbility

Change first paragraph after “BEHAVIOUR DEFINED AS:” to include Clause 74 as follows:

A read-only value that indicates ~~the if the 1000BASE-PX PHY supports the~~ an optional FEC Ssublayer for forward error correction (see 65.2 and Clause 74).

30.5.1.1.14 aFECmode

Change 30.5.1.1.14 to read as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A ENUMERATION that meets the requirement of the description below

unknown	initializing, true state not yet known
disabled	FEC disabled
enabled	FEC enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the ~~1000BASE-PX PHY~~ optional FEC Ssublayer for Fforward error correction (see 65.2 and Clause 74).

A GET operation returns the current mode of operation the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. When Clause 73 Auto-Negotiation is enabled a SET operation is not allowed and a GET operation maps to the variable FEC enabled in Clause 74.

If a Clause 45 MDIO interface to the PCS is present, then this attribute will map to the FEC control register (see 45.2.7.3) for 1000BASE-PX or FEC enable bit in 10GBASE-R FEC control register (see 45.2.1.85).;

30.5.1.1.15 aFECCorrectedBlocks

Change 30.5.1.1.15 to read as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 1 600 000 counts per second for 10Mb/s implementations, ~~and 500 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s implementations.~~

BEHAVIOUR DEFINED AS:

For 1000BASE-PX PHYs or 10GBASE-R PHYs, a count of corrected FEC blocks. This counter will not increment for other PHY types.

Increment the counter by one for each received block that is corrected by the FEC function in the PHY.

If a Clause 45 MDIO interface to the PCS is present, then this attribute will map to the FEC corrected blocks counter (see 45.2.7.5 and 45.2.1.86).;

30.5.1.1.16 aFECUncorrectableBlocks

Change 30.5.1.1.16 to read as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 1 600 000 counts per second for 10Mb/s implementations, ~~and 500 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s implementations.~~

BEHAVIOUR DEFINED AS:

For 1000BASE-PX PHYs or 10GBASE-R PHYs, a count of uncorrectable FEC blocks. This counter will not increment for other PHY types.

Increment the counter by one for each FEC block that is determined to be uncorrectable by the FEC function in the PHY.

If a Clause 45 MDIO interface to the PCS is present, then this attribute will map to the FEC uncorrectable blocks counter (see 45.2.7.6 and 45.2.1.87).;

30.6.1.1.3 aAutoNegRemoteSignaling

Change paragraph after “BEHAVIOUR DEFINED AS:” to include reference to DME signals (Clause 73 Auto-Negotiation) as follows:

The value indicates whether the remote end of the link is operating Auto-Negotiation signaling or not. It shall take the value detected if, during the previous link negotiation, FLP Bursts, ~~or /C/~~ ordered_sets (see 36.2.4.10) or DME signals (see 73.5) were received from the remote end.;

30.6.1.1.4 aAutoNegAutoConfig

Change paragraph after “BEHAVIOUR DEFINED AS:” to include reference to Clause 73 parallel detection as follows:

Indicates whether Auto-Negotiation signaling is in progress or has completed. The enumeration “parallel detect fail” maps to a failure in parallel detection as defined in 28.2.3.1 or 73.7.4.1.;

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Change the following entries of the “APPROPRIATE SYNTAX:” section, to include reference to Annex 28B:

FDX APAUSE	Asymmetric PAUSE operation for full duplex links as defined in Clause 37, <u>Annex 28B</u> , and Annex 31B
FDX SPAUSE	Symmetric PAUSE operation for full duplex links as defined in Clause 37, <u>Annex 28B</u> , and Annex 31B
FDX BPAUSE	Asymmetric and Symmetric PAUSE operation for full duplex links as defined in Clause 37, <u>Annex 28B</u> , and Annex 31B

Insert the following entries of the “APPROPRIATE SYNTAX:” section, after 10GBASE-T (IEEE Std 802.3an-2006):

1000BASE-KXFD	Full duplex 1000BASE-KX as specified in Clause 70
10GBASE-KX4FD	Full duplex 10GBASE-KX4 as specified in Clause 71
10GBASE-KRFD	Full duplex 10GBASE-KR as specified in Clause 72
Rem Fault	Remote fault bit (RF) as specified in Clause 73
FEC Capable	FEC ability as specified in Clause 74

30.6.1.1.6 aAutoNegAdvertisedTechnologyAbility

Change first paragraph after “BEHAVIOUR DEFINED AS” to include Clause 73 Auto-Negotiation base page as follows:

For Clause 28 Auto-Negotiation this GET-SET attribute maps to the Technology Ability field of the Auto-Negotiation Link Codeword. For Clause 37 Auto-Negotiation, this GET-SET attribute maps to bits D0-D13 of Config_Reg base page (see 37.2.1). For Clause 73 Auto-Negotiation, this GET-SET attribute maps to bits D10–D13 and D21–D47 of Link Codeword base page (see 73.6).

30.6.1.1.7 aAutoNegReceivedTechnologyAbility

Change first paragraph after “BEHAVIOUR DEFINED AS:” to include Clause 73 Auto-Negotiation base page as follows:

Indicates the advertised technology ability of the remote hardware. For Clause 28 Auto-Negotiation, this attribute maps to the Technology Ability field of the last received Auto-Negotiation Link Codeword(s). For Clause 37 Auto-Negotiation, this attribute maps to bits D0–D13 of the received Config_Reg base page (see 37.2.1). For Clause 73 Auto-Negotiation, this attribute maps to bits D10–D13 and D21–D47 of the last received Link Codeword base page (see 73.6);

30.6.1.1.8 aAutoNegLocalSelectorAbility

Change first paragraph after “BEHAVIOUR DEFINED AS:” to include Clause 73 Auto-Negotiation Selector field as follows:

This indicates the value of the selector field of the local hardware. Selector field is defined in 28.2.1.2.1 for Clause 28 Auto-Negotiation devices. The enumeration of the Selector field indicates the standard that defines the remaining encodings for Auto-Negotiation using that value of enumeration. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the value ethernet. For Clause 73 Auto-Negotiation devices, the Selector field is defined in 73.6.1.;

30.6.1.1.9 aAutoNegAdvertisedSelectorAbility

Change first paragraph after “BEHAVIOUR DEFINED AS:” as follows:

In the case of Clause 28 Auto-Negotiation, this GET-SET attribute maps to the Message Selector field of the Auto-Negotiation Link Codeword. For Clause 73 Auto-Negotiation, this attribute maps to the Selector field of the Clause 73 Auto-Negotiation Link Codeword (see 73.6.1). A SET operation to a value not available in aAutoNegLocalSelectorAbility will be rejected. A successful SET operation will result in immediate link renegotiation if aAutoNegAdminState is enabled. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the value ethernet.

30.6.1.1.10 aAutoNegReceivedSelectorAbility

Change first paragraph after “BEHAVIOUR DEFINED AS:” as follows:

In the case of Clause 28 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware. Maps to the Message Selector field of the last received Auto-Negotiation Link Codeword. For Clause 73 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware and maps to the Selector field of the last received Clause 73 Auto-Negotiation Link Codeword (see 73.6.1). For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the value ethernet.;

36. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X

36.2.5.2.7 Auto-Negotiation process

Change 36.2.5.2.7 as follows:

The Auto-Negotiation process shall provide the means to exchange configuration information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. When the PCS is used with a PMD other than 1000BASE-KX, see Clause 37 for a description of the Auto-Negotiation process and Config_Reg contents.

Upon successful completion of the Clause 37 Auto-Negotiation process, the xmit flag is set to DATA and normal link operation is enabled. The Clause 37 Auto-Negotiation process utilizes the PCS Transmit and Receive processes to convey Config_Reg contents.

When the PCS is used with a 1000BASE-KX PMD, see Clause 73 for a description of the Auto-Negotiation process. The following requirements apply to a PCS used with a 1000BASE-KX PMD. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when sync_status=FAIL and the value OK when sync_status=OK. The primitive shall be generated when the value of link_status changes. If Clause 37 Auto-Negotiation is not present, xmit shall be DATA. If Clause 37 Auto-Negotiation is present, the variable mr_an_enable should be false when 1000BASE-KX operation is negotiated through Clause 73 Auto-Negotiation.

36.7 Protocol implementation conformance statement (PICS) proforma for Clause 36, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X¹

36.7.4.3 State diagrams

Insert SD7 to SD11 to the table as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
SD7*	Support for use with a 1000BASE-KX PMD	36.2.5.2.7	AN technology dependent interface described in Clause 73	O	Yes []
SD8	AN_LINK.indication primitive	36.2.5.2.7	Support of the primitive AN_LINK.indication(link_status), when the PCS is used with 1000BASE-KX PMD	SD7:M	Yes []
SD9	link_status parameter	36.2.5.2.7	Takes the value OK or FAIL, as described in 36.2.5.2.7	SD7:M	Yes []
SD10	Generation of AN_LINK.indication primitive	36.2.5.2.7	Generated when the value of link_status changes	SD7:M	Yes []
SD11	Value of xmit, when the PCS is used with 1000BASE-KX PMD	36.2.5.2.7	The value of xmit is DATA, when Clause 37 Auto-Negotiation is not present as described in 36.2.5.2.7	SD7:M	Yes []

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45. Management Data Input/Output (MDIO) interface

45.2.1 PMA/PMD registers

Replace the “1.147 through 1.32 767” row of Table 45–3 (IEEE Std 802.3an-2006) with the following rows:

Table 45–3—PMA/PMD registers

Register address	Register name
1.147 through 1.149	Reserved
1.150	10GBASE-KR PMD control
1.151	10GBASE-KR PMD status
1.152	10GBASE-KR LP coefficient update
1.153	10GBASE-KR LP status report
1.154	10GBASE-KR LD coefficient update
1.155	10GBASE-KR LD status report
1.156 through 1.159	Reserved
1.160	1000BASE-KX control
1.161	1000BASE-KX status
1.162 through 1.169	Reserved
1.170	10GBASE-R FEC ability
1.171	10GBASE-R FEC control
1.172 through 1.173	10GBASE-R FEC corrected blocks counter
1.174 through 1.175	10GBASE-R FEC uncorrected blocks counter
1.176 through 1.32 767	Reserved

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change Table 45–4 (IEEE Std 802.3an-2006) to swap bits 13 and 6 to make consistent with Table 22–7:

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.0.13	Speed selection (<u>LSB</u>)	~~13-6~~ <u>1.0.6 1.0.13</u> 1 1 = bits 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
1.0.6	Speed selection (<u>MSB</u>)	~~13-6~~ <u>1.0.6 1.0.13</u> 1 1 = bits 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W

^aR/W = Read/Write

45.2.1.1.1 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

Delete the following note introduced in IEEE Std 802.3an-2006:

~~NOTE—The encoding of bits 13 and 6 is stated to be the same as Clause 22 in the body text above but Table 45–4 is not aligned to the Clause 22 definition. This encoding of these bits in Table 45–4 is expected to be aligned to the Clause 22 definition in amendment IEEE P802.3ap, at date of publication.~~

45.2.1.1.2 PMA loopback (1.0.0)

Change second paragraph to read as follows:

The loopback function is mandatory for the 1000BASE-KX, 10GBASE-KR, and 10GBASE-X port types and optional for all other port types, except 2BASE-TL and 10PASS-TS, which do not support loopback. A device's ability to perform the loopback function is advertised in the loopback ability bit of the related speed-dependent status register. A PMA that is unable to perform the loopback function shall ignore writes to this bit and shall return a value of zero when read. For 10 Gb/s operation, the loopback functionality is detailed in 48.3.3 and 51.8, and the loopback ability bit is specified in the 10G PMA/PMD status 2 register.

Change the reserved descriptions in Table 45–7 (IEEE Std 802.3aq-2006) as follows:

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.7.15:4	Reserved	Value always 0, writes ignored	R/W
1.7.3:0	PMA/PMD type selection	3 2 1 0 1 1 1 1 = 10BASE-T PMA/PMD type 1 1 1 0 = 100BASE-TX PMA/PMD type 1 1 0 1 = ~~Reserved~~ <u>1000BASE-KX PMA/PMD type</u> 1 1 0 0 = 1000BASE-T PMA/PMD type 1 0 1 1 = ~~Reserved~~ <u>10GBASE-KR PMA/PMD type</u> 1 0 1 0 = ~~Reserved~~ <u>10GBASE-KX4 PMA/PMD type</u> 1 0 0 1 = 10GBASE-T PMA type 1 0 0 0 = 10GBASE-LRM PMA/PMD type 0 1 1 1 = 10GBASE-SR PMA/PMD type 0 1 1 0 = 10GBASE-LR PMA/PMD type 0 1 0 1 = 10GBASE-ER PMA/PMD type 0 1 0 0 = 10GBASE-LX4 PMA/PMD type 0 0 1 1 = 10GBASE-SW PMA/PMD type 0 0 1 0 = 10GBASE-LW PMA/PMD type 0 0 0 1 = 10GBASE-EW PMA/PMD type 0 0 0 0 = 10GBASE-CX4 PMA/PMD type	R/W

^aR/W = Read/Write

45.2.1.7.4 Transmit fault (1.8.11)

Change the first paragraph of 45.2.1.7.4 (IEEE Std 802.3aq-2006) as follows:

When read as a one, bit 1.8.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.8.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.8.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The description of the transmit fault function for the 10GBASE-KR PMD is given in 72.6.8, for 10GBASE-LRM serial PMDs ~~is given~~ in 68.4.8, and for other serial PMDs in 52.4.8. The description of the transmit fault function for WWDM PMDs is given in 53.4.10. The description of the transmit fault function for the 10GBASE-CX4 PMD is given in 54.5.10. The description of the transmit fault function for the 10GBASE-T PMA is given in 55.4.2.2. The description of the transmit fault function for the 10GBASE-KX4 PMD is given in 71.6.10. The transmit fault bit shall be implemented with latching high behavior.

45.2.1.7.5 Receive fault (1.8.10)

Change the first paragraph of 45.2.1.7.5 (IEEE Std 802.3aq-2006) as follows:

When read as a one, bit 1.8.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.8.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.8.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The description of the receive fault function for the 10GBASE-KR PMD is given in 72.6.9, for 10GBASE-LRM serial PMDs ~~is given~~ in 68.4.9, and for other serial PMDs in 52.4.9. The description of the receive fault function for WWDM PMDs is given in 53.4.11. The description of the receive fault function for the 10GBASE-CX4 PMD is given in 54.5.11. The description of the receive fault function for the 10GBASE-T PMA is given in 55.4.2.4. The description of the receive fault function for the 10GBASE-KX4 PMD is given in 71.6.11. The receive fault bit shall be implemented with latching high behavior.

45.2.1.8 10G PMA/PMD transmit disable register (Register 1.9)

Change the first paragraph of 45.2.1.8 (IEEE Std 802.3aq-2006) as follows:

The assignment of bits in the 10G PMD transmit disable register is shown in Table 45–10. The transmit disable functionality is optional and a PMD's ability to perform the transmit disable functionality is advertised in the PMD transmit disable ability bit 1.8.8. A PMD that does not implement the transmit disable functionality shall ignore writes to the 10G PMD transmit disable register and may return a value of zero for all bits. A PMD device that operates using a single wavelength and has implemented the transmit disable function shall use bit 1.9.0 to control the function. Such devices shall ignore writes to bits 1.9.4:1 and return a value of zero for those bits when they are read. The transmit disable function for the 10GBASE-KR PMD is described in 72.6.5, for 10GBASE-LRM serial PMDs ~~is described~~ in 68.4.7, and for other serial PMDs in 52.4.7. The transmit disable function for wide wavelength division multiplexing (WWDM) PMDs is described in 53.4.7. The transmit disable function for the 10GBASE-CX4 PMD is described in 54.5.6. The transmit disable function for 10GBASE-KX4 is described in 71.6.6. The transmit disable function for the 10GBASE-T PMA is described in 55.4.2.3.

Change Table 45–11 (IEEE Std 802.3aq-2006) as follows:

Table 45–11—PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.11.15:9	Reserved	Ignore on read	RO
1.11.8	10BASE-T <u>ability</u>	1 = PMA/PMD is able to perform 10BASE-T 0 = PMA/PMD is not able to perform 10BASE-T	RO
1.11.7	100BASE-TX <u>ability</u>	1 = PMA/PMD is able to perform 100BASE-TX 0 = PMA/PMD is not able to perform 100BASE-TX	RO
1.11.6	<u>1000BASE-KX ability</u> ~~Reserved~~	<u>1 = PMA/PMD is able to perform 1000BASE-KX</u> <u>0 = PMA/PMD is not able to perform 1000BASE-KX</u> ~~Ignore on read~~	RO
1.11.5	1000BASE-T <u>ability</u>	1 = PMA/PMD is able to perform 1000BASE-T 0 = PMA/PMD is not able to perform 1000BASE-T	RO
1.11.4	<u>10GBASE-KR ability</u> ~~Reserved~~	<u>1 = PMA/PMD is able to perform 10GBASE-KR</u> <u>0 = PMA/PMD is not able to perform 10GBASE-KR</u> ~~Ignore on read~~	RO
1.11.3	<u>10GBASE-KX4 ability</u> ~~Reserved~~	<u>1 = PMA/PMD is able to perform 10GBASE-KX4</u> <u>0 = PMA/PMD is not able to perform 10GBASE-KX4</u> ~~Ignore on read~~	RO
1.11.2	10GBASE-T <u>ability</u>	1 = PMA/PMD is able to perform 10GBASE-T 0 = PMA/PMD is not able to perform 10GBASE-T	RO
1.11.1	10GBASE-LRM <u>ability</u>	1 = PMA/PMD is able to perform 10GBASE-LRM 0 = PMA/PMD is not able to perform 10GBASE-LRM	RO
1.11.0	10GBASE-CX4 <u>ability</u>	1 = PMA/PMD is able to perform 10GBASE-CX4 0 = PMA/PMD is not able to perform 10GBASE-CX4	RO

^aRO = Read Only

Insert subclauses at the appropriate places in 45.2.1.10 and renumber appropriately:

45.2.1.10.3 1000BASE-KX ability (1.11.6)

When read as a one, bit 1.11.6 indicates that the PMA/PMD is able to operate as 1000BASE-KX. When read as a zero, bit 1.11.6 indicates that the PMA/PMD is not able to operate as 1000BASE-KX.

45.2.1.10.5 10GBASE-KR ability (1.11.4)

When read as a one, bit 1.11.4 indicates that the PMA/PMD is able to operate as 10GBASE-KR. When read as a zero, bit 1.11.4 indicates that the PMA/PMD is not able to operate as 10GBASE-KR.

45.2.1.10.6 10GBASE-KX4 ability (1.11.3)

When read as a one, bit 1.11.3 indicates that the PMA/PMD is able to operate as 10GBASE-KX4. When read as a zero, bit 1.11.3 indicates that the PMA/PMD is not able to operate as 10GBASE-KX4.

Insert the following subclauses after 45.2.1.75 (IEEE Std 802.3an-2006) and renumber the following tables and subclauses as required:

45.2.1.76 10GBASE-KR PMD control register (Register 1.150)

Table 45–53—10GBASE-KR PMD control register

Bit(s)	Name	Description	R/W ^a
1.150.15:2	Reserved	Value always zero, writes ignored	RO
1.150.1	Training enable	1 = Enable the 10GBASE-KR start-up protocol 0 = Disable the 10GBASE-KR start-up protocol	R/W
1.150.0	Restart training	1 = Reset 10GBASE-KR start-up protocol 0 = Normal operation	R/W SC

^aR/W = Read/Write, SC = self-clearing, RO = Read Only

45.2.1.76.1 Restart training (1.150.0)

This bit maps to the state variable `mr_restart_training` as defined in 72.6.10.3.1.

45.2.1.76.2 Training enable (1.150.1)

This bit maps to the state variable `mr_training_enable` as defined in 72.6.10.3.1.

45.2.1.77 10GBASE-KR PMD status register (Register 1.151)

The assignment of bits in the 10GBASE-KR PMD status register is shown in Table 45–54.

Table 45–54—10GBASE-KR PMD status register

Bit(s)	Name	Description	R/W ^a
1.151.15:4	Reserved	Value always zero, writes ignored	RO
1.151.3	Training failure	1 = Training failure has been detected 0 = Training failure has not been detected	RO
1.151.2	Start-up protocol status	1 = Start-up protocol in progress 0 = Start-up protocol complete	RO
1.151.1	Frame lock	1 = Training frame delineation detected 0 = Training frame delineation not detected	RO
1.151.0	Receiver status	1 = Receiver trained and ready to receive data 0 = Receiver training	RO

^aRO = Read Only

45.2.1.77.1 Receiver status (1.151.0)

This bit maps to the state variable rx_trained as defined in 72.6.10.3.1.

45.2.1.77.2 Frame lock (1.151.1)

This bit maps to the state variable frame_lock as defined in 72.6.10.3.1.

45.2.1.77.3 Start-up protocol status (1.151.2)

This bit maps to the state variable training as defined in 72.6.10.3.1.

45.2.1.77.4 Training failure (1.151.3)

This bit maps to the state variable training_failure as defined in 72.6.10.3.1.

45.2.1.78 10GBASE-KR LP coefficient update register (Register 1.152)

The 10GBASE-KR LP coefficient update register reflects the contents of the first 16-bit word of the training frame most recently received from the control channel.

The assignment of bits in the 10GBASE-KR LP coefficient update register is shown in Table 45–55. Normally the bits in this register are read only; however, when training is disabled by setting low bit 1 in the 10GBASE-KR PMD control register, the 10GBASE-KR LP coefficient update register becomes writeable.

45.2.1.78.1 Preset (1.152.13)

The preset control bit requests that the coefficients be set to a state where equalization is turned off. The function and values of the preset bit is defined in 72.6.10.2.3.1.

45.2.1.78.2 Initialize (1.152.12)

The initialize control is sent to request that the coefficients be set to configure the transmit equalizer to its INITIALIZE state. The function and values of the initialize bit is defined in 72.6.10.2.3.2.

45.2.1.78.3 Coefficient (k) update (1.152.5:0)

Each coefficient, k , is assigned a 2-bit field describing a requested update. Three request encodings are defined: increment, decrement, and hold. The valid range for k is -1 to $+1$ where $k = 0$ denotes the main, or gain, tap. The function and values of the coefficient (k) update bits are defined in 72.6.10.2.3.3.

Table 45–55—10GBASE-KR LP coefficient update register bit definitions

Bit(s)	Name	Description	R/W ^a
1.152.15:14	Reserved	Value always zero, writes ignored	RO
1.152.13	Preset	1 = Preset coefficients 0 = Normal operation	R/W
1.152.12	Initialize	1 = Initialize coefficients 0 = Normal operation	R/W
1.152.11:6	Reserved	Value always zero, writes ignored	RO
1.152.5:4	Coefficient (+1) update	$\begin{array}{ll} \underline{5} & \underline{4} \\ 1 & 1 = \text{reserved} \\ 0 & 1 = \text{increment} \\ 1 & 0 = \text{decrement} \\ 0 & 0 = \text{hold} \end{array}$	R/W
1.152.3:2	Coefficient (0) update	$\begin{array}{ll} \underline{3} & \underline{2} \\ 1 & 1 = \text{reserved} \\ 0 & 1 = \text{increment} \\ 1 & 0 = \text{decrement} \\ 0 & 0 = \text{hold} \end{array}$	R/W
1.152.1:0	Coefficient (–1) update	$\begin{array}{ll} \underline{1} & \underline{0} \\ 1 & 1 = \text{reserved} \\ 0 & 1 = \text{increment} \\ 1 & 0 = \text{decrement} \\ 0 & 0 = \text{hold} \end{array}$	R/W

^aR/W = Read/Write, RO = Read Only

45.2.1.79 10GBASE-KR LP status report register (Register 1.153)

The 10GBASE-KR LP status report register reflects the contents of the second 16-bit word of the training frame most recently received from the control channel.

The assignment of bits in the 10GBASE-KR LP status report register is shown in Table 45–55.

Table 45–56—10GBASE-KR LP status report register bit definitions

Bit(s)	Name	Description	R/W ^a
1.153.15	Receiver ready	1 = The LP receiver has determined that training is complete and is prepared to receive data 0 = The LP receiver is requesting that training continue	RO
1.153.14:6	Reserved	Value always 0, writes ignored	RO
1.153.5:4	Coefficient (+1) status	$\frac{5}{1}$ $\frac{4}{1}$ = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.153.3:2	Coefficient (0) status	$\frac{3}{1}$ $\frac{2}{1}$ = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.153.1:0	Coefficient (–1) status	$\frac{1}{1}$ $\frac{0}{1}$ = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO

^aRO = Read Only

45.2.1.79.1 Receiver ready (1.153.15)

The function and values for the receiver ready bit are defined in 72.6.10.2.4.4.

45.2.1.79.2 Coefficient (*k*) status (1.153.5:0)

The function and values for the coefficient status bits are defined in 72.6.10.2.4.5.

45.2.1.80 10GBASE-KR LD coefficient update register (Register 1.154)

The 10GBASE-KR LD coefficient update register reflects the contents of the first 16-bit word of the outgoing training frame as defined by the LD receiver adaptation process in 72.6.10.2.5.

The assignment of bits in the 10GBASE-KR LD coefficient update register is shown in Table 45–56.

45.2.1.80.1 Preset (1.154.13)

The function and values of the preset bit is defined in 72.6.10.2.3.1.

45.2.1.80.2 Initialize (1.154.12)

The function and values of the initialize bit is defined in 72.6.10.2.3.2.

45.2.1.80.3 Coefficient (k) update (1.154.5:0)

The function and values of the coefficient (k) update bits are defined in 72.6.10.2.3.3.

Table 45–57—10GBASE-KR LD coefficient update register bit definitions

Bit(s)	Name	Description	R/W ^a
1.154.15:14	Reserved	Value always zero, writes ignored	RO
1.154.13	Preset	1 = Preset coefficients 0 = Normal operation	RO
1.154.12	Initialize	1 = Initialize coefficients 0 = Normal operation	RO
1.154.11:6	Reserved	Value always 0, writes ignored	RO
1.154.5:4	Coefficient (+1) update	$\begin{array}{cc} \underline{5} & \underline{4} \\ 1 & 1 = \text{reserved} \\ 0 & 1 = \text{increment} \\ 1 & 0 = \text{decrement} \\ 0 & 0 = \text{hold} \end{array}$	RO
1.154.3:2	Coefficient (0) update	$\begin{array}{cc} \underline{3} & \underline{2} \\ 1 & 1 = \text{reserved} \\ 0 & 1 = \text{increment} \\ 1 & 0 = \text{decrement} \\ 0 & 0 = \text{hold} \end{array}$	RO
1.154.1:0	Coefficient (–1) update	$\begin{array}{cc} \underline{1} & \underline{0} \\ 1 & 1 = \text{reserved} \\ 0 & 1 = \text{increment} \\ 1 & 0 = \text{decrement} \\ 0 & 0 = \text{hold} \end{array}$	RO

^aRO = Read Only

45.2.1.81 10GBASE-KR LD status report register (Register 1.155)

The 10GBASE-KR LD status report register reflects the contents of the second 16-bit word of the current outgoing training frame, as defined in the training state diagram in Figure 72–5.

The assignment of bits in the 10GBASE-KR LD status report register is shown in Table 45–58.

Table 45–58—10GBASE-KR LD status report register bit definitions

Bit(s)	Name	Description	R/W ^a
1.155.15	Receiver ready	1 = The LD receiver has determined that training is complete and is prepared to receive data 0 = The LD receiver is requesting that training continue	RO
1.155.14:6	Reserved	Value always 0, writes ignored	RO
1.155.5:4	Coefficient (+1) status	$\frac{5}{1}$ $\frac{4}{1}$ = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.155.3:2	Coefficient (0) status	$\frac{3}{1}$ $\frac{2}{1}$ = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.155.1:0	Coefficient (–1) status	$\frac{1}{1}$ $\frac{0}{1}$ = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO

^aRO = Read Only

45.2.1.81.1 Receiver ready (1.155.15)

The function and values for the receiver ready bit are defined in 72.6.10.2.4.4.

45.2.1.81.2 Coefficient (*k*) status (1.155.5:0)

The function and values for the coefficient status bits are defined in 72.6.10.2.4.5.

45.2.1.82 1000BASE-KX control register (Register 1.160)**Table 45–59—1000BASE-KX control register**

Bit(s)	Name	Description	R/W ^a
1.160.15:1	Reserved	Value always zero, writes ignored	RO
1.160.0	PMD transmit disable	1 = Disable transmitter output 0 = Enable transmitter output	R/W

^aRO = Read Only, R/W = Read/Write**45.2.1.82.1 PMD transmit disable (1.160.0)**

This bit disables the 1000BASE-KX transmitter as defined in 70.6.5.

45.2.1.83 1000BASE-KX status register (Register 1.161)**Table 45–60—1000BASE-KX status register**

Bit(s)	Name	Description	RO ^a
1.161.15:14	Reserved	Value always zero, writes ignored	RO
1.161.13	Transmit fault ability	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/ PMD does not have the ability to detect a fault condition on the transmit path	RO
1.161.12	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/ PMD does not have the ability to detect a fault condition on the receive path	RO
1.161.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	LH
1.161.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	LH
1.161.9	Reserved	Value always zero, writes ignored	RO
1.161.8	PMD transmit disable ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO
1.161.7:1	Reserved	Value always zero, writes ignored	RO
1.161.0	Signal detect signal from PMD	1 = PMD has asserted signal detect 0 = PMD has not asserted signal detect	RO

^aRO = Read Only, LH = Latching High

45.2.1.83.1 PMD transmit fault ability (1.161.13)

When read as a one, bit 1.161.13 indicates that the PMA/PMD has the ability to detect a fault condition on the transmit path. When read as a zero, bit 1.161.13 indicates that the PMA/PMD does not have the ability to detect a fault condition on the transmit path.

45.2.1.83.2 PMD receive fault ability (1.161.12)

When read as a one, bit 1.161.12 indicates that the PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.161.12 indicates that the PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.83.3 PMD transmit fault (1.161.11)

When read as a one, bit 1.161.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.161.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.161.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 1.161.11 is zero.

45.2.1.83.4 PMD receive fault (1.161.10)

When read as a one, bit 1.161.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.161.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.161.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 1.161.10 is zero.

45.2.1.83.5 PMD transmit disable ability (1.161.8)

When read as a one, bit 1.161.8 indicates that the PMD is able to perform the transmit disable function. When read as a zero, bit 1.161.8 indicates that the PMD is not able to perform the transmit disable function.

45.2.1.83.6 1000BASE-KX signal detect (1.161.0)

The PMD signal detect function is optional (see 70.6.4). The 1000BASE-X PCS requires signal detect to be one before synchronization can occur. If the signal detect function is not implemented, this bit is set to one.

45.2.1.84 10GBASE-R FEC ability register (Register 1.170)

The assignment of bits in the 10GBASE-R FEC ability register is shown in Table 45–61.

Table 45–61—10GBASE-R FEC ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.170.15:2	Reserved	Value always zero, writes ignored	RO
1.170.1	10GBASE-R FEC error indication ability	A read of 1 in this bit indicates that the 10GBASE-R PHY is able to report FEC decoding errors to the PCS layer	RO
1.170.0	10GBASE-R FEC ability	A read of 1 in this bit indicates that the 10GBASE-R PHY supports FEC	RO

^aRO Read Only

45.2.1.84.1 10GBASE-R FEC ability (1.170.0)

When read as a one, this bit indicates that the 10GBASE-R PHY supports forward error correction (FEC). When read as a zero, the 10GBASE-R PHY does not support forward error correction.

45.2.1.84.2 10GBASE-R FEC error indication ability (1.170.1)

When read as a one, this bit indicates that the 10GBASE-R FEC is able to indicate decoding errors to the PCS layer (see 74.8.3). When read as a zero, the 10GBASE-R FEC is not able to indicate decoding errors to the PCS layer. 10GBASE-R FEC error indication is controlled by the FEC enable error indication bit in the FEC control register (see 45.2.1.85.2).

45.2.1.85 10GBASE-R FEC control register (Register 1.171)

The assignment of bits in the 10GBASE-R FEC control register is shown in Table 45–62.

Table 45–62—10GBASE-R FEC control register bit definitions

Bit(s)	Name	Description	R/W ^a
1.171.15:2	Reserved	Value always zero, writes ignored	RO
1.171.1	FEC enable error indication	A write of 1 to this bit configures the FEC decoder to indicate errors to the PCS layer	R/W
1.171.0	FEC enable	A write of 1 to this bit enables 10GBASE-R FEC A write of 0 to this bit disables 10GBASE-R FEC	R/W

^aR/W = Read/Write, RO Read Only

45.2.1.85.1 FEC enable (1.171.0)

When written as a one, this bit enables FEC for the 10GBASE-R PHY. When written as a zero, FEC is disabled in the 10GBASE-R PHY. This bit shall be set to zero upon execution of PHY reset.

45.2.1.85.2 FEC enable error indication (1.171.1)

This bit enables the 10GBASE-R FEC decoder to indicate decoding errors to the upper layers (PCS) through the sync bits for the 10GBASE-R PHY in the Local Device. When written as a one, this bit enables indication of decoding errors through the sync bits to the PCS layer. When written as zero, the error indication function is disabled. Writes to this bit are ignored and reads return a zero if the 10GBASE-R FEC does not have the ability to indicate decoding errors to the PCS layer (see 45.2.1.84.2 and 74.8.3).

45.2.1.86 10GBASE-R FEC corrected blocks counter (Register 1.172, 1.173)

The assignment of bits in the 10GBASE-R FEC corrected blocks counter register is shown in Table 45–63. See 74.8.4.1 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.172 and 1.173 are used to read the value of a 32-bit counter. When registers 1.172 and 1.173 are used to read the 32-bit counter value, the register 1.172 is read first. The value of the register 1.173 is latched when (and only when) register 1.172 is read and a subsequent read of register 1.173 returns the latched value rather than the current value of the counter

Table 45–63—10GBASE-R FEC corrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W ^a
1.172.15:0	FEC corrected blocks lower	FEC_corrected_blocks_counter[15:0]	RO, NR
1.173.15:0	FEC corrected blocks upper	FEC_corrected_blocks_counter[31:16]	RO, NR

^aRO = Read Only, NR = Non Roll-over

45.2.1.87 10GBASE-R FEC uncorrected blocks counter (Register 1.174, 1.175)

The assignment of bits in the 10GBASE-R FEC uncorrected blocks counter register is shown in Table 45–64. See 74.8.4.2 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.174 and 1.175 are used to read the value of a 32-bit counter. When registers 1.174 and 1.175 are used to read the 32-bit counter value, the register 1.174 is read first. The value of the register 1.175 is latched when (and only when) register 1.174 is read and a subsequent read of register 1.175 returns the latched value rather than the current value of the counter.

Table 45–64—10GBASE-R FEC uncorrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W ^a
1.174.15:0	FEC uncorrected blocks lower	FEC_uncorrected_blocks_counter[15:0]	RO, NR
1.175.15:0	FEC uncorrected blocks upper	FEC_uncorrected_blocks_counter[31:16]	RO, NR

^aRO = Read Only, NR = Non Roll-over

45.2.7 Auto-Negotiation registers

Replace the “7.34 through 7.32 767” row in Table 45–133 (IEEE Std 802.3an-2006, Table 45–121) with the following:

Table 45–133—Auto-Negotiation MMD registers

Register Address	Register name
7.34 through 7.47	Reserved
7.48	BP Ethernet status
7.49 through 7.32 767	Reserved

45.2.7.2 AN status (Register 7.1)

Change Table 45–135 (IEEE Std 802.3an-2006, Table 45–123) as follows:

Table 45–135—AN status register

Bit(s)	Name	Description	R/W ^a
7.1.15:8	Reserved	Value always 0, writes ignored	RO
7.1.9	Parallel detection fault	1 = A fault has been detected via the parallel detection function 0 = A fault has not been detected via the parallel detection function	RO LH
7.1.8	Reserved	Value always 0, writes ignored	RO
7.1.7	Extended Next Page status	1 = Extended Next Page is used 0 = Extended Next Page is not allowed	RO
7.1.6	Page received	1 = A page has been received 0 = A page has not been received	RO LH
7.1.5	Auto-Negotiation complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
7.1.4	Remote fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO LH
7.1.3	Auto-Negotiation ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
7.1.2	Link status	1 = Link is up 0 = Link is down	RO LL
7.1.1	Reserved	Value always 0, writes ignored	RO
7.1.0	Link partner Auto-Negotiation ability	1 = LP is able to perform Auto-Negotiation 0 = LP is not able to perform Auto-Negotiation	RO

^aRO = Read Only, LH = Latching High, LL = Latching Low

Insert new subclause 45.2.7.2.1 and renumber as required:

45.2.7.2.1 Parallel detection fault (7.1.9)

The parallel detection Fault bit (7.1.9) shall be set to one to indicate that more than one of 1000BASE-KX or 10GBASE-KX4 PMAs have indicated link_status=OK when the autoneg_wait_timer expires. The parallel detection fault bit shall be reset to zero on a read of the AN status register (Register 7.1).

Change Page received subclause (IEEE Std 802.3an-2006, 45.2.7.2.2) as follows:

45.2.7.2.2 Page received (7.1.6)

The Page Received bit (7.1.6) shall be set to one to indicate that a new Link Codeword has been received and stored in the AN LP base page ability registers 7.19–7.21 or AN LP XNP ability registers 7.25–7.27. The contents of register 7.16 the AN LP base page ability registers 7.19–7.21 are valid when bit 7.1.6 is set the first time during the Auto-Negotiation. The Page received bit shall be reset to zero on a read of the AN

status register (Register 7.1) or if present, the Auto-Negotiation expansion register 6 (see 28.2.4.5). This bit is a copy of bit 6.1 in register 6, if present (see 28.2.4.1).

Replace subclause 45.2.7.6 from IEEE Std 802.3an-2006 along with its bit definition table with the following:

45.2.7.6 AN advertisement register (7.16, 7.17, 7.18)

If the BP AN ability bit (7.48.0) in the BP Ethernet status register is set to zero then only 16 bits of the AN advertisement register are used and they are defined in 28.2.1.2.

If the BP AN ability bit (7.48.0) in the BP Ethernet status register is set to one then all 48 bits are used and they are defined in 73.6.

The Selector field (7.16.4:0) is set to “IEEE Std 802.3” as specified in Annex 28A. The Acknowledge bit (7.16.14) is set to zero.

The technology ability field, as defined in 28.2.1.2 and 73.6, represents the technologies supported by the local device. Only bits representing supported technologies may be set. Management may clear bits in the technology ability field and restart Auto-Negotiation to negotiate an alternate common mode.

The management entity initiates renegotiation with the link partner using alternate abilities by setting the Restart Auto-Negotiation bit (7.0.9) in the AN control register to one.

Any writes to this register prior to completion of Auto-Negotiation, as indicated by bit 7.1.5, should be followed by a renegotiation for the new values to take effect. Once Auto-Negotiation has completed, software may examine this register along with the LP base page ability register to determine the highest common denominator technology.

If the Auto-Negotiation advertisement register (Register 4) is present (see 28.2.4.1.3), then this register is a copy of the Auto-Negotiation advertisement register (Register 4). In this case, reads to the AN advertisement register (7.16) report the value of the Auto-Negotiation advertisement register (Register 4); writes to the AN advertisement register (7.16) cause a write to occur to the Auto-Negotiation advertisement register.

The base page value is transferred to `mr_adv_ability` when register 7.16 is written. Therefore, if used, registers 7.17 and 7.18 should be written before 7.16.

Table 45–136—AN advertisement register bit definitions

Bit(s)	Name	Description	R/W ^a
7.16.15	Next Page	See 28.2.1.2 and 73.6.9	R/W
7.16.14	Acknowledge	Value always 0, writes ignored	RO
7.16.13	Remote fault	See 28.2.1.2 and 73.6.7	R/W
7.16.12:5	D12:D5	See 28.2.1.2 and 73.6	R/W
7.16.4:0	Selector field	See Annex 28A	R/W
7.17.15:0	D31:D16	See 73.6	R/W
7.18.15:0	D47:D32	See 73.6	R/W

^aR/W = Read/Write, RO = Read Only

NOTE 1—Auto-Negotiation that supports a 48-bit base page uses registers 7.16, 7.17, and 7.18 for storing base page information; Auto-Negotiation that supports a 16-bit base page only uses register 7.16 for storing base page information.

NOTE 2—Clause 37 1000BASE-X Auto-Negotiation is controlled through Clause 22 registers.

Replace subclause 45.2.7.7 from IEEE Std 802.3an-2006 along with its bit definition table with the following:

45.2.7.7 AN LP base page ability register (7.19, 7.20, 7.21)

All of the bits in the AN LP base page ability register are read only. A write to the AN LP base page ability register shall have no effect.

Register 7.19 is a copy of register 5, if present (see 28.2.4.1).

When registers 7.20 and 7.21 are used, the value of the registers 7.20 and 7.21 is latched when register 7.19 is read and reads of registers 7.20 and 7.21 return the latched value rather than the current value.

Bit 7.19.12 is reserved for Backplane Ethernet port types as they do not use Extended Next Pages.

Table 45–137—AN LP base page ability register bit definitions

Bit(s)	Name	Description	RO ^a
7.19.15:0	D15:D0	See 28.2.1.2 and 73.6	RO
7.20.15:0	D31:D16	See 73.6	RO
7.21.15:0	D47:D32	See 73.6	RO

^aRO = Read Only

NOTE—Auto-Negotiation that supports a 48-bit base page uses registers 7.19, 7.20, and 7.21 for storing LP base page information; Auto-Negotiation that supports a 16-bit base page only uses register 7.19 for storing LP base page information.

Replace subclause 45.2.7.8 from IEEE Std 802.3an-2006 with the following:

45.2.7.8 AN XNP transmit register (7.22, 7.23, 7.24)

If the BP AN ability bit (7.48.0) in the BP Ethernet status register is set to zero then Extended Next Pages are enabled by setting bit 7.0.13 to one and the AN XNP transmit register contains the Next Page link codeword to be transmitted as defined in 28.2.3.4.

If the BP AN ability bit (7.48.0) is set to one then Next Page transmission is always enabled and the register contains the AN LD Next Page Link Codeword of the BP Ethernet PHY as defined in 73.7.7.1. Even though Backplane Ethernet does not use Extended Next Pages, XNP is still used in the register name.

On power-up or AN reset, this register shall contain the default value, which represents a Message Page with the Message Code set to Null Message. This value may be replaced by any valid Extended Next Page Message Code that the device intends to transmit.

A write to register 7.23 or 7.24 does not set `mr_next_page_loaded`. Only a write to register 7.22 sets `mr_next_page_loaded` true as described in 28.2.4.1.8. Therefore, registers 7.23 and 7.24 register should be written before register 7.22.

Change rows in Table 45–138 (IEEE Std 802.3an-2006, Table 45–126) as follows:

Table 45–138—AN XNP transmit register bit definitions

Bit(s)	Name	Description	R/W ^a
7.22.15	Next Page	See 28.2.3.4 and 73.7.7.1	R/W
7.22.14	Reserved	Value always 0, writes ignored	RO
7.22.13	Message Page	See 28.2.3.4 and 73.7.7.1	R/W
7.22.12	Acknowledge 2	See 28.2.3.4 and 73.7.7.1	R/W
7.22.11	Toggle	See 28.2.3.4 and 73.7.7.1	RO
7.22.10:0	Message/Unformatted Code field	See 28.2.3.4 and 73.7.7.1	R/W
7.23.15:0	Unformatted Code field 1	See 28.2.3.4 and 73.7.7.1	R/W
7.24.15:0	Unformatted Code field 2	See 28.2.3.4 and 73.7.7.1	R/W

^aR/W = Read/Write, RO = Read Only

Change AN LP XNP ability register subclause (IEEE Std 802.3an-2006, 45.2.7.9) as follows:

45.2.7.9 AN LP XNP ability register (7.25, 7.26, 7.27)

AN LP XNP ability register (registers 7.25, 7.26, and 7.27) store link partner Extended Next Pages as shown in Table 45–140. All of the bits in the AN LP XNP ability register are read only. A write to the AN LP XNP ability register shall have no effect.

The value of registers 7.26 and 7.27 is latched when register 7.25 is read and reads of registers 7.26 and 7.27 return the latched value rather than the current value.

NOTE—If this register is used to store multiple link partner Extended Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent link partner Extended Next Pages.

Change rows in Table 45–139 (IEEE Std 802.3an-2006, Table 45–127) as follows:

Table 45–139—AN LP XNP ability register bit definitions

Bit(s)	Name	Description	RO ^a
7.25.15	Next Page	See 28.2.3.4 and 73.7.7.1	RO
7.25.14	Acknowledge	See 28.2.3.4 and 73.7.7.1	RO
7.25.13	Message Page	See 28.2.3.4 and 73.7.7.1	RO
7.25.12	Acknowledge 2	See 28.2.3.4 and 73.7.7.1	RO
7.25.11	Toggle	See 28.2.3.4 and 73.7.7.1	RO
7.25.10:0	Message/Unformatted Code field	See 28.2.3.4 and 73.7.7.1	RO
7.26.15:0	Unformatted Code field 1	See 28.2.3.4 and 73.7.7.1	RO
7.27.15:0	Unformatted Code field 2	See 28.2.3.4 and 73.7.7.1	RO

^aRO = Read Only

Insert new subclauses as follows:

45.2.7.12 Backplane Ethernet status (Register 7.48)

The assignment of bits in the Backplane Ethernet status register is shown in Table 45–154.

Table 45–154—Backplane Ethernet status register bit definitions

Bit(s)	Name	Description	RO ^a
7.48.15:4	Reserved	Ignore on read	RO
7.48.4	10GBASE-KR FEC negotiated	1 = PMA/PMD is negotiated to perform 10GBASE-KR FEC 0 = PMA/PMD is not negotiated to perform 10GBASE-KR FEC	RO
7.48.3	10GBASE-KR	1 = PMA/PMD is negotiated to perform 10GBASE-KR 0 = PMA/PMD is not negotiated to perform 10GBASE-KR	RO
7.48.2	10GBASE-KX4	1 = PMA/PMD is negotiated to perform 10GBASE-KX4 0 = PMA/PMD is not negotiated to perform 10GBASE-KX4	RO
7.48.1	1000BASE-KX	1 = PMA/PMD is negotiated to perform 1000BASE-KX 0 = PMA/PMD is not negotiated to perform 1000BASE-KX	RO
7.48.0	BP AN ability	If a 1000BASE-KX, 10GBASE-KX4 or 10GBASE-KR PHY type is implemented, this bit is set to 1	RO

^aRO = Read Only

45.2.7.12.1 10GBASE-KR FEC negotiated (7.48.4)

When the Auto-Negotiation process has completed as indicated by the AN complete bit (7.1.5), bit 7.48.4 indicates that 10GBASE-KR FEC operation has been negotiated. This bit is set only if 10GBASE-KR operation has also been negotiated.

45.2.7.12.2 Negotiated Port Type (7.48.1, 7.48.2, 7.48.3)

When the AN process has been completed as indicated by the AN complete bit, one of the three bits (1000BASE-KX, 10GBASE-KX4, 10GBASE-KR) indicates the negotiated port type. Only one of the three bits is set depending on the priority resolution function.

45.2.7.12.3 Backplane Ethernet AN ability (7.48.0)

If a 1000BASE-KX, 10GBASE-KX4, or 10GBASE-KR PHY type is implemented, this bit shall be set to 1.

When read as a one, bit 7.48.0 indicates that the PMA/PMD has the ability to perform Backplane Ethernet AN. When read as a zero, bit 7.48.0 indicates that the PMA/PMD lacks the ability to perform Backplane Ethernet AN.

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, MDIO interface²

45.5.3 PICS proforma tables for Management Data Input Output (MDIO) interface

45.5.3.2 PMA/PMD MMD options

Insert rows to the end of table as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
*KX	Implementation of 1000BASE-KX PMA/PMD			PMA:O	Yes [] No []
*KX4	Implementation of 10GBASE-KX4 PMA/PMD			PMA:O	Yes [] No []
*KR	Implementation of 10GBASE-KR PMA/PMD			PMA:O	Yes [] No []
*FEC-R	Implementation of 10GBASE-R FEC			PMA:O	Yes [] No []

²Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

45.5.3.3 PMA/PMD management functions*Insert rows to the end of the table as follows:*

Item	Feature	Subclause	Value/Comment	Status	Support
MM109	A PMA/PMD that is unable to detect a transmit fault returns a value of zero for the transmit fault bit	45.2.1.83.3		KX:M	Yes [] N/A []
MM110	The transmit fault bit is implemented with latching high behavior	45.2.1.83.3		KX:M	Yes [] N/A []
MM111	A PMA/PMD that is unable to detect a receive fault returns a value of zero for the receive fault bit	45.2.1.83.4		KX:M	Yes [] N/A []
MM112	The receive fault bit is implemented with latching high behavior	45.2.1.83.4		KX:M	Yes [] N/A []
MM113	FEC enable is set to zero upon execution of PHY reset	45.2.1.85.1		FEC-R:M	Yes [] N/A []
MM114	FEC corrected blocks counter is reset when read or upon PHY reset	45.2.1.86		FEC-R:M	Yes [] N/A []
MM115	FEC corrected blocks counter is held at all ones in the case of overflow	45.2.1.86		FEC-R:M	Yes [] N/A []
MM116	FEC uncorrected blocks counter is reset when read or upon PHY reset	45.2.1.87		FEC-R:M	Yes [] N/A []
MM117	FEC uncorrected blocks counter is held at all ones in the case of overflow	45.2.1.87		FEC-R:M	Yes [] N/A []
MM118	Backplane Ethernet AN ability bit is set to 1 for 1000BASE-KX, 10GBASE-KX4, and 10GBASE-KR PHYs	45.2.7.12.3		KX:M KX4:M KR:M	Yes [] N/A []

45.5.3.8 Auto-Negotiation options*Insert rows at the end of the table as follows:*

Item	Feature	Subclause	Value/Comment	Status	Support
*AB	Implementation of Backplane Ethernet Auto-Negotiation	45.2.7		AN:M	Yes [] No [] N/A []
*ABN	Implementation of Next Page support for Backplane Ethernet Auto-Negotiation	45.2.7		AB:M	Yes [] No [] N/A []

45.5.3.9 Auto-Negotiation management functions

Change AM22 introduced by IEEE Std 802.3an-2006 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
AM22	Writing the bit to one is ignored <u>if 7.1.3 = 0 or Auto-Negotiation is disabled</u>	45.2.7.1.4		AN:M	Yes [] N/A []

Insert rows at the end of the table as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
AM55	Parallel detection fault (7.1.9)	45.2.7.2.1	ONE to indicate more than one Backplane Ethernet PMA indicates link_status of OK when autoneg_wait_timer expires.	AB:M	Yes [] N/A []
AM56	Parallel detection fault clearing	45.2.7.2.1	ZERO on read of the AN status register.	AN:M	Yes [] N/A []
AM57	Bit 7.48.0 set to 1	45.2.7.12.3	Set to 1 if KX, KX4, or KR PHY is implemented.	AB:M	Yes [] N/A []