

IEEE Standard for Ethernet

Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

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USA

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(Amendment to
IEEE Std 802.3™-2012
as amended by
IEEE Std 802.3bk™-2013)

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IEEE Computer Society

Approved 12 June 2014

IEEE-SA Standards Board

Abstract: 100 Gb/s Physical Layer (PHY) specifications and management parameters for operation on electrical backplanes and twinaxial copper cables are added by this amendment to IEEE Std 802.3-2012. This amendment also specifies optional Energy Efficient Ethernet (EEE) for 40 Gb/s and 100 Gb/s operation over electrical backplanes and copper cables.

Keywords: 100 Gb/s Ethernet, 100GBASE-CR10, 100GBASE-CR4, 100GBASE-KP4, 100GBASE-KR4, 40 Gb/s Ethernet, 40GBASE-CR4, 40GBASE-KR4, amendment, Auto-Negotiation (AN), Backplane Ethernet, Energy Efficient Ethernet (EEE), Ethernet, Forward Error Correction (FEC), IEEE 802.3™, IEEE 802.3bj™, Physical Medium Attachment (PMA) sublayer, Physical Medium Dependent (PMD) sublayer

*Dedicated to the memory of our friend
and colleague Hugh Barrass*

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Introduction

This introduction is not part of IEEE Std 802.3bj-2014, IEEE Standard for Ethernet—Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables.

IEEE Std 802.3 was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The Media Access Control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x™ specified full duplex operation and a flow control protocol, IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile), and IEEE Std 802.3ba™ added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2012 and are not maintained as separate documents.

At the date of IEEE Std 802.3bj-2014 publication, IEEE Std 802.3 is comprised of the following documents:

IEEE Std 802.3-2012

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 90 and Annex 83A through Annex 86A. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 89 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bk-2013

Amendment 1—This amendment includes changes to EPON as defined in IEEE Std 802.3-2012 and adds the physical layer specifications and management parameters for EPON operation on point-to-multipoint passive optical networks supporting extended power budget classes of PX30 (29 dB for 1G-EPON), PX40 (33 dB for 1G-EPON), PRX40 (33 dB for 10/1G-EPON), and PR40 (33 dB for 10/10G-EPON).

IEEE Std 802.3bj-2014

Amendment 2—This amendment includes changes to IEEE Std 802.3-2012 and adds Clause 91 through Clause 94 as well as associated annexes. This amendment adds 100 Gb/s Physical Layer (PHY) specifications and management parameters for operation on electrical backplanes and twinaxial copper cables. This amendment also specifies optional Energy Efficient Ethernet (EEE) for 40 Gb/s and 100 Gb/s operation over electrical backplanes and copper cables.

A companion document IEEE Std 802.3.1™ describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables

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(This amendment is based on IEEE Std 802.3™-2012 as amended by IEEE Std 802.3bk™-2013.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.¹

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. Change is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strike through~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

¹Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.4 Definitions

Insert the following definition after 1.4.49 “10GBASE-X” (renumbered from 1.4.50 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013) as follows:

1.4.49a 100GBASE-P: An IEEE 802.3 family of Physical Layer devices using 100GBASE-R encoding and a PMD that employs pulse amplitude modulation with more than 2 levels. (See IEEE Std 802.3, Clause 80.)

Change 1.4.50 (renumbered from 1.4.51 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013) as follows:

1.4.50 100GBASE-R: ~~An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 82 for 100 Gb/s operation. (See IEEE Std 802.3, Clause 82.)~~ An IEEE 802.3 family of Physical Layer devices using 100GBASE-R encoding and a PMD that employs 2-level pulse amplitude modulation. (See IEEE Std 802.3, Clause 80.)

Insert the following definitions after 1.4.50 “100GBASE-R” (renumbered from 1.4.51 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013):

1.4.50a 100GBASE-R encoding: The physical coding sublayer encoding defined in Clause 82 for 100 Gb/s operation. (See IEEE Std 802.3, Clause 82.)

1.4.50b 100GBASE-CR4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding and Clause 91 RS-FEC over four lanes of shielded balanced copper cabling, with reach up to at least 5 m. (See IEEE Std 802.3, Clause 92.)

Insert the following definitions after 1.4.52 “100GBASE-CR10” (renumbered from 1.4.53 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013):

1.4.52a 100GBASE-KP4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding, Clause 91 RS-FEC, and 4-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 33 dB at 7 GHz. (See IEEE Std 802.3, Clause 94.)

1.4.52b 100GBASE-KR4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding, Clause 91 RS-FEC, and 2-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 35 dB at 12.9 GHz. (See IEEE Std 802.3 Clause 93.)

Change 1.4.59 (renumbered from 1.4.60 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013) as follows:

1.4.59 40GBASE-R: ~~An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 82 for 40 Gb/s operation. (See IEEE Std 802.3, Clause 82.)~~ An IEEE 802.3 family of Physical Layer devices using 40GBASE-R encoding. (See IEEE Std 802.3, Clause 80.)

Insert the following definition after 1.4.59 “40GBASE-R” (renumbered from 1.4.60 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013):

1.4.59a 40GBASE-R encoding: The physical coding sublayer encoding defined in Clause 82 for 40 Gb/s operation. (See IEEE Std 802.3, Clause 82.)

Insert the following definition after 1.4.127 “channel insertion loss” (renumbered from 1.4.128 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013):

1.4.128a Channel Operating Margin (COM): A figure of merit for a channel derived from a measurement of its scattering parameters. (See IEEE Std 802.3, Clause 93A.1.)

Insert the following definition after 1.4.166 “dedicated service:” (renumbered from 1.4.167 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013):

1.4.166a deep sleep: One of the two modes of operation for Energy-Efficient Ethernet. Deep sleep refers to the mode for which the transmitter ceases transmission during Low Power Idle to maximize the energy saving potential. (See IEEE Std 802.3, Figure 78-3).

Insert the following definition after 1.4.182 “End-of-Stream Delimiter (ESD)” (renumbered from 1.4.183 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013):

1.4.182a Energy-Efficient Ethernet (EEE): Provides a protocol for PHYs to coordinate transitions to or from a lower level of power consumption, without changing the link status and without dropping or corrupting frames. (See IEEE Std 802.3, Clause 78).

Insert the following definition after 1.4.190 “Fast Link Pulse (FLP) Burst Sequence” (renumbered from 1.4.191 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013):

1.4.190a fast wake: One of the two modes of operation for Energy-Efficient Ethernet (EEE). Fast wake refers to the mode for which the transmitter continues to transmit signals during Low Power Idle so that the receiver can resume operation with a shorter wake time. (See IEEE Std 802.3, Figure 78-3a).

Insert the following definition after 1.4.209 “frame ground” (renumbered from 1.4.210 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013):

1.4.209a frame loss ratio: The number of transmitted frames not received as valid by the MAC divided by the total number of transmitted frames.

1.5 Abbreviations

Insert the following new abbreviations into the abbreviations list in alphabetical order:

COM	Channel Operating Margin
DLL	Data Link Layer
RS-FEC	Reed-Solomon Forward Error Correction

30. Management

30.2 Managed objects

30.2.5 Capabilities

Insert two new objects into Table 30-1e before aIdleErrorCount:

Table 30-1e—Capabilities

			DTE	Repeater	MAU	
			Basic Package (mandatory)			
			Mandatory Package (mandatory)			
			Recommended Package (optional)			
			Optional Package (optional)			
			Array Package (optional)			
			Excessive Deferral Package (optional)			
			Multiple PHY Package (optional)			
			PHY Error Monitor Capability (optional)			
			Basic Control Capability (mandatory)			
			Performance Monitor Capability (optional)			
			Address Tracking Capability (optional)			
			100/1000 Mb/s Monitor Capability (optional)			
			1000 Mb/s Burst Monitor Capability (optional)			
			Basic Package (mandatory)			
			MAU Control Package (optional)			
			Media Loss Tracking Package (conditional)			
			Broadband DTE MAU Package (conditional)			
			MII Capability (conditional)			
			PHY Error Monitor Capability (optional)			
			10GBASE-T Operating Margin package (conditional)			
			Forward Error Correction Package (conditional)			
			Auto-Negotiation Package (mandatory)			
oMAU managed object class (30.5.1)						
aRSFECBIPErrCount	ATTRIBUTE	GET				X
aRSFECLaneMapping	ATTRIBUTE	GET				X

Table 30–7—LLDP capabilities (*continued*)

				LLDP IEEE Local Package (optional)
				LLDP IEEE Remote Package (optional)
aLldpXdot3LocRxFw	ATTRIBUTE	GET	X	
aLldpXdot3LocRxFwEcho	ATTRIBUTE	GET	X	
oLldpXdot3RemSystemsGroup managed object class (30.12.3)				
aLldpXdot3RemTxFw	ATTRIBUTE	GET		X
aLldpXdot3RemTxFwEcho	ATTRIBUTE	GET		X
aLldpXdot3RemRxFw	ATTRIBUTE	GET		X
aLldpXdot3RemRxFwEcho	ATTRIBUTE	GET		X

30.3 Layer management for DTEs

30.3.2.1.2 aPhyType

Change entry in APPROPRIATE SYNTAX and insert a new entry below that as follows:

APPROPRIATE SYNTAX:

...
100GBASE-R Clause 82 100 Gb/s multi-PCS lane ~~64B/66B~~ using 2-level PAM
100GBASE-P Clause 82 100 Gb/s multi-PCS lane using >2-level PAM

30.3.2.1.3 aPhyTypeList

Change entry in APPROPRIATE SYNTAX and insert a new entry below that as follows:

APPROPRIATE SYNTAX:

...
100GBASE-R Clause 82 100 Gb/s multi-PCS lane ~~64B/66B~~ using 2-level PAM
100GBASE-P Clause 82 100 Gb/s multi-PCS lane using >2-level PAM

30.5 Layer management for medium attachment units (MAUs)

30.5.1.1.2 aMAUType

Change entry in APPROPRIATE SYNTAX and insert new entries below that as follows:

APPROPRIATE SYNTAX:

...
100GBASE-R Multi-lane PCS as specified in Clause 82 over undefined 100GBASE-R or

	<u>100GBASE-P PMA/PMD</u>
<u>100GBASE-CR4</u>	<u>100GBASE-R PCS/PMA over 4 lane shielded copper balanced cable PMD as specified in Clause 92</u>
<u>100GBASE-KR4</u>	<u>100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 93</u>
<u>100GBASE-KP4</u>	<u>100GBASE-P PCS/PMA over an electrical backplane PMD as specified in Clause 94</u>

30.5.1.1.11 aBIPErrCount

Change the first paragraph in BEHAVIOUR DEFINED AS section of 30.5.1.1.11 as follows:

BEHAVIOUR DEFINED AS:

For 40/100GBASE-R PHYs and 100GBASE-P PHYs, an array of BIP error counters. The counters ~~will~~do not increment for other PHY types. The indices of this array (0 to n – 1) denote the PCS lane number where n is the number of PCS lanes in use. Each element of this array contains a count of BIP errors for that PCS lane. Increment the counter by one for each BIP error detected during alignment marker removal in the PCS for the corresponding lane.

30.5.1.1.12 aLaneMapping

Change the first paragraph in BEHAVIOUR DEFINED AS section of 30.5.1.1.12 as follows:

BEHAVIOUR DEFINED AS:

For 40/100GBASE-R PHYs and 100GBASE-P PHYs, an array of PCS lane identifiers. The indices of this array (0 to n – 1) denote the service interface lane number where n is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane that has been detected in the corresponding service interface lane.

Change 30.5.1.1.15, 30.5.1.1.16, 30.5.1.1.17, and 30.5.1.1.18 for RS-FEC as follows:

30.5.1.1.15 aFECability

ATTRIBUTE

APPROPRIATE SYNTAX:

~~A ENUMERATION~~ An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
supported	FEC supported
not supported	FEC not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional FEC sublayer for forward error correction (see 65.2 and Clause 74) or supports the Clause 91 mandatory RS-FEC.

If a Clause 45 MDIO Interface ~~to the PCS~~ is present, then this attribute ~~will~~maps to the FEC capability register (see 45.2.8.2 or 45.2.1.89);

30.5.1.1.16 aFECmode

ATTRIBUTE

APPROPRIATE SYNTAX:

~~A ENUMERATION~~ An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
disabled	FEC disabled
enabled	FEC enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the optional FEC sublayer for forward error correction (see 65.2 and Clause 74).

A GET operation returns the current mode of operation of the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. When Clause 73 Auto-Negotiation is enabled for a PHY supporting Clause 74 FEC a SET operation is not allowed and a GET operation maps to the variable ~~FEC_enabled~~ FEC_enable in Clause 74.

If a Clause 45 MDIO Interface ~~to the PCS~~ is present, then this attribute ~~will~~ maps to the FEC control register (see 45.2.8.3) for 1000BASE-PX or FEC enable bit in BASE-R FEC control register (see 45.2.1.90).;

30.5.1.1.17 aFECCorrectedBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/40/100BASE-R, ~~100BASE-P~~, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of corrected FEC block counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the ~~PCS lane~~ the FEC sublayer instance number where N is the number of ~~PCS lanes~~ FEC sublayer instances in use. The number of ~~PCS lanes~~ FEC sublayer instances in use is set to one for PHYs that do not use PCS lanes or use a single FEC instance for multiple FEC lanes. Each element of this array contains a count of corrected FEC blocks for that ~~PCS lane~~ FEC sublayer instance.

Increment the counter by one for each received block that is corrected by the FEC function in the PHY for the corresponding lane or FEC sublayer instance.

If a Clause 45 MDIO Interface ~~to the PCS~~ is present, then this attribute maps to the FEC corrected blocks counter(s) (see 45.2.7.5 and 45.2.1.91 for 10GBASE-R, 45.2.3.39 for 10GBASE-PR and 10/1GBASE-PRX, ~~and~~ 45.2.1.93 for BASE-R, and 45.2.1.92c for RS-FEC).;

30.5.1.1.18 aFECUncorrectableBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/40/100GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of uncorrectable FEC block counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the ~~PCS lane~~ the FEC sublayer instance number where N is the number of ~~PCS lanes~~ FEC sublayer instances in use. The number of ~~PCS lanes~~ FEC sublayer instances in use is set to one for PHYs that do not use PCS lanes or use a single FEC instance for multiple FEC lanes. Each element of this array contains a count of corrected FEC blocks for that ~~PCS lane~~ FEC sublayer instance.

Increment the counter by one for each FEC block that is determined to be uncorrectable by the FEC function in the PHY for the corresponding lane or FEC sublayer instance.

If a Clause 45 MDIO Interface ~~to the PCS~~ is present, then this attribute ~~will~~ maps to the FEC uncorrectable blocks counter(s) (see 45.2.7.5 and 45.2.1.92 for 10GBASE-R, 45.2.3.40 for 10GBASE-PR and 10/1GBASE-PRX, ~~and~~ 45.2.1.94 for BASE-R, and 45.2.1.92d for RS-FEC).;

Insert 30.5.1.1.26, 30.5.1.1.27, 30.5.1.1.28, 30.5.1.1.29, 30.5.1.1.30, and 30.5.1.1.31 after 30.5.1.1.25:

30.5.1.1.26 aRSFECBIPErrorCount

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresetable counters. Each counter has a maximum increment rate of 5 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 100GBASE-R and 100GBASE-P PHYs, an array of BIP error counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the PCS lane number where N is the number of PCS lanes in use. Each element of this array contains a count of BIP errors for that PCS lane.

Increment the counter by one for each BIP error detected during alignment marker removal in the PCS for the corresponding lane.

If a Clause 45 MDIO Interface is present, then this attribute maps to the BIP error counters (see 45.2.1.92h and 45.2.1.92i).;

30.5.1.1.27 aRSFECLaneMapping

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of INTEGERS.

BEHAVIOUR DEFINED AS:

For 100GBASE-R and 100GBASE-P PHYs, an array of PCS lane identifiers. The indices of this array (0 to N – 1) denote the service interface lane number where N is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane that has been detected in the corresponding service interface lane.

If a Clause 45 MDIO Interface is present, then this attribute maps to the Lane mapping registers (see 45.2.1.92j and 45.2.1.92k).;

30.5.1.1.28 aRSFECBypassAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown initializing, true state not yet known

supported	FEC bypass ability supported
not supported	FEC bypass ability not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional RS-FEC bypass ability (see 91.5.3.3).
If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC status register (see 45.2.1.92b).;

30.5.1.1.29 aRSFECIndicationAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
supported	FEC error indication bypass ability supported
not supported	FEC error indication bypass ability not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional RS-FEC error indication bypass ability (see 91.5.3.3).
If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC status register (see 45.2.1.92b).;

30.5.1.1.30 aRSFECBypassEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
disabled	FEC bypass disabled
enabled	FEC bypass enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC bypass function (see 91.5.3.3).
A GET operation returns the current mode of operation of the RS-FEC. A SET operation changes the mode of operation of the RS-FEC to the indicated value.
If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC control register (see 45.2.1.92a).;

30.5.1.1.31 aRSFECIndicationEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
disabled	FEC error indication bypass disabled
enabled	FEC error indication bypass enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC error indication bypass function (see 91.5.3.3).

A GET operation returns the current mode of operation of the RS-FEC. A SET operation changes the mode of operation of the RS-FEC to the indicated value.
If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC control register (see 45.2.1.92a).;

30.6 Management for link Auto-Negotiation

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert 100GBASE-CR4, 100GBASE-KR4, and 100GBASE-KP4 after 100GBASE-CR10 as follows:

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

global	Reserved for future use
other	See 30.2.5
unknown	Initializing, true state or type not yet known
10BASE-T	10BASE-T half duplex as defined in Clause 14
10BASE-TFD	Full duplex 10BASE-T as defined in Clause 14 and Clause 31
100BASE-T4	100BASE-T4 half duplex as defined in Clause 23
100BASE-TX	100BASE-TX half duplex as defined in Clause 25
100BASE-TXFD	Full duplex 100BASE-TX as defined in Clause 25 and Clause 31
FDX PAUSE	PAUSE operation for full duplex links as defined in Annex 31B
FDX APAUSE	Asymmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
FDX SPAUSE	Symmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
FDX BPAUSE	Asymmetric and Symmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
100BASE-T2	100BASE-T2 half duplex as defined in Clause 32
100BASE-T2FD	Full duplex 100BASE-T2 as defined in Clause 31 and Clause 32
1000BASE-X	1000BASE-X half duplex as specified in Clause 36
1000BASE-XFD	Full duplex 1000BASE-X as specified in Clause 31 and Clause 36
1000BASE-T	1000BASE-T half duplex PHY as specified in Clause 40
1000BASE-TFD	Full duplex 1000BASE-T PHY as specified in Clause 31 and as specified in Clause 40
Rem Fault1	Remote fault bit 1 (RF1) as specified in Clause 37
Rem Fault2	Remote fault bit 2 (RF2) as specified in Clause 37
10GBASE-T	10GBASE-T PHY as specified in Clause 55
1000BASE-KXFD	Full duplex 1000BASE-KX as specified in Clause 70
10GBASE-KX4FD	Full duplex 10GBASE-KX4 as specified in Clause 71
10GBASE-KRFD	Full duplex 10GBASE-KR as specified in Clause 72
40GBASE-KR4	40GBASE-KR4 as specified in Clause 84
40GBASE-CR4	40GBASE-CR4 as specified in Clause 85
100GBASE-CR10	100GBASE-CR10 as specified in Clause 85
<u>100GBASE-CR4</u>	<u>100GBASE-CR4 as specified in Clause 92</u>
<u>100GBASE-KR4</u>	<u>100GBASE-KR4 as specified in Clause 93</u>
<u>100GBASE-KP4</u>	<u>100GBASE-KP4 as specified in Clause 94</u>
Rem Fault	Remote fault bit (RF) as specified in Clause 73
FEC Capable	FEC ability as specified in Clause 73 (see 73.7) and Clause 74
FEC Requested	FEC requested as specified in Clause 73 (see 73.7) and Clause 74
isoethernet	IEEE Std 802.9 ISLAN-16T

30.12 Layer Management for Link Layer Discovery Protocol (LLDP)

30.12.2 LLDP Local System Group managed object class

30.12.2.1 LLDP Local System Group attributes

Insert new subclauses 30.12.2.1.30 through 30.12.2.1.33 after 30.12.2.1.29:

30.12.2.1.30 aLldpXdot3LocTxFw

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the local system can support in the transmit direction. This attribute maps to the variable LocTxSystemFW as defined in 78.4.2.3;

30.12.2.1.31 aLldpXdot3LocTxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the remote system is advertising that it can support in the transmit direction and is echoed by the local system under the control of the IEEE DLL receiver state diagram. This attribute maps to the variable LocTxSystemFWEcho as defined in 78.4.2.3;

30.12.2.1.32 aLldpXdot3LocRxFw

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the local system is requesting in the receive direction. This attribute maps to the variable LocRxSystemFW as defined in 78.4.2.3;

30.12.2.1.33 aLldpXdot3LocRxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the remote system is advertising that it is requesting in the receive direction and is echoed by the local system under the control of the IEEE DLL transmitter state diagram. This attribute maps to the variable LocRxSystemFWEcho as defined in 78.4.2.3;

30.12.3 LLDP Remote System Group managed object class

30.12.3.1 LLDP Remote System Group attributes

Insert new subclauses 30.12.3.1.24 through 30.12.3.1.27 after 30.12.3.1.23:

30.12.3.1.24 aLldpXdot3RemTxFw

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the remote system can support in the transmit direction. This attribute maps to the variable RemTxSystemFW as defined in 78.4.2.3;

30.12.3.1.25 aLldpXdot3RemTxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the local system is advertising that it can support in the transmit direction as echoed by the remote system under the control of the IEEE DLL receiver state diagram. This attribute maps to the variable RemTxSystemFWEcho as defined in 78.4.2.3;

30.12.3.1.26 aLldpXdot3RemRxFw

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the remote system is requesting in the receive direction. This attribute maps to the variable RemRxSystemFW as defined in 78.4.2.3;

30.12.3.1.27 aLldpXdot3RemRxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the local system is advertising that it is requesting in the receive direction as echoed by the remote system under the control of the IEEE DLL transmitter state diagram. This attribute maps to the variable RemRxSystemFWEcho as defined in 78.4.2.3;

45. Management Data Input/Output (MDIO) Interface

45.2.1 PMA/PMD registers

Change the identified Reserved row in Table 45-3 as follows:

Table 45-3—PMA/PMD registers

Register address	Register name	Subclause
~~1.16 through 1.29~~	~~Reserved~~	
<u>1.16</u>	<u>EEE capability register</u>	<u>45.2.1.13a</u>
<u>1.17 through 1.29</u>	<u>Reserved</u>	

Change Table 45-3 from register addresses 1.162 through 1.1499 as follows:

Table 45-3—PMA/PMD registers

Register address	Register name	Subclause
~~1.162 through 1.169~~	~~Reserved~~	
<u>1.162 through 1.164</u>	<u>PMA overhead control 1, 2, and 3 registers</u>	<u>45.2.1.88a</u>
<u>1.165, 1.166</u>	<u>PMA overhead status 1 and 2 registers</u>	<u>45.2.1.88b</u>
<u>1.167 through 1.169</u>	<u>Reserved</u>	
<u>1.170</u>	<u>BASE-R FEC ability</u>	<u>45.2.1.89</u>
<u>1.171</u>	<u>BASE-R FEC control</u>	<u>45.2.1.90</u>
<u>1.172 through 1.173</u>	<u>10GBASE-R FEC corrected blocks counter</u>	<u>45.2.1.91</u>
<u>1.174 through 1.175</u>	<u>10GBASE-R FEC uncorrected blocks counter</u>	<u>45.2.1.92</u>
~~1.176 through 1.209~~	~~Reserved~~	
<u>1.176 through 1.199</u>	<u>Reserved</u>	
<u>1.200</u>	<u>RS-FEC control register</u>	<u>45.2.1.92a</u>
<u>1.201</u>	<u>RS-FEC status register</u>	<u>45.2.1.92b</u>
<u>1.202, 1.203</u>	<u>RS-FEC corrected codewords counter</u>	<u>45.2.1.92c</u>
<u>1.204, 1.205</u>	<u>RS-FEC uncorrected codewords counter</u>	<u>45.2.1.92d</u>
<u>1.206</u>	<u>RS-FEC lane mapping register</u>	<u>45.2.1.92e</u>
<u>1.207 through 1.209</u>	<u>Reserved</u>	
<u>1.210 through 1.217</u>	<u>RS-FEC symbol error counter, lane 0 to 3</u>	<u>45.2.1.92f</u> , <u>45.2.1.92g</u>
<u>1.218 through 1.229</u>	<u>Reserved</u>	
<u>1.230 through 1.249</u>	<u>RS-FEC BIP error counter, lane 0 to 19</u>	<u>45.2.1.92h</u> , <u>45.2.1.92i</u>
<u>1.250 through 1.269</u>	<u>RS-FEC PCS lane mapping, lane 0 to 19</u>	<u>45.2.1.92j</u> , <u>45.2.1.92k</u>
<u>1.270 through 1.279</u>	<u>Reserved</u>	
<u>1.280 through 1.283</u>	<u>RS-FEC PCS alignment status 1 through 4</u>	<u>45.2.1.92l</u>

Table 45–3—PMA/PMD registers (continued)

Register address	Register name	Subclause
<u>1.284 through 1.299</u>	<u>Reserved</u>	
1.300 through 1.339	BASE-R FEC corrected blocks counter, lanes 0 through 19	45.2.1.93
1.340 through 1.699	Reserved	
1.700 through 1.739	BASE-R FEC uncorrected blocks counter, lanes 0 through 19	45.2.1.94
1.740 through 1.1099	Reserved	
1.1100	BASE-R LP coefficient update, lane 0 (copy)	45.2.1.81
1.1101 through 1.1109	BASE-R LP coefficient update, lanes 1 through 9	45.2.1.95
1.1110 through 1.1199	Reserved	
1.1200	BASE-R LP status report, lane 0 (copy)	45.2.1.82
1.1201 through 1.1209	BASE-R LP status report, lanes 1 through 9	45.2.1.96
1.1210 through 1.1299	Reserved	
1.1300	BASE-R LD coefficient update, lane 0 (copy)	45.2.1.83
1.1301 through 1.1309	BASE-R LD coefficient update, lanes 1 through 9	45.2.1.97
1.1310 through 1.1399	Reserved	
1.1400	BASE-R LD status report, lane 0 (copy)	45.2.1.84
1.1401 through 1.1409	BASE-R LD status report, lanes 1 through 9	45.2.1.98
<u>1.1410 through 1.1499</u>	<u>Reserved</u>	
<u>1.1410 through 1.1449</u>	<u>Reserved</u>	
<u>1.1450 through 1.1453</u>	<u>PMD training pattern, lanes 0 to 3</u>	<u>45.2.1.98a</u>
<u>1.1454 through 1.1499</u>	<u>Reserved</u>	

45.2.1.2 PMA/PMD status 1 register (Register 1.1)

Change the first row of Table 45-5 and insert the following rows below that row:

Table 45–5—PMA/PMD status 1 register bit definitions

Bit(s)	Name	Description	R/W ^a
<u>1.1.15:810</u>	Reserved	<u>Ignore on read. Value always 0, writes ignored</u>	RO
<u>1.1.9</u>	<u>PIASA</u>	<u>PMA ingress AUI stop ability</u>	<u>RO</u>
<u>1.1.8</u>	<u>PEASA</u>	<u>PMA egress AUI stop ability</u>	<u>RO</u>

^aRO = Read only, LL = Latching low

Insert the following subclauses after 45.2.1.2 (before 45.2.1.2.1):

45.2.1.2.a PMA ingress AUI stop ability (1.1.9)

If bit 1.1.9 is set to one, then the PMA is indicating that the PMA sublayer attached by the ingress AUI is permitted to stop signaling during LPI. If the bit is set to zero, then the PMA is indicating that the PMA sublayer attached by the ingress AUI is not permitted to stop signaling during LPI. If the PMA sublayer attached by the ingress AUI does not support EEE capability or is not capable to stop signaling, then this bit has no effect.

45.2.1.2.b PMA egress AUI stop ability (1.1.8)

If bit 1.1.8 is set to one, then the PMA is indicating that the PMA sublayer attached by the egress AUI is permitted to stop signaling during LPI. If the bit is set to zero, then the PMA is indicating that the PMA sublayer attached by the egress AUI is not permitted to stop signaling during LPI. If the PMA sublayer attached by the egress AUI does not support EEE capability or is not capable to stop signaling, then this bit has no effect.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change Table 45-7 as follows:

Table 45-7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.7.15:6	Reserved	Value always 0, writes ignored	R/W
1.7.9	PIASE	PMA ingress AUI stop enable	R/W
1.7.8	PEASE	PMA egress AUI stop enable	R/W
1.7.7:6	Reserved	Value always 0, writes ignored	R/W

Table 45–7—PMA/PMD control 2 register bit definitions (*continued*)

Bit(s)	Name	Description	R/W ^a
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 x x x x = reserved for future use ~~1 0 1 1 x x = reserved for future use~~ ~~1 0 1 1 1 1 = reserved for future use~~ <u>1 0 1 1 1 0 = 100GBASE-CR4 PMA/PMD</u> <u>1 0 1 1 0 1 = 100GBASE-KR4 PMA/PMD</u> <u>1 0 1 1 0 0 = 100GBASE-KP4 PMA/PMD</u> 1 0 1 0 1 1 = 100GBASE-ER4 PMA/PMD 1 0 1 0 1 0 = 100GBASE-LR4 PMA/PMD 1 0 1 0 0 1 = 100GBASE-SR10 PMA/PMD 1 0 1 0 0 0 = 100GBASE-CR10 PMA/PMD 1 0 0 1 1 x = reserved for future use 1 0 0 1 0 1 = reserved for future use 1 0 0 1 0 0 = 40GBASE-FR PMA/PMD 1 0 0 0 1 1 = 40GBASE-LR4 PMA/PMD 1 0 0 0 1 0 = 40GBASE-SR4 PMA/PMD 1 0 0 0 0 1 = 40GBASE-CR4 PMA/PMD 1 0 0 0 0 0 = 40GBASE-KR4 PMA/PMD 0 1 1 1 1 1 = 10/1GBASE-PRX-U4 0 1 1 1 1 0 = 10GBASE-PR-U4 0 1 1 1 0 1 = 10/1GBASE-PRX-D4 0 1 1 1 0 0 = 10GBASE-PR-D4 0 1 1 0 1 1 = reserved 0 1 1 0 1 0 = 10GBASE-PR-U3 0 1 1 0 0 1 = 10GBASE-PR-U1 0 1 1 0 0 0 = 10/1GBASE-PRX-U3 0 1 0 1 1 1 = 10/1GBASE-PRX-U2 0 1 0 1 1 0 = 10/1GBASE-PRX-U1 0 1 0 1 0 1 = 10GBASE-PR-D3 0 1 0 1 0 0 = 10GBASE-PR-D2 0 1 0 0 1 1 = 10GBASE-PR-D1 0 1 0 0 1 0 = 10/1GBASE-PRX-D3 0 1 0 0 0 1 = 10/1GBASE-PRX-D2 0 1 0 0 0 0 = 10/1GBASE-PRX-D1 0 0 1 1 1 1 = 10BASE-T PMA/PMD 0 0 1 1 1 0 = 100BASE-TX PMA/PMD 0 0 1 1 0 1 = 1000BASE-KX PMA/PMD 0 0 1 1 0 0 = 1000BASE-T PMA/PMD 0 0 1 0 1 1 = 10GBASE-KR PMA/PMD 0 0 1 0 1 0 = 10GBASE-KX4 PMA/PMD 0 0 1 0 0 1 = 10GBASE-T PMA 0 0 1 0 0 0 = 10GBASE-LRM PMA/PMD 0 0 0 1 1 1 = 10GBASE-SR PMA/PMD 0 0 0 1 1 0 = 10GBASE-LR PMA/PMD 0 0 0 1 0 1 = 10GBASE-ER PMA/PMD 0 0 0 1 0 0 = 10GBASE-LX4 PMA/PMD 0 0 0 0 1 1 = 10GBASE-SW PMA/PMD 0 0 0 0 1 0 = 10GBASE-LW PMA/PMD 0 0 0 0 0 1 = 10GBASE-EW PMA/PMD 0 0 0 0 0 0 = 10GBASE-CX4 PMA/PMD	R/W

^aR/W = Read/Write

Insert the following new subclauses after 45.2.1.6 (before 45.2.1.6.1):

45.2.1.6.a PMA ingress AUI stop enable (1.7.9)

If bit 1.7.9 is set to 1 then the PMA may stop the ingress direction AUI signaling during LPI otherwise it shall keep active signaling on that AUI. If the PMA does not support EEE capability or is not able to stop the ingress direction AUI signaling (see 45.2.1.2.a) then this bit has no effect.

45.2.1.6.b PMA egress AUI stop enable (1.7.8)

If bit 1.7.8 is set to 1 then the PMA may stop the egress direction AUI signaling during LPI otherwise it shall keep active signaling on that AUI. If the PMA does not support EEE capability or is not able to stop the egress direction AUI signaling (see 45.2.1.2.b) then this bit has no effect.

45.2.1.7.4 Transmit fault (1.8.11)

Insert the following rows between “40GBASE-FR” and “100GBASE-LR4, 100GBASE-ER4” in Table 45-9:

Table 45–9—Transmit fault description location

PMA/PMD	Description location
100GBASE-KP4	94.3.8
100GBASE-KR4	93.7.10
100GBASE-CR4	92.7.10

45.2.1.7.5 Receive fault (1.8.10)

Insert the following rows between “40GBASE-FR” and “100GBASE-LR4, 100GBASE-ER4” in Table 45-10:

Table 45–10—Receive fault description location

PMA/PMD	Description location
100GBASE-KP4	94.3.9
100GBASE-KR4	93.7.11
100GBASE-CR4	92.7.11

Change 45.2.1.8 for transmit disable as follows:

45.2.1.8 PMD transmit disable register (Register 1.9)

The assignment of bits in the PMD transmit disable register is shown in Table 45-11. The transmit disable functionality is optional and a PMD’s ability to perform the transmit disable functionality is advertised in the PMD transmit disable ability bit 1.8.8. A PMD that does not implement the transmit disable functionality