

IEEE Standard for Ethernet

Amendment 3: Physical Layer Specifications and Management Parameters for 40 Gb/s and 100 Gb/s Operation over Fiber Optic Cables

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

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(Amendment to
IEEE Std 802.3™-2012
as amended by IEEE Std 802.3bk™-2013
and IEEE Std 802.3bj™-2014)

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**LAN/MAN Standards Committee
of the
IEEE Computer Society**

Approved 16 February 2015
IEEE-SA Standards Board

Abstract: Physical Layer specifications and management parameters for 40 Gb/s operation over single-mode fiber (40GBASE-ER4) and for 100 Gb/s operation over multimode fiber (100GBASE-SR4) are added by this amendment. This amendment also specifies a four-lane variant of the 100 Gigabit Attachment Unit Interface (CAUI-4) and optional Energy Efficient Ethernet (EEE) for 40 Gb/s and 100 Gb/s operation over fiber optic cables.

Keywords: 100 Gb/s Ethernet, 100GBASE-ER4, 100GBASE-LR4, 100GBASE-SR10, 100GBASE-SR4, 40 Gb/s Ethernet, 40GBASE-ER4, 40GBASE-FR, 40GBASE-LR4, 40GBASE-SR4, amendment, CAUI-4, Energy Efficient Ethernet (EEE), Ethernet, forward error correction (FEC), IEEE 802.3™, IEEE 802.3bm™, MMF, Physical Medium Dependent (PMD) sublayer, SMF

*Dedicated to the memory of our friend
and colleague Brian J. Misek*

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Introduction

This introduction is not part of IEEE Std 802.3bm-2015, IEEE Standard for Ethernet—Amendment 3: Physical Layer Specifications and Management Parameters for 40 Gb/s and 100 Gb/s Operation over Fiber Optic Cables.

IEEE Std 802.3 was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3bm-2015).

The Media Access Control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x specified full duplex operation and a flow control protocol, IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2012 and are not maintained as separate documents.

At the date of IEEE Std 802.3bm-2015 publication, IEEE Std 802.3 is comprised of the following documents:

IEEE Std 802.3-2012

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification.

Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 90 and Annex 83A through Annex 86A. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 89 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bk™-2013

Amendment 1—This amendment includes changes to EPON as defined in IEEE Std 802.3-2012 and adds the physical layer specifications and management parameters for EPON operation on point-to-multipoint passive optical networks supporting extended power budget classes of PX30 (29 dB for 1G-EPON), PX40 (33 dB for 1G-EPON), PRX40 (33 dB for 10/1G-EPON), and PR40 (33 dB for 10/10G-EPON).

IEEE Std 802.3bj™-2014

Amendment 2—This amendment includes changes to IEEE Std 802.3-2012 and adds Clause 91 through Clause 94 as well as associated annexes. This amendment adds 100 Gb/s Physical Layer (PHY) specifications and management parameters for operation on electrical backplanes and twinaxial copper cables. This amendment also specifies optional Energy Efficient Ethernet (EEE) for 40 Gb/s and 100 Gb/s operation over electrical backplanes and copper cables.

IEEE Std 802.3bm™-2015

Amendment 3—This amendment includes changes to IEEE Std 802.3-2012 and adds Clause 95 as well as associated annexes. This amendment adds Physical Layer (PHY) specifications and management parameters for 40 Gb/s operation over single-mode fiber (40GBASE-ER4) and for 100 Gb/s operation over multimode fiber (100GBASE-SR4). This amendment also specifies a four-lane variant of the 100 Gigabit Attachment Unit Interface (CAUI-4) and optional Energy Efficient Ethernet (EEE) for 40 Gb/s and 100 Gb/s operation over fiber optic cables.

A companion document IEEE Std 802.3.1™ describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 3: Physical Layer Specifications and Management Parameters for 40 Gb/s and 100 Gb/s Operation over Fiber Optic Cables

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(This amendment is based on IEEE Std 802.3™-2012 as amended by IEEE Std 802.3bk™-2013 and IEEE Std 802.3bj™-2014.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in bold italic. Four editing instructions are used: change, delete, insert, and replace. Change is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strike through~~ (to remove old material) and underscore (to add new material). Delete removes existing material. Insert adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Replace is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.¹

¹Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement this standard.

1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Change item m) in 1.1.3.2 as follows:

- m) *100 Gigabit Attachment Unit Interface (CAUI-n)*. The CAUI-n is a physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 100 Gb/s speeds. The CAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Two widths of CAUI-n are defined: a ten-lane version (CAUI-10) in Annex 83A and Annex 83B, and a four-lane version (CAUI-4) in Annex 83D and Annex 83E. No mechanical connector is specified for use with the CAUI-n. The CAUI-n is optional.

1.3 Normative references

Insert the following references in alphanumerical order into 1.3:

IEC 61753-1:2007, Fibre optic interconnecting devices and passive components performance standard—Part 1: General and guidance for performance standards.

IEC 61754-7-1:2014, Fibre optic interconnecting devices and passive components—Fibre optic connector interfaces—Part 7-1: Type MPO connector family—One fibre row.

1.4 Definitions

Insert the following new definition after 1.4.53 “100GBASE-LR4” (renumbered from 1.4.54 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013):

1.4.53a 100GBASE-SR4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over four lanes of multimode fiber, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 95.)

Insert the following new definition after 1.4.60 “40GBASE-CR4” (renumbered from 1.4.61 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013):

1.4.60a 40GBASE-ER4: IEEE 802.3 Physical Layer specification for 40 Gb/s using 40GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 40 km. (See IEEE Std 802.3, Clause 87.)

Change 1.4.73 (renumbered from 1.4.74 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013) as follows:

1.4.73 100 Gigabit Attachment Unit Interface (CAUI-n): A physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. Two widths of CAUI-n are defined: a ten-lane version (CAUI-10) and a four-lane version (CAUI-4). (See IEEE Std 802.3, Annex 83A and Annex 83B for CAUI-10, or Annex 83D and Annex 83E for CAUI-4.)

1.5 Abbreviations

Change the abbreviation “CAUI” in 1.5 as follows:

CAUI- <u>n</u>	100 Gigabit Attachment Unit Interface <u>over n lanes</u>
----------------	---

22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

22.2 Functional specifications

22.2.4 Management functions

22.2.4.3 Extended capability registers

22.2.4.3.1 PHY Identifier (Registers 2 and 3)

Insert the following note at the end of 22.2.4.3.1:

NOTE—The use of only 22 bits of the OUI as described here has been deprecated by the IEEE Registration Authority. The definition of vendor-specific device identifiers for other applications is expected to use the full 24 bits to accommodate the use of either an OUI or Company ID.

30. Management

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert 40GBASE-ER4 PHY type into the “APPROPRIATE SYNTAX” section of 30.5.1.1.2 after 40GBASE-LR4:

...
40GBASE-ER4 40GBASE-R PCS/PMA over 4 WDM lane single mode fiber PMD, with
extended reach, as specified in Clause 87
...

Insert 100GBASE-SR4 PHY type into the “APPROPRIATE SYNTAX” section of 30.5.1.1.2 before 100GBASE-SR10:

...
100GBASE-SR4 100GBASE-R PCS/PMA over 4 lane multimode fiber PMD as specified in
Clause 95
...

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the identified reserved row in Table 45–3 (as modified by IEEE Std 802.3bj-2014) and insert four new rows after the changed row as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.176 through 1.199	Reserved	
1.179	CAUI-4 chip-to-module recommended CTLE	45.2.1.92aa
1.180 through 1.183	CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 0 through lane 3	45.2.1.92ab 45.2.1.92ac
1.184 through 1.187	CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 through lane 3	45.2.1.92ad 45.2.1.92ae
1.188 through 1.199	Reserved	

45.2.1.3 PMA/PMD device identifier (Registers 1.2 and 1.3)

Change 45.2.1.3 to add a note as follows:

Registers 1.2 and 1.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PMA/PMD. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number.

A PMA/PMD may return a value of zero in each of the 32 bits of the PMA/PMD device identifier to indicate that a unique identifier as described above is not provided.

The format of the PMA/PMD device identifier is specified in 22.2.4.3.1.

NOTE—The use of only 22 bits of the OUI as described here has been deprecated by the IEEE Registration Authority. The definition of vendor-specific device identifiers for other applications is expected to use the full 24 bits to accommodate the use of either an OUI or Company ID.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change Table 45–7 (as modified by IEEE Std 802.3bj-2014 and IEEE Std 802.3bk-2013) as follows:

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.7.15:10	Reserved	Value always 0, writes ignored	R/W
1.7.9	PIASE	PMA ingress AUI stop enable	R/W
1.7.8	PEASE	PMA egress AUI stop enable	R/W
1.7.7:6	Reserved	Value always 0, writes ignored	R/W
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 x x x x = reserved for future use 1 0 1 1 1 1 = <u>100GBASE-SR4 PMA/PMD</u> ~~reserved for future use~~ 1 0 1 1 1 0 = 100GBASE-CR4 PMA/PMD 1 0 1 1 0 1 = 100GBASE-KR4 PMA/PMD 1 0 1 1 0 0 = 100GBASE-KP4 PMA/PMD 1 0 1 0 1 1 = 100GBASE-ER4 PMA/PMD 1 0 1 0 1 0 = 100GBASE-LR4 PMA/PMD 1 0 1 0 0 1 = 100GBASE-SR10 PMA/PMD 1 0 1 0 0 0 = 100GBASE-CR10 PMA/PMD 1 0 0 1 1 x = reserved for future use 1 0 0 1 0 1 = <u>40GBASE-ER4 PMA/PMD</u> ~~reserved for future use~~ 1 0 0 1 0 0 = 40GBASE-FR PMA/PMD 1 0 0 0 1 1 = 40GBASE-LR4 PMA/PMD 1 0 0 0 1 0 = 40GBASE-SR4 PMA/PMD 1 0 0 0 0 1 = 40GBASE-CR4 PMA/PMD 1 0 0 0 0 0 = 40GBASE-KR4 PMA/PMD 0 1 1 1 1 1 = 10/1GBASE-PRX-U4 0 1 1 1 1 0 = 10GBASE-PR-U4 0 1 1 1 0 1 = 10/1GBASE-PRX-D4 0 1 1 1 0 0 = 10GBASE-PR-D4 0 1 1 0 1 1 = reserved 0 1 1 0 1 0 = 10GBASE-PR-U3 0 1 1 0 0 1 = 10GBASE-PR-U1 0 1 1 0 0 0 = 10/1GBASE-PRX-U3 0 1 0 1 1 1 = 10/1GBASE-PRX-U2 0 1 0 1 1 0 = 10/1GBASE-PRX-U1 0 1 0 1 0 1 = 10GBASE-PR-D3 0 1 0 1 0 0 = 10GBASE-PR-D2 0 1 0 0 1 1 = 10GBASE-PR-D1 0 1 0 0 1 0 = 10/1GBASE-PRX-D3 0 1 0 0 0 1 = 10/1GBASE-PRX-D2 0 1 0 0 0 0 = 10/1GBASE-PRX-D1 0 0 1 1 1 1 = 10BASE-T PMA/PMD 0 0 1 1 1 0 = 100BASE-TX PMA/PMD 0 0 1 1 0 1 = 1000BASE-KX PMA/PMD 0 0 1 1 0 0 = 1000BASE-T PMA/PMD 0 0 1 0 1 1 = 10GBASE-KR PMA/PMD 0 0 1 0 1 0 = 10GBASE-KX4 PMA/PMD 0 0 1 0 0 1 = 10GBASE-T PMA 0 0 1 0 0 0 = 10GBASE-LRM PMA/PMD 0 0 0 1 1 1 = 10GBASE-SR PMA/PMD 0 0 0 1 1 0 = 10GBASE-LR PMA/PMD 0 0 0 1 0 1 = 10GBASE-ER PMA/PMD 0 0 0 1 0 0 = 10GBASE-LX4 PMA/PMD 0 0 0 0 1 1 = 10GBASE-SW PMA/PMD 0 0 0 0 1 0 = 10GBASE-LW PMA/PMD 0 0 0 0 0 1 = 10GBASE-EW PMA/PMD 0 0 0 0 0 0 = 10GBASE-CX4 PMA/PMD	R/W

^aR/W = Read/Write

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Change Table 45–9 (as modified by IEEE Std 802.3bj-2014) as follows:

Table 45–9—Transmit fault description location

PMA/PMD	Description location
10GBASE-KR	72.6.8
10GBASE-LRM	68.4.8
10GBASE-S, 10GBASE-L, 10GBASE-E	52.4.8
10GBASE-LX4	53.4.10
10GBASE-CX4	54.5.10
10GBASE-T	55.4.2.2
10GBASE-KX4	71.6.10
40GBASE-KR4	84.7.10
40GBASE-CR4, 100GBASE-CR10	85.7.10
40GBASE-SR4, 100GBASE-SR10	86.5.10
40GBASE-LR4, 40GBASE-ER4	87.5.10
40GBASE-FR	89.5.8
100GBASE-KP4	94.3.8
100GBASE-KR4	93.7.10
100GBASE-CR4	92.7.10
100GBASE-SR4	95.5.10
100GBASE-LR4, 100GBASE-ER4	88.5.10

45.2.1.7.5 Receive fault (1.8.10)

Change Table 45–10 (as modified by IEEE Std 802.3bj-2014) as follows:

Table 45–10—Receive fault description location

PMA/PMD	Description location
10GBASE-KR	72.6.9
10GBASE-LRM	68.4.9
10GBASE-S, 10GBASE-L, 10GBASE-E	52.4.9
10GBASE-LX4	53.4.11
10GBASE-CX4	54.5.11

Table 45–10—Receive fault description location (*continued*)

PMA/PMD	Description location
10GBASE-T	55.4.2.4
10GBASE-KX4	71.6.11
40GBASE-KR4	84.7.11
40GBASE-CR4, 100GBASE-CR10	85.7.11
40GBASE-SR4, 100GBASE-SR10	86.5.11
40GBASE-LR4, <u>40GBASE-ER4</u>	87.5.11
40GBASE-FR	89.5.9
100GBASE-KP4	94.3.9
100GBASE-KR4	93.7.11
100GBASE-CR4	92.7.11
<u>100GBASE-SR4</u>	<u>95.5.11</u>
100GBASE-LR4, 100GBASE-ER4	88.5.11

45.2.1.8 PMD transmit disable register (Register 1.9)

Change Table 45–11a (as inserted by IEEE Std 802.3bj-2014) as follows:

Table 45–11a—Transmit disable description location

PMA/PMD	Description location
10GBASE-KR	72.6.5
10GBASE-LRM	68.4.7
Other 10GBASE-R	52.4.7
10GBASE-LX4	53.4.7
10GBASE-CX4	54.5.6
10GBASE-T	55.4.2.3
10GBASE-KX4	71.6.6
40GBASE-KR4	84.7.6
40GBASE-CR4 and 100GBASE-CR10	85.7.6
40GBASE-SR4 and 100GBASE-SR10	86.5.7
40GBASE-LR4 <u>and 40GBASE-ER4</u>	87.5.7
40GBASE-FR	89.5.6
100GBASE-KP4	94.3.6.6
100GBASE-KR4	93.7.6

Table 45–11a—Transmit disable description location (*continued*)

PMA/PMD	Description location
100GBASE-CR4	92.7.6
<u>100GBASE-SR4</u>	<u>95.5.7</u>
100GBASE-LR4 and 100GBASE-ER4	88.5.7

45.2.1.12 40G/100G PMA/PMD extended ability register (Register 1.13)

Change Table 45–15 (as modified by IEEE Std 802.3bj-2014) as follows:

Table 45–15—40G/100G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.13.15	PMA remote loopback ability	1 = PMA has the ability to perform a remote loopback function 0 = PMA does not have the ability to perform a remote loopback function	RO
1.13.14	100GBASE-CR4 ability	1 = PMA/PMD is able to perform 100GBASE-CR4 0 = PMA/PMD is not able to perform 100GBASE-CR4	RO
1.13.13	100GBASE-KR4 ability	1 = PMA/PMD is able to perform 100GBASE-KR4 0 = PMA/PMD is not able to perform 100GBASE-KR4	RO
1.13.12	100GBASE-KP4 ability	1 = PMA/PMD is able to perform 100GBASE-KP4 0 = PMA/PMD is not able to perform 100GBASE-KP4	RO
1.13.11	100GBASE-ER4 ability	1 = PMA/PMD is able to perform 100GBASE-ER4 0 = PMA/PMD is not able to perform 100GBASE-ER4	RO
1.13.10	100GBASE-LR4 ability	1 = PMA/PMD is able to perform 100GBASE-LR4 0 = PMA/PMD is not able to perform 100GBASE-LR4	RO
1.13.9	100GBASE-SR10 ability	1 = PMA/PMD is able to perform 100GBASE-SR10 0 = PMA/PMD is not able to perform 100GBASE-SR10	RO
1.13.8	100GBASE-CR10 ability	1 = PMA/PMD is able to perform 100GBASE-CR10 0 = PMA/PMD is not able to perform 100GBASE-CR10	RO
<u>1.13.7</u>	<u>100GBASE-SR4 ability</u>	<u>1 = PMA/PMD is able to perform 100GBASE-SR4</u> <u>0 = PMA/PMD is not able to perform 100GBASE-SR4</u>	<u>RO</u>
~~1.13.67–5~~	Reserved	Ignore on read	RO
<u>1.13.5</u>	<u>40GBASE-ER4 ability</u>	<u>1 = PMA/PMD is able to perform 40GBASE-ER4</u> <u>0 = PMA/PMD is not able to perform 40GBASE-ER4</u>	<u>RO</u>
1.13.4	40GBASE-FR ability	1 = PMA/PMD is able to perform 40GBASE-FR 0 = PMA/PMD is not able to perform 40GBASE-FR	RO
1.13.3	40GBASE-LR4 ability	1 = PMA/PMD is able to perform 40GBASE-LR4 0 = PMA/PMD is not able to perform 40GBASE-LR4	RO
1.13.2	40GBASE-SR4 ability	1 = PMA/PMD is able to perform 40GBASE-SR4 0 = PMA/PMD is not able to perform 40GBASE-SR4	RO
1.13.1	40GBASE-CR4 ability	1 = PMA/PMD is able to perform 40GBASE-CR4 0 = PMA/PMD is not able to perform 40GBASE-CR4	RO
1.13.0	40GBASE-KR4 ability	1 = PMA/PMD is able to perform 40GBASE-KR4 0 = PMA/PMD is not able to perform 40GBASE-KR4	RO

^aRO = Read only

Insert 45.2.1.12.5a and 45.2.1.12.5b after 45.2.1.12.5 as follows:

45.2.1.12.5a 100GBASE-SR4 ability (1.13.7)

When read as a one, bit 1.13.7 indicates that the PMA/PMD is able to operate as a 100GBASE-SR4 PMA/PMD type. When read as a zero, bit 1.13.7 indicates that the PMA/PMD is not able to operate as a 100GBASE-SR4 PMA/PMD type.

45.2.1.12.5b 40GBASE-ER4 ability (1.13.5)

When read as a one, bit 1.13.5 indicates that the PMA/PMD is able to operate as a 40GBASE-ER4 PMA/PMD type. When read as a zero, bit 1.13.5 indicates that the PMA/PMD is not able to operate as a 40GBASE-ER4 PMA/PMD type.

Insert 45.2.1.92aa through 45.2.1.92ae after 45.2.1.92 (and before 45.2.1.92a as inserted by IEEE Std 802.3bj-2014) as follows:

45.2.1.92aa CAUI-4 chip-to-module recommended CTLE register (Register 1.179)

The assignment of bits in the CAUI-4 chip-to-module recommended CTLE register is shown in Table 45–71aa.

Table 45–71aa—CAUI-4 chip-to-module recommended CTLE register bit definitions

Bit(s)	Name	Description	R/W ^a
1.179.15:5	Reserved	Value always 0, writes ignored	RO
1.179.4:1	Recommended CTLE peaking	4 3 2 1 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = 9 dB 1 0 0 0 = 8 dB 0 1 1 1 = 7 dB 0 1 1 0 = 6 dB 0 1 0 1 = 5 dB 0 1 0 0 = 4 dB 0 0 1 1 = 3 dB 0 0 1 0 = 2 dB 0 0 0 1 = 1 dB 0 0 0 0 = Reserved	R/W
1.179.0	Reserved	Value always 0, writes ignored	RO

^aR/W = Read/Write, RO = Read only

45.2.1.92aa.1 Recommended CTLE peaking (1.179.4:1)

The value of these bits sets the CTLE peaking value recommended by a host that implements the optional CAUI-4 chip-to-module interface defined in Annex 83E (see 83E.3.1.6). The module may optionally use this information to adjust its CTLE setting.

45.2.1.92ab CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 0 register (Register 1.180)

The assignment of bits in the CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 0 register is shown in Table 45–71ab. The transmitter, receive direction, is the transmitter that sends data towards the PCS.

Table 45–71ab—CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.180.15	Request flag	1 = Change in equalization is requested 0 = No change in equalization is requested	RO
1.180.14:12	Post-cursor request	14 13 12 1 1 1 Reserved 1 1 0 Reserved 1 0 1 <i>Requested_eq_cl</i> = 5 (c(1) ratio –0.25) 1 0 0 <i>Requested_eq_cl</i> = 4 (c(1) ratio –0.2) 0 1 1 <i>Requested_eq_cl</i> = 3 (c(1) ratio –0.15) 0 1 0 <i>Requested_eq_cl</i> = 2 (c(1) ratio –0.1) 0 0 1 <i>Requested_eq_cl</i> = 1 (c(1) ratio –0.05) 0 0 0 <i>Requested_eq_cl</i> = 0 (c(1) ratio 0)	RO
1.180.11:10	Pre-cursor request	11 10 1 1 <i>Requested_eq_cm1</i> = 3 (c(–1) ratio –0.15) 1 0 <i>Requested_eq_cm1</i> = 2 (c(–1) ratio –0.1) 0 1 <i>Requested_eq_cm1</i> = 1 (c(–1) ratio –0.05) 0 0 <i>Requested_eq_cm1</i> = 0 (c(–1) ratio 0)	RO
1.180.9:7	Post-cursor remote setting	9 8 7 1 1 1 Reserved 1 1 0 Reserved 1 0 1 <i>Remote_eq_cl</i> = 5 (c(1) ratio –0.25) 1 0 0 <i>Remote_eq_cl</i> = 4 (c(1) ratio –0.2) 0 1 1 <i>Remote_eq_cl</i> = 3 (c(1) ratio –0.15) 0 1 0 <i>Remote_eq_cl</i> = 2 (c(1) ratio –0.1) 0 0 1 <i>Remote_eq_cl</i> = 1 (c(1) ratio –0.05) 0 0 0 <i>Remote_eq_cl</i> = 0 (c(1) ratio 0)	R/W
1.180.6:5	Pre-cursor remote setting	6 5 1 1 <i>Remote_eq_cm1</i> = 3 (c(–1) ratio –0.15) 1 0 <i>Remote_eq_cm1</i> = 2 (c(–1) ratio –0.1) 0 1 <i>Remote_eq_cm1</i> = 1 (c(–1) ratio –0.05) 0 0 <i>Remote_eq_cm1</i> = 0 (c(–1) ratio 0)	R/W
1.180.4:2	Post-cursor local setting	4 3 2 1 1 1 Reserved 1 1 0 Reserved 1 0 1 <i>Local_eq_cl</i> = 5 (c(1) ratio –0.25) 1 0 0 <i>Local_eq_cl</i> = 4 (c(1) ratio –0.2) 0 1 1 <i>Local_eq_cl</i> = 3 (c(1) ratio –0.15) 0 1 0 <i>Local_eq_cl</i> = 2 (c(1) ratio –0.1) 0 0 1 <i>Local_eq_cl</i> = 1 (c(1) ratio –0.05) 0 0 0 <i>Local_eq_cl</i> = 0 (c(1) ratio 0)	R/W
1.180.1:0	Pre-cursor local setting	1 0 1 1 <i>Local_eq_cm1</i> = 3 (c(–1) ratio –0.15) 1 0 <i>Local_eq_cm1</i> = 2 (c(–1) ratio –0.1) 0 1 <i>Local_eq_cm1</i> = 1 (c(–1) ratio –0.05) 0 0 <i>Local_eq_cm1</i> = 0 (c(–1) ratio 0)	R/W

^aR/W = Read/Write, RO = Read only

45.2.1.92ab.1 Request flag (1.180.15)

The value of this bit indicates the value of the variable *Request_flag* in the lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). This indicates whether the CAUI-4 chip-to-chip device is issuing a request to change the remote transmitter equalization in the CAUI-4 chip-to-chip lane 0 transmitter in the receive direction. If a lane 0 CAUI-4 receiver in the receive direction is not present in the package, then the value returned for this bit should be zero.

45.2.1.92ab.2 Post-cursor request (1.180.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). When *Request_flag* is equal to 1, this value indicates the ratio of the post-cursor coefficient $c(1)$, which is requested for the transmitter equalization in the CAUI-4 chip-to-chip lane 0 transmitter in the receive direction.

45.2.1.92ab.3 Pre-cursor request (1.180.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). When *Request_flag* is equal to 1, this value indicates the ratio of the pre-cursor coefficient $c(-1)$, which is requested for the transmitter equalization in the CAUI-4 chip-to-chip lane 0 transmitter in the receive direction.

45.2.1.92ab.4 Post-cursor remote setting (1.180.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). This is used by a CAUI-4 receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient $c(1)$ being used in lane 0 of the CAUI-4 transmitter in the receive direction (see 83D.3.1.1). It may be used to generate values for the request flag and the request bits. If a lane 0 CAUI-4 receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.92ab.5 Pre-cursor remote setting (1.180.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). This is used by a CAUI-4 receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient $c(-1)$ being used in lane 0 of the CAUI-4 transmitter in the receive direction (see 83D.3.1.1). It may be used to generate values for the request flag and the request bits. If a lane 0 CAUI-4 receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.92ab.6 Post-cursor local setting (1.180.4:2)

The value of these bits sets the variable *Local_eq_c1* for the lane 0 CAUI-4 transmitter in the receive direction (see 83D.3.1.1 and Table 83D-3), which controls the weight of the transmitter equalization post-cursor coefficient $c(1)$. If a lane 0 CAUI-4 transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.92ab.7 Pre-cursor local setting (1.180.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the lane 0 CAUI-4 transmitter in the receive direction (see 83D.3.1.1 and Table 83D-2), which controls the weight of the transmitter equalization pre-cursor coefficient $c(-1)$. If a lane 0 CAUI-4 transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.92ac CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 1 through lane 3 registers (Registers 1.181, 1.182, 1.183)

The CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 1 through lane 3 registers are defined similarly to register 1.180 (which is used for lane 0, see 45.2.1.92ab) but for lanes 1 through 3, respectively. The transmitter, receive direction, is the transmitter that sends data towards the PCS.

45.2.1.92ad CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 register (Register 1.184)

The assignment of bits in the CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 register is shown in Table 45–71ac. The transmitter, transmit direction, is the transmitter that sends data towards the PMD.

Table 45–71ac—CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.184.15	Request flag	1 = Change in equalization is requested 0 = No change in equalization is requested	RO
1.184.14:12	Post-cursor request	14 13 12 1 1 1 Reserved 1 1 0 Reserved 1 0 1 <i>Requested_eq_cl</i> = 5 (c(1) ratio –0.25) 1 0 0 <i>Requested_eq_cl</i> = 4 (c(1) ratio –0.2) 0 1 1 <i>Requested_eq_cl</i> = 3 (c(1) ratio –0.15) 0 1 0 <i>Requested_eq_cl</i> = 2 (c(1) ratio –0.1) 0 0 1 <i>Requested_eq_cl</i> = 1 (c(1) ratio –0.05) 0 0 0 <i>Requested_eq_cl</i> = 0 (c(1) ratio 0)	RO
1.184.11:10	Pre-cursor request	11 10 1 1 <i>Requested_eq_cm1</i> = 3 (c(–1) ratio –0.15) 1 0 <i>Requested_eq_cm1</i> = 2 (c(–1) ratio –0.1) 0 1 <i>Requested_eq_cm1</i> = 1 (c(–1) ratio –0.05) 0 0 <i>Requested_eq_cm1</i> = 0 (c(–1) ratio 0)	RO
1.184.9:7	Post-cursor remote setting	9 8 7 1 1 1 Reserved 1 1 0 Reserved 1 0 1 <i>Remote_eq_cl</i> = 5 (c(1) ratio –0.25) 1 0 0 <i>Remote_eq_cl</i> = 4 (c(1) ratio –0.2) 0 1 1 <i>Remote_eq_cl</i> = 3 (c(1) ratio –0.15) 0 1 0 <i>Remote_eq_cl</i> = 2 (c(1) ratio –0.1) 0 0 1 <i>Remote_eq_cl</i> = 1 (c(1) ratio –0.05) 0 0 0 <i>Remote_eq_cl</i> = 0 (c(1) ratio 0)	R/W
1.184.6:5	Pre-cursor remote setting	6 5 1 1 <i>Remote_eq_cm1</i> = 3 (c(–1) ratio –0.15) 1 0 <i>Remote_eq_cm1</i> = 2 (c(–1) ratio –0.1) 0 1 <i>Remote_eq_cm1</i> = 1 (c(–1) ratio –0.05) 0 0 <i>Remote_eq_cm1</i> = 0 (c(–1) ratio 0)	R/W

Table 45–71ac—CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 register bit definitions (*continued*)

Bit(s)	Name	Description	R/W ^a
1.184.4:2	Post-cursor local setting	4 3 2 1 1 1 Reserved 1 1 0 Reserved 1 0 1 <i>Local_eq_c1</i> = 5 (c(1) ratio –0.25) 1 0 0 <i>Local_eq_c1</i> = 4 (c(1) ratio –0.2) 0 1 1 <i>Local_eq_c1</i> = 3 (c(1) ratio –0.15) 0 1 0 <i>Local_eq_c1</i> = 2 (c(1) ratio –0.1) 0 0 1 <i>Local_eq_c1</i> = 1 (c(1) ratio –0.05) 0 0 0 <i>Local_eq_c1</i> = 0 (c(1) ratio 0)	R/W
1.184.1:0	Pre-cursor local setting	1 0 1 1 <i>Local_eq_cm1</i> = 3 (c(–1) ratio –0.15) 1 0 <i>Local_eq_cm1</i> = 2 (c(–1) ratio –0.1) 0 1 <i>Local_eq_cm1</i> = 1 (c(–1) ratio –0.05) 0 0 <i>Local_eq_cm1</i> = 0 (c(–1) ratio 0)	R/W

^aR/W = Read/Write, RO = Read only

45.2.1.92ad.1 Request flag (1.184.15)

The value of this bit indicates the value of the variable *Request_flag* in the lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). This indicates whether the CAUI-4 chip-to-chip device is issuing a request to change the remote transmitter equalization in the CAUI-4 chip-to-chip lane 0 transmitter in the transmit direction. If a lane 0 CAUI-4 receiver in the transmit direction is not present in the package, then the value returned for this bit should be zero.

45.2.1.92ad.2 Post-cursor request (1.184.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). When *Request_flag* is equal to 1, this value indicates the ratio of the post-cursor coefficient c(1), which is requested for the transmitter equalization in the CAUI-4 chip-to-chip lane 0 transmitter in the transmit direction.

45.2.1.92ad.3 Pre-cursor request (1.184.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). When *Request_flag* is equal to 1, this value indicates the ratio of the pre-cursor coefficient c(–1), which is requested for the transmitter equalization in the CAUI-4 chip-to-chip lane 0 transmitter in the transmit direction.

45.2.1.92ad.4 Post-cursor remote setting (1.184.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). This is used by a CAUI-4 receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient c(1) being used in lane 0 of the CAUI-4 transmitter in the transmit direction (see 83D.3.1.1). It may be used to generate values for the request flag and the request bits. If a lane 0 CAUI-4 receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.92ad.5 Pre-cursor remote setting (1.184.6:5)

The value of these bits sets the variable *Remote_eq_cml* for the lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). This is used by a CAUI-4 receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient $c(-1)$ being used in lane 0 of the CAUI-4 transmitter in the transmit direction (see 83D.3.1.1). It may be used to generate values for the request flag and the request bits. If a lane 0 CAUI-4 receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.92ad.6 Post-cursor local setting (1.184.4:2)

The value of these bits sets the variable *Local_eq_cl* for the lane 0 CAUI-4 transmitter in the transmit direction (see 83D.3.1.1 and Table 83D-3), which controls the weight of the transmitter equalization post-cursor coefficient $c(1)$. If a lane 0 CAUI-4 transmitter in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.92ad.7 Pre-cursor local setting (1.184.1:0)

The value of these bits sets the variable *Local_eq_cml* for the lane 0 CAUI-4 transmitter in the transmit direction (see 83D.3.1.1 and Table 83D-2), which controls the weight of the transmitter equalization pre-cursor coefficient $c(-1)$. If a lane 0 CAUI-4 transmitter in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.92ae CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 3 registers (Registers 1.185, 1.186, 1.187)

The CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 3 registers are defined similarly to register 1.184 (which is used for lane 0, see 45.2.1.92ad) but for lanes 1 through 3, respectively. The transmitter, transmit direction, is the transmitter that sends data towards the PMD.

45.2.3 PCS registers

45.2.3.46 Lane 0 mapping register (Register 3.400)

Change Table 45-140 as follows:

Table 45-140—Lane 0 mapping register bit definitions

Bit(s)	Name	Description	R/W ^a
3.400.15:56	Reserved	Ignore when read	RO
3.400.45:0	Lane 0 mapping	PCS lane received in service interface lane 0	RO

^aRO = Read only

69. Introduction to Ethernet operation over electrical backplanes

69.1 Overview

69.1.2 Relationship of Backplane Ethernet to the ISO OSI reference model

Change items f) and g) (as respectively modified and inserted by IEEE Std 802.3bj-2014) in 69.1.2 (as renumbered from 69.1.3 by IEEE Std 802.3bj-2014) as follows:

- f) The PMA service interface, which, when physically implemented as XLAUI (40 Gigabit Attachment Unit Interface) or as CAUI-4 (100 Gigabit four-lane Attachment Unit Interface) at an observable interconnection port, uses a four-lane data path as specified in Annex 83A or Annex 83D, respectively.
- g) The PMA service interface, which, when physically implemented as CAUI-10 (100 Gigabit ten-lane Attachment Unit Interface) at an observable interconnection port, uses a ten-lane data path as specified in Annex 83A.

69.2 Summary of Backplane Ethernet Sublayers

69.2.3 Physical Layer signaling systems

Change Table 69–1a (as inserted by IEEE Std 802.3bj-2014) as follows:

Table 69–1a—Nomenclature and clause correlation for 40 Gb/s and 100 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause																
	73	74	78	81			82		83		83A		<u>83D</u>	84	91	93	94
	Auto-Negotiation	BASE-R FEC	Energy-Efficient Ethernet (EEE)	RS	XLGMII	CGMII	40GBASE-R PCS	100GBASE-R PCS	40GBASE-R PMA	100GBASE-R PMA	XLAUI	CAUI-10	<u>CAUI-4</u>	40GBASE-KR4 PMD	RS-FEC	100GBASE-KR4 PMD	100GBASE-KP4 PMA/PMD
40GBASE-KR4	M ^a	O ^a	O	M	O		M		M		O			M			
100GBASE-KR4	M		O	M		O		M		M		O	<u>O</u>		M	M	
100GBASE-KP4	M		O	M		O		M				O	<u>O</u>		M		M

^aO = Optional, M = Mandatory

74. Forward Error Correction (FEC) sublayer for BASE-R PHYs

74.4 Inter-sublayer interfaces

Change the second paragraph of 74.4 as follows:

For 40GBASE-R and 100GBASE-R the FEC service interface can either connect to the PCS as illustrated in [Figure 74–1](#) or the PMA as illustrated in Figure 83–2 where the FEC and PCS are in separate devices connected by XLAUI/CAUI-n.

74.5 FEC service interface

Change the third paragraph of 74.5 as follows:

Optional physical instantiations of the PMA service interface have been defined (see [Clause 51](#), Annex 83A, ~~and Annex 83B, Annex 83D, and Annex 83E~~). There is XSBI (10 Gigabit Sixteen-Bit Interface) for 10GBASE-R, XLAUI for 40GBASE-R and CAUI-n for 100GBASE-R. These physical instantiations, with a PMA if required, may also be used for the FEC service interface.

78. Energy-Efficient Ethernet (EEE)

78.1 Overview

Change the third paragraph of 78.1 (as inserted by IEEE Std 802.3bj-2014) as follows:

EEE supports operation over twisted-pair cabling systems, twinax cable, electrical backplanes, optical fiber, the XGXS for 10 Gb/s PHYs, the XLAUI for 40 Gb/s PHYs, and the CAUI-10 or CAUI-4 for 100 Gb/s PHYs. Table 78–1 lists the supported PHYs and interfaces and their associated clauses.

78.1.1 LPI Signaling

Change the fifth paragraph of 78.1.1 (as inserted by IEEE Std 802.3bj-2014) as follows:

Coding defined in Clause 83 also allows LPI transmit quiet and alert requests from the PCS to be signaled over the XLAUI and CAUI-n interfaces. The XLAUI and CAUI-n receive interfaces infer the quiet and alert requests from the data received over the interface and use that to recreate the transmit or receive direction signaling. See 83.5.11.1.

78.1.3 Reconciliation sublayer operation

78.1.3.3 PHY LPI operation

78.1.3.3.1 PHY LPI transmit operation

Change the last paragraph of 78.1.3.3.1 (as inserted by IEEE Std 802.3bj-2014) as follows:

For PHYs with an operating speed of 40 Gb/s or greater that implement the optional EEE capability, two modes of LPI operation may be supported: deep sleep and fast wake. *Deep sleep* refers to the mode for which the transmitter ceases transmission during Low Power Idle (as shown in Figure 78–3) and is equivalent to the only mechanism defined for PHYs with an operating speed less than 40 Gb/s. Deep sleep support is optional for PHYs with an operating speed of 40 Gb/s or greater that implement EEE with the exception of the PHYs noted in Table 78–1 that do not support deep sleep. *Fast wake* refers to the mode for which the transmitter continues to transmit signals during Low Power Idle so that the receiver can resume operation with a shorter wake time (as shown in Figure 78–3a). For transmit, other than the PCS encoding LPI, there is no difference between fast wake and normal operation. Fast wake support is mandatory for PHYs with an operating speed of 40 Gb/s or greater that implement EEE.

78.1.4 PHY types optionally supporting EEE

Change Table 78–1 (as modified by IEEE Std 802.3bj-2014) as follows:

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
10BASE-T _e	14
100BASE-TX	24, 25
1000BASE-KX	70, 36
1000BASE-T	40
XGXS (XAUI)	47, 48
10GBASE-KX4	71, 48
10GBASE-KR	72, 51, 49, 74
10GBASE-T	55
XLAUI/CAUI-10 ^a	83A
40GBASE-KR4	82, 83, 84, 74
40GBASE-CR4	82, 83, 85, 74
40GBASE-SR4 ^b	82, 83, 86
40GBASE-FR ^b	82, 83, 89
40GBASE-LR4 ^b	82, 83, 87
40GBASE-ER4 ^b	82, 83, 87
CAUI-4 ^a	83D
100GBASE-KP4	82, 91, 94
100GBASE-KR4	82, 83, 91, 93
100GBASE-CR10	82, 83, 85, 74
100GBASE-CR4	82, 83, 91, 92
100GBASE-SR10 ^b	82, 83, 86
100GBASE-SR4 ^b	82, 83, 91, 95
100GBASE-LR4 ^b	82, 83, 88
100GBASE-ER4 ^b	82, 83, 88

^aXLAUI/CAUI-n shutdown is supported only when deep sleep is enabled for the associated PHY.

^bThe deep sleep mode of EEE is not supported for this PHY.

78.5 Communication link access latency

Change the row for XLAUI/CAUI in Table 78–4 (as modified by IEEE Std 802.3bj-2014) as follows:

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w_sys_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy_shrink_tx}$ (max) (μs)	$T_{phy_shrink_rx}$ (max) (μs)	$T_{w_sys_rx}$ (min) (μs)
100BASE-TX		30	20.5	5.0	15	10
1000BASE-T	Case-1	16.5	16.5	5.0	2.5	1.76
	Case-2	16.5	16.5	12.24	9.74	1.76
1000BASE-KX		13.26	11.25	5.0	6.5	1.76
XGXS (XAUI)		12.38	9.25	5.0	4.5	2.88
10GBASE-T	Case-1	7.36	7.36	4.48	0	2.88
	Case-2	4.48	4.48	1.6	0	2.88
10GBASE-KX4		12.38	9.25	5.0	4.5	2.88
10GBASE-KR	Case-1	15.38	12.25	5.0	7.5	2.88
	Case-2	17.38	14.25	5.0	9.5	2.88
40GBASE-R fast wake		0.34	0.3	0	0	0.25
40GBASE-CR4	Case-1	5.5	5.5	2	3	1.2
	Case-2	6.5	6.5	2	3	1.2
40GBASE-KR4	Case-1	5.5	5.5	2	3	1.2
	Case-2	6.5	6.5	2	3	1.2
100GBASE-R fast wake		0.34	0.3	0	0	0.25
100GBASE-CR10	Case-1	5.5	5.5	2	3	1
	Case-2	7.5	7.5	2	3	1
100GBASE-CR4		5.5	5.5	2	3	1
100GBASE-KR4		5.5	5.5	2	3	1
100GBASE-KP4		5.5	5.5	2	3	1
XLAUI/CAUI- <u>n</u> ^a		1				

^a $T_{w_sys_tx}$ is increased by 1 μs for each instance of XLAUI/CAUI-n with shutdown enabled on the transmit path. The receiver should negotiate an increase for remote T_{w_sys} for the link partner of 1 μs for each instance of XLAUI/CAUI-n with shutdown enabled on the receive path.

Change the title and text of 78.5.2 (as inserted by IEEE Std 802.3bj-2014) as follows:

78.5.2 40 Gb/s and 100 Gb/s PHY extension using XLAUI or CAUI-n

40 Gb/s ~~and 100 Gb/s~~ PHYs may be extended using XLAUI and 100 Gb/s PHYs may be extended using CAUI-10 or CAUI-4 as a physical instantiation of the inter-sublayer service interface to separate functions between devices. The LPI signaling can operate across XLAUI/CAUI-n with no change to the PHY timing parameters described in Table 78-4 or the operation of the Data Link Layer Capabilities negotiation described in 78.4.

If PMA Egress AUI Stop Enable (PEASE, see 83.3; MDIO register bit 1.7.8) is asserted for any of the PMA sublayers, the PMA may stop signaling on the XLAUI/CAUI-n in the transmit direction to conserve energy. If PEASE is asserted, the RS defers sending data following deassertion of LPI by an additional time equal to $T_{w_sys_tx} - T_{w_sys_rx}$ as shown in Table 78-4 for each PMA with PEASE asserted (see 81.3a.2.1).

If PMA Ingress AUI Stop Enable (PIASE, see 83.3; MDIO register bit 1.7.9) is asserted for any of the PMA sublayers, the PMA may stop signaling on the XLAUI/CAUI-n in the receive direction to conserve energy. The receiver should negotiate an additional time for the remote T_{w_sys} (equal to $T_{w_sys_tx} - T_{w_sys_rx}$ for the XLAUI/CAUI-n as shown in Table 78-4) for each PMA with PIASE to be asserted before setting the PIASE bits.

80. Introduction to 40 Gb/s and 100 Gb/s networks

80.1 Overview

80.1.3 Relationship of 40 Gigabit and 100 Gigabit Ethernet to the ISO OSI reference model

Change items c), d), and h) in 80.1.3 (as modified by IEEE Std 802.3bj-2014) as follows:

- c) The PMA service interface, which, when physically implemented as XLAUI (40 Gigabit Attachment Unit Interface) or CAUI-4 (100 Gigabit four-lane Attachment Unit Interface) at an observable interconnection port, uses a 4 lane data path as specified in Annex 83A, ~~or Annex 83B, Annex 83D, or Annex 83E.~~
- d) The PMA service interface, which, when physically implemented as CAUI-10 (100 Gigabit ten-lane Attachment Unit Interface) at an observable interconnection port, uses a 10 lane data path as specified in Annex 83A or Annex 83B.
- ...
- h) The MDIs as specified in Clause 85 for 40GBASE-CR4, in Clause 86 for 40GBASE-SR4, in Clause 87 for 40GBASE-LR4 and 40GBASE-ER4, in Clause 88 for 100GBASE-LR4 and 100GBASE-ER4, ~~and in Clause 92 for 100GBASE-CR4, and in Clause 95 for 100GBASE-SR4~~ all use a 4 lane data path.

80.1.4 Nomenclature

Insert a new row for 40GBASE-ER4 after 40GBASE-LR4 and a new row for 100GBASE-SR4 before 100GBASE-SR10 in Table 80–1 (as modified by IEEE Std 802.3bj-2014) as follows (unchanged rows not shown):

Table 80–1—40 Gb/s and 100 Gb/s PHYs

Name	Description
40GBASE-ER4	40 Gb/s PHY using 40GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 40 km (see Clause 87)
...	
100GBASE-SR4	100 Gb/s PHY using 100GBASE-R encoding over four lanes of multimode fiber, with reach up to at least 100 m (see Clause 95)

80.1.5 Physical Layer signaling systems

Change the text of 80.1.5 (as modified by IEEE Std 802.3bj-2014), change Table 80–2 (as modified by IEEE Std 802.3bj-2014), replace Table 80–2a (which was inserted by IEEE Std 802.3bj-2014), and insert Table 80–2b as follows:

This standard specifies a family of Physical Layer implementations. Table 80–2, ~~and Table 80–2a, and Table 80–2b~~ specify the correlation between nomenclature and clauses. Implementations conforming to one or more nomenclatures must meet the requirements of the corresponding clauses.

Table 80–2—Nomenclature and clause correlation (40GBASE)

Nomenclature	Clause ^a															
	73	74	78	81		82	83	83A	83B	84	85	86	86A	87		89
	Auto-Negotiation	BASE-R FEC	EEE	RS	XLGMII	40GBASE-R PCS	40GBASE-R PMA	XLAUI	XLAUI	40GBASE-KR4 PMD	40GBASE-CR4 PMD	40GBASE-SR4 PMD	XLPII	40GBASE-LR4 PMD	40GBASE-ER4 PMD	40GBASE-FR PMD
40GBASE-KR4	M	O	O	M	O	M	M	O		M						
40GBASE-CR4	M	O	O	M	O	M	M	O			M					
40GBASE-SR4			<u>O</u>	M	O	M	M	O	O			M	O			
40GBASE-FR			<u>O</u>	M	O	M	M	O	O							M
40GBASE-LR4			<u>O</u>	M	O	M	M	O	O				O	M		
40GBASE-ER4			<u>O</u>	<u>M</u>	<u>O</u>	<u>M</u>	<u>M</u>	<u>O</u>	<u>O</u>						<u>M</u>	

^aO = Optional, M = Mandatory.

Table 80–2a—Nomenclature and clause correlation (100GBASE copper)

Nomenclature	Clause ^a													
	73	74	78	81		82	83	83A	83D	85	91	92	93	94
	Auto-Negotiation	BASE-R FEC	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10	CAUI-4	100GBASE-CR10 PMD	RS-FEC	100GBASE-CR4 PMD	100GBASE-KR4 PMD	100GBASE-KP4 PMD
100GBASE-KR4	M		O	M	O	M	M	O	O		M		M	
100GBASE-KP4	M		O	M	O	M	O	O	O		M			M
100GBASE-CR4	M		O	M	O	M	M	O	O		M	M		
100GBASE-CR10	M	O	O	M	O	M	M	O	O	M				

^aO = Optional, M = Mandatory.

Table 80–2b—Nomenclature and clause correlation (100GBASE optical)

Nomenclature	Clause ^a														
	78	81		82	83	83A	83B	83D	83E	86	86A	88		91	95
	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10	CAUI-10	CAUI-4	CAUI-4	100GBASE-SR10 PMD	CPPI	100GBASE-LR4 PMD	100GBASE-ER4 PMD	RS-FEC	100GBASE-SR4 PMD
100GBASE-SR10	O	M	O	M	M	O	O	O	O	M	O				
100GBASE-SR4	O	M	O	M	M	O	O	O	O					M	M
100GBASE-LR4	O	M	O	M	M	O	O	O	O			M			
100GBASE-ER4	O	M	O	M	M	O	O	O	O				M		

^aO = Optional, M = Mandatory.

80.2 Summary of 40 Gigabit and 100 Gigabit Ethernet sublayers

80.2.3 Forward Error Correction (FEC) sublayers

Change the first paragraph of 80.2.3 (as modified by IEEE Std 802.3bj-2014) as follows:

A Forward Error Correction sublayer is available for all 40GBASE-R and 100GBASE-R copper and backplane PHYs as well as the 100GBASE-SR4 PHY. It is optional for 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10 PHYs and mandatory for 100GBASE-CR4, 100GBASE-KR4, ~~and 100GBASE-KP4,~~ and 100GBASE-SR4 PHYs.

80.2.5 Physical Medium Dependent (PMD) sublayer

Change the second paragraph of 80.2.5 (as modified by IEEE Std 802.3bj-2014) as follows:

The 40GBASE-R, 100GBASE-R, and 100GBASE-P PMDs and their corresponding media are specified in Clause 84 through Clause 89 and Clause 92 through ~~Clause 94~~ Clause 95.

80.4 Delay constraints

Change the second paragraph of 80.4 as follows:

See 44.3 for the calculation of bit time per meter of fiber or electrical cable. Equation (80–1) specifies the calculation of cable delay in nanoseconds per meter of fiber or electrical cable, based upon the parameter n , which represents the ratio of the speed of electromagnetic propagation in the fiber or electrical cable to the speed of light in a vacuum, $c = 3 \times 10^8$ m/s.

$$\text{cable delay} = \frac{10^9}{nc} \text{ ns/m} \quad (80-1)$$

The value of n should be available from the fiber or electrical cable manufacturer; but if no value is known, then a conservative delay estimate can be calculated using a default value of $n = 0.66$, which yields a default cable delay of 5 ns/m.

Insert a new row for 40GBASE-ER4 after 40GBASE-LR4 and a new row for 100GBASE-SR4 before 100GBASE-SR10 in Table 80–3 (as modified by IEEE Std 802.3bj-2014) as follows (unchanged rows not shown):

Table 80–3—Sublayer delay constraints

Sublayer	Maximum (bit time) ^a	Maximum (pause_quantum) ^b	Maximum (ns)	Notes ^c
40GBASE-ER4 PMD	1024	2	25.6	Includes 2 m of fiber. See 87.3.1.
...				
100GBASE-SR4 PMD	2048	4	20.48	Includes 2 m of fiber. See 95.3.1.

^a For 40GBASE-R, 1 bit time (BT) is equal to 25 ps and for 100GBASE-R, 1 bit time (BT) is equal to 10 ps. (See 1.4.110 for the definition of bit time.)

^b For 40GBASE-R, 1 pause_quantum is equal to 12.8 ns and for 100GBASE-R, 1 pause_quantum is equal to 5.12 ns. (See 31B.2 for the definition of pause_quantum.)

^c Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

80.5 Skew constraints

Change the third, fourth, and fifth paragraphs of 80.5 as follows:

The maximum Skew and Skew Variation at physically instantiated interfaces is specified at Skew points SP1, SP2, and SP3 for the transmit direction and SP4, SP5, and SP6 for the receive direction as illustrated in Figure 80–4 (single XLAUI or CAUI- $\underline{n}$ interface) and Figure 80–5 (multiple XLAUI or CAUI- $\underline{n}$ interfaces).

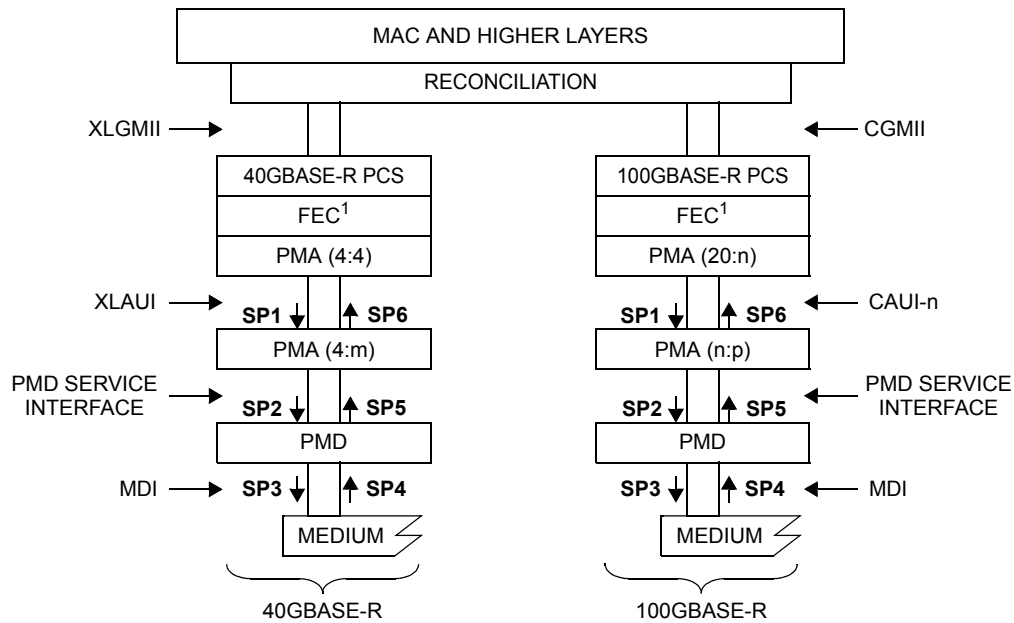
In the transmit direction, the Skew points are defined in the following locations:

- SP1 on the XLAUI/CAUI- $\underline{n}$ interface, at the input of the PMA closest to the PMD;
- SP2 on the PMD service interface, at the input of the PMD;
- SP3 at the output of the PMD, at the MDI.

In the receive direction, the Skew points are defined in the following locations:

- SP4 at the MDI, at the input of the PMD;
- SP5 on the PMD service interface, at the output of the PMD;
- SP6 on the XLAUI/CAUI- $\underline{n}$ interface, at the output of the PMA closest to the PCS.

Replace Figure 80–4, Figure 80–5, and Figure 80–5a (as modified or inserted by IEEE Std 802.3bj-2014) for CAUI naming as follows:

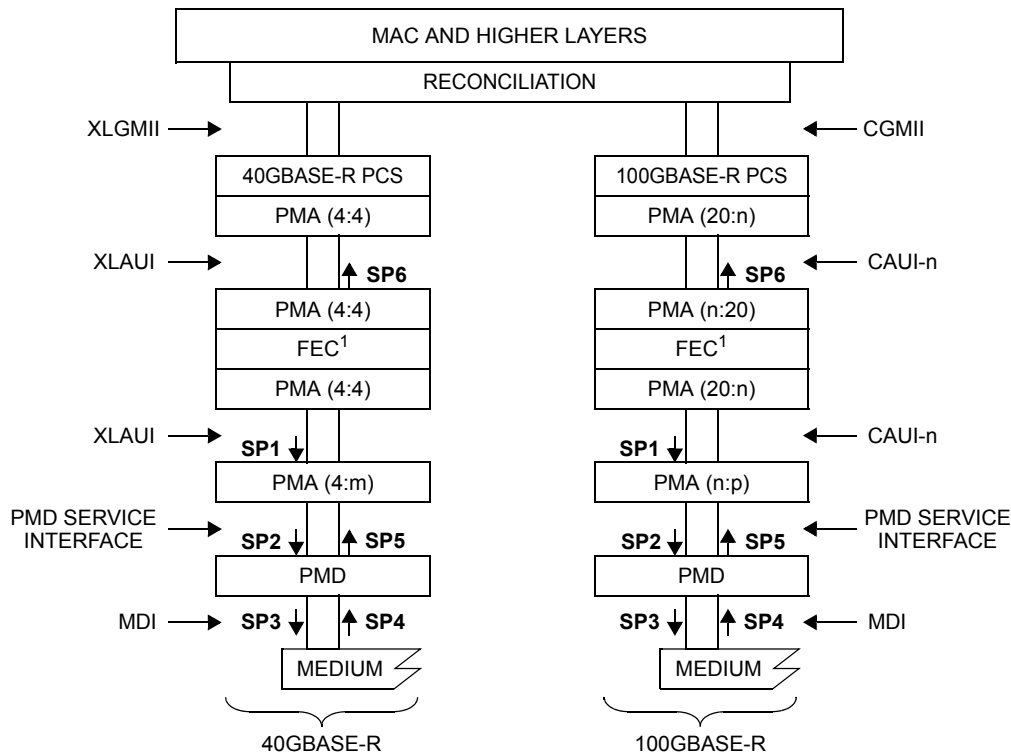


CAUI-n = 100 Gb/s ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

m = 1 or 4
n = 4 or 10
p = 4 or 10
NOTE1—CONDITIONAL BASED ON PHY TYPE

Figure 80–4—40GBASE-R and 100GBASE-R Skew points for single XLAUI or CAUI-n



CAUI-n = 100 Gb/s ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

m = 1 or 4
n = 4 or 10
p = 4 or 10

NOTE1—CONDITIONAL BASED ON PHY TYPE

Figure 80-5—40GBASE-R and 100GBASE-R Skew points for multiple XLAUI or CAUI-n