

IEEE Standard for Ethernet

Amendment 3: Physical Layers and Management Parameters for 25 Gb/s and 40 Gb/s Operation, Types 25GBASE-T and 40GBASE-T

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

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3 Park Avenue
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USA

IEEE Std 802.3bq™-2016
(Amendment to
IEEE Std 802.3™-2015
as amended by
IEEE Std 802.3bw™-2015, and
IEEE Std 802.3by™-2016)

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Abstract: This amendment to IEEE Std 802.3-2015 specifies new Physical Coding Sublayer (PCS) interfaces and new Physical Medium Attachment (PMA) sublayer interfaces for 25 Gb/s Ethernet and 40 Gb/s Ethernet. 25GBASE-T and 40GBASE-T specify LAN interconnects for up to 30 m of balanced twisted-pair structured cabling, for 25 Gb/s and 40 Gb/s, respectively.

Keywords: 25GBASE-T, 25 Gigabit Ethernet, 25GMII, 40GBASE-T, 40 Gigabit Ethernet, Auto-Negotiation, Ethernet, IEEE 802[®], IEEE 802.3[™], IEEE 802.3bq[™], Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, structured cabling, XLGMII

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Introduction

This introduction is not part of IEEE Std 802.3bq™-2016, IEEE Standard for Ethernet—Amendment 3: Physical Layer and Management Parameters for 25 Gb/s and 40 Gb/s Operation, Types 25GBASE-T and 40GBASE-T.

IEEE Std 802.3 was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel, and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile), and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the date of IEEE Std 802.3bq-2016 publication, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats, and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted-pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 109C, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

IEEE Std 802.3bq-2016

Amendment 3—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 113 and Annex 113A. This amendment adds new Physical Layers for 25 Gb/s and 40 Gb/s operation over balanced twisted-pair structured cabling systems.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 3: Physical Layer and Management Parameters for 25 Gb/s and 40 Gb/s Operation, Types 25GBASE-T and 40GBASE-T

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(This amendment is based on IEEE Std 802.3™-2015 as amended by IEEE Std 802.3bw™-2015 and IEEE Std 802.3by™-2016.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in **bold italic**. Four editing instructions are used: change, delete, insert, and replace. **Change** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strike through~~ (to remove old material) and underscore (to add new material). **Delete** removes existing material. **Insert** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. **Replace** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.¹

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

¹Notes in text, tables, and figures are given for information only, and do not contain requirements needed to implement the standard.

1. Introduction

1.3 Normative references

Insert the following references in alphanumeric order:

ANSI/TIA-568-C.2-1-2016, Balanced Twisted-Pair Telecommunications Cabling and Components Standard, Addendum 1: Specifications for 100 Ω Category 8 Cabling.²

ISO/IEC DIS 11801-1:2016, Information technology—Generic cabling for customer premises—Part 1: General Requirements.³

1.4 Definitions

Insert the 25GBASE-T definition after 1.4.64g 25GBASE-SR (added by IEEE Std 802.3by-2016) as follows:

1.4.64h 25GBASE-T: IEEE 802.3 Physical Layer specification for a 25 Gb/s LAN using four pairs of ANSI/TIA Category 8, ISO/IEC Class I, or ISO/IEC Class II balanced copper cabling. (See IEEE Std 802.3, Clause 113.)

Insert the 40GBASE-T definition after 1.4.72 40GBASE-SR4 as follows:

1.4.72a 40GBASE-T: IEEE 802.3 Physical Layer specification for a 40 Gb/s LAN using four pairs of ANSI/TIA Category 8, ISO/IEC Class I, or ISO/IEC Class II balanced copper cabling. (See IEEE Std 802.3, Clause 113.)

Insert the Category 8 balanced cabling definition after 1.4.131 Category 7A balanced cabling as follows:

1.4.131a Category 8 balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 2000 MHz (i.e., cabling components that meet the Category 8.1 or Category 8.2 requirements specified in ISO/IEC DIS 11801-1:2016 or Category 8 specified in ANSI/TIA-568-C.2-1-2016). In addition to the requirements outlined in ISO/IEC DIS 11801-1 and ANSI/TIA-568-C.2-1, IEEE Std 802.3 [Clause 14](#), [Clause 23](#), [Clause 25](#), [Clause 40](#), Clause 55, and Clause 113 specify additional requirements for this cabling when used with 10BASE-T, 100BASE-T, 10GBASE-T, 25GBASE-T, and 40GBASE-T.

Insert the Infocfield definition into the list after 1.4.237 in-band signaling and insert the MultiGBASE-T definition into the list after 1.4.277 mixing segment as follows:

1.4.237a Infocfield: A 16 octet frame transmitted at regular intervals containing messages for startup operation by certain PHYs. (See IEEE Std 802.3, Clause 55 and Clause 113).

1.4.277a MultiGBASE-T: PHYs that belong to the set of specific BASE-T PHYs at speeds in excess of 1000 Mb/s, including 10GBASE-T, 25GBASE-T, and 40GBASE-T. (See IEEE Std 802.3, Clause 55 and Clause 113).

²ANSI publications are available from the American National Standards Institute (<http://www.ansi.org>).

³ISO/IEC publications are available from the ISO Central Secretariat (<http://www.iso.org/>). ISO publications are also available in the United States from the American National Standards Institute (<http://www.ansi.org/>).

1.5 Abbreviations

Insert the following new abbreviation in alphanumeric order:

ACRF attenuation to crosstalk ratio, far-end

28. Physical Layer link signaling for Auto-Negotiation on twisted pair

28.3 State diagrams and variable definitions

28.3.1 State diagram variables

Insert rows for 25GigT and 40GigT in the first list in 28.3.1 below the row for 10GigT as follows:

25GigT;represents that the 25GBASE-T PMA is the signal source.

40GigT;represents that the 40GBASE-T PMA is the signal source.

28.3.2 State diagram timers

Change last sentence in the first paragraph of definition of link_fail_inhibit_timer as follows:

link_fail_inhibit_timer

Timer for qualifying a link_status=FAIL indication or a link_status=READY indication when a specific technology link is first being established. A link will only be considered “failed” if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The link_fail_inhibit_timer shall expire 750 ms to 1000 ms after entering the FLP LINK GOOD CHECK state for devices operating at 10/100/1000 Mb/s. The link_fail_inhibit_timer shall expire 2000 ms to 2250 ms after entering the FLP LINK GOOD CHECK state for devices ~~operating at 10 Gb/s in the MultiGBASE-T PHY set.~~

Change description for the link_fail_inhibit_timer (10 Gb/s devices) Parameter in Table 28–9 as follows (unchanged rows not shown):

Table 28–9—Timer min./max. value summary

Parameter	Min.	Typ.	Max.	Units
link_fail_inhibit_timer (~~10 Gb/s devices in the~~ MultiGBASE-T set)	2000		2250	ms

28.5 Protocol implementation conformance statement (PICS) proforma for Clause 28, Physical Layer link signaling for Auto-Negotiation on twisted pair⁴

28.5.3 Major capabilities/options

*Change row for *10G in 28.5.3 as follows (unchanged rows not shown):*

Item	Feature	Subclause	Status	Support	Value/Comment
* ~~40~~ <u>MG</u>	Implementation supports a <u>member of the MultiGBASE-T PHY set (see 1.4.277a)</u> ~~10GBASE-T PHY~~	<u>55 and</u>	O		N/A

⁴Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

28.5.4 PICS proforma tables for Physical Layer link signaling for Auto-Negotiation on twisted pair

28.5.4.8 State diagrams

Change rows for Items SD10 and SD11 in 28.5.4.8 as follows (unchanged rows not shown):

Item	Feature	Subclause	Status	Support	Value/Comment
SD10	link_fail_inhibit_timer (10/100/1000 Mb/s)	28.3.2	~~!40MG:~~ M		Expires 750 ms to 1000 ms after entering the FLP LINK GOOD CHECK state
SD11	link_fail_inhibit_timer (~~MultiGBASE-T devices~~ 10- Gb/s)	28.3.2	~~40MG:~~ M		Expires 2000 ms to 2250 ms after entering the FLP LINK GOOD CHECK state upon successful master/slave resolution

30. Management

30.2 Managed objects

30.2.5 Capabilities

Change column header from 10GBASE-T Operating Margin package (conditional) to MultiGBASE-T Operating Margin package (conditional) in Table 30-1e as follows (unchanged lines not shown):

Table 30-1e—Capabilities

			DTE	Repeater	MAU	
			Basic Package (mandatory)			
			Mandatory Package (mandatory)			
			Recommended Package (optional)			
			Optional Package (optional)			
			Array Package (optional)			
			Excessive Deferral Package (optional)			
			Multiple PHY Package (optional)			
			PHY Error Monitor Capability (optional)			
			Basic Control Capability (mandatory)			
			Performance Monitor Capability (optional)			
			Address Tracking Capability (optional)			
			100/1000 Mb/s Monitor Capability (optional)			
			1000 Mb/s Burst Monitor Capability (optional)			
			Basic Package (mandatory)			
			MAU Control Package (optional)			
			Media Loss Tracking Package (conditional)			
			Broadband DTE MAU Package (conditional)			
			MI Capability (conditional)			
			PHY Error Monitor Capability (optional)			
			40MultiGBASE-T Operating Margin package (conditional)			
			Forward Error Correction Package (conditional)			
			Energy-Efficient Ethernet (optional)			
			Auto-Negotiation Package (mandatory)			

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert new entries in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3bw-2015 and IEEE Std 802.3by-2016) after the entries for 25GBASE-R (25GBASE-T) and for 40GBASE-R (40GBASE-T) as follows:

25GBASE-T	Clause 113 25 Gb/s DSQ128
40GBASE-T	Clause 113 40 Gb/s DSQ128

30.3.2.1.3 aPhyTypeList

Insert new entries in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3bw-2015 and IEEE Std 802.3by-2016) after the entries for 25GBASE-R (25GBASE-T) and for 40GBASE-R (40GBASE-T) as follows:

25GBASE-T	Clause 113 25 Gb/s DSQ128
40GBASE-T	Clause 113 40 Gb/s DSQ128

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert new entries in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3bw-2015 and IEEE Std 802.3by-2016) after the entries for 25GBASE-SR (25GBASE-T) and for 40GBASE-FR (40GBASE-T) as follows:

25GBASE-T	Four-pair twisted-pair balanced copper cabling PHY as specified in Clause 113
40GBASE-T	Four-pair twisted-pair balanced copper cabling PHY as specified in Clause 113

30.5.1.1.4 aMediaAvailable

Change the sixth paragraph of BEHAVIOUR DEFINED AS (as modified by IEEE Std 802.3bw-2015 and IEEE Std 802.3by-2016) as follows:

For 40 Gb/s and 100 Gb/s the enumerations map to value of the link_fault variable (see 81.3.4) within the Link Fault Signaling state diagram (see 81.3.4.1 and Figure 46-11) as follows: the values OK and Link Interruption maps to the enumeration “available”, the value Local Fault maps to the enumeration “not available” and the value Remote Fault maps to the enumeration “remote fault.”

Change the eighth paragraph of BEHAVIOUR DEFINED AS (as modified by IEEE Std 802.3by-2016) as follows:

For 10 Gb/s and 25 Gb/s the enumerations map to value of the link_fault variable within the Link Fault Signaling state diagram (Figure 46-11) as follows: the values OK and Link Interruption maps to the enumeration “available”, the value Local Fault maps to the enumeration “not available” and the value Remote Fault maps to the enumeration “remote fault”.

30.5.1.1.19 aSNROpMarginChnIA

Change text to include both 25GBASE-T and 40GBASE-T (as part of the MultiGBASE-T operating package) as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current SNR operating margin measured at the slicer input for channel A for the ~~10GBASE-T~~ MultiGBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. If a [Clause 45](#) MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel A register (see 45.2.1.66).;

30.5.1.1.20 aSNROpMarginChnIB

Change text to include 25GBASE-T and 40GBASE-T (as part of the MultiGBASE-T operating package) as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:

The current SNR operating margin measured at the slicer input for channel B for the ~~10GBASE-T~~ MultiGBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel B register (see 45.2.1.67).;

30.5.1.1.21 aSNROpMarginChnIC

Change text to include 25GBASE-T and 40GBASE-T (as part of the MultiGBASE-T operating package) as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:

The current SNR operating margin measured at the slicer input for channel C for the ~~10GBASE-T~~ MultiGBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel C register (see 45.2.1.68).;

30.5.1.1.22 aSNROpMarginChnID

Change text to include 25GBASE-T and 40GBASE-T (as part of the MultiGBASE-T operating package) as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:

The current SNR operating margin measured at the slicer input for channel D for the ~~10GBASE-T~~ MultiGBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel D register (see 45.2.1.69).;

30.5.1.1.24 aLDFastRetrainCount

Change text of aLDFastRetrainCount to include 25GBASE-T and 40GBASE-T (as part of the Energy Efficient Ethernet package (optional)) as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1000 counts per second

BEHAVIOUR DEFINED AS:

A count of the number of ~~10GBASE-T~~ fast retrains initiated by the local device. ~~The indication reflects the state of the PHY event.~~ This counter can be derived from fr_tx_counter (see 45.2.1.79.2 and 55.4.5.4) and 113.4.5.4-). If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute can be derived from the LD fast retrain count register (see 45.2.1.79.2).;

30.5.1.1.25 aLPFastRetrainCount

Change text of aLPFastRetrainCount to include 25GBASE-T and 40GBASE-T (as part of the Energy Efficient Ethernet package (optional)) as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1000 counts per second

BEHAVIOUR DEFINED AS:

A count of the number of ~~10GBASE-T~~ fast retrains initiated by the link partner. ~~The indication reflects the state of the PHY event.~~ This counter can be derived from fr_rx_counter (see 45.2.1.79.1 and 55.4.5.4) and 113.4.5.4-). If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute can be derived from to the LP fast retrain count register (see 45.2.1.79.1).;

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert new entries in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3by-2016) after the entries for 10GBASE-KRFD (25GBASE-T) and for 40GBASE-CR4 (40GBASE-T) as follows:

25GBASE-T	25GBASE-T as specified in Clause 113
40GBASE-T	40GBASE-T as specified in Clause 113

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the names for register addresses 1.129 to 1.144, 1.145 through 1.146, and 1.147 in Table 45–3 as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.129	~~40~~ MultiGBASE-T status	45.2.1.62
1.130	~~40~~ MultiGBASE-T pair swap and polarity	45.2.1.63
1.131	~~40~~ MultiGBASE-T TX power backoff and PHY short reach setting	45.2.1.64
1.132	~~40~~ MultiGBASE-T test mode	45.2.1.65
1.133	~~40~~ GBASE-T SNR operating margin channel A	45.2.1.66
1.134	~~40~~ GBASE-T SNR operating margin channel B	45.2.1.67
1.135	~~40~~ GBASE-T SNR operating margin channel C	45.2.1.68
1.136	~~40~~ GBASE-T SNR operating margin channel D	45.2.1.69
1.137	~~40~~ GBASE-T ~~m~~ Minimum margin channel A	45.2.1.70
1.138	~~40~~ GBASE-T ~~m~~ Minimum margin channel B	45.2.1.71
1.139	~~40~~ GBASE-T ~~m~~ Minimum margin channel C	45.2.1.72
1.140	~~40~~ GBASE-T ~~m~~ Minimum margin channel D	45.2.1.73
1.141	~~40~~ GBASE-T RX signal power channel A	45.2.1.74
1.142	~~40~~ GBASE-T RX signal power channel B	45.2.1.75
1.143	~~40~~ GBASE-T RX signal power channel C	45.2.1.76
1.144	~~40~~ GBASE-T RX signal power channel D	45.2.1.77
1.145 through 1.146	~~40~~ MultiGBASE-T skew delay	45.2.1.78
1.147	~~40~~ MultiGBASE-T fast retrain status and control register	45.2.1.79

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change the indicated two reserved rows and insert four new rows (two of which are reserved) in alphanumeric order in the 1.7.5:0 row of Table 45-7 (as modified by IEEE Std 802.3bw-2015 and IEEE Std 802.3by-2016), as follows (unchanged rows not shown):

Table 45-7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.7.5:0	PMA/PMD type selection	<u>1 1 0 1 1 1 = 25GBASE-T PMA</u> <u>1 1 0 1 1 0 = reserved</u> <u>1 1 0 1 0 x = reserved</u> <u>1 1 0 x x x = reserved for future use</u> <u>1 0 0 1 1 x = reserved</u> <u>1 0 0 1 1 0 = 40GBASE-T PMA</u>	R/W

^aR/W = Read/Write, RO = Read only

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Insert description locations for 25GBASE-T after 25GBASE-SR (see IEEE Std 802.3by-2016) and before 40GBASE-KR4 and description for 40GBASE-T after the row for 40GBASE-FR in Table 45-9 as follows (unchanged rows not shown):

Table 45-9—Transmit fault description location

PMA/PMD	Description location
<u>25GBASE-T</u>	<u>113.4.2.2</u>
<u>40GBASE-T</u>	<u>113.4.2.2</u>

45.2.1.7.5 Receive fault (1.8.10)

Insert description locations for 25GBASE-T after 25GBASE-SR (see IEEE Std 802.3by-2016) and before 40GBASE-KR4 and description for 40GBASE-T after the row for 40GBASE-FR in Table 45-10 as follows (unchanged rows not shown):

Table 45-10—Receive fault description location

PMA/PMD	Description location
<u>25GBASE-T</u>	<u>113.4.2.4</u>
<u>40GBASE-T</u>	<u>113.4.2.4</u>

45.2.1.8 PMD transmit disable register (Register 1.9)

Insert description location for 25GBASE-T after row for 25GBASE-SR (see IEEE Std 802.3by-2016) and before 40GBASE-KR and 40GBASE-T after the row for 40GBASE-FR in Table 45–12 as follows (unchanged rows not shown):

Table 45–12—Transmit disable description location

PMA/PMD	Description location
25GBASE-T	113.4.2.3
40GBASE-T	113.4.2.3

45.2.1.12 40G/100G PMA/PMD extended ability register (Register 1.13)

Change the name and description for bit 1.13.6 in Table 45–16 as follows (unchanged rows not shown):

Table 45–16—40G/100G PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.13.6	~~Reserved~~ 40GBASE-T ability	~~Value always 0~~ 1 = PMA/PMD is able to perform 40GBASE-T 0 = PMA/PMD is not able to perform 40GBASE-T	RO

^aRO = Read only

45.2.1.9a 40GBASE-T ability (1.13.6)

Insert 45.2.1.12.9a after 45.2.1.12.9 as follows:

When read as a one, bit 1.13.6 indicates that the PMA/PMD is able to operate as a 40GBASE-T PMA type.
When read as a zero, bit 1.13.6 indicates that the PMA/PMD is not able to operate as a 40GBASE-T PMA type.

45.2.1.14b 25G PMA/PMD extended ability register (Register 1.19)

Change the reserved row, and insert a row below it with the description for bit 1.19.5 in Table 45–17bb (inserted by IEEE Std 802.3by-2016) as follows (unchanged rows not shown):

Table 45–17b—25G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.19.15:6 5	Reserved	Value always 0	RO
1.19.5	25GBASE-T ability	1 = PMA/PMD is able to perform 25GBASE-T 0 = PMA/PMD is not able to perform 25GBASE-T	RO

^aRO = Read only

45.2.1.14b.a 25GBASE-T ability (1.19.5)

Insert 45.2.1.14b.a before 45.2.1.14b.1 (inserted by IEEE Std 802.3by-2016) as follows:

When read as a one, bit 1.19.5 indicates that the PMA/PMD is able to operate as a 25GBASE-T PMA type. When read as a zero, bit 1.19.5 indicates that the PMA/PMD is not able to operate as a 25GBASE-T PMA type.

Change the title and text of 45.2.1.62 to include 25GBASE-T and 40GBASE-T as follows:

45.2.1.62 40MultiGBASE-T status (Register 1.129)

The assignments of bits in the 40MultiGBASE-T status register is shown in Table 45–54.

45.2.1.62.1 LP information valid (1.129.0)

Change the text of 45.2.1.62.1 to include 25GBASE-T and 40GBASE-T as follows:

When read as a one, bit 1.129.0 indicates that the startup protocol defined in 55.4.2.5 (for 10GBASE-T) or 113.4.2.5 (for 25G/40GBASE-T) has been completed, and that the contents of bits 1.130.11:0, 1.131.15:10, 1.145.14:8, 1.146.14:8, and 1.146.6:0, which are established during the startup protocol, are valid. When read as a zero, bit 1.129.0 indicates that the startup process has not been completed, and that the contents of these bits that are established during the startup protocol are invalid. A 40GBASE-T PMA in the MultiG-BASE-T set shall return a value of zero in bit 1.129.1 if PMA link_status=FAIL.

Change title of Table 45–54 to include 25GBASE-T and 40GBASE-T as follows:

Table 45–54—40MultiGBASE-T status register bit definitions

Change the title of 45.2.1.63 to include 25GBASE-T and 40GBASE-T as follows:

45.2.1.63 40MultiGBASE-T pair swap and polarity register (Register 1.130)

Change the title in Table 45–55 to include 25GBASE-T and 40GBASE-T as follows:

Table 45–55—40MultiGBASE-T pair swap and polarity register bit definitions

Change the title and text of 45.2.1.64 to include 25GBASE-T and 40GBASE-T as follows:

45.2.1.64 ~~40~~MultiGBASE-T TX power backoff and PHY short reach setting (Register 1.131)

The complete assignment of bits in the ~~40~~MultiGBASE-T TX power backoff and short reach mode settings register is shown in Table 45–56.

Change the title in Table 45–56 to include 25GBASE-T and 40GBASE-T as follows:

Table 45–56—~~40~~MultiGBASE-T TX power backoff and PHY short reach setting register bit definitions

Change the title and text of 45.2.1.64.1 to include 25GBASE-T and 40GBASE-T as follows:

45.2.1.64.1 ~~40~~MultiGBASE-T TX power backoff settings (1.131.15:10)

The ~~40~~MultiGBASE-T TX power backoff settings reflects the TX power backoff selected during the startup negotiation process. The 10GBASE-T startup negotiation process and all TX power backoff settings are defined in 55.4.2.5 and 55.4.5.1. The 25GBASE-T and 40GBASE-T startup negotiation process and all TX power backoff settings are defined in 113.4.2.5 and 113.4.5.1. If LP information valid bit, 1.129.0, is set to one then bits 1.131.15:13 indicates the TX power backoff setting of the link partner and bits 1.131.12:10 indicates the TX power backoff setting of the local device.

45.2.1.64.2 PHY short reach mode (1.131.0)

Change the text of 45.2.1.64.2 to include 25GBASE-T and 40GBASE-T as follows:

The short reach mode of the 10GBASE-T PHY provides a means for operation on a cable plant that has parametric performance equivalent to 30 m of Class F and Class EA cabling as defined in 55.5.4.5. The short reach mode of the 25GBASE-T and 40GBASE-T PHYs provides for operation on a direct attach link segment that has parametric performance defined in 113.7.4. If bit 1.131.0 is a one, the PHY is in short reach mode. If bit 1.131.0 is a zero, the PHY is not in short reach mode; the PHY is operating in normal mode. The default value for this bit is zero. For 25GBASE-T and 40GBASE-T, setting this bit to a one puts the PHY in short reach mode, and setting this bit to a zero puts the PHY into normal (non-short reach) mode.

Change the title and text of 45.2.1.65 to include 25GBASE-T and 40GBASE-T as follows:

45.2.1.65 ~~40~~MultiGBASE-T test mode register (Register 1.132)

The assignment of bits in the ~~40~~MultiGBASE-T test mode register is shown in Table 45–57. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Change the title in Table 45–57 to include 25GBASE-T and 40GBASE-T as follows:

Table 45–57—~~40~~MultiGBASE-T test mode register bit definitions

Change text of 45.2.1.65.1 and 45.2.1.65.2 to include references to 25G/40GBASE-T and Clause 113 as follows:

45.2.1.65.1 Test mode control (1.132.15:13)

Transmitter test mode operations defined by bits 1.132.15:13, are described for 10GBASE-T in 55.5.2 and Table 55–12, and for 25G/40GBASE-T in 113.5.2 and Table 113–17. The default value for bits 1.132.15:13 is zero.

45.2.1.65.2 Transmitter test frequencies (1.132.12:10)

When test mode 4 is selected by setting bits 1.132.15:13 to one, zero, zero respectively, bits 1.132.12:10 select the transmit test frequency as shown in Table 45–57. Detailed use and operation of these transmitter test frequencies is described in 55.5.2 and 113.5.2.

45.2.1.66 SNR operating margin channel A register (Register 1.133)

Change the text of 45.2.1.66 to include 25GBASE-T and 40GBASE-T as follows:

Register 1.133 contains the current SNR operating margin measured at the slicer input for channel A for the 10GBASE-T PMA_s in the MultiGBASE-T set. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.67 SNR operating margin channel B register (Register 1.134)

Change the text of 45.2.1.67 to include 25GBASE-T and 40GBASE-T as follows:

Register 1.134 contains the current SNR operating margin measured at the slicer input for channel B for the 10GBASE-T PMA_s in the MultiGBASE-T set. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.68 SNR operating margin channel C register (Register 1.135)

Change the text of 45.2.1.68 to include 25GBASE-T and 40GBASE-T as follows:

Register 1.135 contains the current SNR operating margin measured at the slicer input for channel C for the 10GBASE-T PMA_s in the MultiGBASE-T set. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.69 SNR operating margin channel D register (Register 1.136)

Change the text of 45.2.1.69 to include 25GBASE-T and 40GBASE-T as follows:

Register 1.136 contains the current SNR operating margin measured at the slicer input for channel D for the 10GBASE-T PMA_s in the MultiGBASE-T set. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.74 RX signal power channel A register (Register 1.141)

Change the text of 45.2.1.74 to include 25GBASE-T and 40GBASE-T as follows:

The RX signal power channel A register is read only and contains the receive signal power measured at the MDI during training as described in [55.4.3.1](#) and [113.4.3.1](#). The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or MA_Training_Init_S (as appropriate, see [55.4.6.1](#) and [113.4.6.1](#)), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.75 RX signal power channel B register (Register 1.142)

Change the text of 45.2.1.75 to include 25GBASE-T and 40GBASE-T as follows:

The RX signal power channel B register is read only and contains the receive signal power measured at the MDI during training as described in [55.4.3.1](#) and [113.4.3.1](#). The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or MA_Training_Init_S (as appropriate, see [55.4.6.1](#) and [113.4.6.1](#)), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.76 RX signal power channel C register (Register 1.143)

Change the text of 45.2.1.76 to include 25GBASE-T and 40GBASE-T as follows:

The RX signal power channel C register is read only and contains the receive signal power measured at the MDI during training as described in [55.4.3.1](#) and [113.4.3.1](#). The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or MA_Training_Init_S (as appropriate, see [55.4.6.1](#) and [113.4.6.1](#)), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.77 RX signal power channel D register (Register 1.144)

Change the text of 45.2.1.77 to include 25GBASE-T and 40GBASE-T as follows:

The RX signal power channel D register is read only and contains the receive signal power measured at the MDI during training as described in [55.4.3.1](#) and [113.4.3.1](#). The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or MA_Training_Init_S (as appropriate, see [55.4.6.1](#) and [113.4.6.1](#)), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

Change the title and text of 45.2.1.78 to include 25GBASE-T and 40GBASE-T as follows:

45.2.1.78 ~~40~~MultiGBASE-T skew delay register (Registers 1.145 and 1.146)

The skew delay register reports the current skew delay on each of the pair with respect to physical pair A (see Table 45–58). It is reported with ~~1.25 ns~~ resolution to an accuracy of 2.5 ns equal to one symbol period

(see [55.1.3](#) and [113.1.2](#)) of the PHY (e.g., 1.25 ns for 10GBASE-T) to an accuracy of two symbol periods (e.g., 2.5 ns for 10GBASE-T). The number reported is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceeds the maximum amount that can be represented by the range (−64 symbols to +63 symbols)~~−80 ns to +78.75 ns~~, the field displays the maximum respective value. The value shall be updated at least once per second.

Change title of Table 45–58 to include 25GBASE-T and 40GBASE-T.

Table 45–58—~~40~~MultiGBASE-T skew delay register bit definitions

Change the title of 45.2.1.79 to include 25GBASE-T and 40GBASE-T as follows:

45.2.1.79 ~~40~~MultiGBASE-T fast retrain status and control register (Register 1.147)

Change the title of Table 45–59 to include 25GBASE-T and 40GBASE-T as follows

Table 45–59—~~40~~MultiGBASE-T fast retrain status and control register bit definitions

45.2.1.79.1 LP fast retrain count (1.147.15:11)

Change the text of 45.2.1.79.1 to include 25GBASE-T and 40GBASE-T as follows:

These bits map to fr_rx_counter as defined in [55.4.5.4](#)~~4~~ for 10GBASE-T and [113.4.5.4](#) for 25GBASE-T and 40GBASE-T. The counter is a 5-bit count of the number of ~~10GBASE-T~~ fast retrains requested by the link partner. These bits shall be reset to all zeros when read or upon execution of the PMA reset. These bits shall be held at all ones in the case of overflow.

45.2.1.79.2 LD fast retrain count (1.147.10:6)

Change the text of 45.2.1.79.2 to include 25GBASE-T and 40GBASE-T as follows:

These bits map to fr_tx_counter as defined in [55.4.5.4](#)~~4~~ for 10GBASE-T and [113.4.5.4](#) for 25GBASE-T and 40GBASE-T. The counter is a 5-bit count of the number of ~~10GBASE-T~~ fast retrains requested by the local device. These bits shall be reset to all zeros when read or upon execution of the PMA reset. These bits shall be held at all ones in the case of overflow.

45.2.1.79.5 Fast retrain signal type (1.147.2:1)

Change the text of 45.2.1.79.5 to add reference to 113.3.6.2.2 as follows:

For PHYs that support fast retrain, these bits map to fr_sigtype as defined in [55.3.6.2.2](#) and [113.3.6.2.2](#). When Fast retrain signal type is set to 00, the PMA sends IDLE characters on the receive path during fast retrain. When Fast retrain signal type is set to 01, the PMA sends Local Fault on the receive path during fast retrain. When Fast retrain signal type is set to 10, the PMA sends Link Interruption on the receive path during fast retrain.

45.2.1.79.6 Fast retrain enable (1.147.0)

Change the text of 45.2.1.79.6 to add reference to 113.4.5.1 as follows:

For PHYs that support fast retrain, this bit controls fr_enable as defined in [55.4.5.1](#) and [113.4.5.1](#). When PMA reset is executed, this bit is set to one.

NOTE—Setting this bit to zero while a link is up will cause the PHY to stop supporting fast retrain, and the link will drop if the link partner initiates a fast retrain.

45.2.3 PCS registers

Change the names of register addresses 3.20, 3.21, 3.32 and 3.33 in Table 45–119 as follows (unchanged rows not shown):

Table 45–119—PCS registers

Register address	Register name	Subclause
3.20	EEE control and capability 1	45.2.3.9
3.21	~~Reserved~~ EEE control and capability 2	~~45.2.3.9a~~
3.32	BASE-R and ~~40~~ MultiGBASE-T PCS status 1	45.2.3.13
3.33	BASE-R and ~~40~~ MultiGBASE-T PCS status 2	45.2.3.14

45.2.3.1 PCS control 1 register (Register 3.0)

45.2.3.1.2 Loopback (3.0.14)

Change the text of 45.2.3.1.2 to include 25GBASE-T and 40GBASE-T as follows:

When ~~the 10GBASE-T~~ any MultiGBASE-T or the 10GBASE-R mode of operation is selected for the PCS using the PCS type selection field (3.7.23:0), the PCS shall be placed in a loopback mode of operation when bit 3.0.14 is set to a one. When bit 3.0.14 is set to a one, the 10GBASE-R or ~~10GBASE-T~~ any PCS in the MultiGBASE-T set shall accept data on the transmit path and return it on the receive path. The speed of the loopback is selected by the PCS control 1 (Register 3.0) defined in 45.2.3.1. The specific behavior of the 10GBASE-R PCS during loopback is specified in 49.2. The specific behavior for the 10GBASE-T PCS during loopback is specified in 55.3.7.3. The specific behavior for the 25GBASE-T and 40GBASE-T PCS during loopback is specified in 113.3.7.3. For all other port types, the PCS loopback functionality is not applicable and writes to this bit shall be ignored and reads from this bit shall return a value of zero.

45.2.3.2 PCS status 1 register (Register 3.1)

45.2.3.2.7 PCS receive link status (3.1.2)

Change the text of 45.2.3.2.7 to include 25GBASE-T and 40GBASE-T as follows:

When read as a one, bit 3.1.2 indicates that the PCS receive link is up. When read as a zero, bit 3.1.2 indicates that the PCS receive link is down. When a 10/40/100GBASE-R, 10GBASE-W, or ~~10GBASE-T~~ any MultiGBASE-T mode of operation is selected for the PCS using the PCS type selection field (3.7.23:0), this bit is a latching low version of bit 3.32.12. When a 10GBASE-X mode of operation is selected for the PCS using the PCS type selection field (3.7.23:0), this bit is a latching low version of bit 3.24.12. The receive link status bit shall be implemented with latching low behavior.

45.2.3.6 PCS control 2 register (Register 3.7)

Change Table 45–123 (as modified by IEEE Std 802.3by-2016) as follows:

Table 45–123—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.7:15:34	Reserved	Value always 0	RO
3.7.23:0	PCS type selection	3 2 1 0 1 1 x x= reserved 1 0 1 x= reserved 1 0 0 1= Select 25GBASE-T PCS type 1 0 0 0= reserved 0 1 1 1= Select 25GBASE-R PCS type 0 1 1 0= reservedSelect 40GBASE-T PCS type 0 1 0 1= Select 100GBASE-R PCS type 0 1 0 0= Select 40GBASE-R PCS type 0 0 1 1= Select 10GBASE-T PCS type 0 0 1 0= Select 10GBASE-W PCS type 0 0 0 1= Select 10GBASE-X PCS type 0 0 0 0= Select 10GBASE-R PCS type	R/W

^aR/W = Read/Write, RO = Read only

45.2.3.6.1 PCS type selection (3.7.23:0)

Change the title and text of 45.2.3.6.1 (as modified by IEEE Std 802.3by-2016) to include revised PCS selection bits as follows:

The PCS type shall be selected using bits 23 through 0. The PCS type abilities of the PCS are advertised in bits 3.8.9 and 3.8.7:0. A PCS shall ignore writes to the PCS type selection bits that select PCS types it has not advertised in the PCS status 2 register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY. The PCS type selection defaults to a supported ability.

45.2.3.7 PCS status 2 register (Register 3.8)

Change the reserved row in Table 45–124 (as modified by IEEE Std 802.3by-2016) as shown below, insert a new row for name and description for bit 3.8.9 above the reserved row, and change the reserved row 3.8.6 (as inserted by IEEE Std 802.3by-2016) as follows (unchanged rows not shown):

Table 45–124—PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.8.9	25GBASE-T capable	1 = PCS is able to support 25GBASE-T PCS type 0 = PCS is not able to support 25GBASE-T PCS type	RO
3.8.9:8	Reserved	Value always 0	RO
3.8.6	~~Reserved~~ 40GBASE-T capable	~~Value always 0~~ 1 = PCS is able to support 40GBASE-T PCS type 0 = PCS is not able to support 40GBASE-T PCS type	RO

^aRO = Read only, LH = Latching high

Insert 45.2.3.7.3aa after 45.2.3.7.3 and before 45.2.3.7.3a (as inserted by IEEE Std 802.3by-2016) as follows:

45.2.3.7.3aa 25GBASE-T capable (3.8.9)

When read as a one, bit 3.8.9 indicates that the PCS is able to support the 25GBASE-T PCS type. When read as a zero, bit 3.8.9 indicates that the PCS is not able to support the 25GBASE-T PCS type.

Insert 45.2.3.7.3b after 45.2.3.7.3a (as inserted by IEEE Std 802.3by-2016) as follows:

45.2.3.7.3b 40GBASE-T capable (3.8.6)

When read as a one, bit 3.8.6 indicates that the PCS is able to support the 40GBASE-T PCS type. When read as a zero, bit 3.8.6 indicates that the PCS is not able to support the 40GBASE-T PCS type.

Change the name of Register 3.20 in title and text as shown:

45.2.3.9 EEE control and capability 1 (Register 3.20)

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type. The assignment of bits in the EEE control and capability 1 register is shown in Table 45–125.

Change the title of Table 45-125, and the name and definition of bit 3.20.7 as follows (unchanged rows not shown):

Table 45-125—EEE control and capability 1 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.20.7	~~Reserved~~ 40GBASE-T EEE	~~Value always 0~~ = EEE is supported for 40GBASE-T 0 = EEE is not supported for 40GBASE-T	RO

^a Read/Write, RO = Read only

Insert 45.2.3.9.4a after 45.2.3.9.4 as follows:

45.2.3.9.4a 40GBASE-T EEE supported (3.20.7)

If the device supports EEE operation for 40GBASE-T as defined in 113.1.3.3, this bit shall be set to one.

Insert 45.2.3.9a, Table 45-125a, and 45.2.3.9a.1 after 45.2.3.9 as follows:

45.2.3.9a EEE control and capability 2 (Register 3.21)

Register 3.21 extends register 3.20 and is used to indicate the capability of the PCS to support EEE functions for each PHY type. The assignment of bits in the EEE control and capability 2 register is shown in Table 45-125a.

Table 45-125a—EEE control and capability 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.21.15:3	Reserved	Value always 0	RO
3.21.2	25GBASE-T EEE	1 = EEE is supported for 25GBASE-T 0 = EEE is not supported for 25GBASE-T	RO
3.21.1:0	Reserved	Value always 0	RO

^a Read/Write, RO = Read only

45.2.3.9a.1 25GBASE-T EEE supported (3.21.2)

If the device supports EEE operation for 25GBASE-T as defined in 113.1.3.3, this bit shall be set to one.

45.2.3.13 BASE-R and 40MultiGBASE-T PCS status 1 register (Register 3.32)

Change the title and text of 45.2.3.13 to include 25GBASE-T and 40GBASE-T as follows:

The assignment of bits in the BASE-R and 40MultiGBASE-T PCS status 1 register is shown in Table 45-128. All the bits in the BASE-R and 40MultiGBASE-T PCS status 1 register are read only; a write to the BASE-R and 40MultiGBASE-T PCS status 1 register shall have no effect. A PCS device that ~~does not~~ implements neither BASE-R and 10GBASE-T nor any member of the MultiGBASE-T set shall return a zero for all bits in the BASE-R and 40MultiGBASE-T PCS status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The

contents of register 3.32 are undefined when the BASE-R-PCS or MultiGBASE-T the ~~10GBASE-T~~ PCS is operating in seed test-pattern mode, PRBS31 test-pattern mode, or PRBS9 test-pattern mode.

Change the title and names and descriptions of bits 3.32.12, 3.32.1, and 3.32.0 rows in Table 45–128 as follows (unchanged bits not shown):

Table 45–128—BASE-R and ~~40~~MultiGBASE-T PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.32.12	BASE-R and ~~40~~ <u>Multi</u> G-BASE-T receive link status	1 = BASE-R or ~~40~~ <u>Multi</u> GBASE-T any <u>MultiGBASE-T</u> PCS receive link up 0 = BASE-R or ~~40~~ <u>Multi</u> GBASE-T any <u>MultiGBASE-T</u> PCS receive link down	RO
3.32.1	BASE-R and ~~40~~ <u>Multi</u> G-BASE-T PCS high BER	1 = BASE-R or ~~40~~ <u>Multi</u> GBASE-T any <u>MultiGBASE-T</u> PCS reporting a high BER 0 = BASE-R or ~~40~~ <u>Multi</u> GBASE-T any <u>MultiGBASE-T</u> PCS not reporting a high BER	RO
3.32.0	BASE-R and ~~40~~ <u>Multi</u> G-BASE-T PCS block lock	1 = BASE-R or ~~40~~ <u>Multi</u> GBASE-T any <u>MultiGBASE-T</u> PCS locked to received blocks 0 = BASE-R or ~~40~~ <u>Multi</u> GBASE-T any <u>MultiGBASE-T</u> PCS not locked to received blocks	RO

^aRO = Read only

45.2.3.13.1 BASE-R and ~~40~~MultiGBASE-T receive link status (3.32.12)

Change the title and text of 45.2.3.13.1 to include 25GBASE-T and 40GBASE-T as follows:

When read as a one, bit 3.32.12 indicates that the PCS is in a fully operational state. When read as a zero, bit 3.32.12 indicates that the PCS is not fully operational. This bit is a reflection of the PCS_status variable defined in 49.2.14.1 for 10GBASE-R, in 55.3.6.1 for 10GBASE-T, in 113.3.7.1 for 25GBASE-T and 40GBASE-T, and in 82.3.1 for 40/100GBASE-R.

45.2.3.13.4 BASE-R and ~~40~~MultiGBASE-T PCS high BER (3.32.1)

Change the title and text of 45.2.3.13.4 to include 25GBASE-T and 40GBASE-T as follows:

For BASE-R, when read as a one, bit 3.32.1 indicates that the 64B/66B receiver is detecting a BER of $\geq 10^{-4}$. When read as a zero, bit 3.32.1 indicates that the 64B/66B receiver is detecting a BER of $< 10^{-4}$. This bit is a direct reflection of the state of the hi_ber variable in the 64B/66B state diagram and is defined in 49.2.13.2.2 for 10GBASE-R and in 82.2.19.2.2 for 40/100GBASE-R.

For ~~40~~MultiGBASE-T any member of the MultiGBASE-T set, when read as a one, bit 3.32.1 indicates that the 64B/65B receiver is detecting a BER of $\geq 10^{-4}$. When read as a zero, bit 3.32.1 indicates that the 64B/65B receiver is detecting a BER of $< 10^{-4}$. This bit is a direct reflection of the state of the hi_lfr variable in the MultiGBASE-T 64B/65B state diagrams, and is defined in 55.3.6.1 for 10GBASE-T and 113.3.6.2.2 for 25GBASE-T and 40GBASE-T.

Change the title and text of 45.2.3.13.5 to include 25GBASE-T and 40GBASE-T as follows:

45.2.3.13.5 BASE-R and ~~40~~MultiGBASE-T block lock (3.32.0)

When read as a one, bit 3.32.0 indicates that the 64B/66B receiver for BASE-R or the 64B/65B receiver for the ~~10GBASE-T~~ a member of the MultiGBASE-T set has block lock. When read as a zero, bit 3.32.0 indicates that the 64B/66B receiver for BASE-R or the 64B/65B receiver for the ~~10GBASE-T~~ member of the MultiGBASE-T set has not achieved block lock. This bit is a direct reflection of the state of the block_lock variable in the 64B/66B state diagram and is defined in 49.2.13.2.2 for 10GBASE-R and in 82.2.19.2.2 for 40/100GBASE-R. For the 10GBASE-T PCS the block_lock variable in the 64B/65B state diagram is defined in 55.3.2.3. For both the 25GBASE-T and 40GBASE-T PCS, the block_lock variable in the 64B/65B state diagram is defined in 113.3.6.2.2. For a multi-lane PCS, this bit indicates that the receiver has both block lock and alignment for all lanes and is identical to 3.50.12 (see 45.2.3.21.1).

Change the title and text of 45.2.3.14 to include 25GBASE-T and 40GBASE-T as follows:

45.2.3.14 BASE-R and ~~40~~MultiGBASE-T PCS status 2 register (Register 3.33)

The assignment of bits in the BASE-R and ~~40~~MultiGBASE-T PCS status 2 register is shown in Table 45–129. All the bits in the BASE-R and ~~40~~MultiGBASE-T PCS status 2 register are read only; a write to the BASE-R and ~~40~~MultiGBASE-T PCS status 2 register shall have no effect. A PCS device that ~~does not~~ implements neither BASE-R and ~~10GBASE-T~~ nor any member of the MultiGBASE-T set shall return a zero for all bits in the BASE-R and ~~40~~MultiGBASE-T PCS status 2 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.33 are undefined when the BASE-R or the ~~40GBASE-T~~MultiGBASE-T set PCS is operating seed test-pattern mode, PRBS31 test-pattern mode, or PRBS9 test-pattern mode.

Change the title and descriptions of bits 3.33.15 and 3.33.14 in Table 45–129 as follows (unchanged bits not shown):

Table 45–129—BASE-R and ~~40~~MultiGBASE-T PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.33.15	Latched block lock	1 = BASE-R or ~~40GBASE-T~~ any MultiGBASE-T PCS has block lock 0 = BASE-R or ~~40GBASE-T~~ any MultiGBASE-T PCS does not have block lock	RO/LL
3.33.14	Latched high BER	1 = BASE-R or ~~40GBASE-T~~ any MultiGBASE-T PCS has reported a high BER 0 = BASE-R or ~~40GBASE-T~~ any MultiGBASE-T PCS has not reported a high BER	RO/LH

^aRO = Read only, LL = Latching low, LH = Latching high, NR = Non Roll-over

45.2.3.14.1 Latched block lock (3.33.15)

Change the text of 45.2.3.14.1 to include 25GBASE-T and 40GBASE-T as follows:

When read as a one, bit 3.33.15 indicates that the 10/40/100GBASE-R or the ~~10GBASE-T~~ a member of the MultiGBASE-T set PCS has achieved block lock. When read as a zero, bit 3.33.15 indicates that the 10/40/100GBASE-R or the ~~10GBASE-T~~ a member of the MultiGBASE-T set PCS has lost block lock.

The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 10/40/100GBASE-R and ~~10~~MultiGBASE-T PCS block lock status bit (3.32.0).

45.2.3.14.2 Latched high BER (3.33.14)

Change the text of 45.2.3.14.2 to include 25GBASE-T and 40GBASE-T as follows:

When read as a one, bit 3.33.14 indicates that the 10/40/100GBASE-R or ~~the 10GBASE-T~~ a member of the MultiGBASE-T set PCS has detected a high BER. When read as a zero, bit 3.33.14 indicates that the 10/40/100GBASE-R or ~~the 10GBASE-T~~ a member of the MultiGBASE-T set PCS has not detected a high BER.

The latched high BER bit shall be implemented with latching high behavior.

This bit is a latching high version of the 10/40/100GBASE-R and ~~10~~MultiGBASE-T PCS high BER status bit (3.32.1).

45.2.3.14.3 BER (3.33.13:8)

Change the text of 45.2.3.14.3 to include 25GBASE-T and 40GBASE-T as follows:

The BER counter is a six bit count as defined by the ber_count variable in 49.2.14.2 and 82.2.19.2.4 for 10/40/100GBASE-R and defined by ~~the counter lfer_count variable~~ in 55.3.6.2 for 10GBASE-T and in 113.3.6.2.2 for 25GBASE-T and 40GBASE-T. These bits shall be reset to all zeros when the BASE-R and ~~10~~MultiGBASE-T PCS status 2 register is read by the management function or upon execution of the PCS reset. If the BER high order counter, 3.44 (see 45.2.3.23) is not implemented then these bits shall be held at all ones in the case of overflow.

45.2.3.14.4 Errored blocks (3.33.7:0)

Change the text of 45.2.3.14.4 to include 25GBASE-T and 40GBASE-T as follows:

The errored blocks counter is an eight bit count defined by the errored_block_count counter specified in 49.2.14.2 for 10GBASE-R, in 82.3.1 for 40/100GBASE-R and defined by ~~the counter~~ errored_block_count variable in 55.3.6.2 for 10GBASE-T and in 113.3.6.2 for 25GBASE-T and 40GBASE-T. These bits shall be reset to all zeros when the errored blocks count is read by the management function or upon execution of the PCS reset. If the Errored blocks high order counter, 3.45 (see 45.2.3.20) is not implemented then these bits shall be held at all ones in the case of overflow.

45.2.7 Auto-Negotiation registers

Change the title and names for register addresses 7.32 and 7.33 to reference MultiGBASE-T (unchanged rows not shown), insert rows for registers 7.64 and 7.65 (to end of table, after 7.63) for MultiGBASE-T AN control 2 and MultiGBASE-T status 2 registers, adjust the reserved row, and add a new reserved row in Table 45–200 as follows:

Table 45–200—Auto-Negotiation MMD registers

Register address	Register name	Subclause
7.32	~~40~~ MultiGBASE-T AN control 1	45.2.7.10
7.33	~~40~~ MultiGBASE-T AN status 1	45.2.7.11
7.62 through 7.632–767	Reserved	
7.64	MultiGBASE-T AN control 2	45.2.7.14a
7.65	MultiGBASE-T AN status 2	45.2.7.14b
7.66 through 7.32 767	Reserved	

Change title and the text of 45.2.7.10 to include 25GBASE-T and 40GBASE-T as follows:

45.2.7.10 ~~40~~MultiGBASE-T AN control 1 register (Register 7.32)

The assignment of bits in the ~~40~~MultiGBASE-T AN control 1 register is shown in Table 45–207. The default values for each bit of the ~~40~~MultiGBASE-T AN control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Change the title, the reserved row, and the name and description of bits 7.32.0, 7.32.1, 7.32.2 in Table 45–207 and insert rows for bits 7.32.11, 7.32.10, 7.32.9, and 7.32.3 above and below the reserved row, respectively, as follows (unchanged rows not shown):

Table 45–207—~~40~~MultiGBASE-T AN control 1 register

Bit(s)	Name	Description	R/W ^a
7.32.11	40GBASE-T ability	1 = Advertise PHY as 40GBASE-T capable 0 = Do not advertise the PHY as 40GBASE-T capable	R/W
7.32.10	25GBASE-T ability	1 = Advertise PHY as 25GBASE-T capable 0 = Do not advertise the PHY as 25GBASE-T capable	R/W
7.32.9	25GBASE-T Fast retrain ability	1 = Advertise PHY as 25GBASE-T fast retrain capable 0 = Do not advertise PHY as 25GBASE-T fast retrain capable	R/W
7.32.11:38 :4	Reserved	Value always 0	RO
7.32.3	40GBASE-T Fast retrain ability	1 = Advertise PHY as 40GBASE-T fast retrain capable 0 = Do not advertise PHY as 40GBASE-T fast retrain capable	R/W
7.32.2	10GBASE-T LD PMA training reset request	1 = Local device requests that link partner reset PMA training PRBS every frame 0 = Local device requests that link partner run PMA training PRBS continuously NOTE — the periodic training sequence request functionality is deprecated. Link partners may ignore a value of one in this bit. It is recommended to always set this bit to zero.	R/W

Table 45–207—~~40~~MultiGBASE-T AN control 1 register (continued)

Bit(s)	Name	Description	R/W ^a
7.32.1	<u>10GBASE-T</u> Fast retrain ability	1 = Advertise PHY as 10GBASE-T fast retrain capable 0 = Do not advertise PHY as 10GBASE-T fast retrain capable	R/W
7.32.0	<u>10GBASE-T</u> LD loop timing ability	1 = Advertise PHY as capable of <u>10GBASE-T</u> loop timing 0 = Do not advertise PHY as <u>10GBASE-T</u> loop timing	R/W

^aR/W = Read/Write, RO = Read only

Insert 45.2.7.10.4a through 45.2.7.10.4d after 45.2.7.10.4 as follows:

45.2.7.10.4a 40GBASE-T capability (7.32.11)

Bit 7.32.11 is used to select whether or not Auto-Negotiation advertises the ability to operate as a 40GBASE-T PHY. If bit 7.32.11 is set to one the PHY shall advertise 40GBASE-T PHY capability. If bit 7.32.11 is set to zero the PHY shall not advertise 40GBASE-T PHY capability.

45.2.7.10.4b 25GBASE-T capability (7.32.10)

Bit 7.32.10 is used to select whether or not Auto-Negotiation advertises the ability to operate as a 25GBASE-T PHY. If bit 7.32.10 is set to one the PHY shall advertise 25GBASE-T PHY capability. If bit 7.32.10 is set to zero the PHY shall not advertise 25GBASE-T PHY capability.

45.2.7.10.4c 25GBASE-T Fast retrain ability (7.32.9)

Bit 7.32.9 is used to select whether or not the 25GBASE-T PHY advertises the ability to support 25GBASE-T fast retrain. Fast retrain ability is exchanged during link training, see 113.4.2.5.10. If bit 7.32.9 is set to one, the PHY shall advertise fast retrain ability. If bit 7.32.9 is set to zero, the PHY shall not advertise fast retrain ability.

45.2.7.10.4d 40GBASE-T Fast retrain ability (7.32.3)

Bit 7.32.3 is used to select whether or not the 40GBASE-T PHY advertises the ability to support 40GBASE-T fast retrain. Fast retrain ability is exchanged during link training, see 113.4.2.5.10. If bit 7.32.3 is set to one, the PHY shall advertise fast retrain ability. If bit 7.32.3 is set to zero, the PHY shall not advertise fast retrain ability.

Change the title and the text of 45.2.7.10.5 as shown:

45.2.7.10.5 10GBASE-T LD PMA training reset request (7.32.2)

For 10GBASE-T, if bit 7.32.2 is set to one then the local device expects the link partner to reset the PMA training PRBS for every PMA training frame. If bit 7.32.2 is zero then the local device expects link partner to run PMA training PRBS continuously through every PMA training frame.

The periodic training sequence request functionality is deprecated and may be unsupported by some implementations. The link partner may ignore a request caused by setting this bit to one. It is recommended to always set this bit to zero.

Change the title of 45.2.7.10.6 as follows:

45.2.7.10.6 10GBASE-T Fast retrain ability (7.32.1)

Change the title of 45.2.7.10.7 as follows:

45.2.7.10.7 10GBASE-T LD loop timing ability (7.32.0)

Change the title and the text of 45.2.7.11 to include 40GBASE-T as follows:

45.2.7.11 ~~40~~MultiGBASE-T AN status 1 register (Register 7.33)

The assignment of bits in the ~~40~~MultiGBASE-T AN status 1 register is shown in Table 45–208. All the bits in the ~~40~~MultiGBASE-T AN status 1 register are read only; a write shall have no effect.

Change the title, the reserved row, and the names and descriptions for bits 7.33.9 (and NOTE), 7.33.1, and 7.33.0, insert rows for bit 7.33.8 and 7.33.7 before the reserved row, and bit 7.33.2 after reserved row in Table 45–208 as follows (unchanged rows not shown):

Table 45–208—~~40~~MultiGBASE-T AN status 1 register

Bit(s)	Name	Description	R/W ^a
7.33.9	<u>10GBASE-T</u> LP PMA training reset request	1 = Link partner requests that local device reset PMA training PRBS every frame 0 = Link partner requests that local device run PMA training PRBS continuously <u>See NOTE.</u>	RO
<u>7.33.8</u>	<u>Link partner</u> <u>40GBASE-T capability</u>	<u>1 = Link partner is able to operate as 40GBASE-T</u> <u>0 = Link partner is not able to operate as 40GBASE-T</u>	<u>RO</u>
<u>7.33.7</u>	<u>Link partner</u> <u>25GBASE-T capability</u>	<u>1 = Link partner is able to operate as 25GBASE-T</u> <u>0 = Link partner is not able to operate as 25GBASE-T</u>	<u>RO</u>
~~7.33.8–2~~ <u>6.3</u>	Reserved	Value always 0	RO
<u>7.33.2</u>	<u>25GBASE-T Fast</u> <u>retrain ability</u>	<u>1 = Link partner is capable of 25GBASE-T fast retrain</u> <u>0 = Link partner is not capable of 25GBASE-T fast retrain</u>	<u>RO</u>
7.33.1	<u>10GBASE-T</u> Fast retrain ability	1 = Link partner is capable of 10GBASE-T fast retrain 0 = Link partner is not capable of 10GBASE-T fast retrain	RO
7.33.0	~~Reserved~~ <u>40GBASE-T</u> <u>Fast retrain ability</u>	~~Value always 0~~ <u>1 = Link partner is capable of 40GBASE-T fast retrain</u> <u>0 = Link partner is not capable of 40GBASE-T fast retrain</u>	RO
NOTE — The periodic training sequence request functionality is deprecated. Implementations may ignore a value of one in this bit or have it always read as zero.			

^aRO = Read only, SC = Self-clearing, LH = Latching high

45.2.7.11.1 MASTER-SLAVE configuration fault (7.33.15)

Change the text of 45.2.7.11.1 to include 25GBASE-T and 40GBASE-T as follows:

MASTER-SLAVE configuration fault bit 7.33.15 shall be set in the event that determination of the MASTER-SLAVE cannot be successfully concluded. MASTER-SLAVE configuration fault, as well as the