



IEEE Standard for Ethernet

Amendment 4: Physical Layer Specifications and Management Parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Based on 100 Gb/s Signaling

IEEE Computer Society

Developed by the
LAN/MAN Standards Committee

IEEE Std 802.3ck™-2022

(Amendment to IEEE Std 802.3™-2022
as amended by IEEE Std 802.3dd™-2022,
IEEE Std 802.3cs™-2022,
and IEEE Std 802.3db™-2022)

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IEEE SA Standards Board

Abstract: This amendment to IEEE Std 802.3-2022 adds Clause 161 through Clause 163, Annex 120F, Annex 120G, and Annex 162A through Annex 162D, Annex 163A, and Annex 163B. This amendment includes Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s electrical interfaces based on 100 Gb/s signaling.

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Introduction

This introduction is not part of IEEE Std 802.3ck-2022, IEEE Standard for Ethernet—Amendment 4: Physical Layer Specifications and Management Parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Based on 100 Gb/s Signaling.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. “Local Area Networks: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications” was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol and the ability to use an EtherType to specify the MAC client protocol were added in 1997. The title was changed to Standard for Ethernet with the 2012 Revision.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2022 and are not maintained as separate documents.

At the date of IEEE Std 802.3ck-2022 publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2022

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex K and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33A. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 140 and Annex 119A through Annex 136D. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well as 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 includes general information on 2.5 Gb/s and 5 Gb/s operation. Clause 126 through Clause 130 and associated annexes include 2.5 Gb/s and 5 Gb/s Physical Layer specifications. Clause 131 provides general information on 50 Gb/s operation. Clause 132 through Clause 140 and associated annexes include 50 Gb/s Physical Layer specifications and additional 100 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications.

Section Nine—Includes Clause 141 through Clause 160 and Annex 142A through Annex 154A. Clause 141 through Clause 144 and associated annexes specify symmetric and asymmetric operation of Ethernet passive optical networks over multiple 25 Gb/s channels. Clause 145 and associated annexes specify increased power delivery using all four pairs in the structured wiring plant. Clause 146 through Clause 149 and associated annexes specify Physical Layers for 10 Mb/s, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation over a single balanced pair of conductors. Clause 150 and Clause 151 include additional 400 Gb/s Physical Layer specifications. Clause 153 and Clause 154 specify 100 Gb/s operation over DWDM channels. Clause 157 through Clause 160 include 10 Gb/s, 25 Gb/s, and 50 Gb/s bidirectional Physical Layer specifications.

IEEE Std 802.3dd™-2022

Amendment 1—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 104, Power over Data Lines of Single Pair Ethernet, and related portions of the standard.

IEEE Std 802.3cs™-2022

Amendment 2—This amendment to IEEE Std 802.3-2022 defines Super-PON optical subscriber access networks, in the family of Ethernet passive optical networks (EPONs). Super-PON has a reach of up to 50 km and up to 1024 ONUs over a point-to-multipoint passive optical distribution network (ODN)

through wavelength division multiplexing (WDM). A Super-PON ODN contains a passive wavelength router that determines the channels used by the ODN. This standard specifies the Super-PON Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), Physical Media Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer at a MAC data rate of 10 Gb/s in the downstream direction and of 10 Gb/s or 2.5 Gb/s in the upstream direction.

IEEE Std 802.3db™-2022

Amendment 3—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 167. This amendment adds Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s over one, two, and four pairs of multimode fiber based on 100 Gb/s optical signaling.

IEEE Std 802.3ck™-2022

Amendment 4—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 161 through Clause 163, Annex 120F, Annex 120G, Annex 162A through Annex 162D, Annex 163A, and Annex 163B. This amendment includes Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s electrical interfaces based on 100 Gb/s signaling.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 4: Physical Layer Specifications and Management Parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Based on 100 Gb/s Signaling

(This amendment is based on IEEE Std 802.3™-2022 as amended by IEEE Std 802.3dd™-2022, IEEE Std 802.3cs™-2022, and IEEE Std 802.3db™-2022.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~striketrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.⁶

⁶ Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Change list item q) “100 Gb/s Attachment Unit Interface (CAUI-n/100GAUI-n)” in 1.1.3.2 as follows:

- q) *100 Gb/s Attachment Unit Interface (CAUI-n/100GAUI-n).* The CAUI-n/100GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 100 Gb/s speeds. The CAUI-n/100GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. ThreeFor chip-to-chip interfaces and for chip-to-module interfaces, four widths of CAUI-n/100GAUI-n are defined: a ten-lane version (CAUI-10) in Annex 83A and Annex 83B, a four-lane version (CAUI-4/100GAUI-4) in Annex 83D, Annex 83E, Annex 135D, and Annex 135E, ~~and~~ a two-lane version (100GAUI-2) in Annex 135F and Annex 135G, and a one-lane version (100GAUI-1) in Annex 120F and Annex 120G. No mechanical connector is specified for use with the CAUI-n/100GAUI-n. The CAUI-n/100GAUI-n is optional.

Change list item t) “200 Gb/s Attachment Unit Interface (200GAUI-n)” in 1.1.3.2 as follows:

- t) *200 Gb/s Attachment Unit Interface (200GAUI-n).* The 200GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 200 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 200 Gb/s speeds. The 200GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. TwoFor chip-to-chip interfaces and for chip-to-module interfaces, three widths of 200GAUI-n are defined: an eight-lane version (200GAUI-8) in Annex 120B and Annex 120C, ~~and~~ a four-lane version (200GAUI-4) in Annex 120D and Annex 120E, and a two-lane version (200GAUI-2) in Annex 120F and Annex 120G. No mechanical connector is specified for use with the 200GAUI-n. The 200GAUI-n is optional.

Change list item v) “400 Gb/s Attachment Unit Interface (400GAUI-n)” in 1.1.3.2 as follows:

- v) *400 Gb/s Attachment Unit Interface (400GAUI-n).* The 400GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 400 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 400 Gb/s speeds. The 400GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. TwoFor chip-to-chip interfaces and for chip-to-module interfaces, three widths of 400GAUI-n are defined: a sixteen-lane version (400GAUI-16) in Annex 120B and Annex 120C, ~~and~~ an eight-lane version (400GAUI-8) in Annex 120D and Annex 120E, and a four-lane version (400GAUI-4) in Annex 120F and Annex 120G. No mechanical connector is specified for use with the 400GAUI-n. The 400GAUI-n is optional.

1.3 Normative references

Insert the following new references in alphanumeric order:

DSFP MSA Dual small form factor pluggable module, Rev. 1.0, September 12, 2018.⁷

OSFP MSA Specification for OSFP octal small form factor pluggable module, Rev 4.1, August 2, 2021.⁸

QSFP-DD/QSFP-DD800/QSFP112 Hardware Specification for QSFP Double Density 8X and QSFP 4X Pluggable Transceivers, Revision 6.01, May 28, 2021.⁹

SFP-DD/SFP-DD112/SFP112 Hardware Specification for SFP112 and SFP Double Density Pluggable Transceiver, Revision 5.0, October 1, 2021.¹⁰

Change the entry for SFF-8432 as follows:

SFF-8432, Rev 5.15.2a, August 8, 2012November 30, 2018, Specification for SFP+ Module and Cage.

1.4 Definitions

Insert the following new definition after 1.4.24 “100BASE-X”:

1.4.24a 100GBASE-CR1: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over one lane of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 162.)

Insert the following new definition after 1.4.31 “100GBASE-KP4”:

1.4.31a 100GBASE-KR1: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over one lane of an electrical backplane. (See IEEE Std 802.3, Clause 163.)

Change 1.4.44 as follows:

1.4.44 100 Gb/s Attachment Unit Interface (CAUI-n, 100GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. ThreeFor chip-to-module interconnections and for chip-to-chip interconnections, four widths are defined: a ten-lane version (CAUI-10), two four-lane versions (CAUI-4, 100GAUI-4), ~~and~~ a two-lane version (100GAUI-2), and a single-lane version (100GAUI-1). (See IEEE Std 802.3, Annex 83A and Annex 83B for CAUI-10, Annex 83D and Annex 83E for CAUI-4, Clause 135, Annex 135D, and Annex 135E for 100GAUI-4, ~~or~~ Clause 135, Annex 135F, and Annex 135G for 100GAUI-2, or Clause 135, Annex 120F, and Annex 120G for 100GAUI-1.)

Insert the following new definition after 1.4.101 “2.5GSEI”:

1.4.101a 200GBASE-CR2: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over two lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 162.)

⁷ DSFP specifications are available from DSFP MSA (<https://dsfpmsa.org/>).

⁸ OSFP specifications are available from OSFP MSA (<https://osfpmsa.org/>).

⁹ QSFP-DD, QSFP-DD800, and QSFP112 specifications are available from QSFP-DD MSA (<http://www.qsfp-dd.com/>).

¹⁰ SFP-DD112 and SFP112 specifications are available from SFP-DD MSA (<http://sfp-dd.com/>).

Insert the following new definition after 1.4.105 “200GBASE-FR4”:

1.4.105a 200GBASE-KR2: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over two lanes of an electrical backplane. (See IEEE Std 802.3, Clause 163.)

Change 1.4.110 as follows:

1.4.110 200 Gb/s Attachment Unit Interface (200GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 200 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. ~~Two~~For chip-to-module interconnections and for chip-to-chip interconnections, three widths of 200GAUI-n are defined: an eight-lane version (200GAUI-8), ~~and a four-lane version (200GAUI-4), and a two-lane version (200GAUI-2).~~ (See IEEE Std 802.3, [Annex 120B](#) and [Annex 120C](#) for 200GAUI-8, ~~or Annex 120D~~ and [Annex 120E](#) for 200GAUI-4, ~~or Annex 120F and Annex 120G for 200GAUI-2.~~)

Insert the following new definition after 1.4.134 “2-Event class signature”:

1.4.134a 400GBASE-CR4: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding over four lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 162.)

Insert the following new definition after 1.4.138 “400GBASE-FR8”:

1.4.138a 400GBASE-KR4: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding over four lanes of an electrical backplane. (See IEEE Std 802.3, Clause 163.)

Change 1.4.145 as follows:

1.4.145 400 Gb/s Attachment Unit Interface (400GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 400 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. ~~Two~~For chip-to-module interconnections and for chip-to-chip interconnections, three widths of 400GAUI-n are defined: a sixteen-lane version (400GAUI-16), ~~and an eight-lane version (400GAUI-8), and a four-lane version (400GAUI-4).~~ (See IEEE Std 802.3, [Annex 120B](#) and [Annex 120C](#) for 400GAUI-16, ~~or Annex 120D~~ and [Annex 120E](#) for 400GAUI-8, ~~or Annex 120F and Annex 120G for 400GAUI-4.~~)

1.5 Abbreviations

Change the abbreviation of 100GAUI as follows:

100GAUI-n 100 Gb/s Attachment Unit Interface over n lanes

Insert the following new acronym in alphanumeric order:

VEC vertical eye closure

30. Management

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.5.1.1.2 after the entry for 50GBASE-SR:

100GBASE-CR1	100GBASE-R PCS/PMA over shielded balanced copper cable PMD as specified in Clause 162
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Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.5.1.1.2 after the entry for 100GBASE-KP4:

100GBASE-KR1	100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 163
--------------	--

Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.5.1.1.2 after the entry for 100GBASE-ZR:

200GBASE-CR2	200GBASE-R PCS/PMA over 2 lane shielded balanced copper cable PMD as specified in Clause 162
--------------	--

Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.5.1.1.2 after the entry for 200GBASE-FR4:

200GBASE-KR2	200GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 163
--------------	--

Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.5.1.1.2 after the entry for 200GBASE-VR2 (as inserted by IEEE Std 802.3db-2022):

400GBASE-CR4	400GBASE-R PCS/PMA over 4 lane shielded balanced copper cable PMD as specified in Clause 162
--------------	--

Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.5.1.1.2 after the entry for 400GBASE-FR8:

400GBASE-KR4	400GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 163
--------------	--

30.5.1.1.16 aFECmode

Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.5.1.1.16 after the entry for RS-FEC enabled:

RS-FEC-Int enabled	RS-FEC-Int enabled
--------------------	--------------------

Change the first three paragraphs of the “BEHAVIOUR DEFINED AS:” section of 30.5.1.1.16 as follows:

A read-write value for a PHY that supports an optional FEC sublayer that indicates the mode of operation of the FEC sublayer for forward error correction across the MDI (see 65.2, [Clause 74](#), [Clause 91](#), ~~and [Clause 108](#)~~, and [Clause 161](#)).

A GET operation returns the current mode of operation of the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. The enumerations “BASE-R enabled”, ~~and “RS-FEC enabled”, and “RS-FEC-Int enabled”~~ are only used ~~for by~~ PHYs which support more than one type of FEC operation. For 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, and 25GBASE-KR-S PHYs where operation in the no-FEC mode maps to the enumeration “disabled”, operation in the BASE-R FEC mode maps to the enumeration “BASE-R enabled”, and operation in the RS-FEC mode maps to the enumeration “RS-FEC enabled” (see 110.6 and 111.6). For 100GBASE-CR1 and 100GBASE-KR1 PHYs, operation in RS-FEC mode maps to the enumeration “RS-FEC enabled” (see 91.6.7a) and operation in interleaved RS-FEC mode maps to the enumeration “RS-FEC-Int enabled” (see 161.6.3).

When [Clause 73](#) Auto-Negotiation is enabled for a 25GBASE-R PHY, a SET operation is not allowed and a GET operation maps to the variables `FEC_enable` in [Clause 74](#) and `FEC_enable` in [Clause 108](#). When [Clause 73](#) Auto-Negotiation is enabled for a non-25GBASE-R PHY supporting [Clause 74](#) FEC a SET operation is not allowed and a GET operation maps to the variable `FEC_enable` in [Clause 74](#). When [Clause 73](#) Auto-Negotiation is enabled for a 100GBASE-R PHY supporting [Clause 161](#) FEC a SET operation is not allowed and a GET operation maps to the variable `100G_RS_FEC_enable` in [Clause 91](#) and `100G_RS_FEC_Int_enable` in [Clause 161](#).

30.5.1.1.17 aFECCorrectedBlocks

Change the final paragraph of 30.5.1.1.17 as follows:

If a [Clause 45](#) MDIO Interface is present, then this attribute maps to the FEC corrected blocks counter(s) (see [45.2.10.5](#) and [45.2.1.109](#) for 10GBASE-R, [45.2.3.41](#) for 10GBASE-PR and 10/1GBASE-PRX, [45.2.1.131](#) for BASE-R, [45.2.1.118](#) for RS-FEC and RS-FEC-Int, [45.2.3.62](#) for PCS FEC, and [45.2.1.227](#) for SC-FEC).;

30.5.1.1.18 aFECUncorrectedBlocks

Change the final paragraph of 30.5.1.1.18 as follows:

If a [Clause 45](#) MDIO Interface is present, then this attribute maps to the FEC uncorrectable blocks counter(s) (see [45.2.10.6](#) and [45.2.1.110](#) for 10GBASE-R, [45.2.3.42](#) for 10GBASE-PR and 10/1GBASE-PRX, [45.2.1.149](#) for BASE-R, [45.2.1.119](#) for RS-FEC and RS-FEC-Int, [45.2.3.63](#) for PCS FEC, and [45.2.1.228](#) for SC-FEC).;

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.6.1.1.5 after the entry for 100GR2:

100GR1	100GBASE-CR1 as specified in Clause 162 or 100GBASE-KR1 as specified in Clause 163
--------	--

Insert the following new entries into the “APPROPRIATE SYNTAX” section of 30.6.1.1.5 after the entry for 200GR4:

200GR2	200GBASE-CR2 as specified in Clause 162 or 200GBASE-KR2 as specified in Clause 163
400GR4	400GBASE-CR4 as specified in Clause 162 or 400GBASE-KR4 as specified in Clause 163

Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.6.1.1.5 after the entry for BASE-RFEC25G Req:

RS-FEC-Int Req	RS-FEC-Int requested as specified in 73.6.5 and Clause 161
----------------	--

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change Table 45–3 as follows (some unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
...		
1.207 through 1.209	~~RS-FEC codeword counter~~ ~~Reserved~~	<u>45.2.1.120a</u>
...		
1.300 through 1.339	BASE-R FEC corrected blocks counter, lanes 0 through 19	<u>45.2.1.131</u>
<u>1.340 through 1.369</u>	<u>RS-FEC codeword error bin 1 through 15</u>	<u>45.2.1.131a</u>
~~1.340~~ <u>1.370</u> through 1.399	Reserved	
...		
1.1511	<u>PRBS9Q testing control</u> ~~Reserved~~	<u>45.2.1.171a</u>
...		

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change the description for bits 1.7.6:0 in Table 45–7 as follows (unchanged table rows and bit description lines not shown):

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
1.7.6:0	PMA/PMD type selection	6 5 4 3 2 1 0 ... 1 0 1 1 1 1 0 = ~~400GBASE-CR4 PMA/PMD reserved~~ 1 0 1 1 1 0 1 = ~~400GBASE-KR4 PMA/PMD reserved~~ ... ~~1 0 1 0 1 1 x = reserved~~ <u>1 0 1 0 1 1 1 = 200GBASE-CR2 PMA/PMD</u> <u>1 0 1 0 1 1 0 = 200GBASE-KR2 PMA/PMD</u> ... ~~1 0 0 0 1 1 x = reserved~~ <u>1 0 0 0 1 1 1 = 100GBASE-CR1 PMA/PMD</u> <u>1 0 0 0 1 1 0 = 100GBASE-KR1 PMA/PMD</u> ...	R/W

^aR/W = Read/Write, RO = Read only

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Change Table 45–9 as follows (some unchanged rows not shown):

Table 45–9—Transmit fault description location

PMA/PMD	Description location
...	
50GBASE-BR10, 50GBASE-BR20, 50GBASE-BR40	160.5.8
<u>100GBASE-KR1, 200GBASE-KR2, 400GBASE-KR4</u>	<u>163.8.9</u>
100GBASE-KP4	94.3.8
100GBASE-KR4	93.7.10
<u>100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4</u>	<u>162.8.9</u>
100GBASE-CR4	92.7.10
...	

45.2.1.7.5 Receive fault (1.8.10)

Change Table 45–10 as follows (some unchanged rows not shown):

Table 45–10—Receive fault description location

PMA/PMD	Description location
...	
50GBASE-BR10, 50GBASE-BR20, 50GBASE-BR40	160.5.9
<u>100GBASE-KR1, 200GBASE-KR2, 400GBASE-KR4</u>	<u>163.8.10</u>
100GBASE-KP4	94.3.9
100GBASE-KR4	93.7.11
<u>100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4</u>	<u>162.8.10</u>
100GBASE-CR4	92.7.11
...	

45.2.1.8 PMD transmit disable register (Register 1.9)

Change Table 45–12 as follows (some unchanged rows not shown):

Table 45–12—Transmit disable description location

PMA/PMD	Description location
...	
50GBASE-BR10, 50GBASE-BR20, and 50GBASE-BR40	160.5.6
<u>100GBASE-KR1, 200GBASE-KR2, and 400GBASE-KR4</u>	<u>163.8.6</u>
100GBASE-KP4	94.3.6.6
100GBASE-KR4	93.7.6
<u>100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4</u>	<u>162.8.6</u>
100GBASE-CR4	92.7.6
...	

45.2.1.21 200G PMA/PMD extended ability (Register 1.23)

Change the row for bits 1.23.8:7 in Table 45–24 (as modified by IEEE Std 802.3db-2022) as follows (unchanged rows not shown):

Table 45–24—200G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
~~1.23.8:7~~	~~Reserved~~	~~Value always 0~~	~~RO~~
<u>1.23.8</u>	<u>200GBASE-CR2 ability</u>	<u>1 = PMA/PMD is able to perform 200GBASE-CR2</u> <u>0 = PMA/PMD is not able to perform 200GBASE-CR2</u>	<u>RO</u>
<u>1.23.7</u>	<u>200GBASE-KR2 ability</u>	<u>1 = PMA/PMD is able to perform 200GBASE-KR2</u> <u>0 = PMA/PMD is not able to perform 200GBASE-KR2</u>	<u>RO</u>
...			

^aRO = Read only

Insert 45.2.1.21.1c and 45.2.1.21.1d after 45.2.1.21.1b (inserted by IEEE Std 802.3db-2022) as follows:

45.2.1.21.1c 200GBASE-CR2 ability (1.23.8)

When read as a one, bit 1.23.8 indicates that the PMA/PMD is able to operate as a 200GBASE-CR2 PMA/PMD type. When read as a zero, bit 1.23.8 indicates that the PMA/PMD is not able to operate as a 200GBASE-CR2 PMA/PMD type.

45.2.1.21.1d 200GBASE-KR2 ability (1.23.7)

When read as a one, bit 1.23.7 indicates that the PMA/PMD is able to operate as a 200GBASE-KR2 PMA/PMD type. When read as a zero, bit 1.23.7 indicates that the PMA/PMD is not able to operate as a 200GBASE-KR2 PMA/PMD type.

45.2.1.22 400G PMA/PMD extended ability register (Register 1.24)

Change the row for bits 1.24.1:0 in Table 45–25 as follows (unchanged rows not shown):

Table 45–25—400G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
~~1.24.1:0~~	~~Reserved~~	~~Value always 0~~	~~RO~~
<u>1.24.1</u>	<u>400GBASE-CR4 ability</u>	<u>1 = PMA/PMD is able to perform 400GBASE-CR4</u> <u>0 = PMA/PMD is not able to perform 400GBASE-CR4</u>	<u>RO</u>
<u>1.24.0</u>	<u>400GBASE-KR4 ability</u>	<u>1 = PMA/PMD is able to perform 400GBASE-KR4</u> <u>0 = PMA/PMD is not able to perform 400GBASE-KR4</u>	<u>RO</u>

^aRO = Read only

Insert 45.2.1.22.11 and 45.2.1.22.12 after 45.2.1.22.10 as follows:

45.2.1.22.11 400GBASE-CR4 ability (1.24.1)

When read as a one, bit 1.24.1 indicates that the PMA/PMD is able to operate as a 400GBASE-CR4 PMA/PMD type. When read as a zero, bit 1.24.1 indicates that the PMA/PMD is not able to operate as a 400GBASE-CR4 PMA/PMD type.

45.2.1.22.12 400GBASE-KR4 ability (1.24.0)

When read as a one, bit 1.24.0 indicates that the PMA/PMD is able to operate as a 400GBASE-KR4 PMA/PMD type. When read as a zero, bit 1.24.0 indicates that the PMA/PMD is not able to operate as a 400GBASE-KR4 PMA/PMD type.

45.2.1.24 40G/100G PMA/PMD extended ability 2 (Register 1.26)

Change the row for bits 1.26.1:0 in Table 45–27 (as modified by IEEE Std 802.3db-2022) as follows (unchanged rows not shown):

Table 45–27—40G/100G PMA/PMD extended ability register 2 bit definitions

Bit(s)	Name	Description	R/W ^a
...			
~~1.26.1:0~~	~~Reserved~~	~~Value always 0~~	~~RO~~
<u>1.26.1</u>	<u>100GBASE-CR1 ability</u>	<u>1 = PMA/PMD is able to perform 100GBASE-CR1</u> <u>0 = PMA/PMD is not able to perform 100GBASE-CR1</u>	<u>RO</u>
<u>1.26.0</u>	<u>100GBASE-KR1 ability</u>	<u>1 = PMA/PMD is able to perform 100GBASE-KR1</u> <u>0 = PMA/PMD is not able to perform 100GBASE-KR1</u>	<u>RO</u>

^aRO = Read only

Insert 45.2.1.24.9 and 45.2.1.24.10 after 45.2.1.24.8 (as inserted by IEEE Std 802.3db-2022) as follows:

45.2.1.24.9 100GBASE-CR1 ability (1.26.1)

When read as a one, bit 1.26.1 indicates that the PMA/PMD is able to operate as a 100GBASE-CR1 PMA/PMD type. When read as a zero, bit 1.26.1 indicates that the PMA/PMD is not able to operate as a 100GBASE-CR1 PMA/PMD type.

45.2.1.24.10 100GBASE-KR1 ability (1.26.0)

When read as a one, bit 1.26.0 indicates that the PMA/PMD is able to operate as a 100GBASE-KR1 PMA/PMD type. When read as a zero, bit 1.26.0 indicates that the PMA/PMD is not able to operate as a 100GBASE-KR1 PMA/PMD type.

45.2.1.95 BASE-R PMD control register (Register 1.150)

Change the first sentence of 45.2.1.95 as follows:

The BASE-R PMD control register is used for 10GBASE-KR and other PHY types using the PMDs described in [Clause 72](#), [Clause 84](#), [Clause 85](#), [Clause 92](#), [Clause 93](#), [Clause 94](#), [Clause 110](#), [Clause 111](#), [Clause 136](#), ~~or~~ [Clause 137](#), [Clause 162](#), or [Clause 163](#).

45.2.1.96 BASE-R PMD status register (Register 1.151)

Change the first sentence of 45.2.1.96 as follows:

The BASE-R PMD status register is used for 10GBASE-KR and other PHY types using the PMDs described in [Clause 72](#), [Clause 84](#), [Clause 85](#), [Clause 92](#), [Clause 93](#), [Clause 94](#), [Clause 110](#), [Clause 111](#), [Clause 136](#), ~~or~~ [Clause 137](#), [Clause 162](#), or [Clause 163](#).

45.2.1.116 RS-FEC control register (Register 1.200)

Change the row for bits 1.200.15:5 in Table 45–94 as follows (unchanged rows not shown):

Table 45–94—RS-FEC control register bit definitions

Bit(s)	Name	Description	R/W ^a
1.200.15:7	Reserved	Value always 0	RO
1.200.6	100G RS-FEC enable ^b	1 = Clause 91 RS-FEC is enabled 0 = Clause 91 RS-FEC is disabled	R/W
1.200.5	100G RS-FEC-Int enable	1 = Clause 161 codeword-interleaved RS-FEC is enabled 0 = Clause 161 codeword-interleaved RS-FEC is disabled	R/W
...			

^aR/W = Read/Write, RO = Read only

^bBit 1.200.6 is present only in PHYs that include an alternative FEC sublayer, such as RS-FEC-Int defined in Clause 161

Insert 45.2.1.116.a and 45.2.1.116.b before 45.2.116.1 as follows:

45.2.1.116.a 100G RS-FEC enable (1.200.6)

Bit 1.200.6 enables the Reed-Solomon FEC described in Clause 91 for PHYs that include multiple FEC sublayers.

45.2.1.116.b 100G RS-FEC-Int enable (1.200.5)

Bit 1.200.5 enables the codeword-interleaved Reed-Solomon FEC described in Clause 161.

45.2.1.116.1 FEC degraded SER enable (1.200.4)

Change the first sentence of 45.2.1.116.1 as follows:

This bit enables the RS-FEC decoder to indicate the presence of a degraded SER (see 91.5.3.3.1, ~~and 134.5.3.3.2,~~ and 161.5.3.3.2).

45.2.1.116.4 FEC bypass indication enable (1.200.1)

Change the last sentence of 45.2.1.116.4 as follows:

Writes to bit 1.200.1 are ignored and reads return a zero if the RS-FEC does not have the ability to bypass indicating decoding errors to the PCS layer (see 91.5.3.3, 108.5.3.2, ~~and 134.5.3.3.1,~~ and 161.5.3.3.1).

45.2.1.117 RS-FEC status register (Register 1.201)

45.2.1.117.1 PCS align status (1.201.15)

Change the second sentence of 45.2.1.117.1 as follows:

For the RS-FEC described in Clause 91, ~~or Clause 134,~~ and Clause 161, PCS alignment is defined as block lock, alignment marker lock, and deskew of all transmit PCS lanes.

45.2.1.117.2 RS-FEC align status (1.201.14)

Change the second sentence of 45.2.1.117.2 as follows:

For the RS-FEC described in Clause 91, ~~or Clause 134,~~ and Clause 161, PMA alignment is defined as alignment marker lock and deskew of all lanes on the PMA service interface.

45.2.1.117.3 FEC AM lock 3 (1.201.11)

Change 45.2.1.117.3 as follows:

When read as a one, bit 1.201.11 indicates that the RS-FEC described in Clause 91 and Clause 161 has locked and aligned lane 3 of the PMA service interface. When read as a zero, bit 1.201.11 indicates that the RS-FEC has not locked and aligned lane 3 of the PMA service interface. This bit reflects the state of `amps_lock[3]` (see [91.5.3.1](#) and 161.5.3.1).

45.2.1.117.4 FEC AM lock 2 (1.201.10)

Change 45.2.1.117.4 as follows:

When read as a one, bit 1.201.10 indicates that the RS-FEC described in Clause 91 and Clause 161 has locked and aligned lane 2 of the PMA service interface. When read as a zero, bit 1.201.10 indicates that the RS-FEC has not locked and aligned lane 2 of the PMA service interface. This bit reflects the state of `amps_lock[2]` (see [91.5.3.1](#) and 161.5.3.1).

45.2.1.117.5 FEC AM lock 1 (1.201.9)

Change 45.2.1.117.5 as follows:

When read as a one, bit 1.201.9 indicates that the RS-FEC described in Clause 91, ~~or Clause 134,~~ and Clause 161 has locked and aligned lane 1 of the PMA service interface. When read as a zero, bit 1.201.9 indicates that the RS-FEC has not locked and aligned lane 1 of the PMA service interface. This bit reflects the state of `amps_lock[1]` (see [91.5.3.1](#) and 161.5.3.1).

45.2.1.117.6 FEC AM lock 0 (1.201.8)

Change 45.2.1.117.6 as follows:

When read as a one, bit 1.201.8 indicates that the RS-FEC described in Clause 91, ~~or Clause 134,~~ and Clause 161 has locked and aligned lane 0 of the PMA service interface. When read as a zero, bit 1.201.8 indicates that the RS-FEC has not locked and aligned lane 0 of the PMA service interface. This bit reflects the state of `amps_lock[0]` (see [91.5.3.1](#) and 161.5.3.1).

45.2.1.117.8 FEC degraded SER (1.201.4)

Change the first sentence of 45.2.1.117.8 as follows:

This bit (1.201.4) reflects the state of the variable FEC_degraded_SER (see [91.6.12](#), ~~and [134.6.9](#)~~, and [161.6.10](#)).

45.2.1.117.9 FEC degraded SER ability (1.201.3)

Change the first sentence of 45.2.1.117.9 as follows:

This bit is set to one to indicate that the decoder has the ability to indicate the presence of a degraded SER (see [91.5.3.3.1](#), ~~and [134.5.3.3.2](#)~~, and [161.5.3.3.2](#)).

45.2.1.117.10 RS-FEC high SER (1.201.2)

Change the first sentence of 45.2.1.117.10 as follows:

When FEC_bypass_indication_enable is set to one, bit 1.201.2 is set to one if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold (see [91.5.3.3](#), [108.5.3.2](#), ~~and [134.5.3.3.1](#)~~, and [161.5.3.3.1](#)) and is set to zero otherwise.

45.2.1.117.11 FEC bypass indication ability (1.201.1)

Change the first sentence of 45.2.1.117.11 as follows:

The Reed-Solomon decoder may have the option to perform error detection without error indication (see [91.5.3.3](#), [108.5.3.2](#), ~~and [134.5.3.3.1](#)~~, and [161.5.3.3.1](#)) to reduce the delay contributed by the RS-FEC sublayer.

45.2.1.118 RS-FEC corrected codewords counter (Register 1.202, 1.203)

Change the second sentence of 45.2.1.118 as follows:

See [91.6.16](#), ~~and [108.6.7](#)~~, and [161.6.13](#) for a definition of this register.

45.2.1.119 RS-FEC uncorrected codewords counter (Register 1.204, 1.205)

Change the second sentence of 45.2.1.119 as follows:

See [91.6.17](#), ~~and [108.6.8](#)~~, and [161.6.14](#) for a definition of this register.

Insert 45.2.1.120a before 45.2.121 as follows:

45.2.1.120a RS-FEC codeword counter register (Register 1.207, 1.208, 1.209)

The assignment of bits in the RS-FEC codeword counter register is shown in Table 45–98a. The RS-FEC codeword counter register applies to the codeword-interleaved RS-FEC defined in Clause 161. See [161.6.21](#) for a definition of this register. It is a 48-bit counter that counts once for each FEC codeword received when RS-FEC align status (1.201.14) is set to one. Its bits are reset to all zeros when the register is read by the management function or upon reset, and held at all ones in the case of overflow.

Registers 1.207, 1.208, and 1.209 are used to read the value of the 48-bit counter. When using these registers to read the 48-bit counter value, the register 1.207 is read first, the values of the registers 1.208 and 1.209 are

latched when (and only when) register 1.207 is read, and reads of registers 1.208 and 1.209 return their latched values rather than the current value of the counter.

Table 45–98a—RS-FEC codeword counter bit definitions

Bit(s)	Name	Description	R/W ^a
1.207.15:0	RS-FEC codewords lower	FEC_cw_counter[15:0]	RO, NR
1.208.15:0	RS-FEC codewords middle	FEC_cw_counter[31:16]	RO, NR
1.209.15:0	RS-FEC codewords upper	FEC_cw_counter[47:32]	RO, NR

^aRO = Read only, NR = Non Roll-over

45.2.1.121 RS-FEC symbol error counter lane 0 (Register 1.210, 1.211)

Change the third sentence of 45.2.1.121 as follows:

See [91.6.19](#), ~~and 108.6.9~~, and [161.6.16](#) for a definition of this register.

45.2.1.123 RS-FEC BIP error counter lane 0 (Register 1.230)

Change the second sentence of 45.2.1.123 as follows:

The RS-FEC described in Clause 91, ~~or Clause 134~~, and [Clause 161](#) calculates a BIP value for each PCS lane (see [91.5.2.4](#), ~~91.6.8~~[91.6.21](#), [161.5.2.6](#)).

45.2.1.127 RS-FEC PCS alignment status 1 register (Register 1.280)

45.2.1.127.1 Block lock 7 (1.280.7)

Change the last sentence of 45.2.1.127.1 as follows:

This bit reflects the state of block_lock[7] (see [91.5.2.1](#), [161.6.22](#)).

45.2.1.127.2 Block lock 6 (1.280.6)

Change the last sentence of 45.2.1.127.2 as follows:

This bit reflects the state of block_lock[6] (see [91.5.2.1](#), [161.6.22](#)).

45.2.1.127.3 Block lock 5 (1.280.5)

Change the last sentence of 45.2.1.127.3 as follows:

This bit reflects the state of block_lock[5] (see [91.5.2.1](#), [161.6.22](#)).

45.2.1.127.4 Block lock 4 (1.280.4)

Change the last sentence of 45.2.1.127.4 as follows:

This bit reflects the state of block_lock[4] (see [91.5.2.1](#), [161.6.22](#)).

45.2.1.127.5 Block lock 3 (1.280.3)

Change the last sentence of 45.2.1.127.5 as follows:

This bit reflects the state of block_lock[3] (see 91.5.2.1, 161.6.22).

45.2.1.127.6 Block lock 2 (1.280.2)

Change the last sentence of 45.2.1.127.6 as follows:

This bit reflects the state of block_lock[2] (see 91.5.2.1, 161.6.22).

45.2.1.127.7 Block lock 1 (1.280.1)

Change the last sentence of 45.2.1.127.7 as follows:

This bit reflects the state of block_lock[1] (see 91.5.2.1, 161.6.22).

45.2.1.127.8 Block lock 0 (1.280.0)

Change the last sentence of 45.2.1.127.8 as follows:

This bit reflects the state of block_lock[0] (see 91.5.2.1, 161.6.22).

45.2.1.128 RS-FEC PCS alignment status 2 register (Register 1.281)

45.2.1.128.1 Block lock 19 (1.281.11)

Change the last sentence of 45.2.1.128.1 as follows:

This bit reflects the state of block_lock[19] (see 91.5.2.1, 161.6.22).

45.2.1.128.2 Block lock 18 (1.281.10)

Change the last sentence of 45.2.1.128.2 as follows:

This bit reflects the state of block_lock[18] (see 91.5.2.1, 161.6.22).

45.2.1.128.3 Block lock 17 (1.281.9)

Change the last sentence of 45.2.1.128.3 as follows:

This bit reflects the state of block_lock[17] (see 91.5.2.1, 161.6.22).

45.2.1.128.4 Block lock 16 (1.281.8)

Change the last sentence of 45.2.1.128.4 as follows:

This bit reflects the state of block_lock[16] (see 91.5.2.1, 161.6.22).

45.2.1.128.5 Block lock 15 (1.281.7)

Change the last sentence of 45.2.1.128.5 as follows:

This bit reflects the state of block_lock[15] (see 91.5.2.1, 161.6.22).

45.2.1.128.6 Block lock 14 (1.281.6)

Change the last sentence of 45.2.1.128.6 as follows:

This bit reflects the state of block_lock[14] (see 91.5.2.1, 161.6.22).

45.2.1.128.7 Block lock 13 (1.281.5)

Change the last sentence of 45.2.1.128.7 as follows:

This bit reflects the state of block_lock[13] (see 91.5.2.1, 161.6.22).

45.2.1.128.8 Block lock 12 (1.281.4)

Change the last sentence of 45.2.1.128.8 as follows:

This bit reflects the state of block_lock[12] (see 91.5.2.1, 161.6.22).

45.2.1.128.9 Block lock 11 (1.281.3)

Change the last sentence of 45.2.1.128.9 as follows:

This bit reflects the state of block_lock[11] (see 91.5.2.1, 161.6.22).

45.2.1.128.10 Block lock 10 (1.281.2)

Change the last sentence of 45.2.1.128.10 as follows:

This bit reflects the state of block_lock[10] (see 91.5.2.1, 161.6.22).

45.2.1.128.11 Block lock 9 (1.281.1)

Change the last sentence of 45.2.1.128.11 as follows:

This bit reflects the state of block_lock[9] (see 91.5.2.1, 161.6.22).

45.2.1.128.12 Block lock 8 (1.281.0)

Change the last sentence of 45.2.1.128.12 as follows:

This bit reflects the state of block_lock[8] (see 91.5.2.1, 161.6.22).

45.2.1.129 RS-FEC PCS alignment status 3 register (Register 1.282)

45.2.1.129.1 Lane 7 aligned (1.282.7)

Change the last sentence of 45.2.1.129.1 as follows:

This bit reflects the state of `am_lock[7]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.129.2 Lane 6 aligned (1.282.6)

Change the last sentence of 45.2.1.129.2 as follows:

This bit reflects the state of `am_lock[6]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.129.3 Lane 5 aligned (1.282.5)

Change the last sentence of 45.2.1.129.3 as follows:

This bit reflects the state of `am_lock[5]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.129.4 Lane 4 aligned (1.282.4)

Change the last sentence of 45.2.1.129.4 as follows:

This bit reflects the state of `am_lock[4]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.129.5 Lane 3 aligned (1.282.3)

Change the last sentence of 45.2.1.129.5 as follows:

This bit reflects the state of `am_lock[3]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.129.6 Lane 2 aligned (1.282.2)

Change the last sentence of 45.2.1.129.6 as follows:

This bit reflects the state of `am_lock[2]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.129.7 Lane 1 aligned (1.282.1)

Change the last sentence of 45.2.1.129.7 as follows:

This bit reflects the state of `am_lock[1]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.129.8 Lane 0 aligned (1.282.0)

Change the last sentence of 45.2.1.129.8 as follows:

This bit reflects the state of `am_lock[0]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.130 RS-FEC PCS alignment status 4 register (Register 1.283)

45.2.1.130.1 Lane 19 aligned (1.283.11)

Change the last sentence of 45.2.1.130.1 as follows:

This bit reflects the state of `am_lock[19]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.130.2 Lane 18 aligned (1.283.10)

Change the last sentence of 45.2.1.130.2 as follows:

This bit reflects the state of `am_lock[18]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.130.3 Lane 17 aligned (1.283.9)

Change the last sentence of 45.2.1.130.3 as follows:

This bit reflects the state of `am_lock[17]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.130.4 Lane 16 aligned (1.283.8)

Change the last sentence of 45.2.1.130.4 as follows:

This bit reflects the state of `am_lock[16]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.130.5 Lane 15 aligned (1.283.7)

Change the last sentence of 45.2.1.130.5 as follows:

This bit reflects the state of `am_lock[15]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.130.6 Lane 14 aligned (1.283.6)

Change the last sentence of 45.2.1.130.6 as follows:

This bit reflects the state of `am_lock[14]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.130.7 Lane 13 aligned (1.283.5)

Change the last sentence of 45.2.1.130.7 as follows:

This bit reflects the state of `am_lock[13]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.130.8 Lane 12 aligned (1.283.4)

Change the last sentence of 45.2.1.130.8 as follows:

This bit reflects the state of `am_lock[12]` (see [91.5.2.2](#), [161.5.2.2](#)).

45.2.1.130.9 Lane 11 aligned (1.283.3)

Change the last sentence of 45.2.1.130.9 as follows:

This bit reflects the state of am_lock[11] (see 91.5.2.2, 161.5.2.2).

45.2.1.130.10 Lane 10 aligned (1.283.2)

Change the last sentence of 45.2.1.130.10 as follows:

This bit reflects the state of am_lock[10] (see 91.5.2.2, 161.5.2.2).

45.2.1.130.11 Lane 9 aligned (1.283.1)

Change the last sentence of 45.2.1.130.11 as follows:

This bit reflects the state of am_lock[9] (see 91.5.2.2, 161.5.2.2).

45.2.1.130.12 Lane 8 aligned (1.283.0)

Change the last sentence of 45.2.1.130.12 as follows:

This bit reflects the state of am_lock[8] (see 91.5.2.2, 161.5.2.2).

Insert 45.2.1.131a before 45.2.132 as follows:

45.2.1.131a RS-FEC codeword error bin registers 1 through 15 (Registers 1.340 through 1.369)

The assignment of bits in the RS-FEC codeword error bin 1 register is shown in Table 45–105a. The assignment of bits in the other RS-FEC codeword error bin registers is identical to that of bin 1. The RS-FEC codeword error bin registers increment depending upon the error signature of a corrected codeword (see 161.6.17). Their bits are reset to all zeros when the register is read by the management function or upon reset, and held at all ones in the case of overflow.

Two registers are used to read the value of each 32-bit counter, the value of the second register is latched when the first register is read. For example when registers 1.340 and 1.341 are used to read the 32-bit counter value of FEC_codeword_error_bin_1, the register 1.340 is read first, the value of the register 1.341 is latched when (and only when) register 1.340 is read, and reads of register 1.341 return the latched value rather than the current value of the counter.

Table 45–105a—RS-FEC codeword error bin 1 bit definitions

Bit(s)	Name	Description	R/W ^a
1.340.15:0	RS-FEC codeword error bin 1 lower	FEC_codeword_error_bin_1[15:0]	RO, NR
1.341.15:0	RS-FEC codeword error bin 1 upper	FEC_codeword_error_bin_1[31:16]	RO, NR

^aRO = Read only, NR = Non Roll-over

45.2.1.146 RS-FEC degraded SER activate threshold register (Register 1.650, 1.651)

Change the second sentence of 45.2.1.146 as follows:

The value controls the threshold used to set the FEC degraded SER bit (1.201.4) as defined in 91.5.3.3.1, ~~and 134.5.3.3.2, and 161.5.3.3.2.~~

45.2.1.147 RS-FEC degraded SER deactivate threshold register (Register 1.652, 1.653)

Change the second sentence of 45.2.1.147 as follows:

The value controls the threshold used to clear the FEC degraded SER bit (1.201.4) as defined in 91.5.3.3.1, ~~and 134.5.3.3.2, and 161.5.3.3.2.~~

45.2.1.148 RS-FEC degraded SER interval register (Register 1.654, 1.655)

Change the second sentence of 45.2.1.148 as follows:

The value controls the interval used to set and clear the FEC degraded SER bit (1.201.4) as defined in 91.5.3.3.1, ~~and 134.5.3.3.2, and 161.5.3.3.2.~~

45.2.1.161 BASE-R PAM4 PMD training LP control, lane 0 through lane 3 registers (Register 1.1120 through 1.1123)

Change Table 45–129 as follows:

Table 45–129—BASE-R PAM4 PMD training LP control, lane 0 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1120.15:14	Reserved	Value always 0	RO
~~1.1120.13:12~~ 1.1120.13:11	Initial condition request ^b	13 12 11 1 1 1 = Reserved 1 0 1 = Reserved 0 1 1 = Preset 5 0 0 1 = Preset 4 1 1 0 = Preset 3 1 0 0 = Preset 2 0 1 0 = Preset 1 0 0 0 = Individual coefficient control	R/W
~~1.1120.11:10~~ 1.1120.10	Reserved	Value always 0	RO
1.1120.9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	R/W
1.1120.7:5	Reserved	Value always 0	RO