



IEEE Standard for Ethernet

Amendment 2: Physical Layers and Management Parameters for Increased-Reach Point-to-Multipoint Ethernet Optical Subscriber Access (Super-PON)

IEEE Computer Society

Developed by the
LAN/MAN Standards Committee

IEEE Std 802.3cs™-2022
(Amendment to IEEE Std 802.3™-2022
as revised by IEEE Std 802.3dd™-2022)

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IEEE SA Standards Board

Abstract: Super-PON optical subscriber access networks, which are in the family of Ethernet passive optical networks (EPONs), are defined in this amendment to IEEE Std 802.3-2022. Super-PON has a reach of up to 50 km and up to 1024 ONUs over a point-to-multipoint passive optical distribution network (ODN) through wavelength division multiplexing (WDM). A Super-PON ODN contains a passive wavelength router that determines the channels used by the ODN. This standard specifies the Super-PON Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer at a MAC data rate of 10 Gb/s in the downstream direction and of 10 Gb/s or 2.5 Gb/s in the upstream direction.

Keywords: amendment, IEEE 802.3™, IEEE 802.3cs™, Multipoint MAC Control (MPMC), Optical Distribution Network (ODN), Passive Optical Network (PON), Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Physical Medium Dependent (PMD), Point-to-Multipoint (P2MP), Reconciliation Sublayer (RS), Super-PON

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Introduction

This introduction is not part of IEEE Std 802.3cs-2022, IEEE Standard for Ethernet—Amendment 2: Physical Layers and Management Parameters for Increased-Reach Point-to-Multipoint Ethernet Optical Subscriber Access (Super-PON).

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. “Local Area Networks: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications” was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol and the ability to use an EtherType to specify the MAC client protocol were added in 1997. The title was changed to Standard for Ethernet with the 2012 Revision.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2022 and are not maintained as separate documents.

At the date of this IEEE Std 802.3dd-2022 publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2022

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex K and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33A. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 140 and Annex 119A through Annex 136D. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well as 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 includes general information on 2.5 Gb/s and 5 Gb/s operation. Clause 126 through Clause 130 and associated annexes include 2.5 Gb/s and 5 Gb/s Physical Layer specifications. Clause 131 provides general information on 50 Gb/s operation. Clause 132 through Clause 140 and associated annexes include 50 Gb/s Physical Layer specifications and additional 100 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications.

Section Nine—Includes Clause 141 through Clause 160 and Annex 142A through Annex 154A. Clause 141 through Clause 144 and associated annexes specify symmetric and asymmetric operation of Ethernet passive optical networks over multiple 25 Gb/s channels. Clause 145 and associated annexes specify increased power delivery using all four pairs in the structured wiring plant. Clause 146 through Clause 149 and associated annexes specify Physical Layers for 10 Mb/s, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation over a single balanced pair of conductors. Clause 150 and Clause 151 include additional 400 Gb/s Physical Layer specifications. Clause 153 and Clause 154 specify 100 Gb/s operation over DWDM channels. Clause 157 through Clause 160 include 10 Gb/s, 25 Gb/s, and 50 Gb/s bidirectional Physical Layer specifications.

IEEE Std 802.3dd™-2022

Amendment 1—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 104, Power over Data Lines of Single Pair Ethernet, and related portions of the standard.

IEEE Std 802.3cs™-2022

Amendment 2—This amendment to IEEE Std 802.3-2022 defines Super-PON optical subscriber access networks, in the family of Ethernet passive optical networks (EPONs). Super-PON has a reach of up to 50 km and up to 1024 ONUs over a point-to-multipoint passive optical distribution network (ODN)

through wavelength division multiplexing (WDM). A Super-PON ODN contains a passive wavelength router that determines the channels used by the ODN. This standard specifies the Super-PON Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer at a MAC data rate of 10 Gb/s in the downstream direction and of 10 Gb/s or 2.5 Gb/s in the upstream direction.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 2: Physical Layers and Management Parameters for Increased-Reach Point-to-Multipoint Ethernet Optical Subscriber Access (Super-PON)

(This amendment is based on IEEE Std 802.3™-2022 as amended by IEEE Std 802.3dd™-2022.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strike through~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.⁶

⁶Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.3 Normative references

Insert the following references in alphanumerical order:

ITU-T Recommendation G.989.2, 2019—40-Gigabit-capable passive optical networks 2 (NG-PON2): Physical media dependent (PMD) layer specification.

1.4 Definitions

Insert the following new definition after 1.4.197 arbitration:

1.4.197a Asymmetric Super-PON PMDs: Family of Super-PON PMDs supporting the upstream MAC data rate of 2.5 Gb/s. See Clause 164.

Change 1.4.216, to read as follows:

1.4.216 black link approach: The specification of the input, output, and transfer characteristics of the unidirectional transmission path ~~from TP2 to TP3 for a given DWDM channel within a DWDM black link, without specifying how the transmission path is implemented. (See, for example, IEEE Std 802.3, Clause 154, Figure 154-3)~~

- a) From TP2 to TP3 for a given DWDM channel within a DWDM black link (see, for example, IEEE Std 802.3, Clause 154, Figure 154-3).
- b) From MDI to MDI for a given Super-PON channel within a Super-PON black link (see, for example, IEEE Std 802.3, Clause 164, Figure 164-3).

Insert the following new definition after 1.4.289 differential skew:

1.4.289a dispersion compensation module (DCM): A device having a negative dispersion value that reverses the optical fiber chromatic dispersion in an optical network.

Change 1.4.313 as follows:

1.4.313 EQT: The unit of measurement of time for time-related parameters specified in IEEE Std 802.3, Clause 144 and Clause 164 for Nx25G EPON Multipoint MAC Control. Each EQT is equal to the time required to transmit one envelope quantum EQ between the MCRS and the PCS. When an EQ is transmitted across 25GMII (Clause 144), and the EQT is equal to 2.56 ns. When an EQ is transmitted across XGMII (Clause 164), the EQT is equal to 6.4 ns.

Insert the following new definition after 1.4.344 frame loss ratio:

1.4.344a free spectral range (FSR): The spacing in frequency or wavelength between successive repetitions of the properties of an optical filter.

Insert the following new definitions after 1.4.543 stream:

1.4.543a Super-PON PMDs: Family of PMDs for point-to-multipoint (P2MP) networks, operating at a MAC data rate of 10 Gb/s in the downstream direction and at a MAC data rate of 10 Gb/s or 2.5 Gb/s in the upstream direction. See Clause 164.

1.4.543b Symmetric Super-PON PMDs: Family of Super-PON PMDs supporting the upstream MAC data rate of 10 Gb/s. See Clause 164.

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphanumeric order:

CD	chromatic dispersion
DCM	dispersion compensation module
FSR	free spectral range
MPMC	multipoint mac control
PON	passive optical network

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for 10/1GBASE-PRX as follows:

10/2.5GBASE-SP	164.3 10 Gb/s downstream and 2.5 Gb/s upstream Super-PON 256B/257B
----------------	---

Insert new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for 10GBASE-R as follows:

10GBASE-SP	164.3 10 Gb/s Super-PON 256B/257B
------------	-----------------------------------

30.3.2.1.3 aPhyTypeList

Insert new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for 10/1GBASE-PRX as follows:

10/2.5GBASE-SP	164.3 10 Gb/s downstream and 2.5 Gb/s upstream Super-PON 256B/257B
----------------	---

Insert new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for 10GBASE-R as follows:

10GBASE-SP	164.3 10 Gb/s Super-PON 256B/257B
------------	-----------------------------------

30.3.5 MPCP managed object class

30.3.5.1 MPCP Attributes

30.3.5.1.2 aMPCPAdminState

Change the text of the BEHAVIOUR DEFINED AS section of 30.3.5.1.2 as follows:

BEHAVIOUR DEFINED AS:

A read-only value that identifies the operational state of the Multipoint MAC Control sublayer. An interface that can provide the Multipoint MAC Control sublayer functions specified in [Clause 64](#), [Clause 77](#), [or Clause 103](#), [or 164.5](#) is enabled to do so when this attribute has the enumeration “enabled”. When this attribute has the enumeration “disabled”, the interface acts as it would if it had no Multipoint MAC Control sublayer. The operational state of the Multipoint MAC Control sublayer can be changed using the acMPCPAdminControl action.;

30.3.5.1.3 aMPCPMode

Change the text of the BEHAVIOUR DEFINED AS section of 30.3.5.1.3 as follows:

BEHAVIOUR DEFINED AS:

A read-only value that identifies the operational mode of the Multipoint MAC Control sublayer.
An interface that can provide the Multipoint MAC Control sublayer functions specified in [Clause 64](#), [Clause 77](#), ~~or Clause 103~~, or [164.5](#). When this attribute has the enumeration “OLT”, the interface acts as an OLT. When this attribute has the enumeration “ONU”, the interface acts as an ONU. When this attribute has the enumeration “CLT”, the interface acts as a CLT. When this attribute has the enumeration “CNU”, the interface acts as a CNU.;

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for 10/1GBASE-PRX-U4 as follows:

10/2.5GBASE-SP1-Dx	One single-mode fiber 10.3125 GBd continuous downstream / 2.578125 GBd burst mode upstream OLT PHY supporting channel x of Super-PON FSR set 1, as specified in 164.2
10/2.5GBASE-SP1-Uxy	One single-mode fiber 10.3125 GBd continuous downstream / 2.578125 GBd burst mode upstream ONU PHY supporting channels x to y of Super-PON FSR set 1, as specified in 164.2

Insert new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for 10GBASE-R as follows:

10GBASE-SP1-Dx	One single-mode fiber 10.3125 GBd continuous downstream / 10.3125 GBd burst mode upstream OLT PHY supporting channel x of Super-PON FSR set 1, as specified in 164.2
10GBASE-SP1-Uxy	One single-mode fiber 10.3125 GBd continuous downstream / 10.3125 GBd burst mode upstream ONU PHY supporting channels x to y of Super-PON FSR set 1, as specified in 164.2

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface registers

45.2.1 PMA/PMD registers

Change rows in Table 45–3 as shown below (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
...		
1.1003	Super-PON PMA/PMD extended ability	45.2.1.159a
1.1004 through 1.1099	Reserved	
...		

Change 45.2.1.27 as follows:

45.2.1.27 PMA/PMD control 3 register (Register 1.29)

The assignment of bits in the PMA/PMD control 3 register is shown in Table 45–30.

45.2.1.27.1 Downstream differential encoding (1.29.15)

Downstream differential encoding is selected using bit 1.29.15. This bit is read/write in the OLT and read only in the ONU with the default value of 0 (indicating that the downstream differential encoding is not enabled).

In the OLT, this bit controls whether downstream differential encoding is selected for the transmit PMA output.

In the ONU, this bit indicates whether the downstream differential decoding is active~~enabled~~ in the ONU receive PMA.

45.2.1.27.1a Super-PON PMA/PMD transmit channel (1.29.14:11)

The Super-PON PMA/PMD operating transmit channel (see 164.2.2) is selected using bits 14 to 11. The Super-PON operating transmit number is a four-bit number, 0 to 15, represented by bits 14 to 11, as an unsigned integer with bit 14 the most significant bit. The channel interval supported by the PMA/PMD is advertised in the Super-PON PMA/PMD extended ability register (register 1.1003, see 45.2.1.159a).

45.2.1.27.2 PMA/PMD type selection (1.29.5:0)

The PMA/PMD type of the PMA/PMD is selected using bits 5 to 0. The PMA/PMD type abilities of the PMA/PMD for Nx25G-EPON are advertised in the Nx25G-EPON PMA/PMD extended ability registers (registers 1.1000 through 1.1002, see 45.2.1.159). The PMA/PMD type abilities of the PMA/PMD for Super-PON are advertised in the Super-PON PMA/PMD extended ability register (register 1.1003, see 45.2.1.159a). A PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types ~~it has~~ not advertised. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

Table 45–30—PMA/PMD control 3 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.29.15	Downstream differential encoding	1 = Downstream differential encoding enabled/ <u>active</u> 0 = Downstream differential encoding disabled/ <u>inactive</u>	R/W in OLT RO in ONU
<u>1.29.14:1</u> <u>1</u>	<u>Super-PON PMA/PMD</u> <u>transmit channel</u>	<u>Super-PON PMA/PMD operating transmit channel</u>	<u>R/W</u>
<u>1.29.14:1</u> <u>0:6</u>	Reserved	Value always 0	RO
1.29.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 x x x x = Reserved ~~1 0 1 x x x = Reserved~~ 1 0 1 1 x x = Reserved 1 0 1 0 1 1 = 10GBASE-SP1-D 1 0 1 0 1 0 = 10GBASE-SP1-U 1 0 1 0 0 1 = 10/2.5GBASE-SP1-D 1 0 1 0 0 0 = 10/2.5GBASE-SP1-U 1 0 0 1 1 1 = 50GBASE-PQX-U3 1 0 0 1 1 0 = 50GBASE-PQX-U2 1 0 0 1 0 1 = 50GBASE-PQX-D3 1 0 0 1 0 0 = 50GBASE-PQX-D2 1 0 0 0 1 1 = 50GBASE-PQG-U3 1 0 0 0 1 0 = 50GBASE-PQG-U2 1 0 0 0 0 1 = 50GBASE-PQG-D3 1 0 0 0 0 0 = 50GBASE-PQG-D2 0 1 1 1 1 1 = 50/25GBASE-PQX-U3 0 1 1 1 1 0 = 50/25GBASE-PQX-U2 0 1 1 1 0 1 = 50/25GBASE-PQX-D3 0 1 1 1 0 0 = 50/25GBASE-PQX-D2 0 1 1 0 1 1 = 50/25GBASE-PQG-U3 0 1 1 0 1 0 = 50/25GBASE-PQG-U2 0 1 1 0 0 1 = 50/25GBASE-PQG-D3 0 1 1 0 0 0 = 50/25GBASE-PQG-D2 0 1 0 1 1 1 = 50/10GBASE-PQX-U3 0 1 0 1 1 0 = 50/10GBASE-PQX-U2 0 1 0 1 0 1 = 50/10GBASE-PQX-D3 0 1 0 1 0 0 = 50/10GBASE-PQX-D2 0 1 0 0 1 1 = 50/10GBASE-PQG-U3 0 1 0 0 1 0 = 50/10GBASE-PQG-U2 0 1 0 0 0 1 = 50/10GBASE-PQG-D3 0 1 0 0 0 0 = 50/10GBASE-PQG-D2 0 0 1 1 1 1 = 25GBASE-PQX-U3 0 0 1 1 1 0 = 25GBASE-PQX-U2 0 0 1 1 0 1 = 25GBASE-PQX-D3 0 0 1 1 0 0 = 25GBASE-PQX-D2 0 0 1 0 1 1 = 25GBASE-PQG-U3 0 0 1 0 1 0 = 25GBASE-PQG-U2 0 0 1 0 0 1 = 25GBASE-PQG-D3 0 0 1 0 0 0 = 25GBASE-PQG-D2 0 0 0 1 1 1 = 25/10GBASE-PQX-U3 0 0 0 1 1 0 = 25/10GBASE-PQX-U2 0 0 0 1 0 1 = 25/10GBASE-PQX-D3 0 0 0 1 0 0 = 25/10GBASE-PQX-D2 0 0 0 0 1 1 = 25/10GBASE-PQG-U3 0 0 0 0 1 0 = 25/10GBASE-PQG-U2 0 0 0 0 0 1 = 25/10GBASE-PQG-D3 0 0 0 0 0 0 = 25/10GBASE-PQG-D2	R/W

^aR/W = Read/Write, RO = Read only

Insert 45.2.1.159a as follows:

45.2.1.159a Super-PON PMA/PMD extended ability register (Register 1.1003)

The assignment of bits in the Super-PON PMA/PMD extended ability register is shown in Table 45–128a.

Table 45–128a—Super-PON PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1003.15	10GBASE-SP1-D	1 = PMA/PMD is able to perform 10GBASE-SP1-Dxy 0 = PMA/PMD is not able to perform 10GBASE-SP1-Dxy	RO
1.1003.14	10GBASE-SP1-U	1 = PMA/PMD is able to perform 10GBASE-SP1-Uxy 0 = PMA/PMD is not able to perform 10GBASE-SP1-Uxy	RO
1.1003.13	10/2.5GBASE-SP1-D	1 = PMA/PMD is able to perform 10/2.5GBASE-SP1-Dxy 0 = PMA/PMD is not able to perform 10/2.5GBASE-SP1-Dxy	RO
1.1003.12	10/2.5GBASE-SP1-U	1 = PMA/PMD is able to perform 10G/2.5BASE-SP1-Uxy 0 = PMA/PMD is not able to perform 10/2.5GBASE-SP1-Uxy	RO
1.1003.11:8	Reserved	Value always 0	RO
1.1003.7:4	Super-PON channel y	PMA/PMD last transmit channel supported	RO
1.1003.3:0	Super-PON channel x	PMA/PMD first transmit channel supported	RO

^aRO = Read only

45.2.1.159a.1 10GBASE-SP1-D (1.1003.15)

When read as a one, bit 1.1003.15 indicates that the PMA/PMD is able to support a 10GBASE-SP1-Dxy PMA/PMD type, able to operate on any of the Super-PON FSR set 1 channels x (1.1003.3:0) to y (1.1003.7:4). When read as a zero, bit 1.1003.15 indicates that the PMA/PMD is not able to support a 10GBASE-SP1-Dxy PMA/PMD type.

45.2.1.159a.2 10GBASE-SP1-U (1.1003.14)

When read as a one, bit 1.1003.14 indicates that the PMA/PMD is able to support a 10GBASE-SP1-Uxy PMA/PMD type, able to operate on any of the Super-PON FSR set 1 channels x (1.1003.3:0) to y (1.1003.7:4). When read as a zero, bit 1.1003.14 indicates that the PMA/PMD is not able to support a 10GBASE-SP1-Uxy PMA/PMD type.

45.2.1.159a.3 10/2.5GBASE-SP1-D (1.1003.13)

When read as a one, bit 1.1003.13 indicates that the PMA/PMD is able to support a 10/2.5GBASE-SP1-Dxy PMA/PMD type, able to operate on any of the Super-PON FSR set 1 channels x (1.1003.3:0) to y (1.1003.7:4). When read as a zero, bit 1.1003.13 indicates that the PMA/PMD is not able to support a 10/2.5GBASE-SP1-Dxy PMA/PMD type.

45.2.1.159a.4 10/2.5GBASE-SP1-U (1.1003.12)

When read as a one, bit 1.1003.12 indicates that the PMA/PMD is able to support a 10/2.5GBASE-SP1-Uxy PMA/PMD type, able to operate on any of the Super-PON FSR set 1 channels x (1.1003.3:0) to y (1.1003.7:4). When read as a zero, bit 1.1003.12 indicates that the PMA/PMD is not able to support a 10/2.5GBASE-SP1-Uxy PMA/PMD type.

45.2.1.159a.5 Super-PON channel y (1.1003.7:4)

This 4-bit field indicates the highest numbered Super-PON transmit channel supported by the PMA/PMD (see 164.2.2).

45.2.1.159a.6 Super-PON channel x (1.1003.3:0)

This 4-bit field indicates the lowest numbered Super-PON transmit channel supported by the PMA/PMD (see 164.2.2).

45.2.3 PCS registers

Change the identified rows in Table 45–233 (unchanged rows not shown):

Table 45–233—PCS registers

Register address	Register name	Subclause
...	...	...
3.76, 3.77	10G-EPON, ~~and~~ Nx25G-EPON, <u>and Super-PON</u> corrected FEC codewords counter	45.2.3.41
3.78, 3.79	10G-EPON, ~~and~~ Nx25G-EPON, <u>and Super-PON</u> uncorrected FEC codewords counter	45.2.3.42
3.80	10GBASE-PR ~~and~~ , 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, <u>and Super-PON</u> BER monitor interval control	45.2.3.43
3.81	10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, <u>and Super-PON</u> BER monitor status	45.2.3.44
3.82	10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, <u>and Super-PON</u> BER monitor threshold control	45.2.3.45
3.83 through 3.134	Nx25G-EPON <u>and Super-PON</u> synchronization pattern	45.2.3.46
...	...	...

45.2.3.1 PCS control 1 register (Register 3.0)

Change the identified row in Table 45–234 as follows (unchanged rows not shown):

Table 45–234—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W ^a
...	...	...	...
3.0.5:2	Speed selection	5 4 3 2 ~~1 1 x x~~ = ~~Reserved~~ ~~1 1 1 x~~ = ~~Reserved~~ ~~1 1 0 1~~ = ~~Reserved~~ ~~1 1 0 0~~ = ~~10/2.5 Gb/s~~ 1 0 1 1 = 25/10 Gb/s 1 0 1 0 = 400 Gb/s 1 0 0 1 = 200 Gb/s 1 0 0 0 = 5 Gb/s 0 1 1 1 = 2.5 Gb/s 0 1 1 0 = 50 Gb/s 0 1 0 1 = 25 Gb/s 0 1 0 0 = 100 Gb/s 0 0 1 1 = 40 Gb/s 0 0 1 0 = 10/1 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
...	...	...	...

^aRO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.6 PCS control 2 register (Register 3.7)

Change the identified rows in Table 45–237 as follows (unchanged rows not shown):

Table 45–237—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.7.15:5	Reserved	Value always 0	RO
3.7.4:0	PCS type selection	4 3 2 1 0 1 1 x x x = reserved ~~1 0 1 x x~~ = ~~reserved~~ ~~1 0 1 1 x~~ = ~~reserved~~ ~~1 0 1 0 1~~ = ~~Select 10GBASE-SP PCS type~~ ~~1 0 1 0 0~~ = ~~Select 10/2.5GBASE-SP PCS type~~ 1 0 0 1 1 = Select 25GBASE-PQ PCS type 1 0 0 1 0 = Select 25/10GBASE-PQ PCS type 1 0 0 0 1 = Select 25GBASE-PQ PCS type, Tx only 1 0 0 0 0 = Select 25GBASE-PQ PCS type, Rx only 0 1 1 1 1 = Select 5GBASE-R PCS type 0 1 1 1 0 = Select 2.5GBASE-X PCS type 0 1 1 0 1 = Select 400GBASE-R PCS type 0 1 1 0 0 = Select 200GBASE-R PCS type 0 1 0 1 1 = Select 5GBASE-T PCS type 0 1 0 1 0 = Select 2.5GBASE-T PCS type 0 1 0 0 1 = Select 25GBASE-T PCS type 0 1 0 0 0 = Select 50GBASE-R PCS type 0 0 1 1 1 = Select 25GBASE-R PCS type 0 0 1 1 0 = Select 40GBASE-T PCS type 0 0 1 0 1 = Select 100GBASE-R PCS type 0 0 1 0 0 = Select 40GBASE-R PCS type 0 0 0 1 1 = Select 10GBASE-T PCS type 0 0 0 1 0 = Select 10GBASE-W PCS type 0 0 0 0 1 = Select 10GBASE-X PCS type 0 0 0 0 0 = Select 10GBASE-R PCS type	R/W

^aRO = Read only, R/W = Read/Write

Change content of 45.2.3.6.1 as follows:

45.2.3.6.1 PCS type selection (3.7.4:0)

The PCS type shall be selected using bits 4 through 0. The PCS type abilities of the PCS are advertised in bits 3.8.13:12, 3.8.9:0 and 3.9.97:0. A PCS shall ignore writes to the PCS type selection bits that select PCS types it has not advertised in the PCS status 2 register or the PCS status 3 register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY. The PCS type selection defaults to a supported ability.

Table 45–237—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.7.15:5	Reserved	Value always 0	RO
3.7.4:0	PCS type selection	4 3 2 1 0 1 1 x x x = reserved ~~1 0 1 x x = reserved~~ ~~1 0 1 1 x = reserved~~ 1 0 1 0 1 = Select 10GBASE-SP PCS type 1 0 1 0 0 = Select 10/2.5GBASE-SP PCS type 1 0 0 1 1 = Select 25GBASE-PQ PCS type 1 0 0 1 0 = Select 25/10GBASE-PQ PCS type 1 0 0 0 1 = Select 25GBASE-PQ PCS type, Tx only 1 0 0 0 0 = Select 25GBASE-PQ PCS type, Rx only 0 1 1 1 1 = Select 5GBASE-R PCS type 0 1 1 1 0 = Select 2.5GBASE-X PCS type 0 1 1 0 1 = Select 400GBASE-R PCS type 0 1 1 0 0 = Select 200GBASE-R PCS type 0 1 0 1 1 = Select 5GBASE-T PCS type 0 1 0 1 0 = Select 2.5GBASE-T PCS type 0 1 0 0 1 = Select 25GBASE-T PCS type 0 1 0 0 0 = Select 50GBASE-R PCS type 0 0 1 1 1 = Select 25GBASE-R PCS type 0 0 1 1 0 = Select 40GBASE-T PCS type 0 0 1 0 1 = Select 100GBASE-R PCS type 0 0 1 0 0 = Select 40GBASE-R PCS type 0 0 0 1 1 = Select 10GBASE-T PCS type 0 0 0 1 0 = Select 10GBASE-W PCS type 0 0 0 0 1 = Select 10GBASE-X PCS type 0 0 0 0 0 = Select 10GBASE-R PCS type	R/W

^aRO = Read only, R/W = Read/Write

45.2.3.8 PCS status 3 register (Register 3.9)

Change the row for bits 3.9.15:4 in Table 45-182 as follows (unchanged rows not shown):

Insert 45.2.3.8.a through 45.2.3.8.b (before 45.2.3.8.1) as follows:

45.2.3.8.a 10GBASE-SP capable (3.9.9)

When read as a one, bit 3.9.9 indicates that the PCS is able to support the 10GBASE-SP PCS type. When read as a zero, bit 3.9.9 indicates that the PCS is not able to support the 10GBASE-SP PCS type.

Table 45–239—PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.9.15:10 8	Reserved	Value always 0	RO
3.9.9	10GBASE-SP capable	1 = PCS is able to support 10GBASE-SP PCS type 0 = PCS is not able to support 10GBASE-SP PCS type	RO
3.9.8	10/2.5GBASE-SP capable	1 = PCS is able to support 10/2.5GBASE-SP PCS type 0 = PCS is not able to support 10/2.5GBASE-SP PCS type	RO
...			

^aRO = Read only

45.2.3.8.b 10/2.5GBASE-SP capable (3.9.8)

When read as a one, bit 3.9.8 indicates that the PCS is able to support the 10/2.5GBASE-SP PCS type. When read as a zero, bit 3.9.8 indicates that the PCS is not able to support the 10/2.5GBASE-SP PCS type.

Change the title, text and table captions (unchanged table content is not shown) for 45.2.3.41 through 45.2.3.45 as follows:

45.2.3.41 10G-EPON~~, and~~ Nx25G-EPON~~, and~~ Super-PON corrected FEC codewords counter (Register 3.76, 3.77)

The assignment of bits in the 10G-EPON~~, and~~ Nx25G-EPON~~, and~~ Super-PON corrected FEC codewords counter register is shown in Table 45–270. See 76.3.3.3.2 for a definition of the 10G-EPON counters and 142.3.4 for the definition of the Nx25-EPON ~~and~~ Super-PON counters. These bits shall be reset to all zeros when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–270—10G-EPON~~, and~~ Nx25G-EPON~~, and~~ Super-PON corrected FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W ^a
...			

^aRO = Read only, MW = Multi-word, NR = Non Roll-over

45.2.3.42 10G-EPON~~, and~~ Nx25G-EPON~~, and~~ Super-PON uncorrected FEC codewords counter (Register 3.78, 3.79)

The assignment of bits in the 10G-EPON~~, and~~ Nx25G-EPON~~, and~~ Super-PON uncorrected FEC codewords counter register is shown in Table 45–271. See 76.3.3.3.2 for a definition of the 10G-EPON counters and 142.3.4 for the definition of the Nx25-EPON ~~and~~ Super-PON counters. These bits shall be reset to all zeros

when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–271—10G-EPON, ~~and~~ Nx25G-EPON, and Super-PON uncorrected FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
3.79.15:0	uncorrected FEC codewords ~~lowerupper~~	uncorrected_FEC_codewords_counter[321:16]	RO, MW, NR

^aRO = Read only, MW = Multi-word, NR = Non Roll-over

45.2.3.43 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G EPON, and Super-PON BER monitor interval control register (Register 3.80)

The assignment of bits in the 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G EPON, and Super-PON BER monitor interval ~~timer~~ control register is shown in Table 45–272. This register is defined only when 10GBASE-PR, 10/1GBASE-PRX, ~~or~~ Nx25G EPON, or Super-PON ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4. The Nx25G EPON and Super-PON QC-LDPC BER monitor is described in 142.3.5.6.

Table 45–272—10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G EPON, and Super-PON BER monitor interval control register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
3.80.7:0	EPON BER monitor timer interval	For 10GBASE-PR and 10/1GBASE-PRX: Duration (in units of 5 micro-seconds) of the timer used by the BER monitor function. Default value is 25 (i.e., 125 micro seconds). A value of zero indicates that the BER monitor function is disabled. For Nx25G EPON <u>and Super-PON</u> : QC-LDPC codeword count (in units of 16 codewords) of the monitoring interval used by the BER monitor function. Default value is 12 (i.e., 192 codewords).	R/W

^aRO = Read only, R/W = Read/Write

45.2.3.44 10GBASE-PR, 10/1GBASE-PRX, ~~and Nx25G EPON~~, and Super-PON BER monitor status (register 3.81)

The assignment of bits in the 10GBASE-PR, 10/1GBASE-PRX, ~~and Nx25G EPON~~, and Super-PON BER monitor status register is shown in Table 45–273. This register is defined only when 10GBASE-PR ~~or~~, 10/1GBASE-PRX, ~~or~~ Nx25G EPON, or Super-PON ONU capability is supported.

Table 45–273—10GBASE-PR, 10/1GBASE-PRX, ~~and Nx25G EPON~~, and Super-PON BER monitor status register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
3.81.1	Latched high BER	10GBASE-PR, 10/1GBASE-PRX, ~~or~~ Nx25G EPON, <u>or Super-PON</u> PCS: 1 = reported a high BER. 0 = did not report a high BER.	RO, LH
3.81.0	high BER	10GBASE-PR, 10/1GBASE-PRX, ~~or~~ Nx25G EPON, <u>or Super-PON</u> PCS: 1 = reporting a high BER. 0 = not reporting a high BER.	RO

^aRO Read only, LH = Latching high

45.2.3.44.1 10GBASE-PR, 10/1GBASE-PRX, ~~and Nx25G EPON~~, and Super-PON PCS high BER (3.81.0)

In the 10GBASE-PR, 10/1GBASE-PRX, ~~and Nx25G EPON~~, and Super-PON PCS, when read as a one, bit 3.81.0 indicates that the receiver is detecting a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.0 indicates that the receiver is detecting a BER lower than the configurable threshold (low BER state). This bit mirrors the state of the hi_ber variable, defined in 76.3.3.4 for 10GBASE-PR and, 10/1GBASE-PRX, and the HiBer variable in 142.3.5.2 for Nx25G EPON and Super-PON.

45.2.3.44.2 10GBASE-PR, 10/1GBASE-PRX, ~~and Nx25G EPON~~, and Super-PON PCS latched high BER (3.81.1)

In the 10GBASE-PR, 10/1GBASE-PRX, ~~and Nx25G EPON~~, and Super-PON PCS, when read as a one, bit 3.81.1 indicates that the receiver detected a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.1 indicates that the receiver detected BER lower than the configurable threshold (low BER state).

This bit is a latching high version of the 10GBASE-PR, 10/1GBASE-PRX, ~~and Nx25G EPON~~, and Super-PON high BER status bit (3.81.0).

45.2.3.45 10GBASE-PR, 10/1GBASE-PRX, ~~and Nx25G EPON~~, and Super-PON BER monitor threshold control (register 3.82)

The assignment of bits in the 10GBASE-PR, 10/1GBASE-PRX, ~~and Nx25G EPON~~, and Super-PON BER monitor threshold control register is shown in Table 45–274. This register is defined only when 10GBASE-PR ~~or~~, 10/1GBASE-PRX, ~~or~~ Nx25G EPON, or Super-PON ONU capability is supported. The 10G-EPON