



IEEE Standard for Ethernet

Amendment 8: Physical Layer Specifications and Management Parameters for 25 Gb/s Electrical Automotive Ethernet

IEEE Computer Society

Developed by the
LAN/MAN Standards Committee

IEEE Std 802.3cy™-2023

(Amendment to IEEE Std 802.3™-2022
as amended by IEEE Std 802.3dd™-2022,
IEEE Std 802.3cs™-2022, IEEE Std 802.3db™-2022,
IEEE Std 802.3ck™-2022, IEEE Std 802.3de™-2022,
IEEE Std 802.3cx™-2023, and IEEE Std 802.3cz™-2023)

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IEEE Std 802.3cs™-2022,
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and IEEE Std 802.3cz™-2023)

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Approved 29 June 2023
IEEE SA Standards Board

Abstract: This amendment to IEEE Std 802.3-2022 adds Physical Layer specifications and management parameters for 25 Gb/s operation on a single balanced pair of conductors suitable for automotive applications.

Keywords: 25GBASE-T1, amendment, automotive Ethernet, IEEE 802.3™, IEEE 802.3cy™, Medium Dependent Interface, Physical Coding Sublayer, Physical Layer, Physical Medium Attachment

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Introduction

This introduction is not part of IEEE Std 802.3cy-2023, IEEE Standard for Ethernet—Amendment 8: Physical Layer Specifications and Management Parameters for 25 Gb/s Electrical Automotive Ethernet.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. “Local Area Networks: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications” was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol and the ability to use an EtherType to specify the MAC client protocol were added in 1997. The title was changed to Standard for Ethernet with the 2012 Revision.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2022 and are not maintained as separate documents.

At the date of IEEE Std 802.3cy-2023 publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2022

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex K and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33A. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 140 and Annex 119A through Annex 136D. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well as 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 includes general information on 2.5 Gb/s and 5 Gb/s operation. Clause 126 through Clause 130 and associated annexes include 2.5 Gb/s and 5 Gb/s Physical Layer specifications. Clause 131 provides general information on 50 Gb/s operation. Clause 132 through Clause 140 and associated annexes include 50 Gb/s Physical Layer specifications and additional 100 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications.

Section Nine—Includes Clause 141 through Clause 160 and Annex 142A through Annex 154A. Clause 141 through Clause 144 and associated annexes specify symmetric and asymmetric operation of Ethernet passive optical networks over multiple 25 Gb/s channels. Clause 145 and associated annexes specify increased power delivery using all four pairs in the structured wiring plant. Clause 146 through Clause 149 and associated annexes specify Physical Layers for 10 Mb/s, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation over a single balanced pair of conductors. Clause 150 and Clause 151 include additional 400 Gb/s Physical Layer specifications. Clause 153 and Clause 154 specify 100 Gb/s operation over DWDM channels. Clause 157 through Clause 160 include 10 Gb/s, 25 Gb/s, and 50 Gb/s bidirectional Physical Layer specifications.

IEEE Std 802.3dd™-2022

Amendment 1—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 104, Power over Data Lines of Single Pair Ethernet, and related portions of the standard.

IEEE Std 802.3cs™-2022

Amendment 2—This amendment to IEEE Std 802.3-2022 defines Super-PON optical subscriber access networks, in the family of Ethernet passive optical networks (EPONs). Super-PON has a reach of up to 50 km and up to 1024 ONUs over a point-to-multipoint passive optical distribution network (ODN)

through wavelength division multiplexing (WDM). A Super-PON ODN contains a passive wavelength router that determines the channels used by the ODN. This standard specifies the Super-PON Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer at a MAC data rate of 10 Gb/s in the downstream direction and of 10 Gb/s or 2.5 Gb/s in the upstream direction.

IEEE Std 802.3db™-2022

Amendment 3—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 167. This amendment adds Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s over one, two, and four pairs of multimode fiber based on 100 Gb/s optical signaling.

IEEE Std 802.3ck™-2022

Amendment 4—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 161 through Clause 163, Annex 120F, Annex 120G, Annex 162A through Annex 162D, Annex 163A, and Annex 163B. This amendment includes Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s electrical interfaces based on 100 Gb/s signaling.

IEEE Std 802.3de™-2022

Amendment 5—This amendment includes changes to IEEE Std 802.3-2022 to add 10 Mb/s Single-Pair Ethernet point-to-point PHYs to the PHYs supporting the MAC Merge function and the Time Synchronization Service Interface (TSSI).

IEEE Std 802.3cx™-2023

Amendment 6—This amendment to IEEE Std 802.3-2022 modifies Clause 30, Clause 45, and Clause 90, and adds Annex 90A to enhance support for time synchronization protocols by providing options for sub-nanosecond reporting of the transmit and receive path data delays, selection of the data delay measurement point, and dynamic reporting of path data delay variation.

IEEE Std 802.3cz™-2023

Amendment 7—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 166. This amendment adds 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, and 50 Gb/s Physical Layer specifications and management parameters for optical automotive Ethernet using graded-index glass optical fiber.

IEEE Std 802.3cy™-2023

Amendment 8—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 165 and Annex 165A. This amendment adds Physical Layer specifications and management parameters for operation at 25 Gb/s over a single balanced pair of conductors.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 8: Physical Layer Specifications and Management Parameters for 25 Gb/s Electrical Automotive Ethernet

(This amendment is based on IEEE Std 802.3™-2022 as amended by IEEE Std 802.3dd™-2022, IEEE Std 802.3cs™-2022, IEEE Std 802.3db™-2022, IEEE Std 802.3ck™-2022, IEEE Std 802.3de™-2022, IEEE Std 802.3cx™-2023, and IEEE Std 802.3cz™-2023.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strike through~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.⁶

⁶ Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.4 Definitions

Insert 1.4.128a after 1.4.128 “25GBASE-T” as follows:

1.4.128a 25GBASE-T1: IEEE 802.3 Physical Layer specification for a 25 Gb/s Ethernet using a single balanced pair of conductors. (See IEEE Std 802.3, Clause 165.)

Change 1.4.407 as follows:

1.4.407 MultiGBASE-T1: PHYs that belong to the set of specific BASE-T1 PHYs at speeds in excess of 1000 Mb/s, including 2.5GBASE-T1, 5GBASE-T1, ~~and 10GBASE-T1,~~ and 25GBASE-T1. (See IEEE Std 802.3, Clause 149 and Clause 165.)

Change 1.4.472 as follows:

1.4.472 PoDL PD: A Powered Device that is intended to receive power from a link section consisting of a single ~~twisted conductor~~ pair. (See IEEE Std 802.3, Clause 104.)

Change 1.4.473 as follows:

1.4.473 PoDL PSE: A device that provides power to a PoDL PD, connected via a link section consisting of a single ~~twisted conductor~~ pair. ~~DTE powering is intended to provide a single 100BASE-T1 or 1000BASE-T1 device with a unified interface for both the reception and transmission of data as well as the power to operate.~~ (See IEEE Std 802.3, Clause 104.)

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for “25GBASE-T” as follows:

25GBASE-T1	Clause 165 25 Gb/s PAM4
------------	-------------------------

30.3.2.1.3 aPhyTypeList

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for “25GBASE-T” as follows:

25GBASE-T1	Clause 165 25 Gb/s PAM4
------------	-------------------------

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for “25GBASE-T” as follows:

25GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 165
------------	---

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for “25GBASE-T” as follows:

25GBASE-T1	25GBASE-T1 as specified in Clause 165
------------	---------------------------------------

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface registers

45.2.1 PMA/PMD registers

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Insert a new row in Table 45–9 after the row for 25GBASE-T as follows (unchanged rows not shown):

Table 45–9—Transmit fault description location

PMA/PMD	Description location
...	
25GBASE-T1	165.4.2.2
...	

45.2.1.7.5 Receive fault (1.8.10)

Insert a new row in Table 45–10 after the row for 25GBASE-T as follows (unchanged rows not shown):

Table 45–10—Receive fault description location

PMA/PMD	Description location
...	
25GBASE-T1	165.4.2.3
...	

45.2.1.16 BASE-T1 PMA/PMD extended ability register (1.18)

Change the row for bits 1.18.15:7 in Table 45–19 and insert a new row below it as follows (unchanged rows not shown):

Table 45–19—BASE-T1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.18.15:8	Reserved	Value always 0	RO
1.18.7	25GBASE-T1 ability	1 = PMA/PMD is able to perform 25GBASE-T1 0 = PMA/PMD is not able to perform 25GBASE-T1	RO
...			

^aRO = Read only

Insert 45.2.1.16.a before 45.2.1.16.1 as follows:

45.2.1.16.a 25GBASE-T1 ability (1.18.7)

When read as a one, bit 1.18.7 indicates that the PMA/PMD is able to operate as a 25GBASE-T1 PMA type.

When read as a zero, bit 1.18.7 indicates that the PMA/PMD is not able to operate as a 25GBASE-T1 PMA type.

45.2.1.214 BASE-T1 PMA/PMD control register (Register 1.2100)

Change the row for bits 1.2100.3:0 in Table 45–178 as follows (unchanged rows not shown):

Table 45–178—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
1.2100.3:0	Type Selection	3 2 1 0 1 x x x = Reserved ~~0 1 1 1 = Reserved~~ <u>0 1 1 1 = 25GBASE-T1</u> 0 1 1 0 = 10GBASE-T1 0 1 0 1 = 5GBASE-T1 0 1 0 0 = 2.5GBASE-T1 0 0 1 1 = 10BASE-T1S 0 0 1 0 = 10BASE-T1L 0 0 0 1 = 1000BASE-T1 0 0 0 0 = 100BASE-T1	R/W

^aRO = Read only, R/W = Read/Write

45.2.1.214.2 Type selection (1.2100.3:0)

Change 45.2.1.214.2 as follows:

Bits 1.2100.3:0 are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. When these bits are set to 0000, the mode of operation is 100BASE-T1. When these bits are set to 0001, the mode of operation is 1000BASE-T1. When these bits are set to 0010, the mode of operation is 10BASE-T1L. When these bits are set to 0011, the mode of operation is 10BASE-T1S. When these bits are set to 0100, the mode of operation is 2.5GBASE-T1. When these bits are set to 0101, the mode of operation is 5GBASE-T1. When these bits are set to 0110, the mode of operation is 10GBASE-T1. When these bits are set to 0111, the mode of operation is 25GBASE-T1. These bits shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

45.2.1.244 MultiGBASE-T1 training register (1.2311)

Change the row for bits 1.2311.12:11 in Table 45–206 as follows (unchanged rows not shown):

Table 45–206—MultiGBASE-T1 training register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
1.2311.12:11	Interleave request	12 11 0 0: L=1, no interleaving, default for 2.5GBASE-T1 0 1: L=2, RS-FEC interleaving factor two, default for 5GBASE-T1, ~~undefined~~ defined for 2.5GBASE-T1 1 0: L=4, RS-FEC interleaving factor four, default for 10GBASE-T1, ~~undefined~~ defined for 2.5GBASE-T1 and 5GBASE-T1 1 1: ~~Reserved~~ L=8, RS-FEC interleaving factor eight, <u>default for 25GBASE-T1, not defined for 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1</u>	R/W
...			

^aRO = Read only, R/W = Read/Write

45.2.1.244.1 Interleave request (1.2311.12:11)

Change 45.2.1.244.1 as follows:

Bits 1.2311.12:11 control the Reed-Solomon interleave setting of this PHY. Reed-Solomon interleaving is described in [149.3.2.2.15](#) and [165.3.2.2.15](#). This is communicated to the link partner via Infobfields as specified in [149.4.2.4.5](#) and [165.4.2.4.5](#).

The values of L = 2, ~~and L = 4, and L = 8~~ are not defined for 2.5GBASE-T1 PHYs, ~~and the values of L = 4 and L = 8 are~~ is not defined for 5GBASE-T1 PHYs, ~~and the value of L = 8 is not defined for 10GBASE-T1 PHYs~~. If bits 1.2311.12:11 are set to these ~~undefined~~ values, the PHY ~~will~~ communicates these values to the link partner, but the requested interleaver depth is out of scope of this standard and may not be supported by the link partner.

45.2.1.245 MultiGBASE-T1 link partner training register (1.2312)

Change the row for bits 1.2312.12:11 in Table 45–207 as follows (unchanged rows not shown):

Table 45–207—MultiGBASE-T1 link partner training register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
1.2312.12:11	Link partner interleave request	12 11 0 0: L=1, no interleaving, default for 2.5GBASE-T1 0 1: L=2, RS-FEC interleaving factor two, default for 5GBASE-T1, ~~undefined~~ for 2.5GBASE-T1 1 0: L=4, RS-FEC interleaving factor four, default for 10GBASE-T1, ~~undefined~~ for 2.5GBASE-T1 and 5GBASE-T1 1 1: ~~Reserved~~ L=8, RS-FEC interleaving factor eight, default for 25GBASE-T1, not defined for 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1	RO
...			

^aRO = Read only

45.2.1.245.1 Link partner interleave request (1.2312.12:11)

Change 45.2.1.245.1 as follows:

Bits 1.2312.12:11 contain the Reed-Solomon interleave setting requested by the link partner. Reed-Solomon interleaving is described in [149.3.2.2.15](#) and [165.3.2.2.15](#). This is communicated by the link partner via Infobfields as specified in [149.4.2.4.5](#) and [165.4.2.4.5](#).

The values of L = 2, ~~and L = 4, and L=8~~ are not defined for 2.5GBASE-T1 PHYs, ~~and the values of L = 4 and L=8~~ are not defined for 5GBASE-T1 PHYs, and the value of L=8 is not defined for 10GBASE-T1 PHYs. Bits 1.2312.12:11 ~~will~~ indicate whatever value is received from the link partner, but if the ~~undefined~~ not defined values are received, the requested interleaver depth is out of scope of this standard and may not be supported by the local PHY.

45.2.1.246 MultiGBASE-T1 test mode control register (1.2313)

45.2.1.246.1 Test mode control (1.2313.15:13)

Change 45.2.1.246.1 as follows:

Transmitter test mode operations defined by bits 1.2313.15:13, are described in [149.5.1](#) ~~and~~ Table 149–17, 165.5.1, and Table 165–12. The default value for bits 1.2313.15:13 is zero.

45.2.1.246.2 Local transmitter precoder override (1.2313.11)

Change 45.2.1.246.2 as follows:

When bit 1.2313.11 is set to one, the local transmitter's precoder shall be controlled by the value of bits 1.2313.10:9, and the precoder requested by the link partner in PrecodeSel shall be ignored. When bit

1.2313.11 is set to zero, the transmitter shall ignore bits 1.2313.10:9, and the precoder is set according to the value of PrecoderSel received from the link partner as specified in [149.3.2.2.20](#) and [165.3.2.2.20](#). The default value of 1.2313.11 is zero.

45.2.1.246.3 Local transmit precoder setting (1.2313.10:9)

Change 45.2.1.246.3 as follows:

When bit 1.2313.11 is set to one, bits 1.2313.10:9 control the precoder setting of the local transmitter, as defined in [149.3.2.2.20](#) and [165.3.2.2.20](#) in the variable precoder_type.

45.2.1.246.4 Jitter test control (1.2313.1:0)

When the transmitter is in test mode 2, bits 1.2313.1:0 control the pattern of the jitter test signal. When the transmitter is not in test mode 2, the setting of bits 1.2313.1:0 has no effect. A value of 00 transmits a square wave from the transmitter, a value of 01 transmits the JP03A pattern, and a value of 10 transmits the JP03B pattern. See [149.5.2.3.1](#) and [149.5.2.3.2](#), [165.5.3.3.1](#), and [165.5.3.3.2](#) for more information.

45.2.3 PCS Registers

45.2.3.87 MultiGBASE-T1 PCS status 2 register (Register 3.2324)

45.2.3.87.2 PCS high RFER (3.2324.9)

Change 45.2.3.87.2 as follows:

When read as a one, bit 3.2324.9 indicates that the MultiGBASE-T1 PCS receiver is detecting 16 or more RS-FEC errored blocks within 88 RS-FEC frames in 312 500 bit times (one rfer_timer interval). When read as a zero, bit 3.2324.9 indicates that the MultiGBASE-T1 PCS is detecting fewer than 16 RS-FEC errored blocks within 88 RS-FEC frames in 312 500 bit times. Bit 3.2324.9 is a reflection of the state of the hi_rfer variable defined in [149.3.7.2.2](#) ~~149.3.8.1~~.

78. Energy-Efficient Ethernet (EEE)

78.1 Overview

78.1.4 PHY types optionally supporting EEE

Insert a row for 25GBASE-T1 after the row for 25GBASE-CR in Table 78–1 as follows (unchanged rows not shown):

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
...	
25GBASE-T1	165
...	

78.2 LPI mode timing parameters description

Insert a row for 25GBASE-T1 above the row for 25GBASE-T in Table 78–2 as follows:

Table 78–2—Summary of the key EEE parameters for supported PHYs or interfaces

PHY or interface type	T_s (μ s)		T_q (μ s)		T_r (μ s)	
	Min	Max	Min	Max	Min	Max
...						
25GBASE-T1	5.3248	5.3248	31.616	31.616	0.3328	0.3328
...						

78.3 Capabilities Negotiation

Insert a new sentence at the end of the first paragraph of 78.3 as follows:

The EEE capability for 25GBASE-T1 is advertised during link training according to 165.4.2.4.

Change the last sentence of the second paragraph of 78.3 as follows:

The same applies to 2.5GBASE-T, 2.5GBASE-T1, 5GBASE-T, 5GBASE-T1, 10GBASE-T1, 25GBASE-T, 25GBASE-T1, and 40GBASE-T except that the EEE capabilities are exchanged and resolved during link training instead of during Auto-Negotiation.

78.5 Communication link access latency

Insert a row in Table 78–4 for 25GBASE-T1 above the row for 25GBASE-T as follows (unchanged rows not shown):

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w_sys_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy_shrink_tx}$ (max) (μs)	$T_{phy_shrink_rx}$ (max) (μs)	$T_{w_sys_rx}$ (min) (μs)
...						
25GBASE-T1	Case-1	15.9744	15.9744	10.6496	0	5.325
	Case-2	9.318	9.318	3.994	0	5.325
	Case-3	45.2608	45.2608	39.936	0	5.325
	Case-4	38.6	38.6	33.28	0	5.325
...						

98. Auto-Negotiation for single differential-pair media

98.5 Detailed functions and state diagrams

98.5.1 State diagram variables

Insert a new item at the end of the dashed list after the first paragraph of 98.5.1 as follows:

- 25GigT1; represents that the 25GBASE-T1 PMA is the signal source.

104. Power over Data Lines (PoDL) of Single-Pair Ethernet

104.1 Overview

104.1.3 PoDL system types

Change the last sentence of the second paragraph in 104.1.3 as follows:

A Type F PSE and Type F PD are compatible with 2.5GBASE-T1, 5GBASE-T1, ~~and~~ 10GBASE-T1, and
25GBASE-T1 PHYs.

105. Introduction to 25 Gb/s networks

105.1 Overview

105.1.2 Relationship of 25 Gigabit Ethernet to the ISO OSI reference model

Replace Figure 105–1 as amended by IEEE Std 802.3cz-2023 with the following figure, which adds 25GBASE-T1 and NOTE 2:

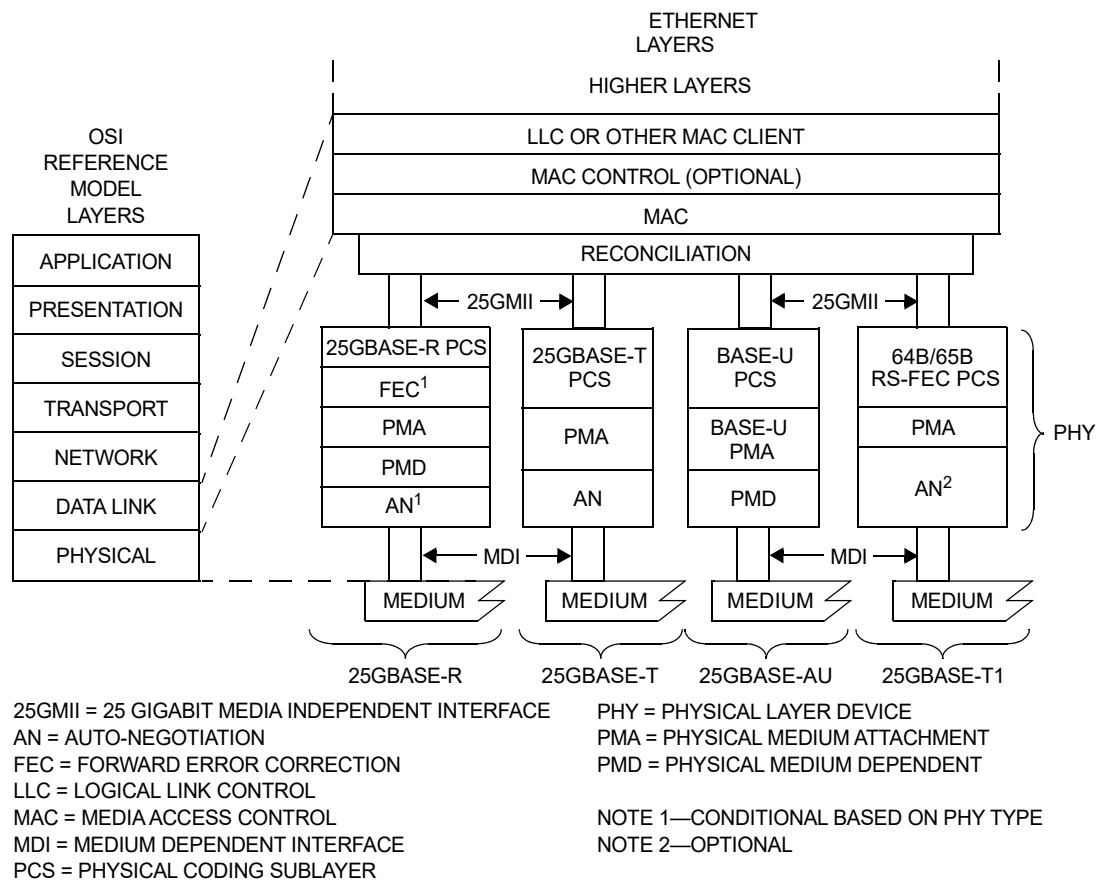


Figure 105–1—Architectural positioning of 25 Gigabit Ethernet

Insert a new item e) at the end of the lettered list in 105.1.2 as follows:

- e) The MDI as specified in Clause 165 for 25GBASE-T1 uses a single-lane data path.

105.1.3 Nomenclature

Insert a new paragraph after the fourth paragraph of 105.1.3 that begins “25GBASE-AU represents” (as inserted by IEEE Std 802.3cz-2023) as follows:

25GBASE-T1 represents Physical Layer devices using Clause 165 Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, for data communication at 25 Gb/s over a point-to-point single balanced pair of conductors. 25GBASE-T1 uses Reed-Solomon FEC and PAM4 modulation.

Insert a row for 25GBASE-T1 after the row for 25GBASE-CR in Table 105–1 (as amended by IEEE Std 802.3cz-2023) as follows (unchanged rows not shown):

Table 105–1—25 Gb/s PHYs

Name	Description
...	
25GBASE-T1	25 Gb/s PHY using Reed-Solomon encoding and PAM4 modulation over a single balanced pair of conductors (see Clause 165).
...	

105.2 Physical Layer signaling systems

Change Table 105–2 (as amended by IEEE Std 802.3cz-2023) as follows:

Table 105–2—Nomenclature and clause correlation, 25 Gb/s Ethernet PHYs

Nomenclature	Clause/Annex																					
	28	73	98	74	78	106	107	108	109	109A	109B	110	111	112	113	114	165	166				
	Auto-Negotiation	Auto-Negotiation	Auto-Negotiation	BASE-R FEC	EEE	RS	25GMII	25GBASE-R PCS	25GBASE-R RS-FEC	PMA	25GAUI C2C	25GAUI C2M	25GBASE-CR PMD	25GBASE-CR-S PMD	25GBASE-KR PMD	25GBASE-KR-S PMD	25GBASE-SR PMD	25GBASE-T PCS/PMA	25GBASE-LR PMD	25GBASE-ER PMD	25GBASE-T1 PCS/PMA	25 BASE-AU PCS/PMA/PMD
25GBASE-KR-S		M ^a		M	O ^a	M	O	M		M	O					M						
25GBASE-KR		M		M	O	M	O	M	M	M	O				M							
25GBASE-CR-S		M		M	O	M	O	M		M	O			M								
25GBASE-CR		M		M	O	M	O	M	M	M	O		M									
25GBASE-T1			O		O	M	O														M	
25GBASE-T	M				O	M	O										M					
25GBASE-AU					O	M	O															M
25GBASE-SR					O	M	O	M	M	M	O	O					M					
25GBASE-LR					O	M	O	M	M	M	O	O							M			
25GBASE-ER					O	M	O	M	M	M	O	O								M		

^a O = Optional, M = Mandatory

105.3 Summary of 25 Gigabit Ethernet sublayers

105.3.2 Physical Coding Sublayer (PCS)

Insert a new paragraph at the end of 105.3.2 as follows:

A 25GBASE-T1 PHY uses the PCS specified in Clause 165. The 25GBASE-T1 PCS performs encoding of data from the 25GMII to 64B/65B RS-FEC code blocks and PAM4 modulation. It then transfers the symbols to the PMA and performs error correction and decoding of PAM4 symbols from the PMA and transfers the decoded data to the 25GMII.

105.3.4 Physical Medium Attachment (PMA) sublayer

Insert a new paragraph at the end of 105.3.4 as follows:

A 25GBASE-T1 PHY uses the PMA specified in Clause 165. The PMA provides for full duplex communications over a single balanced pair of conductors.

105.3.6 Auto-Negotiation (AN)

Insert new paragraph at the end of 105.3.6 as follows:

Clause 98 Auto-Negotiation may be used by the 25GBASE-T1 PHY, but is not required.

105.5 Delay constraints

Insert new rows for 25GBASE-T1 after the row for 25GBASE-T in Table 105–3 (as amended by IEEE Std 802.3cz-2023) as follows (unchanged rows not shown):

Table 105–3—Sublayer delay constraints

Sublayer	Maximum (bit time) ^a	Maximum (pause_quantum) ^b	Maximum (ns)	Notes ^c
...				
25GBASE-T1 PHY	25 600	50	1024	No interleave, see 165.10.
	36 864	72	1474.56	2x interleave, see 165.10.
	58 880	115	2355.2	4x interleave, see 165.10.
	102 400	200	4096	8x interleave, see 165.10.
...				

^a 1 bit time (BT) is equal to 40 ps. (See 1.4.215 for the definition of bit time.)

^b 1 pause_quantum is equal to 20.48 ns. (See 31B.2 for the definition of pause_quantum.)

^c Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

105.7 Protocol implementation conformance statement (PICS) proforma

Change the first paragraph of 105.7 (as amended by IEEE Std 802.3cz-2023) as follows:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 45, [Clause 73](#), [Clause 74](#), [Clause 106](#) through [Clause 112](#), [Clause 114](#), [Clause 166](#), [Clause 165](#), and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

149. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1

149.3 Physical Coding Sublayer (PCS) functions

149.3.7 Detailed functions and state diagrams

149.3.7.2 State diagram parameters

149.3.7.2.2 Variables

Change the definition of “hi_rfer” in 149.3.7.2.2 as follows:

hi_rfer

Boolean variable that is asserted TRUE when the rfer_cnt reaches 16 errors in one RFRX_CNT_LIMIT ~~rfer_timer~~ interval.

Insert new Clause 165 after Clause 164 as follows:

165. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 25GBASE-T1

165.1 Overview

This clause defines the type 25GBASE-T1 Physical Coding Sublayer (PCS) as well as the 25GBASE-T1 Physical Medium Attachment (PMA) sublayer. Together, the corresponding PCS, PMA, and optional Auto-Negotiation sublayers comprise a 25GBASE-T1 Physical Layer device (PHY). Provided in this clause are functional and electrical specifications for the type 25GBASE-T1 PCS and PMA.

A 25GBASE-T1 PHY is intended to be operated over a single balanced pair of conductors. The link segment specifications defined in 165.7 were derived from automotive requirements, but can also be used for non-automotive applications. The conductors supporting the operation of a 25GBASE-T1 PHY are defined in terms of performance requirements between the Medium Dependent Interfaces (MDIs) allowing implementers to provide their own conductors to operate a 25GBASE-T1 PHY as long as the normative requirements included in 165.7 are met.

This clause also specifies an optional Energy-Efficient Ethernet (EEE) capability. A 25GBASE-T1 PHY that supports this capability may enter a Low Power Idle (LPI) mode of operation during periods of low link utilization as described in Clause 78.

165.1.1 Nomenclature

The 25GBASE-T1 PHY defined in this clause is a member of the MultiGBASE-T1 PHY set, as defined in 1.4.407. PHYs in this set share control registers and characteristics. The term ‘MultiGBASE-T1’, when used in this clause, refers to registers and features common to PHYs in this set.

165.1.2 Relationship of 25GBASE-T1 to other standards

The relationship between a 25GBASE-T1 PHY, the ISO Open Systems Interconnection (OSI) reference model, and the IEEE 802.3 Ethernet model is shown in Figure 165–1. The PHY sublayers shown shaded in Figure 165–1 are specified in this clause, while the optional Auto-Negotiation sublayer for a 25GBASE-T1 PHY is defined in Clause 98. The 25GBASE-T1 PHY connects one [Clause 4](#) Media Access Control (MAC) layer to the medium.

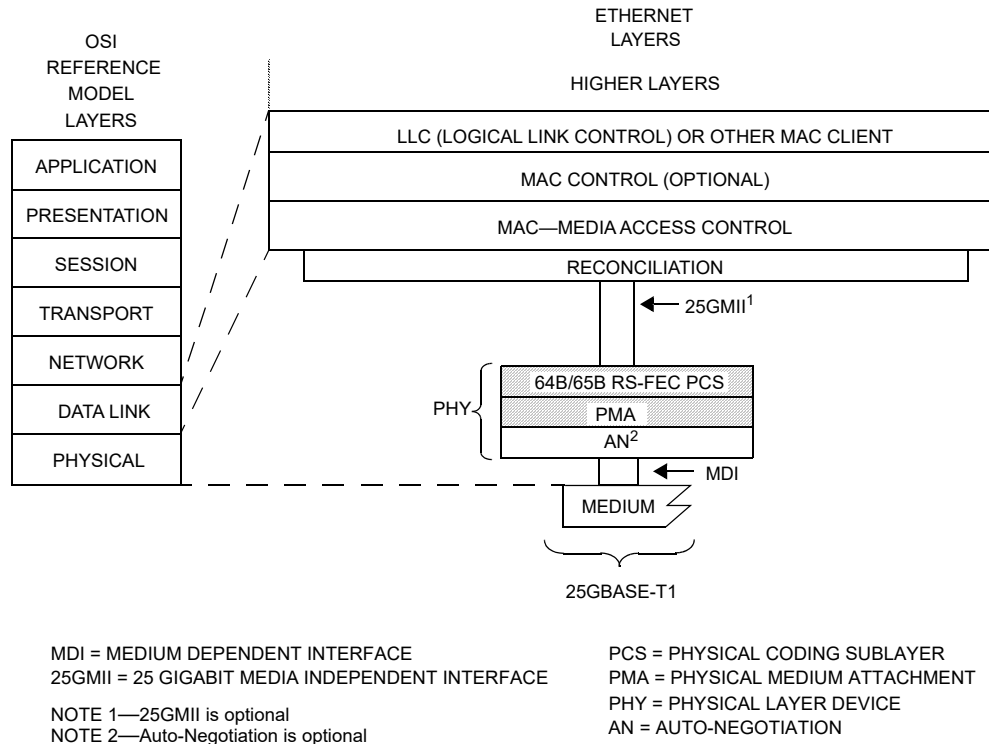


Figure 165-1—Relationship of the 25GBASE-T1 PHY to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

165.1.3 Operation of 25GBASE-T1

The 25GBASE-T1 PHY operates using full-duplex communications over a shielded balanced pair of conductors with an effective rate of 25 Gb/s in each direction simultaneously while meeting the requirements (EMC, temperature, etc.) of automotive environments. The PHY supports operation on an automotive link segment supporting up to two in-line connectors using a single shielded balanced pair of conductors for up to at least 11 m. The 25GBASE-T1 PHY utilizes 4-level pulse amplitude modulation (PAM4) transmitted at 14.0625 GBd. A 33-bit scrambler is used to improve the EMC performance. 25GMII TXD and TXC are encoded together using 64B/65B encoding. To maintain a frame loss ratio (FLR) equivalent to a bit error ratio (BER) of less than or equal to 10^{-12} , a 25GBASE-T1 PHY adds 900 bits of Reed-Solomon forward error correction (RS-FEC) parity to each group of 130 64B/65B blocks. The PAM4 mapping, scrambler, RS-FEC, interleaver, and PAM4 encoder/decoder are all contained in the PCS (see 165.3).

Auto-Negotiation (Clause 98) may optionally be used by 25GBASE-T1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for normal operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding. The implementation of the Auto-Negotiation function is optional. If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.

A 25GBASE-T1 PHY shall be capable of operating as MASTER or SLAVE, per runtime configuration. A MASTER PHY uses a local clock to determine the timing of transmitter operations. A SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations. When Auto-Negotiation is used, the MASTER-SLAVE relationship between two devices sharing a link segment is established during Auto-Negotiation (see Clause 98). If Auto-Negotiation is not used, a MASTER-SLAVE relationship shall be established by management or hardware configuration of a PHY,

and the MASTER and SLAVE are synchronized by the PHY Link Synchronization function in the PHY (see 165.4.2.6).

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

A 25GBASE-T1 PHY may optionally support Energy-Efficient Ethernet (see Clause 78) and advertise the EEE capability as described in 165.4.2.4.5. The EEE capability is a mechanism by which a 25GBASE-T1 PHY adapts signaling during periods of low link utilization to provide opportunities for reduced power consumption independently for each direction of the link.

The 25GBASE-T1 PHY may optionally support the PCS-based operations, administration, and maintenance (OAM). The OAM is useful for monitoring link operation by exchanging PHY link health status and messages. The OAM information for 25GBASE-T1 is exchanged between two 25GBASE-T1 PHYs by interspersing it with the 25 Gb/s Ethernet data stream. The OAM for 25GBASE-T1 is specified in 165.3.9, and the 25GBASE-T1 PHY advertises the OAM for 25GBASE-T1 capability as described in 165.4.2.4.5.

The 25GBASE-T1 PMA couples messages from the PCS to the MDI and provides clock recovery, link management, and PHY Control functions. The PMA provides full duplex communications at 14.0625 GBd for 25GBASE-T1 over a link segment meeting the specifications of 165.7. PMA functionality is described in 165.4. The MDI is specified in 165.8. Figure 165–2 shows the functional block diagram.

165.1.3.1 Physical Coding Sublayer (PCS)

The PCS couples a 25 Gigabit Media Independent Interface (25GMII), as described in Clause 106, to the 25GBASE-T1 Physical Medium Attachment (PMA) sublayer.

In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in normal mode, the PCS receives eight 25GMII data octets provided by two consecutive transfers on the 25GMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two 25GMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 130 blocks. The contents of each group are contained in a vector tx_group130x65B. Next, a 10-bit OAM field is appended to form an 8460-bit RS-FEC input frame. A number, L (see 165.3.2.2.15), of these 8460-bit blocks are formed into an RS-FEC input superframe, then encoded by the RS-FEC(936,846) over $GF(2^{10})$ and the round-robin interleaving as described in 165.3.2.2.16. The RS-FEC output superframe consists of $L \times 9360$ bits. The duration of the superframe is $L \times 332.8$ ns. Finally these bits are exclusive OR'd with a degree 33 scrambler to create the payload. PCS transmit functions are described in 165.3.2.2.

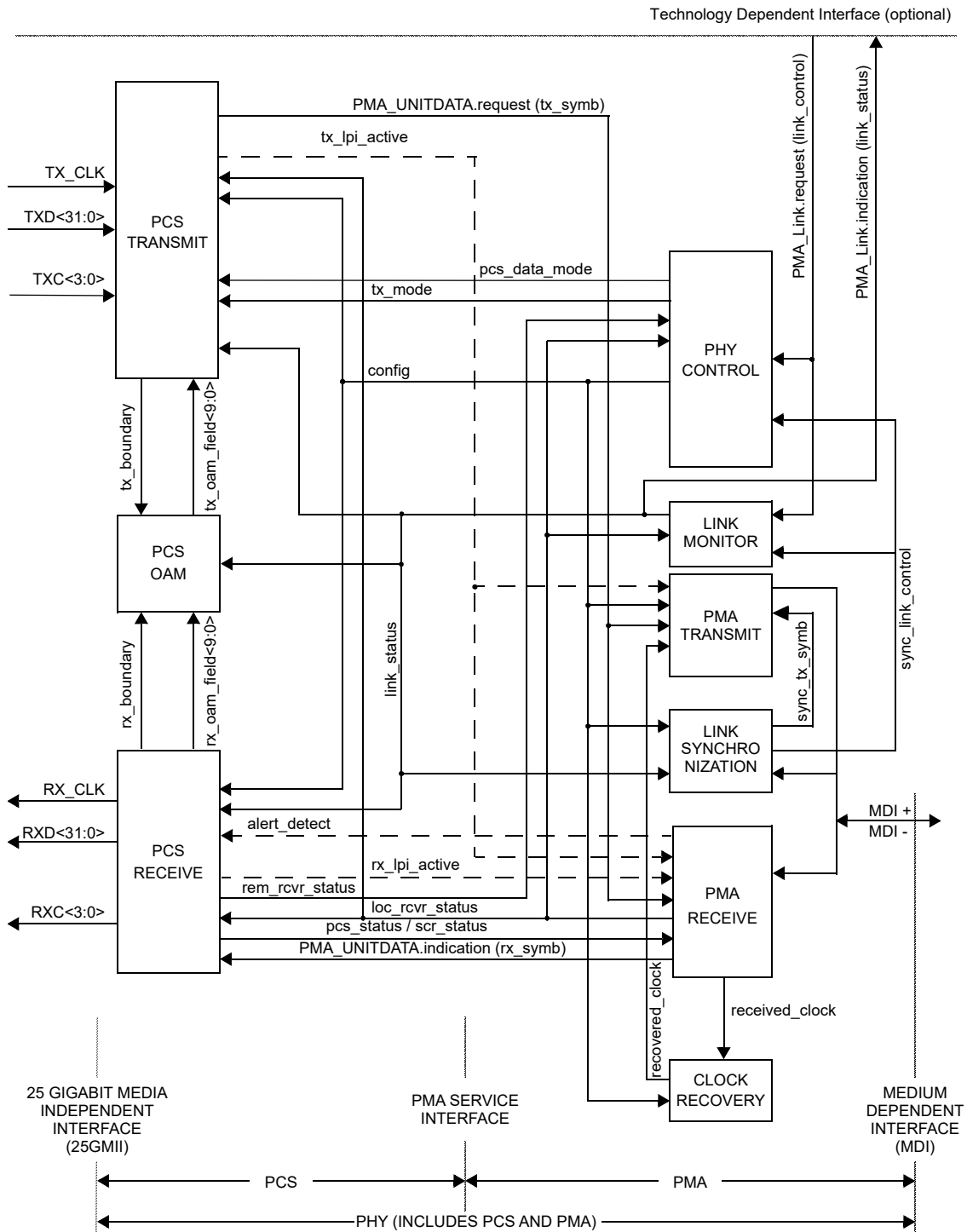
tx_group130x65B<8449:0> is defined as:

$$\text{tx_group130x65B}\langle 65 \times i + j \rangle = \text{tx_coded}_i\langle j \rangle$$

where $i = 0$ to 129, $j = 0$ to 64, and tx_coded _{i} <64:0> is the i th 64B/65B block where tx_coded₀<64:0> is the first block transmitted.

In the training mode (see 165.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges EEE and OAM capabilities.

Details of the PCS functions and state diagrams are covered in 165.3. The interface to the PMA is an abstract message-passing interface specified in 165.4.



NOTE 1—The recovered clock arc is shown to indicate delivery of the received clock signal back to PMA TRANSMIT for loop timing.

NOTE 2—Signals and functions shown with dashed lines are optional.

NOTE 3—The optional AN sublayer is not shown between the PMA sublayer and the MDI.

Figure 165–2—Functional block diagram