



IEEE Standard for Ethernet

Amendment 7: Physical Layer Specifications and Management Parameters for Multi-Gigabit Glass Optical Fiber Automotive Ethernet

IEEE Computer Society

Developed by the
LAN/MAN Standards Committee

IEEE Std 802.3cz™-2023

(Amendment to IEEE Std 802.3™-2022
as amended by IEEE Std 802.3dd™-2022,
IEEE Std 802.3cs™-2022, IEEE Std 802.3db™-2022,
IEEE Std 802.3ck™-2022, IEEE Std 802.3de™-2022,
and IEEE Std 802.3cx™-2023)

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as amended by IEEE Std 802.3dd™-2022,
IEEE Std 802.3cs™-2022,
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Approved 30 March 2023
IEEE SA Standards Board

Abstract: This amendment to IEEE Std 802.3-2022 adds Physical Layer specifications and management parameters for 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, and 50 Gb/s operation on glass optical fiber in an automotive environment.

Keywords: 2.5GBASE-AU, 5GBASE-AU, 10GBASE-AU, 25GBASE-AU, 50GBASE-AU, amendment, automotive Ethernet, Ethernet, IEEE 802.3™, IEEE 802.3cz™, Medium Dependent Interface, Physical Coding Sublayer, Physical Layer, Physical Medium Attachment

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Introduction

This introduction is not part of IEEE Std 802.3cz-2023, IEEE Standard for Ethernet—Amendment 7: Physical Layer Specifications and Management Parameters for Multi-Gigabit Glass Optical Fiber Automotive Ethernet.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. “Local Area Networks: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications” was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol and the ability to use an EtherType to specify the MAC client protocol were added in 1997. The title was changed to Standard for Ethernet with the 2012 Revision.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2022 and are not maintained as separate documents.

At the date of IEEE Std 802.3cz-2023 publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2022

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex K and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33A. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 140 and Annex 119A through Annex 136D. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well as 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 includes general information on 2.5 Gb/s and 5 Gb/s operation. Clause 126 through Clause 130 and associated annexes include 2.5 Gb/s and 5 Gb/s Physical Layer specifications. Clause 131 provides general information on 50 Gb/s operation. Clause 132 through Clause 140 and associated annexes include 50 Gb/s Physical Layer specifications and additional 100 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications.

Section Nine—Includes Clause 141 through Clause 160 and Annex 142A through Annex 154A. Clause 141 through Clause 144 and associated annexes specify symmetric and asymmetric operation of Ethernet passive optical networks over multiple 25 Gb/s channels. Clause 145 and associated annexes specify increased power delivery using all four pairs in the structured wiring plant. Clause 146 through Clause 149 and associated annexes specify Physical Layers for 10 Mb/s, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation over a single balanced pair of conductors. Clause 150 and Clause 151 include additional 400 Gb/s Physical Layer specifications. Clause 153 and Clause 154 specify 100 Gb/s operation over DWDM channels. Clause 157 through Clause 160 include 10 Gb/s, 25 Gb/s, and 50 Gb/s bidirectional Physical Layer specifications.

IEEE Std 802.3dd™-2022

Amendment 1—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 104, Power over Data Lines of Single Pair Ethernet, and related portions of the standard.

IEEE Std 802.3cs™-2022

Amendment 2—This amendment to IEEE Std 802.3-2022 defines Super-PON optical subscriber access networks, in the family of Ethernet passive optical networks (EPONs). Super-PON has a reach of up to 50 km and up to 1024 ONUs over a point-to-multipoint passive optical distribution network (ODN)

through wavelength division multiplexing (WDM). A Super-PON ODN contains a passive wavelength router that determines the channels used by the ODN. This standard specifies the Super-PON Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer at a MAC data rate of 10 Gb/s in the downstream direction and of 10 Gb/s or 2.5 Gb/s in the upstream direction.

IEEE Std 802.3db™-2022

Amendment 3—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 167. This amendment adds Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s over one, two, and four pairs of multimode fiber based on 100 Gb/s optical signaling.

IEEE Std 802.3ck™-2022

Amendment 4—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 161 through Clause 163, Annex 120F, Annex 120G, Annex 162A through Annex 162D, Annex 163A, and Annex 163B. This amendment includes Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s electrical interfaces based on 100 Gb/s signaling.

IEEE Std 802.3de™-2022

Amendment 5—This amendment includes changes to IEEE Std 802.3-2022 to add 10 Mb/s Single-Pair Ethernet point-to-point PHYs to the PHYs supporting the MAC Merge function and the Time Synchronization Service Interface (TSSI).

IEEE Std 802.3cx™-2023

Amendment 6—This amendment to IEEE Std 802.3-2022 modifies Clause 30, Clause 45, and Clause 90, and adds Annex 90A to enhance support for time synchronization protocols by providing options for sub-nanosecond reporting of the transmit and receive path data delays, selection of the data delay measurement point, and dynamic reporting of path data delay variation.

IEEE Std 802.3cz™-2023

Amendment 7—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 166. This amendment adds 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, and 50 Gb/s Physical Layer specifications and management parameters for optical automotive Ethernet using graded-index glass optical fiber.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 7: Physical Layer Specifications and Management Parameters for Multi-Gigabit Glass Optical Fiber Automotive Ethernet

(This amendment is based on IEEE Std 802.3™-2022 as amended by IEEE Std 802.3dd™-2022, IEEE Std 802.3cs™-2022, IEEE Std 802.3db™-2022, IEEE Std 802.3ck™-2022, IEEE Std 802.3de™-2022, and IEEE Std 802.3cx™-2023.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~striking through~~ (to remove old material) and underscoring (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.⁶

⁶ Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.4 Definitions

Insert a new definition for “10GBASE-AU” after 1.4.62 “10BROAD36” as follows:

1.4.62a 10GBASE-AU: IEEE 802.3 Physical Layer specification for 10 Gb/s full duplex Ethernet operation over multimode glass optical fiber in an automotive environment. (See IEEE Std 802.3, Clause 166.)

Insert a new definition for “2.5GBASE-AU” after 1.4.95 “1G-EPON” as follows:

1.4.95a 2.5GBASE-AU: IEEE 802.3 Physical Layer specification for 2.5 Gb/s full duplex Ethernet operation over multimode glass optical fiber in an automotive environment. (See IEEE Std 802.3, Clause 166.)

Insert a new definition for “25GBASE-AU” after 1.4.116 “25GBASE” as follows:

1.4.116a 25GBASE-AU: IEEE 802.3 Physical Layer specification for 25 Gb/s full duplex Ethernet operation over multimode glass optical fiber in an automotive environment. (See IEEE Std 802.3, Clause 166.)

Insert a new definition for “50GBASE-AU” after 1.4.165 “50/50G-EPON” as follows:

1.4.165a 50GBASE-AU: IEEE 802.3 Physical Layer specification for 50 Gb/s full duplex Ethernet operation over multimode glass optical fiber in an automotive environment. (See IEEE Std 802.3, Clause 166.)

Insert a new definition for “5GBASE-AU” after 1.4.178 “50G-EPON” as follows:

1.4.178a 5GBASE-AU: IEEE 802.3 Physical Layer specification for 5 Gb/s full duplex Ethernet operation over multimode glass optical fiber in an automotive environment. (See IEEE Std 802.3, Clause 166.)

Insert a new definition for “BASE-AU” after 1.4.204 “Base Page” as follows:

1.4.204a BASE-AU: The set of PHYs that use a BASE-U PCS and PMA with PMD specifications for operation over multimode glass optical fiber in an automotive environment, including 2.5GBASE-AU, 5GBASE-AU, 10GBASE-AU, 25GBASE-AU, and 50GBASE-AU. (See IEEE Std 802.3, Clause 166.)

Insert a new definition for “BASE-U” after 1.4.206 “BASE-T1” as follows:

1.4.206a BASE-U: IEEE 802.3 PCS and PMA sublayer specifications used by a family of Physical Layer devices. (See IEEE Std 802.3, Clause 166.)

Change 1.4.464 as follows:

1.4.464 physical header data (PHD): ~~Side An~~ information block embedded inside a Transmit Block that is used to exchange control information and for negotiation of PCS and PMA parameters between two link partners. (See IEEE Std 802.3, Clause 115 and Clause 166.)

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for “1000BASE-X” as follows:

2.5GBASE-AU Clause 166 2.5 Gb/s NRZ

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for “2.5GBASE-X” as follows:

5GBASE-AU Clause 166 5 Gb/s NRZ

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for “10/2.5GBASE-SP” (inserted by IEEE Std 802.3cs-2022) as follows:

10GBASE-AU Clause 166 10 Gb/s NRZ

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for “25/10GBASE-PQ” as follows:

25GBASE-AU Clause 166 25 Gb/s NRZ

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for “50/25GBASE-PQ” as follows:

50GBASE-AU Clause 166 50 Gb/s PAM4

30.3.2.1.3 aPhyTypeList

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for “1000BASE-X” as follows:

2.5GBASE-AU Clause 166 2.5 Gb/s NRZ

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for “2.5GBASE-X” as follows:

5GBASE-AU Clause 166 5 Gb/s NRZ

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for “10/2.5GBASE-SP” (inserted by IEEE Std 802.3cs-2022) as follows:

10GBASE-AU Clause 166 10 Gb/s NRZ

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for “25/10GBASE-PQ” as follows:

25GBASE-AU Clause 166 25 Gb/s NRZ

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for “50/25GBASE-PQ” as follows:

50GBASE-AU Clause 166 50 Gb/s PAM4

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for “1000BASE-XHD” as follows:

2.5GBASE-AU Glass optical fiber PHY as specified in Clause 166

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for “2.5GBASE-X” as follows:

5GBASE-AU Glass optical fiber PHY as specified in Clause 166

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for “10/2.5GBASE-SPI-Uxy” (inserted by IEEE Std 802.3cs-2022) as follows:

10GBASE-AU Glass optical fiber PHY as specified in Clause 166

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for “25/10GBASE-PQX-U3” as follows:

25GBASE-AU Glass optical fiber PHY as specified in Clause 166

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for “50/25GBASE-PQX-U3” as follows:

50GBASE-AU Glass optical fiber PHY as specified in Clause 166

44. Introduction to 10 Gb/s baseband networks

44.1 Overview

44.1.1 Scope

Change the first paragraph of 44.1.1 as follows:

10 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 10 Gb/s, coupled with any IEEE 802.3 10GBASE Physical Layer implementation, ~~connected through a 10-Gigabit Media Independent Interface (XGMII) to Physical Layer devices (PHYs) such as 10GBASE-SR, 10GBASE-LX4, 10GBASE-CX4, 10GBASE-LRM, 10GBASE-LR, 10GBASE-ER, 10GBASE-SW, 10GBASE-LW, 10GBASE-EW, 10GBASE-T, and 10GBASE-T1.~~

44.1.3 Relationship of 10 Gigabit Ethernet to the ISO OSI reference model

Replace Figure 44–1 with the following figure, which adds 10GBASE-AU:

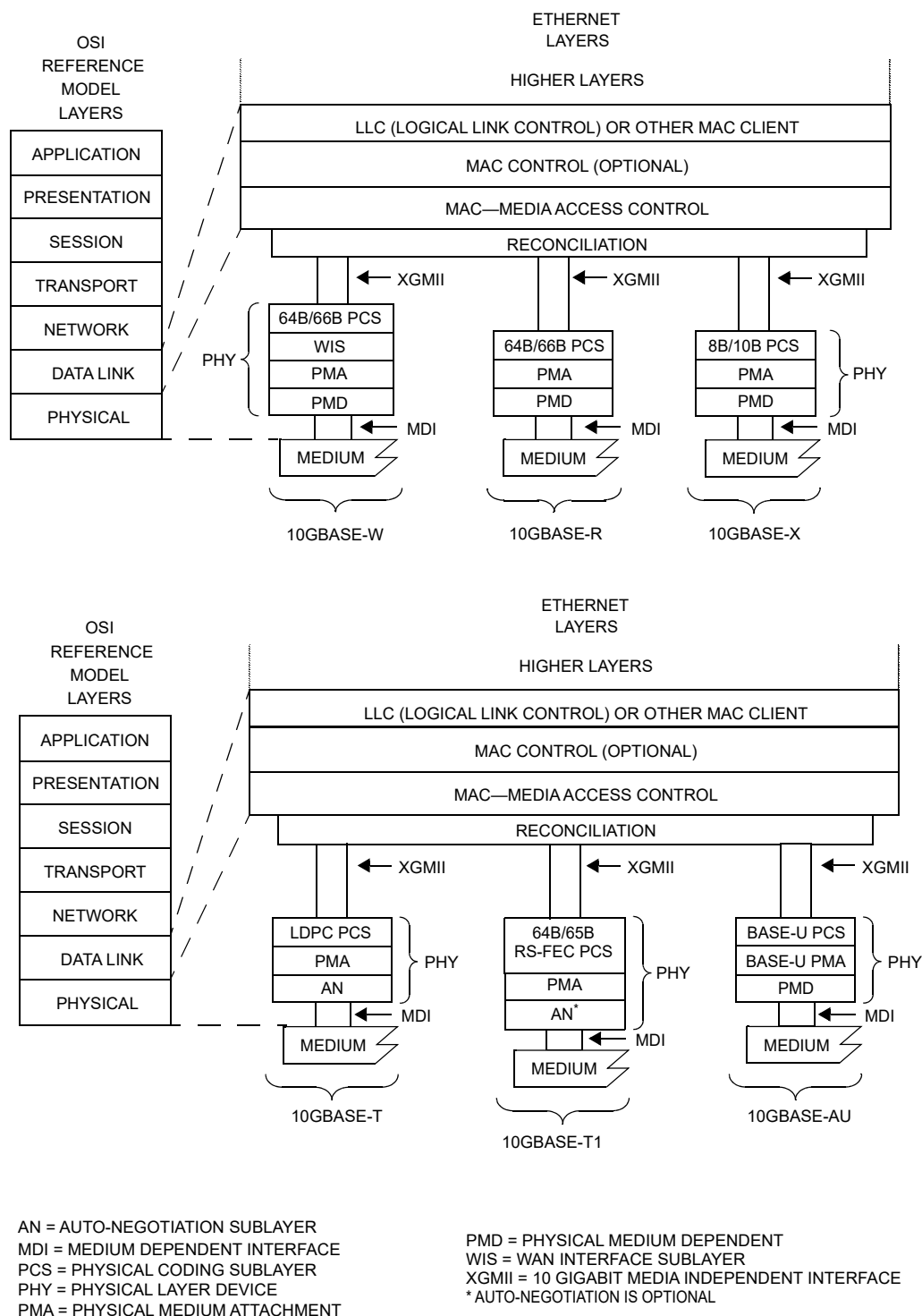


Figure 44–1—Architectural positioning of 10 Gigabit Ethernet

Change item d) of 44.1.3 as follows:

- d) The MDI as specified in [Clause 53](#) for 10GBASE-LX4, in [Clause 54](#) for 10GBASE-CX4, in [Clause 55](#) for 10GBASE-T, in [Clause 68](#) for 10GBASE-LRM, in [Clause 149](#) for 10GBASE-T1, in [Clause 166](#) for 10GBASE-AU, and in [Clause 52](#) for other PMD types.

44.1.4 Summary of 10 Gigabit Ethernet sublayers

44.1.4.1 Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

Change the second paragraph of 44.1.4.1 as follows:

While the XGMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for [Clause 47](#), [Clause 48](#), [Clause 49](#), [Clause 55](#), and [Clause 149](#), and [Clause 166](#).

44.1.4.4 Physical Layer signaling systems

Change Table 44–1 as follows:

Table 44–1—Nomenclature and clause correlation

Nomenclature	Clause ^a												
	48	49	50	51	52			53	54	55	68	149	166
	8B/10B PCS & PMA	64B/66B PCS	WIS	Serial PMA	850 nm Serial PMD	1310 nm Serial PMD	1550 nm Serial PMD	1310 nm WDM PMD	4-Lane electrical PMD	LDPC PCS & 4-pair PMA	1310 nm Serial MMF PMD	RS-FEC PCS & 1-pair PMA	10GBASE-AU PCS/PMA/PMD
10GBASE-CX4	M								M				
10GBASE-T1												M	
10GBASE-T										M			
10GBASE-AU													M
10GBASE-LRM		M		M							M		
10GBASE-SR		M		M	M								
10GBASE-SW		M	M	M	M								
10GBASE-LX4	M							M					
10GBASE-LR		M		M		M							
10GBASE-LW		M	M	M		M							
10GBASE-ER		M		M			M						
10GBASE-EW		M	M	M			M						

^a M = Mandatory

Insert a new paragraph after the seventh paragraph of 44.1.4.4, which begins “The term 10GBASE-T1, ...”, as follows:

The term 10GBASE-AU, specified in Clause 166, refers to a specific Physical Layer implementation based upon 64B/65B data coding method placed in RS-FEC codewords that are transmitted using NRZ modulation on glass optical fiber in an automotive environment.

Change former paragraph 8 (now paragraph 9 due to the above insertion) in 44.1.4.4 as follows:

Physical Layer device specifications are contained in [Clause 52](#), [Clause 53](#), [Clause 54](#), [Clause 55](#), [Clause 68](#), ~~and [Clause 149](#)~~, and [Clause 166](#).

44.3 Delay constraints

Insert a new row at the end of Table 44–2 as follows (unchanged rows not shown):

Table 44–2—Round-trip delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Notes ^a
...			
10GBASE-AU	11 264	22	Does not include delay of medium. See 166.11.

^a Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

44.4 Protocol implementation conformance statement (PICS) proforma

Change the first paragraph of 44.4 as follows:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 45 through [Clause 55](#), [Clause 68](#), ~~and [Clause 149](#)~~, and [Clause 166](#), demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface registers

45.2.1 PMA/PMD registers

Change the rows for register addresses 1.72 to 1.79 and 1.901 to 1.999 in Table 45–3 as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
...		
<u>1.72</u>	<u>BASE-AU PMA/PMD extended ability</u>	<u>45.2.1.60a</u>
~~1.72~~ 1.73 through 1.79	Reserved	
...		
<u>1.901</u>	<u>BASE-AU PMA/PMD control</u>	<u>45.2.1.158a</u>
~~1.901~~ 1.902 through 1.999	Reserved	
...		

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change the description for bits 1.7.6:0 in Table 45–7 as follows (unchanged table rows and bit description lines not shown):

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
1.7.6:0	PMA/PMD type selection	6 5 4 3 2 1 0 ... ~~0 1 1 1 1 1 x = reserved~~ ~~0 1 1 1 1 1 1 = reserved~~ <u>0 1 1 1 1 1 0 = BASE-AU PMA/PMD^d</u> ...	R/W
...			

^aR/W = Read/Write, RO = Read only

^bIf BASE-T1 is selected, bits 1.2100.3:0 are used to differentiate which BASE-T1 PMA/PMD is selected.

^cIf BASE-H PMA/PMD is selected, register 1.900 is used to differentiate which BASE-H PMA/PMD is selected.

^dIf BASE-AU PMA/PMD is selected, register 1.901 is used to differentiate which BASE-AU PMA/PMD is selected.

45.2.1.6.3 PMA/PMD type selection (1.7.6:0)

Change the first paragraph of 45.2.1.6.3 as follows:

The PMA/PMD type of the PMA/PMD shall be selected using bits 6 to 0. The PMA/PMD type abilities of the PMA/PMD are advertised in bits 9 and 7 through 0 of the PMA/PMD status 2 register; the PMA/PMD extended ability register; the 40G/100G PMA/PMD extended ability register; the 50G PMA/PMD extended ability register; the 200G PMA/PMD extended ability register; ~~and the 400G PMA/PMD extended ability register;~~ and the BASE-AU PMA/PMD extended ability register. A PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

Insert new subclause 45.2.1.60a, including Table 45–58a, after 45.2.1.60 as follows:

45.2.1.60a BASE-AU PMA/PMD extended ability register (Register 1.72)

The assignment of bits in the BASE-AU PMA/PMD extended ability register is shown in Table 45–58a.

Table 45–58a—BASE-AU PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.72.15:5	Reserved	Value always 0	RO
1.72.4	50GBASE-AU ability	1 = PMA/PMD is able to perform 50GBASE-AU 0 = PMA/PMD is not able to perform 50GBASE-AU	RO
1.72.3	25GBASE-AU ability	1 = PMA/PMD is able to perform 25GBASE-AU 0 = PMA/PMD is not able to perform 25GBASE-AU	RO
1.72.2	10GBASE-AU ability	1 = PMA/PMD is able to perform 10GBASE-AU 0 = PMA/PMD is not able to perform 10GBASE-AU	RO
1.72.1	5GBASE-AU ability	1 = PMA/PMD is able to perform 5GBASE-AU 0 = PMA/PMD is not able to perform 5GBASE-AU	RO
1.72.0	2.5GBASE-AU ability	1 = PMA/PMD is able to perform 2.5GBASE-AU 0 = PMA/PMD is not able to perform 2.5GBASE-AU	RO

^aRO = Read only

All of the bits in the BASE-AU PMA/PMD extended ability register are read only; a write to the BASE-AU PMA/PMD extended ability register shall have no effect.

Insert new subclause 45.2.1.158a, including Table 45–127a, after 45.2.1.158 as follows:

45.2.1.158a BASE-AU PMA/PMD control register (Register 1.901)

The assignment of bits in the BASE-AU PMA/PMD control register is shown in Table 45–127a.

Table 45–127a—BASE-AU PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W ^a
1.901.15:4	Reserved	Value always 0	RO
1.901.3:0	Type selection	3 2 1 0 1 x x x = Reserved 0 1 1 x = Reserved 0 1 0 1 = Reserved 0 1 0 0 = 50GBASE-AU 0 0 1 1 = 25GBASE-AU 0 0 1 0 = 10GBASE-AU 0 0 0 1 = 5GBASE-AU 0 0 0 0 = 2.5GBASE-AU	R/W

^aRO = Read only, R/W = Read/Write

45.2.1.158a.1 Type selection (1.901.3:0)

Bits 1.901.3:0 shall select only one of the modes of operation specified in Table 45–127a and advertised by register 1.72.

When these bits are set to binary 0000, the mode of operation is 2.5GBASE-AU. When these bits are set to binary 0001, the mode of operation is 5GBASE-AU. When these bits are set to binary 0010, the mode of operation is 10GBASE-AU. When these bits are set to binary 0011, the mode of operation is 25GBASE-AU. When these bits are set to binary 0100, the mode of operation is 50GBASE-AU.

Writes of reserved values or modes of operation not advertised by register 1.72, to bits 1.901.3:0 shall have no effect.

45.2.3 PCS registers

Change the rows for register addresses 3.2325 to 3.32767 in Table 45–233 as follows (unchanged rows not shown):

Table 45–233—PCS registers

Register address	Register name	Subclause
...		
3.2325 through 3.32767	Reserved	
<u>3.2330</u>	<u>BASE-U OAM transmit control</u>	<u>45.2.3.88</u>
<u>3.2331 through 3.2338</u>	<u>BASE-U OAM transmit message</u>	<u>45.2.3.88</u>
<u>3.2339</u>	<u>BASE-U OAM receive control</u>	<u>45.2.3.89</u>
<u>3.2340 through 3.2347</u>	<u>BASE-U OAM receive message</u>	<u>45.2.3.89</u>
<u>3.2348</u>	<u>BASE-U PCS control</u>	<u>45.2.3.90</u>
<u>3.2349</u>	<u>BASE-U PCS status 1</u>	<u>45.2.3.91</u>
<u>3.2350</u>	<u>BASE-U PCS status 2</u>	<u>45.2.3.92</u>
<u>3.2351</u>	<u>BASE-U PCS status 3</u>	<u>45.2.3.93</u>

Table 45–233—PCS registers (*continued*)

Register address	Register name	Subclause
<u>3.2352</u>	<u>BASE-U PCS status 4</u>	<u>45.2.3.94</u>
<u>3.2353</u>	<u>BASE-U PCS status 5</u>	<u>45.2.3.95</u>
<u>3.2354 through 3.32767</u>	<u>Reserved</u>	
...		

Insert 45.2.3.88 through 45.2.3.95 after 45.2.3.87 as follows:

45.2.3.88 BASE-U OAM transmit registers (Registers 3.2330 through 3.2338)

Registers 3.2330 through 3.2338 are used to transmit messages over the BASE-U OAM channel established between two link partners (see 166.7). The BASE-U OAM message is part of the physical header data (PHD) defined for BASE-U (see Table 166–2).

The transmit registers are used to compose a BASE-U OAM message and to control its transmission to the link partner. Register 3.2330 contains control, status, identification, and the beginning of a BASE-U OAM message. Eight additional registers (3.2331 through 3.2338) hold the remainder of the BASE-U OAM message.

The assignment of bits in the BASE-U OAM transmit registers is shown in Table 45–313a.

Table 45–313a—BASE-U OAM transmit register bit definitions

Bit(s)	Name	Description	R/W ^a
3.2330.15	TXO_REQ	1 = Transmission of a BASE-U OAM message is pending; write as 1 to request transmission 0 = BASE-U transmit registers are available for a new BASE-U OAM message	R/W, SC
3.2330.14	TXO_PHYT	The identifier of the last BASE-U OAM message received by the remote PHY	RO
3.2330.13	TXO_MERT	The identifier of the last BASE-U OAM message read by the STA attached to the remote PHY	RO
3.2330.12	TXO_MSGT	BASE-U OAM message identifier; its value changes with each new transmitted message	RO
3.2330.11:0	TXO_DATA0	Transmit BASE-U OAM message 12-bit data word	R/W
3.2331.15:0	TXO_DATA1	Transmit BASE-U OAM message 16-bit data word 1	R/W
3.2332.15:0	TXO_DATA2	Transmit BASE-U OAM message 16-bit data word 2	R/W
3.2333.15:0	TXO_DATA3	Transmit BASE-U OAM message 16-bit data word 3	R/W
3.2334.15:0	TXO_DATA4	Transmit BASE-U OAM message 16-bit data word 4	R/W
3.2335.15:0	TXO_DATA5	Transmit BASE-U OAM message 16-bit data word 5	R/W
3.2336.15:0	TXO_DATA6	Transmit BASE-U OAM message 16-bit data word 6	R/W

Table 45–313a—BASE-U OAM transmit register bit definitions (*continued*)

Bit(s)	Name	Description	R/W ^a
3.2337.15:0	TXO_DATA7	Transmit BASE-U OAM message 16-bit data word 7	R/W
3.2338.15:0	TXO_DATA8	Transmit BASE-U OAM message 16-bit data word 8	R/W

^aR/W = Read/Write, RO = Read only, SC = Self-clearing

45.2.3.88.1 TXO_REQ (3.2330.15)

Bit 3.2330.15 set to one requests the BASE-U based PHY to transmit the BASE-U OAM message written to registers 3.2330 through 3.2338. Bit 3.2330.15 is set to zero by the BASE-U based PHY to indicate that the BASE-U OAM message has been accepted for transmission, and that the BASE-U OAM transmit message registers are free to accept a new BASE-U OAM message.

Bit 3.2330.15, together with bits 3.2330.14 (TXO_PHYT), 3.2330.13 (TXO_MERT), and 3.2330.12 (TXO_MSGT), indicates the status of the BASE-U OAM transmission channel (see 166.7).

45.2.3.88.2 TXO_PHYT (3.2330.14)

Bit 3.2330.14 reflects the value of the bit TXO_MSGT in the last BASE-U OAM message received by the remote BASE-U based PHY.

45.2.3.88.3 TXO_MERT (3.2330.13)

Bit 3.2330.13 reflects the value of the bit TXO_MSGT in the last BASE-U OAM message read by the STA attached to the remote BASE-U based PHY.

45.2.3.88.4 TXO_MSGT (3.2330.12)

Bit 3.2330.12 is used for BASE-U OAM message identification. Bit 3.2330.12 is changed by the BASE-U based PHY when it accepts a new BASE-U OAM message for transmission, acting as a one bit sequence number. Simultaneously with the bit 3.2330.12 change, bit 3.2330.15 is set to zero.

45.2.3.88.5 TXO_DATAx (Bits 3.2330.11:0 and registers 3.2331 through 3.2338)

Bits 3.2330.11:0 (TXO_DATA0) contain the first 12 bits of a BASE-U OAM message, and registers 3.2331 through 3.2338 (TXO_DATA1 through TXO_DATA8) contain the remaining 128 bits of that BASE-U OAM message.

TXO_DATA0 and TXO_DATA1 shall be a 28-bit BASE-U OAM protocol identifier composed of a 24-bit Organizationally Unique Identifier (OUI) or Company ID (CID) followed by a 4-bit protocol number; where TXO_DATA0[11:0] = OUI[23:12], TXO_DATA1[15:4] = OUI[11:0], and TXO_DATA1[3:0] = protocol number. The protocol number and the content of TXO_DATA2 through TXO_DATA8 shall be vendor specific to the assignee of the OUI or CID.

45.2.3.89 BASE-U OAM receive registers (Registers 3.2339 through 3.2347)

Registers 3.2339 through 3.2347 store messages received over the BASE-U OAM channel established between two link partners (see 166.7). Register 3.2339 contains status information, identification, and the first 12 bits of a BASE-U OAM message. Registers 3.2340 through 3.2347 contain the following 128 bits of the received BASE-U OAM message.

The assignment of bits in the BASE-U OAM receive registers is shown in Table 45–313b.

Table 45–313b—BASE-U OAM receive register bit definitions

Bit(s)	Name	Description	R/W ^a
3.2339.15	RXO_VAL	1 = A new BASE-U OAM message has arrived 0 = No new BASE-U OAM message arrived since either the last message was read or PMA reset	RO
3.2339.14:13	Reserved	Value always 0	RO
3.2339.12	RXO_MSGT	Identifier of the received BASE-U OAM message	RO
3.2339.11:0	RXO_DATA0	Receive BASE-U OAM message first 12 bits	RO
3.2340.15:0	RXO_DATA1	Receive BASE-U OAM message 16-bit data word 1	RO
3.2341.15:0	RXO_DATA2	Receive BASE-U OAM message 16-bit data word 2	RO
3.2342.15:0	RXO_DATA3	Receive BASE-U OAM message 16-bit data word 3	RO
3.2343.15:0	RXO_DATA4	Receive BASE-U OAM message 16-bit data word 4	RO
3.2344.15:0	RXO_DATA5	Receive BASE-U OAM message 16-bit data word 5	RO
3.2345.15:0	RXO_DATA6	Receive BASE-U OAM message 16-bit data word 6	RO
3.2346.15:0	RXO_DATA7	Receive BASE-U OAM message 16-bit data word 7	RO
3.2347.15:0	RXO_DATA8	Receive BASE-U OAM message 16-bit data word 8	RO

^aRO = Read only

45.2.3.89.1 RXO_VAL (3.2339.15)

The BASE-U based PHY sets bit 3.2339.15 to one to indicate the reception of a new BASE-U OAM message. The BASE-U based PHY sets bit 3.2339.15 to zero when the last register (3.2347) containing the BASE-U OAM message is read (see Figure 115–43). The BASE-U based PHY does not update the receive message registers until the message is read by the STA as indicated by a read of register 3.2347.

45.2.3.89.2 RXO_MSGT (3.2339.12)

Bit 3.2339.12 is used for message identification. Bit 3.2339.12 changes with every new received BASE-U OAM message, acting as a one bit sequence number.

45.2.3.89.3 RXO_DATAx (Bits 3.2339.11:0 and registers 3.2340 through 3.2347)

Bits 3.2339.11:0 (RXO_DATA0) contain the first 12 bits of a received BASE-U OAM message, and registers 3.2340 through 3.2347 (RXO_DATA1 through RXO_DATA8) contain the remaining 128 data bits of that received BASE-U OAM message.

45.2.3.90 BASE-U PCS control register (Register 3.2348)

The assignment of bits in the BASE-U PCS control register is shown in Table 45–313c. The default value for each bit of the BASE-U PCS control register is chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–313c—BASE-U PCS control register bit definitions

Bit(s)	Name	Description	R/W ^a
3.2348.15:13	Operation mode	15 14 13 0 0 0 = Normal operation 0 0 1 = BER test mode 0 1 0 = SSQWP test pattern 0 1 1 = FSQWP test pattern 1 0 0 = SSPR-NRZ test pattern 1 0 1 = SSPR-PAM4 test pattern 1 1 x = Reserved	R/W
3.2348.12:10	Loopback mode	12 11 10 0 0 0 = No loopback 0 0 1 = xMII level loopback 0 1 0 = PMD interface level loopback 0 1 1 = Line loopback 1 x x = Reserved	R/W
3.2348.9:2	Reserved	Value always 0	RO
3.2348.1	BASE-U OAM advertisement enable	1 = Enable advertisement of BASE-U OAM ability 0 = Disable advertisement of BASE-U OAM ability	R/W
3.2348.0	EEE advertisement enable	1 = Enable advertisement of EEE ability 0 = Disable advertisement of EEE ability	R/W

^aR/W = Read/Write, RO = Read only

45.2.3.90.1 Operation mode (3.2348.15:13)

Bits 3.2348.15:13 shall select one of the BASE-U PCS test mode patterns defined in 166.5 and mapped per Table 45–313c. Bits 3.2348.15:13 shall have a default value of binary 000, selecting normal BASE-U PCS operation. Changes in the operation mode value shall only take effect after a PMA reset (see 166.3.4.1).

45.2.3.90.2 Loopback mode (3.2348.12:10)

Bits 3.2348.12:10 shall select one of the loopback modes defined in 166.8 and mapped per Table 45–313c. Bits 3.2348.12:10 shall have a default value of binary 000 (no loopback). Loopback modes are only available when a BASE-U PCS is in the normal operation mode (binary 000 is selected in 3.2348.15:13). Changes in the loopback mode value shall only take effect after a PMA reset (see 166.3.4.1).

45.2.3.90.3 BASE-U OAM advertisement enable (3.2348.1)

Bit 3.2348.1 controls establishing the BASE-U OAM channel with the link partner (see 166.7). If the BASE-U PCS does not have BASE-U OAM ability (bit 3.2349.1 = 0, see 45.2.3.91.13) setting bit 3.2348.1 shall have no effect. Setting bit 3.2348.1 to zero shall prevent establishment of a BASE-U OAM channel with the link partner. Changes in the BASE-U OAM advertisement enable value shall only take effect after a PMA reset (see 166.3.4.1). Bit 3.2348.1 has no specified default value.

45.2.3.90.4 EEE advertisement enable (3.2348.0)

Setting bit 3.2348.0 to one shall enable the advertisement of local PHY EEE ability (see 166.4). Setting bit 3.2348.0 to zero shall prevent establishment of EEE operation with the link partner. If the BASE-U PHY does not have EEE ability (bit 3.2349.0 = 0, see 45.2.3.91.14) setting bit 3.2348.0 has no effect. Changes in the EEE advertisement enable value shall only take effect after a PMA reset (see 166.3.4.1). Bit 3.2348.0 has no specified default value.

45.2.3.91 BASE-U PCS status 1 register (Register 3.2349)

The assignment of bits in the BASE-U PCS status 1 register is shown in Table 45–313d.

Table 45–313d— BASE-U PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.2349.15	Local receiver status	1 = The local receive operation is reliable 0 = The local receive operation is unreliable	RO
3.2349.14	Remote receiver status	1 = The receive operation of the remote PHY is reliable 0 = The receive operation of the remote PHY is unreliable	RO
3.2349.13	Link status	1 = A bidirectional reliable link is established 0 = A bidirectional reliable link is not established	RO, LL
3.2349.12	Local PHD reception status	1 = PHD reception is reliable for the local PHY 0 = PHD reception is unreliable for the local PHY	RO
3.2349.11	Remote PHD reception status	1 = PHD reception is reliable for the remote PHY 0 = PHD reception is unreliable for the remote PHY	RO
3.2349.10	PHD lock status	1 = PHD transmission and reception are reliable 0 = PHD transmission or reception are unreliable	RO, LL
3.2349.9	Reserved	Value always 0	RO
3.2349.8	Tx Assert LPI received	1 = Tx PCS has received LPI 0 = LPI not received by Tx PCS	RO, LH
3.2349.7	Rx Assert LPI received	1 = Rx PCS has received LPI 0 = LPI not received by Rx PCS	RO, LH
3.2349.6	Tx LPI indication	1 = Tx PCS is currently transmitting LPI 0 = Tx PCS is not currently transmitting LPI	RO
3.2349.5	Rx LPI indication	1 = Rx PCS is currently transmitting LPI 0 = Rx PCS is not currently transmitting LPI	RO
3.2349.4	Reserved	Value always 0	RO
3.2349.3	Remote BASE-U OAM advertisement	1 = The remote PHY has BASE-U OAM ability and it is advertised 0 = The remote PHY does not have BASE-U OAM ability or it is not advertised	RO
3.2349.2	Remote EEE advertisement	1 = The remote PHY has EEE ability and it is advertised 0 = The remote PHY does not have EEE ability or it is not advertised	RO

Table 45–313d— BASE-U PCS status 1 register bit definitions (*continued*)

Bit(s)	Name	Description	R/W ^a
3.2349.1	Local BASE-U OAM ability	1 = The PHY has BASE-U OAM ability 0 = The PHY does not have BASE-U OAM ability	RO
3.2349.0	Local EEE ability	1 = The PHY has EEE ability 0 = The PHY does not have EEE ability	RO

^aRO = Read only, LH = Latching high, LL = Latching low

45.2.3.91.1 Local receiver status (3.2349.15)

Bit 3.2349.15 reflects the value of the state variable `loc_rcvr_status` as determined by the PHY quality monitor state diagram (see 166.3.4.6.4).

45.2.3.91.2 Remote receiver status (3.2349.14)

Bit 3.2349.14 reflects the value of the state variable `rem_rcvr_status` as determined by the link monitor state diagram (see 166.3.4.4).

45.2.3.91.3 Link status (3.2349.13)

Bit 3.2349.13 reflects the value of the state variable `link_status` as determined by the link monitor state diagram (see 166.3.4.4). Bit 3.2349.13 shall have latching low behavior. Bit 1.1.2, bit 3.1.2, and bit 3.2349.13 are identical for BASE-U; a read to any of these three bits shall release the latch for all the bits.

45.2.3.91.4 Local PHD reception status (3.2349.12)

Bit 3.2349.12 reflects the value of the state variable `loc_rcvr_hdr_lock` as determined by the local PHD reception monitor state diagram (see 166.3.4.5).

45.2.3.91.5 Remote PHD reception status (3.2349.11)

Bit 3.2349.11 reflects the value of the state variable `rem_rcvr_hdr_lock` as determined by the remote PHD reception monitor state diagram (see 166.3.4.5).

45.2.3.91.6 PHD lock status (3.2349.10)

Bit 3.2349.10 reflects the value of the state variable `rcvr_hdr_lock` as determined by the PHD monitor state diagram (see 166.3.4.5). Bit 3.2349.10 shall have latching low behavior.

45.2.3.91.7 Tx Assert LPI received (3.2349.8)

When read as a one, bit 3.2349.8 indicates that the transmit BASE-U PCS has received Assert LPI signaling from the transmit RS one or more times since the register was last read. When read as a zero, bit 3.2349.8 indicates that the BASE-U PCS transmitter has not received Assert LPI. Bit 3.2349.8 shall have latching high behavior. Bit 3.2349.8 is a copy of bit 3.1.11; a read of either bit shall release the latch for both of the bits.

45.2.3.91.8 Rx Assert LPI generated (3.2349.7)

When read as a one, bit 3.2349.7 indicates that the receive BASE-U PCS has generated Assert LPI to the receive RS one or more times since the register was last read. When read as a zero, bit 3.2349.7 indicates that the BASE-U PCS receiver has not generated Assert LPI to the receive RS. Bit 3.2349.7 shall have latching high behavior. Bit 3.2349.7 is a copy of bit 3.1.10; a read of either bit shall release the latch for all the bits.

45.2.3.91.9 Tx LPI indication (3.2349.6)

Bit 3.2349.6 indicates the current LPI mode status of the local BASE-U based PHY transmit path. When read as a one, the PHY transmitter is currently in LPI mode (transmitting refresh). When read as a zero, the PHY transmitter is not in LPI mode (see 166.4). Bit 3.2349.6 is a copy of bit 3.1.9.

45.2.3.91.10 Rx LPI indication (3.2349.5)

Bit 3.2349.5 indicates the current LPI mode status of the local BASE-U based PHY receive path. When read as a one, the PHY is receiving LPI mode signals (refresh). When read as a zero, the PHY is not receiving LPI mode signals (see 166.4). Bit 3.2349.5 is a copy of bit 3.1.8.

45.2.3.91.11 Remote BASE-U OAM advertisement (3.2349.3)

Bit 3.2349.3 indicates the BASE-U OAM ability of the remote PHY received in the PHD field PHD.CAP.OAM (see Table 166–2). When read as a one, bit 3.2349.3 indicates that the remote PHY has the BASE-U OAM ability and that BASE-U OAM advertisement is enabled. When read as a zero, bit 3.2349.3 indicates either that the remote PHY does not have BASE-U OAM ability or that BASE-U OAM advertisement is disabled.

45.2.3.91.12 Remote EEE advertisement (3.2349.2)

Bit 3.2349.2 indicates the EEE ability of the remote PHY received in the PHD field PHD.CAP.LPI (see Table 166–2). When read as a one, bit 3.2349.2 indicates that the remote PHY has the EEE ability and that EEE advertisement is enabled. When read as a zero, bit 3.2349.2 indicates either that the remote PHY does not have the EEE ability or that EEE advertisement is disabled.

45.2.3.91.13 Local BASE-U OAM ability (3.2349.1)

Bit 3.2349.1 indicates the BASE-U OAM ability of the BASE-U PHY (see 166.7). When read as a one, bit 3.2349.1 indicates that the BASE-U PHY supports the BASE-U OAM protocol. When read as a zero, bit 3.2349.1 indicates the BASE-U PHY does not support the BASE-U OAM protocol.

A PHY indicating in bit 3.2349.1 support of BASE-U OAM shall provide the functions of registers 3.2330 through 3.2347 as specified in 166.7.

45.2.3.91.14 Local EEE ability (3.2349.0)

Bit 3.2349.0 indicates the EEE ability of the BASE-U PHY. When read as a one, bit 3.2349.0 indicates that the BASE-U PHY implements EEE, and is able to enter LPI mode (see 166.4). When read as a zero, bit 3.2349.0 indicates the BASE-U PHY does not implement EEE operation.

45.2.3.92 BASE-U PCS status 2 register (Register 3.2350)

The assignment of bits in the BASE-U PCS status 2 register is shown in Table 45–313e.

Table 45–313e— BASE-U PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.2350.15:8	Reserved	Value always 0	RO
3.2350.7:0	Local link margin	Reports the local link margin	RO

^aRO = Read only

45.2.3.92.1 Local link margin (3.2350.7:0)

Bits 3.2350.7:0 indicate the link margin of the receiver. Link margin is defined in 166.3.4.6.2 and is fixed-point formatted (8, 3). See 166.1.1 for fixed-point format definition.

45.2.3.93 BASE-U PCS status 3 register (Register 3.2351)

The assignment of bits in the BASE-U PCS status 3 register is shown in Table 45–313f.

Table 45–313f— BASE-U PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.2351.15:8	Reserved	Value always 0	RO
3.2351.7:0	Remote link margin	Link margin reported by the link partner	RO

^aRO = Read only

45.2.3.93.1 Remote link margin (3.2351.7:0)

Bits 3.2351.7:0 report the link margin of the remote PHY receiver as it is received in the PHD field PHD.RX.LINKMARGIN (see Table 166–2). Link margin is defined in 166.3.4.6.2 and is fixed-point formatted (8, 3). See 166.1.1 for fixed-point format definition.

45.2.3.94 BASE-U PCS status 4 register (Register 3.2352)

The assignment of bits in the BASE-U PCS status 4 register is shown in Table 45–313g.

Table 45–313g— BASE-U PCS status 4 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.2352.15:0	BER test mode counter	A 16-bit counter used when operating in BER test mode	RO, NR

^aRO = Read only, NR = Non Roll-over

When the BASE-U based PHY receiver is operating in BER test mode (see 166.5.1), bits 3.2352.15:0 are a 16-bit counter that counts the number of erroneous bits received at the input of the 64B/65B PCS decoder.

These bits shall be reset to all zeros when the counter is read. The counter shall be held at all ones in the case of overflow.

45.2.3.95 BASE-U PCS status 5 register (Register 3.2353)

The assignment of bits in the BASE-U PCS status 5 register is shown in Table 45–313h.

Table 45–313h— BASE-U PCS status 5 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.2353.15:0	RS-FEC codeword error counter	A 16-bit counter used when operating in normal and BER test mode	RO, NR

^aRO = Read only, NR = Non Roll-over

When the BASE-U based PHY receiver is operating in normal or BER test mode (see 166.5.1), bits 3.2353.15:0 are a 16-bit counter that counts the number of erroneous RS-FEC codewords at the input of the 64B/65B PCS decoder (see 166.2.3.2).

These bits shall be reset to all zeros when the counter is read. The counter shall be held at all ones in the case of overflow.

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) Interface⁷

45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) Interface

45.5.3.2 PMA/PMD MMD options

Insert a new row at the end of the table in 45.5.3.2 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
...					
*BAU	Implementation of a BASE-AU PMA/PMD			PMA:O	Yes [] No []

45.5.3.3 PMA/PMD management functions

Insert items MM229 through MM231 at the end of the table in 45.5.3.3 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
...					
MM229	Writes to the BASE-AU PMA/PMD extended ability register 1.72 have no effect	45.2.1.60a		BAU:M	Yes [] N/A []
MM230	Bits 1.901.3:0 select only one of the modes of operation specified in Table 45–127a and advertised by register 1.72	45.2.1.158a		BAU:M	Yes [] N/A []
MM231	Writes of reserved values or modes of operation different of those advertised by register 1.72, to bits 1.901.3:0 have no effect	45.2.1.158a		BAU:M	Yes [] N/A []

⁷Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

45.5.3.6 PCS options

Insert a new row at the end of the table in 45.5.3.6 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
...					
*BUOAM	BASE-U OAM channel implementation	45.2.3.88 and 45.2.3.89		PCS:O	Yes [] No [] N/A []

45.5.3.7 PCS management functions

Insert items RM207 through RM232 at the end of the table in 45.5.3.7 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
...					
RM207	BASE-U OAM message format to be transmitted	45.2.3.88.5	TXO_DATA0[11:0] = OUI[23:12] and TXO_DATA1[15:4] = OUI[11:0] Content of TXO_DATA1[3:0] and TXO_DATA2 through TXO_DATA8 is vendor specific per OUI or CID	PCS *BUOAM:M	Yes [] N/A []
RM208	Default operation mode	45.2.3.90	Default value of bits 3.2348.15:13 is binary 000 (normal mode)	PCS:M	Yes [] N/A []
RM209	Test operation modes	45.2.3.90	Bits 3.2348.15:13 select test modes with behavior per 166.5 and mapped per Table 45–313c	PCS:M	Yes [] N/A []
RM210	Operation mode change effect	45.2.3.90.1	Changes in the value of bits 3.2348.15:13 only take effect after PMA reset	PCS:M	Yes [] N/A []
RM211	Default loopback mode	45.2.3.90.2	Default value of bits 3.2348.12:10 is binary 000 (no loopback)	PCS:M	Yes [] N/A []
RM212	Loopback modes	45.2.3.90.2	Bits 3.2348.12:10 select loopback modes with behavior per 166.8 and mapped per Table 45–313c	PCS:M	Yes [] N/A []
RM213	Loopback mode change effect	45.2.3.90.2	Changes in the value of bits 3.2348.12:10 only take effect after PMA reset	PCS:M	Yes [] N/A []

Item	Feature	Subclause	Value/Comment	Status	Support
RM214	BASE-U OAM conditional enable	45.2.3.90.3	Write of one to bit 3.2348.1 only produces effect if bit 3.2349.1 is read as one	PCS *BUOAM :M	Yes [] N/A []
RM215	BASE-U OAM disable	45.2.3.90.3	Write of zero to bit 3.2348.1 prevents BASE-U OAM channel establishment with link partner	PCS *BUOAM :M	Yes [] N/A []
RM216	BASE-U OAM advertisement enable change effect	45.2.3.90.3	Changes in the value of bit 3.2348.1 only take effect after PMA reset	PCS *BUOAM :M	Yes [] N/A []
RM217	EEE advertisement enable	45.2.3.90.4	Write of one to bit 3.2348.0 enables the advertisement of local PHY EEE ability per 166.4	PCS *EEE:M	Yes [] N/A []
RM218	EEE conditional enable	45.2.3.90.4	Write of one to bit 3.2348.0 only enables EEE capability if bit 3.2349.0 is read as one	PCS *EEE:M	Yes [] N/A []
RM219	EEE disable	45.2.3.90.4	Write of zero to bit 3.2348.0 prevents EEE operation with link partner	PCS *EEE:M	Yes [] N/A []
RM220	EEE advertisement enable change effect	45.2.3.90.4	Changes in the value of bit 3.2348.0 only take effect after PMA reset	PCS *EEE:M	Yes [] N/A []
RM221	Link status behavior	45.2.3.91.3	Bit 3.2349.13 has latching low behavior	PCS:M	Yes [] N/A []
RM222	Link status mirroring	45.2.3.91.3	Bit 3.2349.13, bit 1.1.2, and bit 3.1.2 reflect the same state variable link_status and a read of any of them releases the latch for all the bits	PCS:M	Yes [] N/A []
RM223	PHD lock status behavior	45.2.3.91.6	Bit 3.2349.10 has latching low behavior	PCS:M	Yes [] N/A []
RM224	Tx Assert LPI received behavior	45.2.3.91.7	Bit 3.2349.8 has latching high behavior	PCS *EEE:M	Yes [] N/A []
RM225	Tx Assert LPI received mirroring	45.2.3.91.7	Bit 3.2349.8 is a copy of bit 3.1.11 and a read of either of them releases the latch for both of the bits	PCS *EEE:M	Yes [] N/A []
RM226	Rx Assert LPI generated behavior	45.2.3.91.8	Bit 3.2349.7 has latching high behavior	PCS *EEE:M	Yes [] N/A []
RM227	Rx Assert LPI generated mirroring	45.2.3.91.8	Bit 3.2349.7 is a copy of bit 3.1.10 and a read of either of them releases the latch for both of the bits	PCS *EEE:M	Yes [] N/A []

Item	Feature	Subclause	Value/Comment	Status	Support
RM228	BASE-U OAM ability	45.2.3.91.13	Registers 3.2330 through 3.2347 are implemented and 3.2349.1 reads as one	PCS *BUOAM :M	Yes [] N/A []
RM229	BER test mode counter is reset to all zeros when read	45.2.3.94	Register 3.2352 is reset to all zeros when read	PCS:M	Yes [] N/A []
RM230	BER test mode counter holds all ones in case of overflow	45.2.3.94	Register 3.2352 holds all ones in case of overflow	PCS:M	Yes [] N/A []
RM231	RS-FEC codeword error counter is reset to all zeros when read	45.2.3.95	Register 3.2353 is reset to all zeros when read	PCS:M	Yes [] N/A []
RM232	RS-FEC codeword error counter holds all ones in case of overflow	45.2.3.95	Register 3.2353 holds all ones in case of overflow	PCS:M	Yes [] N/A []

78. Energy-Efficient Ethernet (EEE)

78.1 Overview

78.1.4 PHY types optionally supporting EEE

Insert new rows for “2.5GBASE-AU” after “2.5GBASE-T1”, “5GBASE-AU” after “5GBASE-T1”, “10GBASE-AU” after “10GBASE-T1”, “25GBASE-AU” after “25GBASE-T”, and “50GBASE-AU” after “50GBASE-CR” in Table 78–1 as follows (unchanged rows not shown):

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
...	
2.5GBASE-AU ^b	166
...	
5GBASE-AU ^b	166
...	
10GBASE-AU ^b	166
...	
25GBASE-AU ^b	166
...	
50GBASE-AU ^b	166
...	

^a 25GAUI/XLAUI/CAUI-n shutdown is supported only when deep sleep is enabled for the associated PHY.

^b The deep sleep mode of EEE is not supported for this PHY.

78.5 Communication link access latency

Insert new rows for “2.5GBASE-AU fast wake” after “1000BASE-T”, “5GBASE-AU fast wake” after “2.5GBASE-T”, “10GBASE-AU fast wake” after “5GBASE-T”, “25GBASE-AU fast wake” after “10GBASE-T”, and “50GBASE-AU fast wake” after “40GBASE-T” in Table 78–4 as follows (unchanged rows not shown):

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w_sys_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy_shrink_tx}$ (max) (μs)	$T_{phy_shrink_rx}$ (max) (μs)	$T_{w_sys_rx}$ (min) (μs)
...						
2.5GBASE-AU fast wake		4.1	4.1	0	0	2.05
...						
5GBASE-AU fast wake		2.05	2.05	0	0	1.03
...						
10GBASE-AU fast wake		1.03	1.03	0	0	0.52
...						
25GBASE-AU fast wake		0.41	0.41	0	0	0.21
...						
50GBASE-AU fast wake		0.21	0.21	0	0	0.11
...						

105. Introduction to 25 Gb/s networks

105.1 Overview

105.1.1 Scope

Change the first paragraph of 105.1.1 as follows:

25 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 25 Gb/s, coupled with any IEEE 802.3 25GBASE Physical Layer implementation, connected through a 25 Gigabit Media Independent Interface (25GMII) to Physical Layer devices such as 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-SR, 25GBASE-T, 25GBASE-LR, and 25GBASE-ER.

105.1.2 Relationship of 25 Gigabit Ethernet to the ISO OSI reference model

Replace Figure 105–1 with the following figure, which adds 25GBASE-AU:

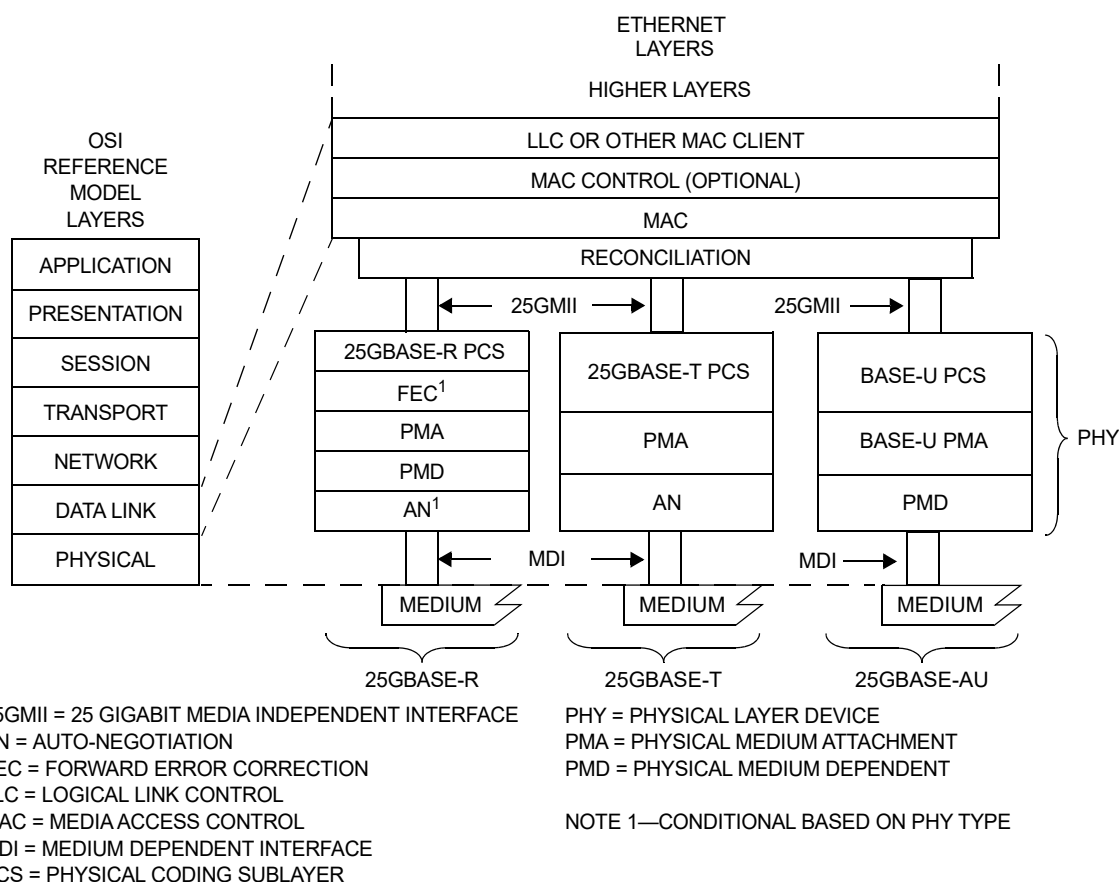


Figure 105–1—Architectural positioning of 25 Gigabit Ethernet

Change the text of list item c) in 105.1.2 as follows:

- c) The Media Dependent Interface (MDI) as specified in [Clause 110](#) for 25GBASE-CR and 25GBASE-CR-S, in [Clause 111](#) for 25GBASE-KR and 25GBASE-KR-S, in [Clause 112](#) for 25GBASE-SR, ~~or in [Clause 114](#) for 25GBASE-LR and 25GBASE-ER,~~ or in [Clause 166](#) for 25GBASE-AU uses a single-lane data path.

105.1.3 Nomenclature

Insert a new paragraph after the third paragraph of 105.1.3 as follows:

25GBASE-AU represents Physical Layer devices using Clause 166 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer, for transmitting 25 Gb/s Ethernet over glass optical fiber in an automotive environment. 25GBASE-AU uses 64B/65B coding placed into RS-FEC codewords that are transmitted using NRZ modulation.

Insert a new row for “25GBASE-AU” after the row for “25GBASE-T” in Table 105–1 as follows (unchanged rows not shown):

Table 105–1—25 Gb/s PHYs

Name	Description
...	
25GBASE-AU	25 Gb/s PHY using 64B/65B and Reed-Solomon encoding with NRZ modulation over glass optical fiber in an automotive environment (see Clause 166).
...	

105.2 Physical Layer signaling systems

Change Table 105–2 as follows:

Table 105–2—Nomenclature and clause correlation, 25 Gb/s Ethernet PHYs

Nomenclature	Clause/Annex																			
	28	73	74	78	106		107	108	109	109A	109B	110		111		112	113	114		166
	Auto-Negotiation	Auto-Negotiation	BASE-R FEC	EEE	RS	25GMII	25GBASE-R PCS	25GBASE-R RS-FEC	PMA	25GAUI C2C	25GAUI C2M	25GBASE-CR PMD	25GBASE-CR-S PMD	25GBASE-KR PMD	25GBASE-KR-S PMD	25GBASE-SR PMD	25GBASE-T PCS/PMA	25GBASE-LR PMD	25GBASE-ER PMD	25 BASE-AU PCS/PMA/PMD
25GBASE-KR-S		M ^a	M	O ^a	M	O	M		M	O					M					
25GBASE-KR		M	M	O	M	O	M	M	M	O				M						
25GBASE-CR-S		M	M	O	M	O	M		M	O			M							
25GBASE-CR		M	M	O	M	O	M	M	M	O		M								
25GBASE-T	M			O	M	O											M			
<u>25GBASE-AU</u>				<u>O</u>	<u>M</u>	<u>O</u>														<u>M</u>
25GBASE-SR				O	M	O	M	M	M	O	O					M				
25GBASE-LR				O	M	O	M	M	M	O	O							M		
25GBASE-ER				O	M	O	M	M	M	O	O								M	

^aO = Optional, M = Mandatory

105.3 Summary of 25 Gigabit Ethernet sublayers

105.3.2 Physical Coding Sublayer (PCS)

Insert a new paragraph at the end of 105.3.2 as follows:

The 25GBASE-AU PCS is specified in Clause 166.

105.3.4 Physical Medium Attachment (PMA) sublayer

Insert a new paragraph at the end of 105.3.4 as follows:

The 25GBASE-AU PMA is specified in Clause 166.