



IEEE Standard for Ethernet

Amendment 9: Media Access Control Parameters for 800 Gb/s and Physical Layers and Management Parameters for 400 Gb/s and 800 Gb/s Operation

IEEE Computer Society

Developed by the
LAN/MAN Standards Committee

IEEE Std 802.3df™-2024

(Amendment to IEEE Std 802.3™-2022
as amended by IEEE Std 802.3dd™-2022,
IEEE Std 802.3cs™-2022, IEEE Std 802.3db™-2022,
IEEE Std 802.3ck™-2022, IEEE Std 802.3de™-2022,
IEEE Std 802.3cx™-2023, IEEE Std 802.3cz™-2023,
and IEEE Std 802.3cy™-2023)

IEEE Std 802.3df™-2024
(Amendment to IEEE Std 802.3™-2022
as amended by IEEE Std 802.3dd™-2022,
IEEE Std 802.3cs™-2022,
IEEE Std 802.3db™-2022,
IEEE Std 802.3ck™-2022,
IEEE Std 802.3de™-2022,
IEEE Std 802.3cx™-2023,
IEEE Std 802.3cz™-2023,
and IEEE Std 802.3cy™-2023)

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Amendment 9: Media Access Control Parameters for 800 Gb/s and Physical Layers and Management Parameters for 400 Gb/s and 800 Gb/s Operation

Developed by the
LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 15 February 2024
IEEE SA Standards Board

Abstract: This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 169 through Clause 173, Annex 172A, and Annex 173A. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 400 Gb/s and 800 Gb/s.

Keywords: 800GAUI-8, 800GBASE-CR8, 400GBASE-DR4-2, 800GBASE-DR8, 800GBASE-DR8-2, 800GBASE-KR8, 800GBASE-R, 800GBASE-SR8, 800GBASE-VR8, 800 Gigabit Ethernet, 800GMII, 800GXS, amendment, FEC, IEEE 802.3™, IEEE 802.3df™, PCS, Physical Coding Sublayer, PMD, Physical Medium Attachment

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Introduction

This introduction is not part of IEEE Std 802.3df-2024, IEEE Standard for Ethernet—Amendment 9: Media Access Control Parameters for 800 Gb/s and Physical Layers and Management Parameters for 400 Gb/s and 800 Gb/s Operation.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. “Local Area Networks: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications” was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol and the ability to use an EtherType to specify the MAC client protocol were added in 1997. The title was changed to Standard for Ethernet with the 2012 Revision.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2022 and are not maintained as separate documents.

At the date of IEEE Std 802.3df-2024 publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2022

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex K and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33A. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 140 and Annex 119A through Annex 136D. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well as 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 includes general information on 2.5 Gb/s and 5 Gb/s operation. Clause 126 through Clause 130 and associated annexes include 2.5 Gb/s and 5 Gb/s Physical Layer specifications. Clause 131 provides general information on 50 Gb/s operation. Clause 132 through Clause 140 and associated annexes include 50 Gb/s Physical Layer specifications and additional 100 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications.

Section Nine—Includes Clause 141 through Clause 160 and Annex 142A through Annex 154A. Clause 141 through Clause 144 and associated annexes specify symmetric and asymmetric operation of Ethernet passive optical networks over multiple 25 Gb/s channels. Clause 145 and associated annexes specify increased power delivery using all four pairs in the structured wiring plant. Clause 146 through Clause 149 and associated annexes specify Physical Layers for 10 Mb/s, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation over a single balanced pair of conductors. Clause 150 and Clause 151 include additional 400 Gb/s Physical Layer specifications. Clause 153 and Clause 154 specify 100 Gb/s operation over DWDM channels. Clause 157 through Clause 160 include 10 Gb/s, 25 Gb/s, and 50 Gb/s bidirectional Physical Layer specifications.

IEEE Std 802.3dd™-2022

Amendment 1—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 104, Power over Data Lines of Single Pair Ethernet, and related portions of the standard.

IEEE Std 802.3cs™-2022

Amendment 2—This amendment to IEEE Std 802.3-2022 defines Super-PON optical subscriber access networks, in the family of Ethernet passive optical networks (EPONs). Super-PON has a reach of up to 50 km and up to 1024 ONUs over a point-to-multipoint passive optical distribution network (ODN)

through wavelength division multiplexing (WDM). A Super-PON ODN contains a passive wavelength router that determines the channels used by the ODN. This standard specifies the Super-PON Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer at a MAC data rate of 10 Gb/s in the downstream direction and of 10 Gb/s or 2.5 Gb/s in the upstream direction.

IEEE Std 802.3db™-2022

Amendment 3—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 167. This amendment adds Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s over one, two, and four pairs of multimode fiber based on 100 Gb/s optical signaling.

IEEE Std 802.3ck™-2022

Amendment 4—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 161 through Clause 163, Annex 120F, Annex 120G, Annex 162A through Annex 162D, Annex 163A, and Annex 163B. This amendment includes Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s electrical interfaces based on 100 Gb/s signaling.

IEEE Std 802.3de™-2022

Amendment 5—This amendment includes changes to IEEE Std 802.3-2022 to add 10 Mb/s Single-Pair Ethernet point-to-point PHYs to the PHYs supporting the MAC Merge function and the Time Synchronization Service Interface (TSSI).

IEEE Std 802.3cx™-2023

Amendment 6—This amendment to IEEE Std 802.3-2022 modifies Clause 30, Clause 45, and Clause 90, and adds Annex 90A to enhance support for time synchronization protocols by providing options for sub-nanosecond reporting of the transmit and receive path data delays, selection of the data delay measurement point, and dynamic reporting of path data delay variation.

IEEE Std 802.3cz™-2023

Amendment 7—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 166. This amendment adds 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, and 50 Gb/s Physical Layer specifications and management parameters for optical automotive Ethernet using graded-index glass optical fiber.

IEEE Std 802.3cy™-2023

Amendment 8—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 165 and Annex 165A. This amendment adds Physical Layer specifications and management parameters for operation at 25 Gb/s over a single balanced pair of conductors.

IEEE Std 802.3df™-2024

Amendment 9—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 169 through Clause 173, Annex 172A, and Annex 173A. This amendment includes Physical Layer specifications and management parameters for 400 Gb/s and 800 Gb/s operation.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and

IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 9: Media Access Control Parameters for 800 Gb/s and Physical Layers and Management Parameters for 400 Gb/s and 800 Gb/s Operation

(This amendment is based on IEEE Std 802.3™-2022 as amended by IEEE Std 802.3dd™-2022, IEEE Std 802.3cs™-2022, IEEE Std 802.3db™-2022, IEEE Std 802.3ck™-2022, IEEE Std 802.3de™-2022, IEEE Std 802.3cx™-2023, IEEE Std 802.3cz™-2023, and IEEE Std 802.3cy™-2023.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strike through~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.⁶

⁶ Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Insert two new list items at the end of the lettered list in 1.1.3.2 as follows:

- w) *800 Gb/s Media Independent Interface (800GMII)*. The 800GMII is designed to connect an 800 Gb/s capable MAC to an 800 Gb/s PHY. The 800GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 800GMII. The 800GMII is optional.
- x) *800 Gb/s Attachment Unit Interface (800GAUI-n)*. An 800GAUI-n is an optional physical instantiation of the PMA service interface to extend the connection between 800 Gb/s capable PMAs. 800GAUI-n C2C is intended for use as a chip-to-chip interface and 800GAUI-n C2M as a chip-to-module interface. One width of 800GAUI-n is defined: eight-lane 800GAUI-8 C2C in Annex 120F and 800GAUI-8 C2M in Annex 120G. No mechanical connector is specified for use with an 800GAUI-n.

1.4 Definitions

Change 1.4.103 as follows:

1.4.103 200GBASE-DR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over four lanes of single-mode fibers in each direction, with reach up to at least 500 m. (See IEEE Std 802.3, [Clause 121](#).)

Change 1.4.108a (as inserted by IEEE Std 802.3db-2022) as follows:

1.4.108a 200GBASE-SR2: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over two lanes of multimode fibers in each direction, with reach up to at least 100 m. (See IEEE Std 802.3, [Clause 167](#).)

Change 1.4.109 as follows:

1.4.109 200GBASE-SR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of multimode fibers in each direction, with reach up to at least 100 m. (See IEEE Std 802.3, [Clause 138](#).)

Change 1.4.109a (as inserted by IEEE Std 802.3db-2022) as follows:

1.4.109a 200GBASE-VR2: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over two lanes of multimode fibers in each direction, with reach up to at least 50 m. (See IEEE Std 802.3, [Clause 167](#).)

Change 1.4.135 as follows:

1.4.135 400GBASE-DR4: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over four lanes of single-mode fibers in each direction, with reach up to at least 500 m. (See IEEE Std 802.3, [Clause 124](#).)

Insert the following new definition after 1.4.135 “400GBASE-DR4”:

1.4.135a 400GBASE-DR4-2: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over four single-mode fibers in each direction, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 124.)

Change 1.4.142 as follows:

1.4.142 400GBASE-SR16: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding over ~~sixteen~~ 16 lanes of multimode fibers in each direction, with reach up to at least 100 m. (See IEEE Std 802.3, [Clause 123](#).)

Change 1.4.142a (as inserted by IEEE Std 802.3db-2022) as follows:

1.4.142a 400GBASE-SR4: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over four ~~lanes of multimode fibers in each direction~~, with reach up to at least 100 m. (See IEEE Std 802.3, ~~Clause 1~~ [Clause 167](#).)

Change 1.4.143 and 1.4.144 as follows:

1.4.143 400GBASE-SR4.2: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding over eight ~~lanes on multimode fiber fibers~~ in a bidirectional WDM format, with reach up to at least 150 m. (See IEEE Std 802.3, [Clause 150](#).)

1.4.144 400GBASE-SR8: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding over eight ~~lanes of multimode fibers in each direction~~, with reach up to at least 100 m. (See IEEE Std 802.3, [Clause 138](#).)

Change 1.4.144a (as inserted by IEEE Std 802.3db-2022) as follows:

1.4.144a 400GBASE-VR4: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over four ~~lanes of multimode fibers in each direction~~, with reach up to at least 50 m. (See IEEE Std 802.3, Clause 167.)

Insert the following 11 new definitions after 1.4.184 “64B/65B transmission code”:

1.4.184a 800GBASE-CR8: IEEE 802.3 Physical Layer specification for 800 Gb/s using 800GBASE-R encoding over eight lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 162.)

1.4.184b 800GBASE-DR8: IEEE 802.3 Physical Layer specification for 800 Gb/s using 800GBASE-R encoding and 4-level pulse amplitude modulation over eight single-mode fibers in each direction, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 124.)

1.4.184c 800GBASE-DR8-2: IEEE 802.3 Physical Layer specification for 800 Gb/s using 800GBASE-R encoding and 4-level pulse amplitude modulation over eight single-mode fibers in each direction, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 124.)

1.4.184d 800GBASE-KR8: IEEE 802.3 Physical Layer specification for 800 Gb/s using 800GBASE-R encoding over eight lanes of an electrical backplane. (See IEEE Std 802.3, Clause 163.)

1.4.184e 800GBASE-R: An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 172 for 800 Gb/s operation. (See IEEE Std 802.3, Clause 172.)

1.4.184f 800GBASE-SR8: IEEE 802.3 Physical Layer specification for 800 Gb/s using 800GBASE-R encoding and 4-level pulse amplitude modulation over eight multimode fibers in each direction, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 167.)

1.4.184g 800GBASE-VR8: IEEE 802.3 Physical Layer specification for 800 Gb/s using 800GBASE-R encoding and 4-level pulse amplitude modulation over eight multimode fibers in each direction, with reach up to at least 50 m. (See IEEE Std 802.3, Clause 167.)

1.4.184h 800 Gb/s Attachment Unit Interface (800GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 800 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module electrical interfaces. For chip-to-module interfaces and for chip-to-chip interfaces, one width of 800GAUI-n is defined: eight-lane 800GAUI-8 C2C and 800GAUI-8 C2M. (See IEEE Std 802.3, Annex 120F and Annex 120G.)

1.4.184i 800 Gb/s Media Independent Interface (800GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 800 Gb/s operation. (See IEEE Std 802.3, Clause 170.)

1.4.184j 800GMII Extender: The 800 Gb/s Media Independent Interface Extender extends the reach of the 800GMII and consists of two 800GXS sublayers with one or two 800GAUI-n between them. (See IEEE Std 802.3, Clause 171.)

1.4.184k 800GXS: The 800GMII Extender Sublayer (800GXS) is part of the 800GMII Extender. In functionality, it is almost identical to the 800GBASE-R PCS defined in Clause 172. Two types of 800GXS are defined: the DTE 800GXS adjacent to the Reconciliation Sublayer (RS) and the PHY 800GXS adjacent to the PHY. (See IEEE Std 802.3, Clause 171.)

Change 1.4.205 as follows:

1.4.205 BASE-R: An IEEE 802.3 family of Physical Layer devices using the 64B/66B encoding defined in [Clause 49](#), [Clause 82](#), [Clause 107](#), [Clause 119](#), [or Clause 129](#), [or Clause 172](#) of IEEE Std 802.3.

Change 1.4.461 as follows:

1.4.461 PCS lane (PCSL): In 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, ~~and 400GBASE-R, and 800GBASE-R~~, the PCS distributes encoded data to multiple logical lanes, ~~these logical lanes that~~ are called PCS lanes. One or more PCS lanes can be multiplexed and carried together on a physical lane ~~together~~ at the PMA service interface. (See IEEE Std 802.3, [Clause 83](#), Clause 120, ~~and Clause 135~~, ~~and Clause 173~~.)

1.5 Abbreviations

Insert the following new abbreviations into the list in 1.5, in alphanumeric order:

800GAUI-n	800 Gb/s Attachment Unit Interface over n lanes
800GMII	800 Gb/s Media Independent Interface
800GXS	800GMII Extender Sublayer

4. Media Access Control

4.4 Specific implementations

4.4.2 MAC parameters

Change Table 4–2 as follows:

Table 4–2—MAC parameters

Parameters	MAC data rate			
	Up to and including 100 Mb/s	1 Gb/s	2.5 Gb/s, 5 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, ~~and~~ 400 Gb/s, <u>and 800 Gb/s</u>	10 Gb/s
slotTime	512 bit times	4096 bit times	not applicable	not applicable
interPacketGap ^a	96 bits	96 bits	96 bits	96 bits
attemptLimit	16	16	not applicable	not applicable
backoffLimit	10	10	not applicable	not applicable
jamSize	32 bits	32 bits	not applicable	not applicable
maxBasicFrameSize	1518 octets	1518 octets	1518 octets	1518 octets
maxEnvelopeFrameSize	2000 octets	2000 octets	2000 octets	2000 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	not applicable	not applicable
ipgStretchRatio	not applicable	not applicable	not applicable	104 bits

^a References to interFrameGap or interFrameSpacing in other clauses (e.g., [Clause 13](#), [Clause 35](#), and [Clause 42](#)) shall be interpreted as interPacketGap.

Change Note 7 in 4.4.2 as follows:

NOTE 7—For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, ~~and 400 Gb/s, and 800 Gb/s~~ operation, the received interpacket gap (the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet) can have a minimum value of 8 BT (bit times), as measured at the XLGMII, 50GMII, CGMII, 200GMII, ~~or 400GMII, or 800GMII~~ receive signals at the DTE due to clock tolerance and lane alignment requirements.

21. Introduction to 100 Mb/s baseband networks, type 100BASE-T

21.6 Protocol implementation conformance statement (PICS) proforma

21.6.2 Abbreviations and special symbols

Change 21.6.2 as follows:

The following symbols are used in the PICS proforma:

M	mandatory field/function
!	negation
O	optional field/function
O.<n>	optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n>	optional field/function, but one and only one of the group of options labeled by the same numeral <n> is required
X	prohibited field/function
<item>:	simple-predicate condition, dependent on the support marked for <item>
<item1>*<item2>:	AND-predicate condition, the requirement has to be met if both optional items are implemented
<u><item1>+<item2>:</u>	<u>OR-predicate condition, the requirement has to be met if one or both of the items is implemented</u>

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.3.2.1.2 after the entry for 400GBASE-R:

800GBASE-R	Clause 172 800 Gb/s multi-PCS lane 64B/66B
------------	--

30.3.2.1.3 aPhyTypeList

Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.3.2.1.3 after the entry for 400GBASE-R:

800GBASE-R	Clause 172 800 Gb/s multi-PCS lane 64B/66B
------------	--

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.5.1.1.2 after the entry for 400GBASE-DR4:

400GBASE-DR4-2	400GBASE-R PCS/PMA over 4 single-mode fibers in each direction PMD with reach up to at least 2 km as specified in Clause 124
----------------	---

Insert the following new entries into the “APPROPRIATE SYNTAX” section of 30.5.1.1.2 (as amended by IEEE Std 802.3db-2022) after the entry for 400GBASE-VR4:

800GBASE-CR8	800GBASE-R PCS/PMA over 8-lane shielded balanced copper cable PMD as specified in Clause 162
800GBASE-DR8	800GBASE-R PCS/PMA over 8 single-mode fibers in each direction PMD with reach up to at least 500 m as specified in Clause 124
800GBASE-DR8-2	800GBASE-R PCS/PMA over 8 single-mode fibers in each direction PMD with reach up to at least 2 km as specified in Clause 124
800GBASE-KR8	800GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 163
800GBASE-R	Multi-lane PCS as specified in Clause 172 over undefined PMA/PMD
800GBASE-SR8	800GBASE-R PCS/PMA over 8 multimode fibers in each direction PMD with reach up to at least 100 m as specified in Clause 167
800GBASE-VR8	800GBASE-R PCS/PMA over 8 multimode fibers in each direction PMD with reach up to at least 50 m as specified in Clause 167

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entry into the “APPROPRIATE SYNTAX” section of 30.6.1.1.5 (as amended by IEEE Std 802.3ck-2022) after the entry for 400GR4:

800GR8	800GBASE-CR8 as specified in Clause 162 or 800GBASE-KR8 as specified in Clause 163
--------	--

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface registers

45.2.1 PMA/PMD registers

Change the rows for registers 1.73 to 1.79, 1.1120 to 1.1199, 1.1220 to 1.1299, 1.1320 to 1.1399, and 1.1420 to 1.1499 in Table 45–3 (as amended by IEEE Std 802.3cz-2023) as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
...		
<u>1.73</u>	<u>800G PMA/PMD ability</u>	<u>45.2.1.60b</u>
<u>1.74 through 1.79</u> ~~1.73 through 1.79~~	Reserved	
...		
<u>1.1120 through 1.1127</u> ~~1.1120 through 1.1123~~	BASE-R PAM4 PMD training LP control, lane 0 through lane ~~73~~	45.2.1.161
<u>1.1128 through 1.1199</u> ~~1.1124 through 1.1199~~	Reserved	
...		
<u>1.1220 through 1.1227</u> ~~1.1220 through 1.1223~~	BASE-R PAM4 PMD training LP status, lane 0 through lane ~~73~~	45.2.1.163
<u>1.1228 through 1.1299</u> ~~1.1224 through 1.1299~~	Reserved	
...		
<u>1.1320 through 1.1327</u> ~~1.1320 through 1.1323~~	BASE-R PAM4 PMD training LD control, lane 0 through lane ~~73~~	45.2.1.165
<u>1.1328 through 1.1399</u> ~~1.1324 through 1.1399~~	Reserved	
...		
<u>1.1420 through 1.1427</u> ~~1.1420 through 1.1423~~	BASE-R PAM4 PMD training LD status, lane 0 through lane ~~73~~	45.2.1.167
<u>1.1428 through 1.1449</u> ~~1.1424 through 1.1449~~	Reserved	
<u>1.1450 through 1.1457</u> ~~1.1450 through 1.1453~~	PMD training pattern, lanes 0 to ~~73~~	45.2.1.168
<u>1.1458 through 1.1499</u> ~~1.1454 through 1.1499~~	Reserved	
...		

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change Table 45–4 as follows (unchanged rows not shown):

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
1.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 1 = <u>Reserved</u> 1 0 1 0 = <u>800 Gb/s</u> 1 0 1 x = <u>Reserved</u> 1 0 0 1 = 400 Gb/s 1 0 0 0 = 200 Gb/s 0 1 1 1 = 5 Gb/s 0 1 1 0 = 2.5 Gb/s 0 1 0 1 = 50 Gb/s 0 1 0 0 = 25 Gb/s 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
...			

^a R/W = Read/Write, SC = Self-clearing, RO = Read only.

45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

Change the last paragraph of 45.2.1.1.3 as follows:

When bits 5 through 2 are set to 0010 the use of a 40G PMA/PMD is selected; when set to 0011 the use of a 100G PMA/PMD is selected; when set to 0100 the use of a 25G PMA/PMD is selected; when set to 0101 the use of a 50G PMA/PMD is selected; when set to 0110 the use of a 2.5G PMA/PMD is selected; when set to 0111 the use of a 5G PMA/PMD is selected; when set to 1000 the use of a 200G PMA/PMD is selected; when set to 1001 the use of a 400G PMA/PMD is selected; when set to 1010 the use of an 800G PMA/PMD is selected. More specific selection is performed using the PMA/PMD control 2 register (register 1.7) (see [45.2.1.6.3](#)).

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change Table 45–7 (as amended by IEEE Std 802.3db-2022, IEEE Std 802.3ck-2022, and IEEE Std 802.3cz-2023) as follows:

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.7.15:10	Reserved	Value always 0	RO
1.7.9	PIASE	PMA ingress AUI stop enable	R/W
1.7.8	PEASE	PMA egress AUI stop enable	R/W
~~1.7.7~~	~~Reserved~~	~~Value always 0~~	~~RO~~
~~1.7.7:0~~ ~~1.7.6:0~~	PMA/PMD type selection	7 6 5 4 3 2 1 0 <u>1 1 x x x x x = reserved</u> <u>1 0 1 x x x x = reserved</u> <u>1 0 0 1 x x x = reserved</u> <u>1 0 0 0 1 x x = reserved</u> <u>1 0 0 0 0 1 x = reserved</u> <u>1 0 0 0 0 1 0 1 = 800GBASE-DR8-2 PMA/PMD</u> <u>1 0 0 0 0 1 0 0 = 800GBASE-DR8 PMA/PMD</u> <u>1 0 0 0 0 0 1 1 = 800GBASE-SR8 PMA/PMD</u> <u>1 0 0 0 0 0 1 0 = 800GBASE-VR8 PMA/PMD</u> <u>1 0 0 0 0 0 0 1 = 800GBASE-CR8 PMA/PMD</u> <u>1 0 0 0 0 0 0 0 = 800GBASE-KR8 PMA/PMD</u> <u>0 1 1 1 1 1 1 1 = reserved</u> <u>0 1 1 1 1 1 1 0 = 400GBASE-SR4 PMA/PMD</u> <u>0 1 1 1 1 1 0 1 = 400GBASE-VR4 PMA/PMD</u> <u>0 1 1 1 1 1 0 0 = 200GBASE-SR2 PMA/PMD</u> <u>0 1 1 1 1 0 1 1 = 200GBASE-VR2 PMA/PMD</u> <u>0 1 1 1 1 0 1 0 = 100GBASE-SR1 PMA/PMD</u> <u>0 1 1 1 1 0 0 1 = 100GBASE-VR1 PMA/PMD</u> <u>0 1 1 1 1 0 0 0 = 50GBASE-BR40-U PMA/PMD</u> <u>0 1 1 1 0 1 1 1 = 50GBASE-BR20-U PMA/PMD</u> <u>0 1 1 1 0 1 1 0 = 50GBASE-BR10-U PMA/PMD</u> <u>0 1 1 1 0 1 0 1 = 50GBASE-BR40-D PMA/PMD</u> <u>0 1 1 1 0 1 0 0 = 50GBASE-BR20-D PMA/PMD</u> <u>0 1 1 1 0 0 1 1 = 50GBASE-BR10-D PMA/PMD</u> <u>0 1 1 1 0 0 1 0 = 25GBASE-BR40-U PMA/PMD</u> <u>0 1 1 1 0 0 0 1 = 25GBASE-BR20-U PMA/PMD</u> <u>0 1 1 1 0 0 0 0 = 25GBASE-BR10-U PMA/PMD</u> <u>0 1 1 0 1 1 1 1 = 25GBASE-BR40-D PMA/PMD</u> <u>0 1 1 0 1 1 1 0 = 25GBASE-BR20-D PMA/PMD</u> <u>0 1 1 0 1 1 0 1 = 25GBASE-BR10-D PMA/PMD</u> <u>0 1 1 0 1 1 0 0 = 10GBASE-BR40-U PMA/PMD</u> <u>0 1 1 0 1 0 1 1 = 10GBASE-BR20-U PMA/PMD</u> <u>0 1 1 0 1 0 1 0 = 10GBASE-BR10-U PMA/PMD</u> <u>0 1 1 0 1 0 0 1 = 10GBASE-BR40-D PMA/PMD</u> <u>0 1 1 0 1 0 0 0 = 10GBASE-BR20-D PMA/PMD</u> <u>0 1 1 0 0 1 1 1 = 10GBASE-BR10-D PMA/PMD</u> <u>0 1 1 0 0 1 1 0 = reserved</u> ~~<u>1 1 0 0 1 0 x = reserved</u>~~ <u>0 1 1 0 0 1 0 1 = reserved</u> <u>0 1 1 0 0 1 0 0 = 400GBASE-DR4-2 PMA/PMD</u> <u>0 1 1 0 0 0 1 1 = 400GBASE-ER8 PMA/PMD</u> <u>0 1 1 0 0 0 1 0 = 400GBASE-LR4-6 PMA/PMD</u>	R/W

Table 45–7—PMA/PMD control 2 register bit definitions (*continued*)

Bit(s)	Name	Description	R/W ^a
1.7.7:0 1.7.6:0 (<i>continued</i>)	PMA/PMD type selection (<i>continued</i>)	01100001 = 400GBASE-FR4 PMA/PMD 01100000 = 400GBASE-SR4.2 PMA/PMD 01011111 = 400GBASE-SR8 PMA/PMD 01011110 = 400GBASE-CR4 PMA/PMD 01011101 = 400GBASE-KR4 PMA/PMD 01011100 = 400GBASE-LR8 PMA/PMD 01011011 = 400GBASE-FR8 PMA/PMD 01011010 = 400GBASE-DR4 PMA/PMD 01011001 = 400GBASE-SR16 PMA/PMD 01011000 = 200GBASE-ER4 PMA/PMD 01010111 = 200GBASE-CR2 PMA/PMD 01010110 = 200GBASE-KR2 PMA/PMD 01010101 = 200GBASE-LR4 PMA/PMD 01010100 = 200GBASE-FR4 PMA/PMD 01010011 = 200GBASE-DR4 PMA/PMD 01010010 = 200GBASE-SR4 PMA/PMD 01010001 = 200GBASE-CR4 PMA/PMD 01010000 = 200GBASE-KR4 PMA/PMD 01001111 = reserved 01001110 = 100GBASE-ZR PMA/PMD 01001101 = 100GBASE-LR1 PMA/PMD 01001100 = 100GBASE-FR1 PMA/PMD 01001011 = 100GBASE-DR PMA/PMD 01001010 = 100GBASE-SR2 PMA/PMD 01001001 = 100GBASE-CR2 PMA/PMD 01001000 = 100GBASE-KR2 PMA/PMD 01000111 = 100GBASE-CR1 PMA/PMD 01000110 = 100GBASE-KR1 PMA/PMD 01000101 = 50GBASE-ER PMA/PMD 01000100 = 50GBASE-LR PMA/PMD 01000011 = 50GBASE-FR PMA/PMD 01000010 = 50GBASE-SR PMA/PMD 01000001 = 50GBASE-CR PMA/PMD 01000000 = 50GBASE-KR PMA/PMD 00111111 = reserved 00111110 = BASE-AU PMA/PMD^b 00111101 = BASE-T1 PMA/PMD^c 00111100 = 5GBASE-KR PMA/PMD 00111011 = 2.5GBASE-KX PMA/PMD 00111010 = 25GBASE-SR PMA/PMD 00111001 = 25GBASE-KR or 25GBASE-KR-S PMA/PMD 00111000 = 25GBASE-CR or 25GBASE-CR-S PMA/PMD 00110111 = 25GBASE-T PMA 00110110 = 25GBASE-ER PMA/PMD 00110101 = 25GBASE-LR PMA/PMD 00110100 = BASE-H PMA/PMD^d 00110011 = 10GPASS-XR-U PMA/PMD 00110010 = 10GPASS-XR-D PMA/PMD 00110001 = 5GBASE-T PMA 00110000 = 2.5GBASE-T PMA 00101111 = 100GBASE-SR4 PMA/PMD 00101110 = 100GBASE-CR4 PMA/PMD 00101101 = 100GBASE-KR4 PMA/PMD 00101100 = 100GBASE-KP4 PMA/PMD 00101011 = 100GBASE-ER4 PMA/PMD 00101010 = 100GBASE-LR4 PMA/PMD 00101001 = 100GBASE-SR10 PMA/PMD 00101000 = 100GBASE-CR10 PMA/PMD 00100111 = reserved	R/W

Table 45–7—PMA/PMD control 2 register bit definitions (*continued*)

Bit(s)	Name	Description	R/W ^a
1.7.7:0 1.7.6:0 (<i>continued</i>)	PMA/PMD type selection (<i>continued</i>)	00100110 = 40GBASE-T PMA 00100101 = 40GBASE-ER4 PMA/PMD 00100100 = 40GBASE-FR PMA/PMD 00100011 = 40GBASE-LR4 PMA/PMD 00100010 = 40GBASE-SR4 PMA/PMD 00100001 = 40GBASE-CR4 PMA/PMD 00100000 = 40GBASE-KR4 PMA/PMD 00011111 = 10/1GBASE-PRX-U4 00011110 = 10GBASE-PR-U4 00011101 = 10/1GBASE-PRX-D4 00011100 = 10GBASE-PR-D4 00011011 = reserved 00011010 = 10GBASE-PR-U3 00011001 = 10GBASE-PR-U1 00011000 = 10/1GBASE-PRX-U3 00010111 = 10/1GBASE-PRX-U2 00010110 = 10/1GBASE-PRX-U1 00010101 = 10GBASE-PR-D3 00010100 = 10GBASE-PR-D2 00010011 = 10GBASE-PR-D1 00010010 = 10/1GBASE-PRX-D3 00010001 = 10/1GBASE-PRX-D2 00010000 = 10/1GBASE-PRX-D1 00001111 = 10BASE-T PMA/PMD 00001110 = 100BASE-TX PMA/PMD 00001101 = 1000BASE-KX PMA/PMD 00001100 = 1000BASE-T PMA/PMD 00001011 = 10GBASE-KR PMA/PMD 00001010 = 10GBASE-KX4 PMA/PMD 00001001 = 10GBASE-T PMA 00001000 = 10GBASE-LRM PMA/PMD 00000111 = 10GBASE-SR PMA/PMD 00000110 = 10GBASE-LR PMA/PMD 00000101 = 10GBASE-ER PMA/PMD 00000100 = 10GBASE-LX4 PMA/PMD 00000011 = 10GBASE-SW PMA/PMD 00000010 = 10GBASE-LW PMA/PMD 00000001 = 10GBASE-EW PMA/PMD 00000000 = 10GBASE-CX4 PMA/PMD	R/W

^a R/W = Read/Write, RO = Read only.

^b If BASE-AU PMA/PMD is selected, register 1.901 is used to differentiate which BASE-AU PMA/PMD is selected.

^c If BASE-T1 is selected, bits 1.2100.3:0 are used to differentiate which BASE-T1 PMA/PMD is selected.

^d If BASE-H PMA/PMD is selected, register 1.900 is used to differentiate which BASE-H PMA/PMD is selected.

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Change the rows that start with “100GBASE-KR1”, “100GBASE-CR1”, “100GBASE-VR1”, and “400GBASE-DR4” in Table 45–9 (as amended by IEEE Std 802.3db-2022 and IEEE Std 802.3ck-2022) as follows (unchanged rows not shown):

Table 45–9—Transmit fault description location

PMA/PMD	Description location
...	
100GBASE-KR1, 200GBASE-KR2, 400GBASE-KR4, <u>800GBASE-KR8</u>	163.8.9
...	
100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4, <u>800GBASE-CR8</u>	162.8.9
...	
100GBASE-VR1, 100GBASE-SR1, 200GBASE-VR2, 200GBASE-SR2, 400GBASE-VR4, 400GBASE-SR4, <u>800GBASE-VR8, 800GBASE-SR8</u>	167.5.10
...	
400GBASE-DR4, <u>400GBASE-DR4-2, 800GBASE-DR8, 800GBASE-DR8-2</u>	124.5.10
...	

45.2.1.7.5 Receive fault (1.8.10)

Change the rows that start with “100GBASE-KR1”, “100GBASE-CR1”, “100GBASE-VR1”, and “400GBASE-DR4” in Table 45–10 (as amended by IEEE Std 802.3db-2022 and IEEE Std 802.3ck-2022) as follows (unchanged rows not shown):

Table 45–10—Receive fault description location

PMA/PMD	Description location
...	
100GBASE-KR1, 200GBASE-KR2, 400GBASE-KR4, <u>800GBASE-KR8</u>	163.8.10
...	
100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4, <u>800GBASE-CR8</u>	162.8.10
...	

Table 45–10—Receive fault description location (*continued*)

PMA/PMD	Description location
100GBASE-VR1, 100GBASE-SR1, 200GBASE-VR2, 200GBASE-SR2, 400GBASE-VR4, 400GBASE-SR4, <u>800GBASE-VR8, 800GBASE-SR8</u>	167.5.11
...	
400GBASE-DR4, <u>400GBASE-DR4-2, 800GBASE-DR8,</u> <u>800GBASE-DR8-2</u>	124.5.11
...	

45.2.1.8 PMD transmit disable register (Register 1.9)

Change the rows that start with “100GBASE-KR1”, “100GBASE-CR1”, “100GBASE-VR1”, and “400GBASE-DR4” in Table 45–12 (as amended by IEEE Std 802.3db-2022 and IEEE Std 802.3ck-2022) as follows (unchanged rows not shown):

Table 45–12—Transmit disable description location

PMA/PMD	Description location
...	
100GBASE-KR1, 200GBASE-KR2, ~~and~~ 400GBASE-KR4, <u>and 800GBASE-KR8</u>	163.8.6
...	
100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, <u>and 800GBASE-CR8</u>	162.8.6
...	
100GBASE-VR1, 100GBASE-SR1, 200GBASE-VR2, 200GBASE-SR2, 400GBASE-VR4, ~~and~~ 400GBASE-SR4, <u>800GBASE-VR8, and 800GBASE-SR8</u>	167.5.7
...	
400GBASE-DR4, <u>400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2</u>	124.5.7
...	

45.2.1.22 400G PMA/PMD extended ability register (Register 1.24)

Change the row for bit 1.24.14 in Table 45–25 (as amended by IEEE Std 802.3db-2022) as follows (unchanged rows not shown):

Table 45–25—400G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
1.24.14	~~Reserved~~ 400GBASE-DR4-2 ability	~~Value always 0~~ 1 = PMA/PMD is able to perform 400GBASE-DR4-2 0 = PMA/PMD is not able to perform 400GBASE-DR4-2	RO
...			

^a RO = Read only.

Insert 45.2.1.22.1aa after 45.2.1.22.1 as follows:

45.2.1.22.1aa 400GBASE-DR4-2 ability (1.24.14)

When read as a one, bit 1.24.14 indicates that the PMA/PMD is able to operate as a 400GBASE-DR4-2 PMA/PMD type. When read as a zero, bit 1.24.14 indicates that the PMA/PMD is not able to operate as a 400GBASE-DR4-2 PMA/PMD type.

45.2.1.23 PMA/PMD extended ability 2 (Register 1.25)

Change Table 45–26 as follows:

Table 45–26—PMA/PMD extended ability 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
~~1.25.15:2~~ ~~1.25.15:1~~	Reserved	Value always 0	RO
<u>1.25.1</u>	<u>800G capable</u>	<u>1 = PMA/PMD is capable of operating at 800 Gb/s and has the abilities listed in register 1.73</u> <u>0 = PMA/PMD is not capable of operating at 800 Gb/s</u>	<u>RO</u>
1.25.0	50G extended abilities	1 = PMA/PMD has 50G extended abilities listed in register 1.20 0 = PMA/PMD does not have 50G extended abilities	RO

^a RO = Read only.

Insert 45.2.1.23.a before 45.2.1.23.1 as follows:

45.2.1.23.a 800G capable (1.25.1)

When read as a one, bit 1.25.1 indicates that the PMA/PMD is capable of operating at 800 Gb/s and has the abilities listed in register 1.73. When read as a zero, bit 1.25.1 indicates that the PMA/PMD is not capable of operating at 800 Gb/s.

Insert 45.2.1.60b after 45.2.1.60a (as inserted by IEEE Std 802.3cz-2023) as follows:

45.2.1.60b 800G PMA/PMD ability (Register 1.73)

The assignment of bits in the 800G PMA/PMD ability register is shown in Table 45–58b.

Table 45–58b—800G PMA/PMD ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.73.15	800G PMA remote loopback ability	1 = 800G PMA is able to perform a remote loopback function 0 = 800G PMA is not able to perform a remote loopback function	RO
1.73.14:6	Reserved	Value always 0	RO
1.73.5	800GBASE-DR8-2 ability	1 = PMA/PMD is able to perform 800GBASE-DR8-2 0 = PMA/PMD is not able to perform 800GBASE-DR8-2	RO
1.73.4	800GBASE-DR8 ability	1 = PMA/PMD is able to perform 800GBASE-DR8 0 = PMA/PMD is not able to perform 800GBASE-DR8	RO
1.73.3	800GBASE-SR8 ability	1 = PMA/PMD is able to perform 800GBASE-SR8 0 = PMA/PMD is not able to perform 800GBASE-SR8	RO
1.73.2	800GBASE-VR8 ability	1 = PMA/PMD is able to perform 800GBASE-VR8 0 = PMA/PMD is not able to perform 800GBASE-VR8	RO
1.73.1	800GBASE-CR8 ability	1 = PMA/PMD is able to perform 800GBASE-CR8 0 = PMA/PMD is not able to perform 800GBASE-CR8	RO
1.73.0	800GBASE-KR8 ability	1 = PMA/PMD is able to perform 800GBASE-KR8 0 = PMA/PMD is not able to perform 800GBASE-KR8	RO

^a RO = Read only.

45.2.1.60b.1 800G PMA remote loopback ability (1.73.15)

When read as a one, bit 1.73.15 indicates that the 800G PMA is able to perform the remote loopback function. When read as a zero, bit 1.73.15 indicates that the 800G PMA is not able to perform the remote loopback function. If a PMA is able to perform the remote loopback function, then it is controlled using the PMA remote loopback bit 1.0.1 (see 45.2.1.1.4).

45.2.1.60b.2 800GBASE-DR8-2 ability (1.73.5)

When read as a one, bit 1.73.5 indicates that the PMA/PMD is able to operate as an 800GBASE-DR8-2 PMA/PMD type. When read as a zero, bit 1.73.5 indicates that the PMA/PMD is not able to operate as an 800GBASE-DR8-2 PMA/PMD type.

45.2.1.60b.3 800GBASE-DR8 ability (1.73.4)

When read as a one, bit 1.73.4 indicates that the PMA/PMD is able to operate as an 800GBASE-DR8 PMA/PMD type. When read as a zero, bit 1.73.4 indicates that the PMA/PMD is not able to operate as an 800GBASE-DR8 PMA/PMD type.

45.2.1.60b.4 800GBASE-SR8 ability (1.73.3)

When read as a one, bit 1.73.3 indicates that the PMA/PMD is able to operate as an 800GBASE-SR8 PMA/PMD type. When read as a zero, bit 1.73.3 indicates that the PMA/PMD is not able to operate as an 800GBASE-SR8 PMA/PMD type.

45.2.1.60b.5 800GBASE-VR8 ability (1.73.2)

When read as a one, bit 1.73.2 indicates that the PMA/PMD is able to operate as an 800GBASE-VR8 PMA/PMD type. When read as a zero, bit 1.73.2 indicates that the PMA/PMD is not able to operate as an 800GBASE-VR8 PMA/PMD type.

45.2.1.60b.6 800GBASE-CR8 ability (1.73.1)

When read as a one, bit 1.73.1 indicates that the PMA/PMD is able to operate as an 800GBASE-CR8 PMA/PMD type. When read as a zero, bit 1.73.1 indicates that the PMA/PMD is not able to operate as an 800GBASE-CR8 PMA/PMD type.

45.2.1.60b.7 800GBASE-KR8 ability (1.73.0)

When read as a one, bit 1.73.0 indicates that the PMA/PMD is able to operate as an 800GBASE-KR8 PMA/PMD type. When read as a zero, bit 1.73.0 indicates that the PMA/PMD is not able to operate as an 800GBASE-KR8 PMA/PMD type.

45.2.1.139 PMA precoder control Tx output (Register 1.600)

Change Table 45–109 as follows:

Table 45–109—PMA precoder control Tx output register bit definitions

Bit(s)	Name	Description	R/W ^a
1.600.15:84	Reserved	Value always 0	RO
<u>1.600.7</u>	<u>Lane 7 Tx output precoder enable</u>	<u>1 = Lane 7 Tx output precoder enabled</u> <u>0 = Lane 7 Tx output precoder disabled</u>	<u>R/W</u>
<u>1.600.6</u>	<u>Lane 6 Tx output precoder enable</u>	<u>1 = Lane 6 Tx output precoder enabled</u> <u>0 = Lane 6 Tx output precoder disabled</u>	<u>R/W</u>
<u>1.600.5</u>	<u>Lane 5 Tx output precoder enable</u>	<u>1 = Lane 5 Tx output precoder enabled</u> <u>0 = Lane 5 Tx output precoder disabled</u>	<u>R/W</u>
<u>1.600.4</u>	<u>Lane 4 Tx output precoder enable</u>	<u>1 = Lane 4 Tx output precoder enabled</u> <u>0 = Lane 4 Tx output precoder disabled</u>	<u>R/W</u>
1.600.3	Lane 3 Tx output precoder enable	1 = Lane 3 Tx output precoder enabled 0 = Lane 3 Tx output precoder disabled	R/W
1.600.2	Lane 2 Tx output precoder enable	1 = Lane 2 Tx output precoder enabled 0 = Lane 2 Tx output precoder disabled	R/W
1.600.1	Lane 1 Tx output precoder enable	1 = Lane 1 Tx output precoder enabled 0 = Lane 1 Tx output precoder disabled	R/W
1.600.0	Lane 0 Tx output precoder enable	1 = Lane 0 Tx output precoder enabled 0 = Lane 0 Tx output precoder disabled	R/W

^a R/W = Read/Write, RO = Read only.

Insert 45.2.1.139.a to 45.2.1.139.d before 45.2.1.139.1 as follows:

45.2.1.139.a Lane 7 Tx output precoder enable (1.600.7)

This bit enables the lane 7 Tx output precoder.

45.2.1.139.b Lane 6 Tx output precoder enable (1.600.6)

This bit enables the lane 6 Tx output precoder.

45.2.1.139.c Lane 5 Tx output precoder enable (1.600.5)

This bit enables the lane 5 Tx output precoder.

45.2.1.139.d Lane 4 Tx output precoder enable (1.600.4)

This bit enables the lane 4 Tx output precoder.

45.2.1.140 PMA precoder control Rx input (Register 1.601)

Change Table 45–110 as follows:

Table 45–110—PMA precoder control Rx input register bit definitions

Bit(s)	Name	Description	R/W ^a
1.601.15:84	Reserved	Value always 0	RO
<u>1.601.7</u>	<u>Lane 7 Rx input precoder enable</u>	<u>1 = Lane 7 Rx input precoder enabled</u> <u>0 = Lane 7 Rx input precoder disabled</u>	<u>R/W</u>
<u>1.601.6</u>	<u>Lane 6 Rx input precoder enable</u>	<u>1 = Lane 6 Rx input precoder enabled</u> <u>0 = Lane 6 Rx input precoder disabled</u>	<u>R/W</u>
<u>1.601.5</u>	<u>Lane 5 Rx input precoder enable</u>	<u>1 = Lane 5 Rx input precoder enabled</u> <u>0 = Lane 5 Rx input precoder disabled</u>	<u>R/W</u>
<u>1.601.4</u>	<u>Lane 4 Rx input precoder enable</u>	<u>1 = Lane 4 Rx input precoder enabled</u> <u>0 = Lane 4 Rx input precoder disabled</u>	<u>R/W</u>
1.601.3	Lane 3 Rx input precoder enable	1 = Lane 3 Rx input precoder enabled 0 = Lane 3 Rx input precoder disabled	R/W
1.601.2	Lane 2 Rx input precoder enable	1 = Lane 2 Rx input precoder enabled 0 = Lane 2 Rx input precoder disabled	R/W
1.601.1	Lane 1 Rx input precoder enable	1 = Lane 1 Rx input precoder enabled 0 = Lane 1 Rx input precoder disabled	R/W
1.601.0	Lane 0 Rx input precoder enable	1 = Lane 0 Rx input precoder enabled 0 = Lane 0 Rx input precoder disabled	R/W

^a R/W = Read/Write, RO = Read only.

Insert 45.2.1.140.a to 45.2.1.140.d before 45.2.1.140.1 as follows:

45.2.1.140.a Lane 7 Rx input precoder enable (1.601.7)

This bit enables the lane 7 Rx input precoder.

45.2.1.140.b Lane 6 Rx input precoder enable (1.601.6)

This bit enables the lane 6 Rx input precoder.

45.2.1.140.c Lane 5 Rx input precoder enable (1.601.5)

This bit enables the lane 5 Rx input precoder.

45.2.1.140.d Lane 4 Rx input precoder enable (1.601.4)

This bit enables the lane 4 Rx input precoder.

45.2.1.141 PMA precoder control Rx output (Register 1.602)

Change Table 45–111 as follows:

Table 45–111—PMA precoder control Rx output register bit definitions

Bit(s)	Name	Description	R/W ^a
1.602.15:82	Reserved	Value always 0	RO
1.602.7	Lane 7 Rx output precoder enable	1 = Lane 7 Rx output precoder enabled 0 = Lane 7 Rx output precoder disabled	R/W
1.602.6	Lane 6 Rx output precoder enable	1 = Lane 6 Rx output precoder enabled 0 = Lane 6 Rx output precoder disabled	R/W
1.602.5	Lane 5 Rx output precoder enable	1 = Lane 5 Rx output precoder enabled 0 = Lane 5 Rx output precoder disabled	R/W
1.602.4	Lane 4 Rx output precoder enable	1 = Lane 4 Rx output precoder enabled 0 = Lane 4 Rx output precoder disabled	R/W
1.602.3	Lane 3 Rx output precoder enable	1 = Lane 3 Rx output precoder enabled 0 = Lane 3 Rx output precoder disabled	R/W
1.602.2	Lane 2 Rx output precoder enable	1 = Lane 2 Rx output precoder enabled 0 = Lane 2 Rx output precoder disabled	R/W
1.602.1	Lane 1 Rx output precoder enable	1 = Lane 1 Rx output precoder enabled 0 = Lane 1 Rx output precoder disabled	R/W
1.602.0	Lane 0 Rx output precoder enable	1 = Lane 0 Rx output precoder enabled 0 = Lane 0 Rx output precoder disabled	R/W

^a R/W = Read/Write, RO = Read only.