

IEEE Standard Backplane Bus Specification for Multiprocessor Architectures: Futurebus+[®]

IEEE Computer Society

Sponsored by the
Technical Committee on Microprocessors and Microcomputers

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Backplane Bus Specification for
Multiprocessor Architectures: Futurebus



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Std 896.1-1987**

An American National Standard

**IEEE Standard
Backplane Bus Specification for
Multiprocessor Architectures: Futurebus**

Sponsor
**Technical Committee on Microprocessors and Microcomputers
of the
IEEE Computer Society**

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Foreword

(This Foreword is not a part of ANSI/IEEE Std 896.1-1987, IEEE Standard Backplane Bus Specification for Multiprocessor Architectures: Futurebus.)

Historical Overview

A Committee on microprocessor standards was set up by the IEEE Computer Society in August 1977. By the middle of 1978, the Committee's efforts toward developing specifications for the 696 (S-100) and 796 (Multibus®) standards had made clear the need to consider future microprocessor bus requirements before the emergence of yet another generation of "de facto" but incompletely specified and incompatible buses.

A subgroup, with the name "FutureBus" Committee led by Cash Olsen, operated for about a year within the 696 project. This subgroup concluded that the buses then being specified by the Microprocessor Standards Committee did not offer the capability of being extended to satisfy the requirements anticipated for future microprocessor-based systems. Three major categories of bus (backplane, local interconnect, and residential) were identified. As a result of this work, Andrew Allison set up an independent subcommittee in June 1979 to study the backplane requirements, and the Project Authorization Request Number P896 was approved by the IEEE Standards Board in September of the same year. In September 1980 Professor J. D. Nicoud was appointed by the Chairman to the position of Vice-Chairman and the leader of the European collaborators.

The first draft approved by the Working Group was submitted to the Microprocessor Standards Committee in December 1981, and was returned to the Working Group for further work in January 1982, causing the resignation of the Chairman and Vice-Chairman. Jim Moyer carried on as Chairman from February until August 1982 considering means to improve performance of the bus. Bob Davis was appointed Chairman in August 1982 and laid the groundwork of requirements and objectives upon which the current work is based. Dr. Paul Borrill, the current Chairman, was appointed in December 1982. EDISG (European Distributed Intelligence Study Group, supported by the Commission of the European Communities) set up a subgroup in May 1980 to interact with the IEEE group. Individuals from the United Kingdom were involved with 896 work from the beginning. Their efforts were coordinated by the IEE (Institution of Electrical Engineers) when it set up a subgroup of its Working Party on Computing Standards in November 1981.

In mid-1982, there was a significant change in objective of the Working Group from providing a processor and manufacturer-independent alternative to the evolving proprietary bus structures, to providing a "significant step forward" in the facilities and performance available to designers of future multiprocessor systems.

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A set of objectives were agreed upon by the Working Group in a questionnaire issued to all members in December 1982, minor modifications of which were made in the P896 Workshop in Oregon, in April 1983, and in a meeting in London earlier the same month.

From this point on, the project was known as “Futurebus,” due to the goal of the Working Group to provide a standard whose performance could improve as technology advances, and therefore to provide some measure of protection, for the benefit users, against technological obsolescence of equipment designed to the standard.

In order to publicize the status of the new specification, a public comment draft of the specification (D6.2) was prepared by the Working Group in November 1983, and published by the IEEE Computer Society in January 1984. In August 1984, several articles were published in *IEEE Micro* related to the specification. Between September 1984 and April 1985, all the comments received by the Working Group were evaluated and used in the preparation of version 7.0 of the specification. Draft 7.0 was finalized by the Working Group Coordinators in September/October 1985, and Draft 7.1 was put to Working Group Ballot in November 1985. By January 1986 no negative ballots had been received. Numerous descriptive and editorial comments, however, were received with the affirmative ballots.

Four significant changes to the specification have been made since Draft 6.2. The first three are technical changes:

- (1) A modification to the control acquisition system to provide “preemption,” a method of allowing a high priority master to access the bus more quickly.
- (2) Incorporation of a scheme for slave intervention to fully support cache-based architectures.
- (3) A modification and additions to the command and status fields of the protocol in order to provide a more comprehensive broadcast facility and to further support cache-based architectures.
- (4) A major restructuring of the document to make it more understandable, one of the most common criticisms of Draft 6.2.

In order to complete the basic Futurebus foundation specification, while not inhibiting further development of the standard, particularly in the higher level layers and the interface to the operating system, the current document is titled 896.1. Work on the higher levels, such as cache consistency protocols, bus repeaters, and software interface, will be collected and put in the next document, and titled 896.2. These two documents have become informally known as the hardware and the firmware documents, respectively.

During the early months of 1986, a revised specification was prepared by the Working Group in response to the comments received during the Draft 7.1 ballot. This document was checked by the Futurebus Task Group coordinators, which resulted in further descriptive refinements to create Draft 7.3.

In July 1986 Draft 7.3 was forwarded to the IEEE Microprocessor Standards Committee for their approval. After corrections to this document were made, Draft 7.4 was sent to the Technical Committee on Microprocessors and Microcomputers for a Sponsor Ballot. This document, along with modifications due to negative responses, was forwarded to the IEEE Standards Board in June 1987 as Draft 7.5 a. The IEEE Standards Board approved this document as an IEEE standard in September 1987.

Major Features of the Specification

The most important overall objective of the 896 Project was to create a bus standard that would provide a *significant* step forward in the facilities and performance available to designers of multiprocessor systems.

This specification is intended to facilitate the design of computer boards that are functionally, operationally, electrically, and mechanically compatible within the same system, and across multiple generations of systems.

The major features of this specification are as follows.

(1) Architecture independence. This standard provides users with a “set of tools” with which to build an implementation, rather than a rigid specification that constrains the user to only one architectural model for their multiprocessor system. This specification may be used to build, for example, *shared memory* systems, which require transactions on the bus to support consistency of data across multiple caches; or *functionally distributed* systems, which require a message passing interface between the boards. It is envisaged that many real systems will be hybrids between these two, and perhaps other, multiprocessor system architectures.

(2) Processor independence. The protocol is designed for maximum efficiency of information transfer between boards, rather than optimizations for any particular manufacturer's device.

(3) Technology independence. The protocols are designed to be independent of the constraints of, for example, manufacturing processes, or tolerances, at the time an implementation is built, while guaranteeing that boards built before, and after, with different manufacturing constraints, are completely compatible.

(4) The elimination of centralized system elements. The smaller the number of single point failure mechanisms in a bus, the more suitable it will be for fault-tolerant applications. Also, by allowing every part of the system to be upgraded independently as technology for the implementations improves, the lack of central elements further supports the requirements of technology independence.

(5) Complete definition of the bus on a single connector, so as not to affect other connectors on the board that may be required for optional use of secondary buses within or without the 896 family, for multiple identical buses in fault-tolerant applications, or for vendor-specific use.

(6) A technology-independent handshake on all bus operations including arbitration. This resulting handshake, based only on cause and effect relationships, is known as a “compelled” protocol. Compelled protocols are theoretically capable of indefinitely fast operation due to the complete elimination of arbitrary timing delays, such as “set-up,” “hold,” and “bus settling” delays between successive events in the protocol.

(7) A solution to the “bus driving problem.” This specification provides an electrical interface that allows the elimination of *all* “bus settling” type delays that could impair performance, with the exception of delays due to the speed of light, and the manufacturing tolerances of components for *specific* implementations of the standard.

(8) A fully asynchronous protocol, using both edges of the synchronization signals, to provide an environment in which to attain the highest bus transfer rate consistent with the widespread manufacture of reliably interchangeable boards.

(9) A set of basic communication primitives, which include:

- “Address-only” transfers
- “Read or write single data” transfers
- “Read or write block data” transfers
- “Read or write broadcast or broadcast” transfers
- “Intervening” transfers
- “Reflecting” transfers

The bus also supports “split” transactions, by virtue of the identity of the current master being visible on the bus during the transaction, wherein the master may relinquish the bus after making the request to a slave, and the slave returns the response at some later time of its own accord.

These basic primitives may be combined to form a powerful set of communication “transactions” between the master and one or more slaves. A master may combine many of these transactions to form a group of operations in a single bus tenure.

(10) Comprehensive facilities for locking and mutual exclusion in a multi-processing environment.

(11) Provision for the protocol to be extended in the future. Specific extensions provided for in the protocol include extension of the width of the address/data path, and a noncompelled handshake mode, which provides the highest possible bandwidth of transfer on a bus system.

The combination of features provided in the electrical specifications solves a number of physical problems that have hitherto prevented computer backplane buses from achieving their full performance capability. This is achieved within a current and power budget that allows the use of octal transceiver packages, and in the future, gate array devices driving the bus directly.

Although the specification of the bus is complete to the level at which systems

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may be built, provision has been explicitly provided to allow compatible extension to higher level protocols. Additional layers of specification to cover noncompelled operation, wider address/data paths, address map assignment, bus repeater and I/O architectures, higher level protocols, etc, are the subject of further development in the Working Group. The ultimate objective of this development is to specify a complete family of standards that may guide the development of advanced systems into the future, so that software developed for a system based on one member of this family of standards may be run, with minimal change, on systems based on any other members of the family.

This specification has been developed over a period of many years by the efforts of volunteers too numerous to mention. The following persons were members of the Working Group while the draft and final specification were compiled:

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1. Scope

This IEEE standard specifies the functional, electrical, and mechanical requirements for a set of signal lines that constitute a backplane bus, and for the interfacing of boards connected to that bus.

The bus provides the means for the transfer of binary digital information between boards over a single backplane. The number of physical modules is restricted to 24 due to electrical and mechanical constraints, even though slot addressing allows up to 31 modules. The modules may contain any combination of one or more processors and immediate peripherals such as memory, peripheral, and communication controllers. Figure 1 shows a block diagram of a typical board.

Two connector pins are allocated for a serial bus, but the provision of such a bus is optional. The purpose of providing a serial bus would be to increase the degree of fault tolerance and survivability of the system. In any high integrity system an alternate control path is required in order to prevent major system faults and allow, at least partially, orderly operation in the event of a component failure associated with the parallel bus. A serial bus is the most cost-effective way of providing such an alternate control path. The definition of the serial bus is outside the scope of this standard. It is anticipated that a common serial bus protocol will be developed within the IEEE P1394 Working Group that will be applicable to all future parallel bus standards.

Protocols are specified for the allocation of bus time to modules needing to conduct transactions with other modules over the bus. However, the standard does not lay down mandatory priority rules for modules to use when competing for use of the bus. These are considered the responsibility and privilege of the system implementer. The standard includes a full set of signaling rules to be followed by all modules in the distributed control acquisition process leading to bus mastership (Section 6). The standard also gives a full set of signaling rules for all modules participating in a bus transaction (Section 7).

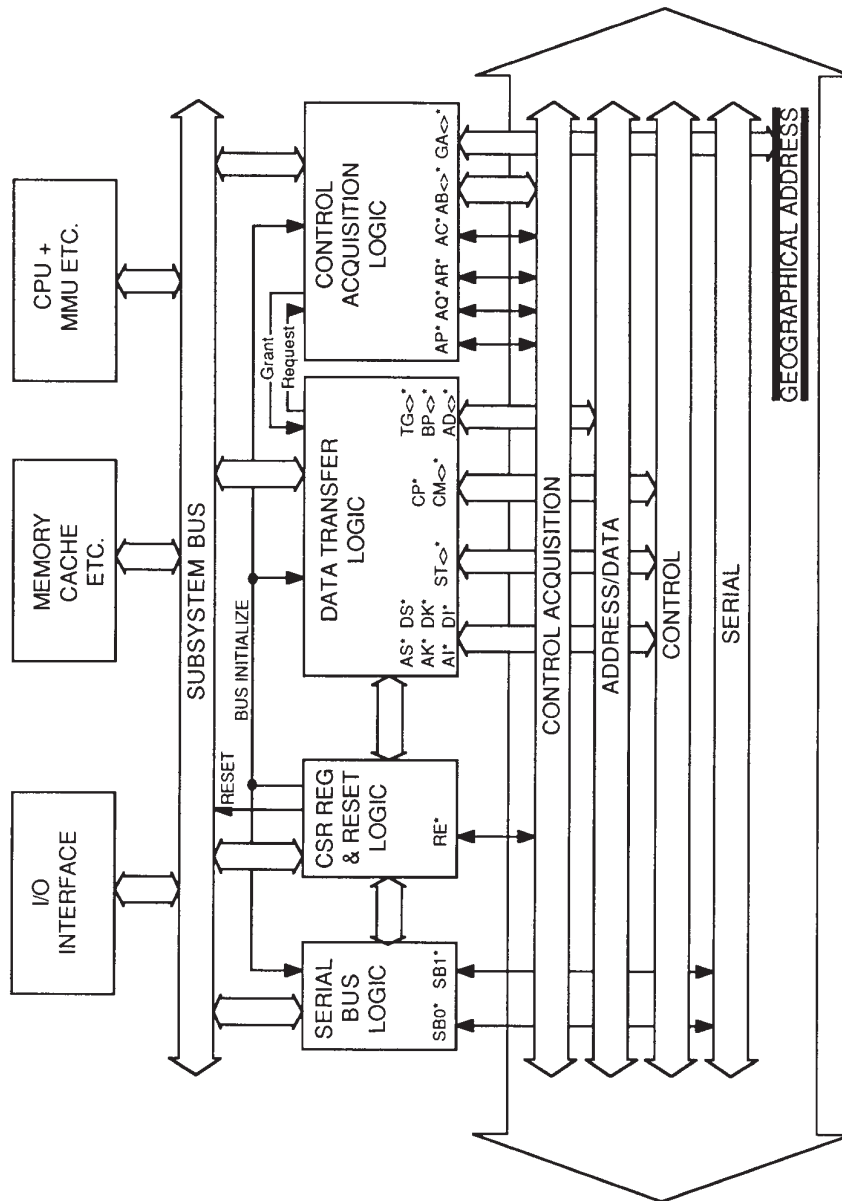


Fig 1
Interfaces in a Typical Board

All signaling rules within this standard are “compelled,” that is, they are governed by a pure cause and effect relationship. This is what gives this standard its technology-independent nature, and is what justifies its title “Futurebus.” This compelled signaling provides a designer with a logical simplicity and instinctive understanding of what takes place in the protocols. As a result, there will be compatibility between products designed to this standard throughout their operational lifetime.

The standard defines the electrical and signal timing characteristics required of transmitters and receivers in modules plugged into the backplane, and of the backplane itself. These include:

- (1) The voltage levels of the active and quiescent logic states on the bus.
- (2) The required characteristics of the backplane and termination networks.
- (3) The required characteristics of the bus transmitters and receivers.

Certain mechanical parameters are specified, including a range of printed circuit board sizes conforming with IEC standards and the connector footprint to be used on the backplane into which the boards plug. The recommended connector also conforms with an IEC standard. These mechanical parameters that directly affect the electrical characteristics of the bus are also specified, for example, the physical length of the bus, the minimum spacing of the connectors on the backplane, and the signal assignments to pins on the connector.

With any bus as advanced and versatile as Futurebus, there is the dilemma of how far the standard should go. There must be a balance between ensuring that all boards made by a variety of manufacturers can operate together, while not restricting the users of the bus to any preconceived system design. The scope of this standard has been restricted to exclude many of the system requirements associated with bus-based computer systems, but these are being addressed in a companion project (896.2¹), which represents the next higher level. The topics to be addressed in this future standard include command and status register space assignments, algorithms to maintain data consistency in cache-based systems, message passing, use of the bus-locking facilities, data tagging, and detailed events (interrupts). This document, however, does set out some requirements and suggestions on these topics.

Where appropriate, each subject of this standard is divided into two parts: a description and a specification. The former is intended only as an aid to understanding the bus, and is not intended to imply any requirements on equipment built to this standard. The specification part contains all of the requirements with which equipment designed to this standard must comply. Should any divergence exist

¹At the time of publication of this standard, document 896.2 was in preparation and was not yet published.

between the description and the specification sections, then the specification shall take precedence.

This standard is intended to provide a foundation level for a multiple level standard family developed within the IEEE Computer Society. The levels identified so far are

- (1) Hardware level (896.1 — this document)
- (2) Firmware level (896.2 — in preparation)
- (3) Software levels (currently under consideration in the System Architecture Study Group).

This document provides a level of specification sufficient to design modules that are functionally, operationally, electrically, and mechanically compatible. Additional documents are necessary only to promote a higher degree of system level compatibility in manufacturers' products.

2. Definitions

2.1 General Definitions

2.1.1 Special Word Usage. In this standard, the word “shall” indicates a mandatory requirement. The word “should” or the phrase “it is recommended” indicates flexibility of choice with a strongly preferred implementation. The word “may” indicates flexibility of choice with no implied preference.

2.1.2 Bus Lines and Signals. A BUS LINE is the medium for the transmission of SIGNALS. Since Futurebus uses open-collector drivers, a bus line may be driven by several modules simultaneously. Therefore, the signal carried by the bus line is the combination of the signals applied to that line from each module.

The signals that a module applies to the bus lines are designated by lower-case labels, for example, **as***. The signal that appears on a bus line as the result of the combination of signals applied to it is designated by an upper-case label, for example **AS***.

The “*” in both cases means that the logic 1 state is represented by a less positive voltage than the logic 0 state. A bus line is said to be ASSERTED if it is at logic 1, and RELEASED if it is at logic 0.

Where a group of bus lines are represented by the same capital letters, the lines within the group are numbered, for example, **AD0***, **AD1***, **AD2***, ..., **AD31***. In order to represent a group of lines or signals in more convenient form, the notation **AD<31..0>*** is used. Also, the notation **AD<>*** may be used to refer to all of the lines within the group.

The suffix “(f)” (filtered) after a signal refers to the bus line signal after it has passed through a receiver and a wired-OR glitch filter (integrator). For example, **AI(f)** refers to the signal on the **AI*** line after it has passed through an (inverting) receiver (to become **AI**) and the wired-OR glitch filter (to become **AI(f)**). It is, however, not correct within the defined meaning of the words “assert” and “release” to say “..when **AI(f)** is detected asserted..” The correct phrase is “..when **AI(f)** is detected at logic one..”

When a group of signals are driving a group of bus lines (for example, **CM<5..0>***), these signals are said to be ACTIVE.

2.1.3 General Definitions

byte. A set of 8 adjacent binary digits.

doublet. A set of 2 adjacent bytes.

quadlet. A set of 4 adjacent bytes.

master. A module that has acquired control of the bus through the control acquisition procedure.

potential slave. A module that is capable of being addressed by and is able to carry out transactions with the master.

selected slave. A potential slave that has been selected by the master because it recognized its address on the bus lines during an address transfer, and will become a connected slave, unless an intervening slave prevents it from becoming so.

unselected slave. A potential slave module that does not recognize its address on the bus during an address transfer.

reflecting slave. An unselected slave that forces the selected slave into a write-only mode. In read transfers the reflecting slave substitutes itself for the selected slave in providing data while causing the selected slave to store the data that appears on the bus. In write transfers the reflecting slave copies the data into itself as well as the selected slave. Reflecting slaves can operate only during single-slave mode transactions.

intervening slave. An unselected slave that disables the selected slave and replaces that selected slave with itself. Intervening slaves can operate only during single-slave mode transactions.

disabled slave. A selected slave that detects that an intervening slave is participating in the data transfer in its place. A disabled slave treats the transaction as an address-only transaction and does not participate in the data transfer phase. A slave may be disabled only during single-slave mode transactions.

diverted slave. A selected slave that detects that a reflecting slave is participating in the data transfer in its place. A diverted slave participates in the transfer by reading the data being transferred between the master and the reflecting slave. A slave may be diverted only during single-slave mode transactions.

connected slave. A slave that is permitted to participate actively in the data transfer handshake. A selected slave that is not disabled (including a diverted slave), a reflecting slave, and an intervening slave are connected slaves. A disabled slave or, an unselected slave that is not intervening or reflecting, is not a connected slave.

bus tenure. The duration of a master's control of the bus.

transaction. The total of all parallel bus activity beginning with an address beat and ending with an end beat, associated with a single address.

beat. A beat consists of the transition on a synchronization line made by a master, followed by the transition of an acknowledge line by the slave(s). Command information and/or data may be sent from the master to the slave(s) during the first half of a beat, and status information and/or data may be returned to the master from the slave(s) during the second half.

address-only transaction. An address beat is carried out followed by an end beat. There is no data transfer phase, and hence no data is transferred with the exception of the information contained within the address itself, the associated command, and the status response.

block write transaction. An address beat followed by a block of one or more data write transfers to a set of contiguous addresses beginning with the address in the address beat. This is terminated by the appropriate style of end beat.

block read transaction. An address beat followed by a block of one or more data read transfers from a set of contiguous addresses beginning with the address in the address beat. This is terminated by the appropriate style of end beat.

mixed transaction. An address beat followed by any number or combination of data write and data read transfers to a single location using the single address transfer mode. This is terminated by the appropriate style of end beat.

potential master. A potential master is a module that is capable of participating in the control acquisition process and taking full control of the bus.

participating slave. A participating slave is a module that never requires control of the bus, but may have to carry out certain actions during the control acquisition process. Such actions include unlocking interfaces to other buses and registering the identity of the master.

locking. The facility by which a module may be forced to inhibit accesses to it from any but one other module. This results in a deterministic serialization of accesses.

inactive modules. This category contains all the modules that have no need to participate in the control acquisition process in any way.

entrant. An entrant module that is in the process of joining the control acquisition process.

free bystander. A free bystander can be a participating slave that is no longer an entrant, or a potential master that has no current need to acquire the bus and is not fairness inhibited.

inhibited bystander. An inhibited bystander is a potential master that has no current need to acquire the bus and is fairness inhibited.

competitor. A competitor is a potential master that requires control of the bus module and is not fairness inhibited.

withholder. A withholder is a potential master that requires control of the bus module and is fairness inhibited.

master elect. A master elect is the module that has won the arbitration process and is waiting for the master to transfer control to it.

recompeting master. The module that is in control of the bus and has initiated a control acquisition procedure in order to unlock slave interfaces.

parking. The process whereby the current master retains control of the bus when there are no other masters wishing to use it.

fairness. A bus request protocol in which a module refrains from acquiring the bus in order to allow other modules of the fairness class to use the bus.

priority. A bus request protocol in which the module with the highest arbitration number acquires the bus.

emergency message. An arbitration cycle with a special high arbitration number, which is selected from a set of numbers assigned to emergency messages.

potential master. A potential master may be in any of these states:

- (1) entrant
- (2) free bystander
- (3) inhibited bystander
- (4) competitor
- (5) withholder
- (6) master elect
- (7) master
- (8) recompeting master

participating slave. A participating slave may be in any of these states:

- (1) entrant
- (2) bystander

skew. The difference between the propagation delays of two or more signals passing through multiple paths in a device or along a set of signal lines in parallel.

CSR. Control and status register.

NOTE: In the specification of the protocols, events described in sequential sections are to be executed in sequential order unless concurrency is explicitly allowed.

2.2 Futurebus Logo. The 896 logo is copyrighted by the IEEE Computer Society, and may be used only on products that fully conform to all mandatory requirements of this document.

Figure 2 shows the 896 logo.

Fig 2
896 Logo



2.3 References. The following publications shall be used in conjunction with this standard.

[1] ANSI/IEEE Std 1101-1987, IEEE Standard for Mechanical Core Specifications for Microcomputers.²

[2] IEC 603-2 (1980), Part 2: Two-Part Connectors for Printed Boards, for Basic Grid of 2.54 mm (0.1 inches), with Common Mounting Features.³

²ANSI/IEEE publications can be obtained from the Sales Department, American National Standards Institute, 1430 Broadway, New York, NY 10018, or from the Institute of Electrical and Electronics Engineers, Service Center, 445 Hoes Lane, Piscataway, NJ 08855-1331.

³IEC publications can be obtained in the US from the Sales Department, American National Standards Institute, 1430 Broadway, New York, NY 10018.

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3. Bus Line Definitions

3.1 Introduction. This standard completely defines the signals used on one 96-pin two-piece connector. 67 active signals are dedicated to the parallel bus, 2 are dedicated to a serial bus, and the remaining 27 are used for power and ground, etc. Table 1 shows the list of bus lines.

Table 1
List of Bus Lines

Data Transfer Lines			
Information Field:	AD<31..0>*	Address/Data	32
	TG*	TaG	1
	CM<5..0>*	CoMmand	6
	ST<3..0>*	STatus	4
	BP<W..Z>*	Bus Parity	4
	TP*	Tag Parity	1
	CP*	Command Parity	1 <u>49</u>
Synchronization Field:	AS*,AK*,AI*	address handshake	3
	DS*,DK*,DI*	data handshake	3 <u>6</u>
Control Acquisition Lines			
Control Acquisition:	AP*,AQ*,AR*	control acq handshake	3
	AC*	control Acq Condition	1
	AB<6..0>*	Arbitration Bus	7
Reset/Bus Initialize:	RE*	REset	1 <u>12</u>
Power Geographical Address Lines			
Geographical Address/AC Grounds:	GA<4..0>*	Geographical Address	5
Power and 0 V Logic:	+5 V DC	+5 V	6
	0 V DC	0 V power return	6
	0 V LOGIC	0 V logic return	10 <u>27</u>
Reserved for Serial Bus			
Serial Bus:	SB<1..0>*	reserved — Serial Bus	2 <u>2</u>
Total lines:			<u>96</u>

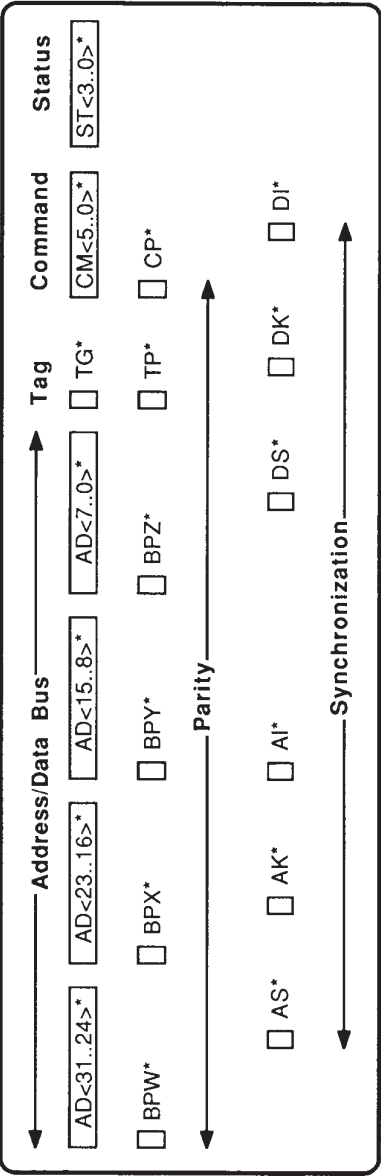


Fig 3
Data Transfer Highway

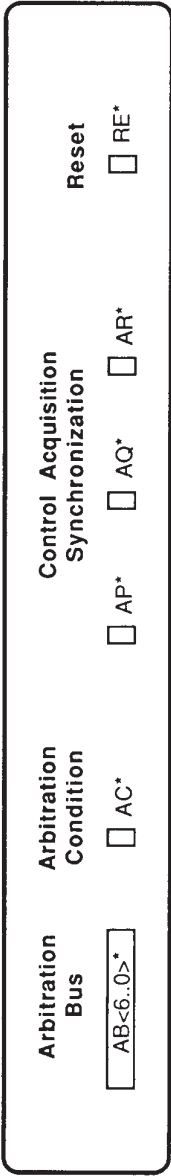


Fig 4
Control Acquisition Highway

3.2 Information Field. The following lines are involved in data transfers.

<u>Name</u>	<u>No.</u>	<u>Description</u>
AD<31..0>*	32	ADDRESS/DATA Bidirectional lines that carry the address during an address transfer, and the read or write data during a data transfer. The address is always transmitted from the master to the slave(s). Data may be transmitted in either direction. The address is associated with a quadlet. AD31* carries the most significant bit of the address and AD2* the least significant bit. During an address transfer AD1* and AD0* are undefined.
TG*	1	TAG Bidirectional line that carries additional information related to that on AD<31..0>* during an address or data transfer, and following the same timing/protocol restraints as one of the AD<31..0>* lines. Although its use is not constrained in this standard, recommendations on how it may be used may be provided in a future standard.
CM<5..0>*	6	COMMAND Information from the master that characterizes the type of transfer in progress or information about the following transfer(s). These lines change their definition between an address transfer and a data transfer. The command is always transmitted from the master to the slave(s). A detailed definition of the individual command lines is given in 7.2.1.1.
ST<3..0>*	4	STATUS Information given by a slave in response to a master's command. It gives information both about the status of the slave and its interpretation of the information received from the master. Status is always transmitted from the slave to the master. The detailed definition of the individual status lines is given in 7.2.1.2.
BP<W..Z>*	4	BUS PARITY Lines that carry the parity code for the AD<31..0>* lines. Each parity bit is such that the number of asserted signals in each byte lane of the AD<31..0>* signals plus the associated parity bit is odd. BPW* is associated with AD<31..24>* , BPX* with AD<23..16>* , BPY* with AD<15..8>* , and BPZ* with AD<7..0>* .
TP*	1	TAG PARITY A line that carries the parity code for the TG* line. The parity bit is such that the number of asserted signals in TG* and TP* is odd.

CP* 1 COMMAND PARITY

A line that carries the parity bit for the **CM**<5..0>* lines, such that the overall number of asserted signals in **CM**<5..0>* plus **CP*** is odd.

3.3 Synchronization Field. These lines carry the “data valid” and “acknowledge” signals for address transfers and data transfers. Detailed operation of these lines is specified in Section 7.

<u>Name</u>	<u>No.</u>	<u>Description</u>
AS*	1	ADDRESS SYNC A synchronization signal controlled by the master that handshakes with AK* and AI* from the slaves.
AK*	1	ADDRESS ACKNOWLEDGE An acknowledge signal controlled by all slaves to handshake with AS* from the master.
AI*	1	ADDRESS ACKNOWLEDGE INVERSE An additional acknowledge signal controlled by all slaves to handshake with AS* from the master.
DS*	1	DATA SYNC A synchronization signal controlled by the master that handshakes with DK* and/or DI* from the slave(s).
DK*	1	DATA ACKNOWLEDGE This line has two functions: (1) An acknowledge signal controlled by nondisabled selected slaves to handshake with DS* from the master or with DI* from a reflecting slave. (2) An additional address transfer status signal controlled by an intervening slave to cause the selected slave to be disabled.
DI*	1	DATA ACKNOWLEDGE INVERSE This line has two functions: (1) In broadcast mode, it is an additional handshake signal controlled by the slaves to handshake with DS* from the master. (2) In single-slave mode, it is an additional handshake and status signal that allows an unselected slave to participate in data transfers during intervening or reflecting transactions.

3.4 Control Acquisition

<u>Name</u>	<u>No.</u>	<u>Description</u>
AP*	1	
AQ*	1	CONTROL ACQUISITION SYNCHRONIZATION
AR*	1	A group of three control acquisition lines that perform a cyclic handshake sequence to control the operations in the various modules during the control acquisition process. Additionally, AQ* is also used to indicate completion of the reset and bus initialize processes.
AC*	1	CONTROL ACQUISITION CONDITION A line used to control the type of operation to be performed by modules at two states in the control acquisition process.
AB<6..0>*	7	ARBITRATION BUS The set of lines that carry the number that signifies the precedence of competitors.

3.5 Reset

<u>Name</u>	<u>No.</u>	<u>Description</u>
RE*	1	RESET A line asserted by any module in order to initialize the bus interface logic of all modules to a specified state, and provide a reset signal for use on the boards. The duration of the asserted state on this line is used to decide whether the signal represents bus initialize or reset.

3.6 Serial Bus

<u>Name</u>	<u>No.</u>	<u>Description</u>
SB<1..0>*	2	SERIAL BUS These lines are reserved for an independent serial communication facility, to be defined under a separate standardization Working Group in the IEEE Computer Society.

3.7 Power Supply and Geographical Address

<u>Name</u>	<u>No.</u>	<u>Description</u>
GA<4..0>*	5	GEOGRAPHICAL ADDRESS These pins on the backplane connector carry the identification of the slot on the backplane, numbered from 1 on the left-hand side when viewed from the front.
0 V LOGIC	10	0 V LOGIC RETURN Bused 0 V logic tracks also connected to the backplane groundplane at each connector position.
0 V DC	6	0 V DC POWER RETURN
+5 V DC	6	+5 VOLT 5 V dc and 0 V dc return lines bused to all connectors and capable of carrying the maximum per slot current in all slot positions on the backplane according to the requirements of the bus connector used.

NOTE: 0 V logic and 0 V dc pins on the connector are electrically tied together on the boards and backplane. The 0 V dc pins, however, are the primary sink for the dc power supplied to the boards and special emphasis is made to minimize the dc resistance through these pins to the ground reference potential of the system.

4. Electrical and Backplane Specifications

4.1 Description. This section describes and specifies the power supply, distribution, and signal line electrical requirements at the bus backplane interface. The performance requirements of the bus make it necessary for this specification to impose constraints on the design of its modules beyond those normally encountered in a specification for backplane buses. These constraints are imposed to satisfy the following requirements:

- (1) optimize the system to accommodate the physical behavior of high-speed signals traveling between boards in a transmission line environment,
- (2) the need to minimize backplane propagation delay and backplane propagation skew between these signals to attain the required performance,
- (3) the need to minimize crosstalk to attain the required reliability of information transfer.

Inherent within this specification is a requirement for signal transceiver devices to have ratios of current driving and capacitance parameters consistent with a solution to the “bus driving problem.” In other words, the transceivers must be capable of properly driving the characteristic impedance of a transmission line that is

- (1) typical of stripline construction and fabricated with standard backplane manufacturing techniques,
- (2) loaded at each slot position with a capacitance equal to that of stray stub capacitances and the capacitance of the transceiver device itself.

Inherent, also, is a requirement for receiver thresholds to be optimized for the reception of signals from such a transmission line system, subject to varying degrees of loading.

Section 5 specifies the pin connections for the main connector and recommends the power connections for the auxiliary connectors.

4.1.1 Backplane Environment. The transmission of data inside the subrack between boards takes place via one or more independent backplane subsystems. Each backplane subsystem supports at least one IEC 603-2 [2]⁴ type connector interface to each of the boards in the system and provides the following facilities:

⁴The numbers in brackets correspond to those of the references listed in Section 2.3.

- (1) 69 bused signal tracks for the main communication highway.
- (2) 10 bused 0 V LOGIC return tracks that should be tied to a groundplane at each connector position.
- (3) Six 5 V dc lines and six 0 V dc return lines tied to a backplane, powerplane, and groundplane, respectively, at each connector position, bused to all connectors, and capable of carrying the maximum per-slot current in all slot positions in the backplane as defined in 4.2.4. Multiple power input positions may be used on the backplane to meet this objective.
- (4) 5 nonbused geographical identifier lines binary encoded at each slot position, using connections to the 0 V backplane groundplane or 5 V planes.
- (5) Identical termination networks at both ends of the backplane.

4.1.2 Skew. Skew is the variance in the speed of propagation of two or more signals that share a common source and destination. Two signal transitions can never be guaranteed to be completely simultaneous. Therefore, a skew between them will always exist.

The skew that is critical in a Futurebus system is that which is measured between the information signals and the handshake signal that marks its validity on the bus. It is the responsibility of the module designer to ensure that the information arriving at the pins of the connector before the validating handshake transition is allowed to arrive at the connector. This skew requirement includes accounting for the delays and any skews that may be introduced by the bus transceivers themselves.

In addition, the module designer must guarantee that the skew introduced to the backplane by capacitive loading not delay the synchronization signals more than the information signals. A module that is logically completely passive is still electrically active with regard to backplane skew. The length of the PCB trace stubs, feed throughs, and the transceivers themselves contribute to the loading.

The backplane must likewise be designed so that the synchronization lines are slower than information lines. This can be done by either lengthening the synchronization lines slightly or by decreasing the impedance of those lines slightly. The guiding principle is that each element of a Futurebus system must guarantee that it not contribute to any detrimental skew delay of information signals relative to synchronization signals.

4.2 Specification. Devices must conform to the following specification over the whole range of environmental operating conditions appropriate to their category, as specified in ANSI/IEEE Std 1101-1987 [1].

All measurements on the power rails or distribution system shall be made relative to the nearest 0 V DC; all measurements of signal voltages shall be made relative to the closest 0 V LOGIC return pin of the connector mounted on the backplane.

4.2.1 Backplane Facilities

4.2.1.1 Minimum Slot Spacing. The minimum slot spacing on any Futurebus backplane shall not be less than 20.32 mm (0.8").

4.2.1.2 Maximum Propagation Delay. The maximum one-way propagation delay t_{pd}' on a signal line fully loaded with modules exhibiting the maximum loading capacitance specified in 4.2.7.2 shall not be greater than 12.5 ns (25 ns round-trip), including connection to termination networks and inclusive of a single passive extender card of up to 280 mm (11.02") in depth, plugged into one end of the backplane (see 4.2.11). It may be assumed that the maximum propagation delay of the extender card is 5 ns.

t_{pd}' is the propagation delay of a signal line loaded with extra distributed capacitance per unit length of C_d , and with an intrinsic (unloaded) propagation delay of t_{pd} .

t_{pd}' is related to t_{pd} by the relationship:

$$t_{pd}' = t_{pd} \sqrt{(1 + C_d/C_o)}$$

where C_o is the intrinsic capacitance per unit length of the transmission line, and C_d is the maximum permitted capacitive loading per unit length.

The backplane shall exhibit a skew such that the propagation delays of the signal lines to the left of the relational operator in relationships (Eq 1), (Eq 2), and (Eq 3) are greater than or equal to the propagation delays of the signal lines to the right of the relational operator in these relationships:

$$(DI^*, DK^*) \geq (AD<31..0>^*, BP<W..Z>^*, ST<3..0>^*, TG^*, TP^*) \quad (\text{Eq 1})$$

$$(AS^*, DS^*) \geq (AD<31..0>^*, BP<W..Z>^*, CM<5..0>^*, CP^*, TG^*, TP^*) \quad (\text{Eq 2})$$

$$(AP^*, AQ^*, AI^*) \geq (AC^*, AB<6..0>^*) \quad (\text{Eq 3})$$

NOTE: The signals DK^* and DI^* are used for both handshake and information. In their role as information signals, the integrator on the signal AI^* is relied upon to provide the required signal skew.

4.2.1.3 +5 V DC Power. +5 V dc power shall be available at pins 2a, 2b, 2c and 31a, 31b, 31c for all backplane connector positions.

4.2.1.4 0 V DC Power Returns. 0 V dc power returns shall be available on pins 1a, 1b, 1c and 32a, 32b, 32c for all backplane connector positions, connected to the backplane groundplane.

4.2.1.5 Signal Lines. The lines comprising the signal highway shall present a uniform characteristic impedance as specified in 4.2.2, and be terminated as specified in 4.2.3.

4.2.1.6 0 V Logic. The 0 V logic returns shall comprise independent tracks similar to the signal tracks and shall be additionally tied to the groundplane at all connector positions.

4.2.2 Backplane and Extender Card Effective Characteristic Impedance. All backplanes with connectors installed and otherwise in a state to accept insertion of boards, but with no boards actually inserted, shall present an effective characteristic impedance of no less than 55 Ω and no greater than 65 Ω when driven by a signal with transition times as specified in 4.2.7.3.5. Effective characteristic impedance, Z'_o is given by Eq 4.

$$Z'_o = \frac{Z_o}{\sqrt{(1 + C_d/C_o)}} \quad (\text{Eq 4})$$

where

Z_o = intrinsic characteristic impedance of the line

C_o = intrinsic capacitance of the line, per unit length

C_d = additional (distributed) capacitance added at each slot position due to the through-plated hole and backplane member of the connector pair

4.2.3 Termination

4.2.3.1 Termination Resistance. Each bus line on the backplane shall be terminated in a resistance of 39 $\Omega \pm 1\%$ to a voltage source of the termination voltage specified in 4.2.3.2 below, at both ends of the backplane. The voltage source should be decoupled with a high frequency capacitance of at least 100 nF as close to the resistors as practicable.

NOTE: Passive extender cards should only be used with removable terminating networks.

4.2.3.2 Termination Voltage. The termination voltage for all lines on the bus signal highway shall be 2.1 V $\pm 1\%$.

4.2.4 Power Rails

4.2.4.1 Power. +5 V dc is the only power supply that is required in all Future-bus systems.

4.2.4.2 Noise and Ripple The noise and ripple on the +5 V dc rail shall remain below 50 mV peak-peak and 20 mV rms under all permitted loading conditions.

4.2.4.3 Overshoot. The overshoot of the power supply at turn-on shall not exceed 10% of the nominal voltage.

4.2.4.4 Rise Time. The rise time of the power supply at turn-on shall be less than 100 ms from 10% to 95% of the nominal voltage.

4.2.4.5 Current Capability. The average current and maximum current drawn by a board shall be indicated in its product specification.

4.2.4.6 Grounding. The grounding rules for systems that adhere to this specification shall follow the individual requirements of the safety regulations of the country in which the equipment is sold or used, or the specifications laid out below, whichever is the stricter, on an item by item basis.