

IEEE Standard for Futurebus+ — Physical Layer and Profile Specification: Errata, Corrections, and Clarifications

Sponsor
**Bus Architecture Standards Committee
of the
IEEE Computer Society**

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Abstract: This supplement contains errata, corrections, and clarifications to IEEE Std 896.2-1991. Futurebus+ standards provide systems developers a set of tools with which high-performance bus-based systems may be developed. This architecture provides a wide range of performance scalability over both cost and time for multiple generations of single- and multiple-bus multiprocessor systems. This document, a companion standard to ISO/IEC 10857 : 1994 [ANSI/IEEE Std 896.1, 1994 Edition], builds on the logical layer by adding requirements for physical layer instantiation. Material in this document includes specifications for node management, live insertion, and profiles. It is to these profiles that products will claim conformance. Other specifications that may be required in conjunction with this standard are the following: IEEE Std 896.3-1993; IEEE Std 1212-1991; IEEE Std 1194.1-1991; and the IEEE 1301 series of standards.

Keywords: application environment profiles, bus architecture, Futurebus+, live insertion, multiprocessor systems, node management, physical layer

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Foreword

(This foreword is not a part of IEEE Std 896.2a-1994, IEEE Standard for Futurebus+ — Physical Layer and Profile Specification: Errata, Corrections, and Clarifications.)

IEEE Std 896.1-1991, entitled IEEE Standard for Futurebus+ — Logical Protocol Specification, and IEEE Std 896.2-1991, entitled IEEE Standard for Futurebus+ — Physical Layer and Profile Specification, were approved by the IEEE in 1991. During implementation of products that meet these standards, designers identified errors and ambiguities in both of these specifications. The errata and clarifications to IEEE Std 896.1-1991 were corrected in IEEE Std 896.1a-1993 and folded into the base standard in a new International edition of the standard, ISO/IEC 10857 : 1994. The purpose of this document, IEEE Std 896.2a-1994, is to correct errors and to clarify ambiguities found in IEEE Std 896.2-1991. This document should be used as a supplement until a revised IEEE Std 896.2 that incorporates this errata is published. Members of the 896.2a Working Group have made a diligent effort to ensure completeness, but errors and ambiguities have undoubtedly been missed. Questions and comments may identify additional errors or ambiguities in this standard; these should be forwarded to the IEEE Standards Board, who will pass them on to the Bus Architecture Standards Committee (BASC) for action.

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IEEE Standard for Futurebus+ — Physical Layer and Profile Specification:

Errata, Corrections, and Clarifications

This supplement provides errata, corrections, and clarifications to IEEE Std 896.2-1991. These are presented as a list of changes, replacements, and additions or deletions to the existing text of IEEE Std 896.2-1991.

Changes are shown, as often as possible and reasonable, within their context; for example, a sentence or paragraph, in which a change or changes are to be made, is presented in its entirety with new text underlined and old text ~~struck through~~. Text shown in ***bold italics*** provides instructions necessary to incorporating these changes into the base document. The section, subsection, figure, and table numbering in the following list corresponds to the numbering in the base document, IEEE Std 896.2-1991, IEEE Standard for Futurebus+ — Physical Layer and Profile Specification.

On pages 19, 21, 23, 25, replace the right side of the running heads with the following:

IEEE
Std 896.2-1991

On pages 27–101 and 113–221 (odd pages), replace the left side of the running heads with the following:

PHYSICAL LAYER AND PROFILE SPECIFICATION

1.2.1 Protocol Stack Specification

Update the indicated references as follows. All internal references should be updated accordingly.

[2] ISO/IEC 10857 : 1994 [ANSI/IEEE Std 896.1, 1994 Edition], Information technology—Microprocessor systems—Futurebus+ — Logical protocol specification.

[3] IEEE Std 896.3-1993, IEEE Recommended Practices for Futurebus+ (ANSI).

[4] IEEE Std 896.4-1993, IEEE Standard for Conformance Test Requirements for Futurebus+ (ANSI).

[5] IEEE Std 896.5-1993, IEEE Standard for Futurebus+, Profile M (Military) (ANSI).

[10] IEEE Std 1156.1-1993, IEEE Standard for Microprocessor Environment Specifications for Computer Modules (ANSI).

[13] IEEE Std 1212.1-1993, IEEE Standard for Communicating Among Processors and Peripherals Using Shared Memory (Direct Memory Access—DMA) (ANSI).

Add the following reference (p. 18):

[18] P1275.4, Standard for Boot (Initialization Configuration) Firmware—IEEE 896 (Futurebus+) Bus.¹

2.2 Definitions

Add the following definition (p. 20):

byte. A set of eight adjacent binary digits.

Change the the following definition as shown (p. 21):

intermateable. Mechanical compatibility between modules with the backplane, card cage, and system into which they are inserted. Sometimes includes compatibility in the assignment of power and ground ~~pins~~ blades.

3.1.1.3 Hybrid Addressing

Change the first paragraph of the subsection as follows (p. 28):

Futurebus+ nodes must support A32 and may support A64 (64-bit addressing). Futurebus+ modules that support only A32 can coexist on the same backplane with modules that are using A64 without fear of aliasing. To support hybrid systems, since all Futurebus+ modules are required to support A32, all transactions with 32-bit equivalents shall be done with A32 transactions. A node that is A64 internally shall be designed to recognize a bus address of less than 3.75 Gbyte (the bottom 15/16 of 32-bit address space) as shown in Table 1, and convert it to A32. This slightly increases the cost of 64-bit nodes, but ensures compatibility with the elementary 32-bit only designs. A node shall not generate a Futurebus+ transaction with an A64 address that is less than 0xF000 0000 or greater than or equal to 0xFFFF FFFF F000 0000. A master than uses 64-bit addresses internally shall convert any internal addresses within the excluded ranges to A32 external (Futurebus+) addresses, as shown in Table 1.

Delete the second paragraph of the subsection (p. 29).

Table 1, Hybrid Addressing

Edit the fourth row and add a fifth row to the table that appears on p. 29 as follows::

CM7*	ADDRESS FIELD		DESCRIPTION
	FROM	TO	
0	0000 0000	EEEE FFFF	A32 Memory Address Space
0	F000 0000	FFFF FFFF	Node CSR Space
1	0000 0000 0000 0000	0000 0000 EFFF FFFF	PROHIBITED (Use the A32 Equivalent)
1	0000 0000 F000 0000	FFFF FFFF EFFF FFFF	A64 Memory Address Space
1	FFFF FFFF F000 0000	FFFF FFFF FFFF FFFF	Prohibited (Use A32 [CSR Space])

¹A draft of this project will be available in July, 1994. Contact the IEEE Standards Department, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331 USA [telephone 1 (908) 562-3800] for information.

3.1.2.8 Node State Control

Replace the last four paragraphs of the subsection with the following sentence (p. 35):

If a module contains two nodes, receiving ATN or OFF at either node causes the action at both nodes.

Table 7, STATE_CLEAR and STATE_SET CSRs Bit Descriptions

Replace the descriptive text for the ATN bit field with the following (p. 49):

When this bit is set to a one, it shall inform software that the node should be prepared for live removal. This bit is expected to be set by a front-panel switch, a special command on a redundant diagnostic bus, or some other implementation-dependent mechanism. This is an indication to software only and shall have no direct effect on the node's operation. Housekeeping preparations for live removal could include flushing caches, reassigning tasks, saving state information, removal of module power, etc.

Replace the descriptive text for the OFF bit field with the following (p. 49):

Setting this bit shall cause the node to logically disconnect from the bus. The bus interface shall be gracefully inhibited from participating in or generating any further bus transactions as specified in 7.2.3.5 of ISO/IEC 10857 : 1994. Thus, this bit can never be cleared via the Futurebus+ interface, but may be accessed via an alternate path. Clearing this bit shall cause the node to logically connect to the bus. The bus interface shall be aligned to the bus and allowed to participate in bus transactions as specified in 7.2.3.4 of ISO/IEC 10857 : 1994. Setting/clearing the OFF bit in one node shall cause the OFF bit in the other node on the same bus interface, if present, to be set/cleared also.

3.2.2.3 RESET_START CSR

Change the second paragraph of the subsection as follows (p. 51):

A reset resulting from writing to the RESET_START CSR, shall not cause the module to assert RE* long enough for a BUS_INIT or SYSTEM_RESET to be detected on the bus. This allows a module to use RE* to realign after a directed reset. A reset resulting from writing to the RESET_START CSR shall cause only the addressed node to be reset.

Table 10, Internal INDIRECT_DATA CSR Bit Descriptions

Change the value in the POWER-UP column as follows (p. 53):

0 undefined

3.2.2.6 Argument CSRs

Add the following paragraph to the end of 3.2.2.6, before Table 12 (p. 54):

If a System Reset or Power-Up causes extended, manual, or system diagnostic tests to be performed, the state of this CSR shall be the result of the last test that was initiated as a result of either bus management operation; otherwise, following a System Reset or Power-Up, this CSR shall be set to zeros.

Table 12, Argument CSRs Bit Description

Change the descriptive text for the ENB bit as follows (p. 54):

When the CAT field of the TEST_START CSR = extended diagnostic, this bit set, and the MASTER_ENABLE bit in LOGICAL_COMMON_CONTROL CSR set, the node ~~may~~ shall perform tests that generate Futurebus+ transactions to remote (i.e., off-node) memory starting at the address in the ARGUMENT-HI/ARGUMENT-LO register. All other uses of this bit are user-defined.

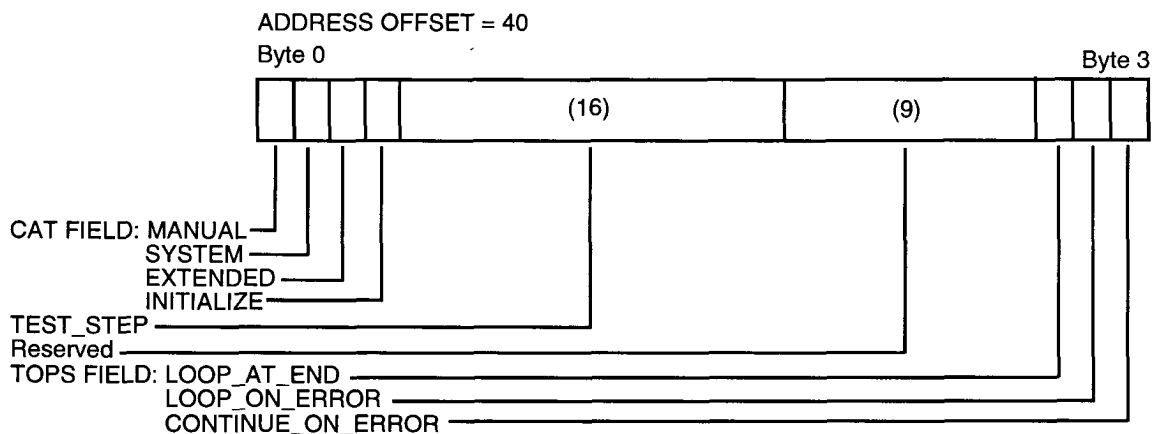
3.2.2.7 TEST_START CSR

Change the subsection as follows (p. 55):

(See Table 13 and Fig 15.) Writing to this CSR shall cause the diagnostic specified by the test_step field to begin execution. The state of the test shall be immediately visible in the TEST_STATE field of the TEST_STATUS CSR. Nodes in a module may have different values in their TEST_START CSRs. The effect of writing a new value to the TEST_START CSR while a test is in progress is implementation-dependent. ~~Following a System Reset, this CSR shall be set to all zeros.~~ If a System Reset or Power-Up causes diagnostic tests to be performed, the state of this CSR shall be the result of the last test initiated or zero if no tests were performed. Following a Bus Initialize, tests shall be halted but the contents of the CSR shall be unchanged.

Figure 15, Format of the TEST_START CSR

Replace Fig 15 with the following figure (p. 57):



3.2.2.8 TEST_STATUS CSR

Change the first paragraph as follows (p. 58):

(See Table 14 and Fig 16.) The TEST_STATUS CSR shall present the status of the running diagnostic or the most recently run diagnostic. This CSR shall not be modified from remote nodes. ~~Following a System Reset this CSR shall be set to zeros.~~ If a System Reset or Power-Up causes diagnostic tests to be performed, the state of this CSR shall reflect the result of the last test run. Following a Bus Initialize all tests shall be halted and, if a test was in progress, the ACTIVE bit shall be clear in the TEST_STATE field. No other changes to the CSR shall be made. Nodes in the same module may have different values in the TEST_STATUS CSRs.